

# JRA1 – Next Steps towards the Final Telescope

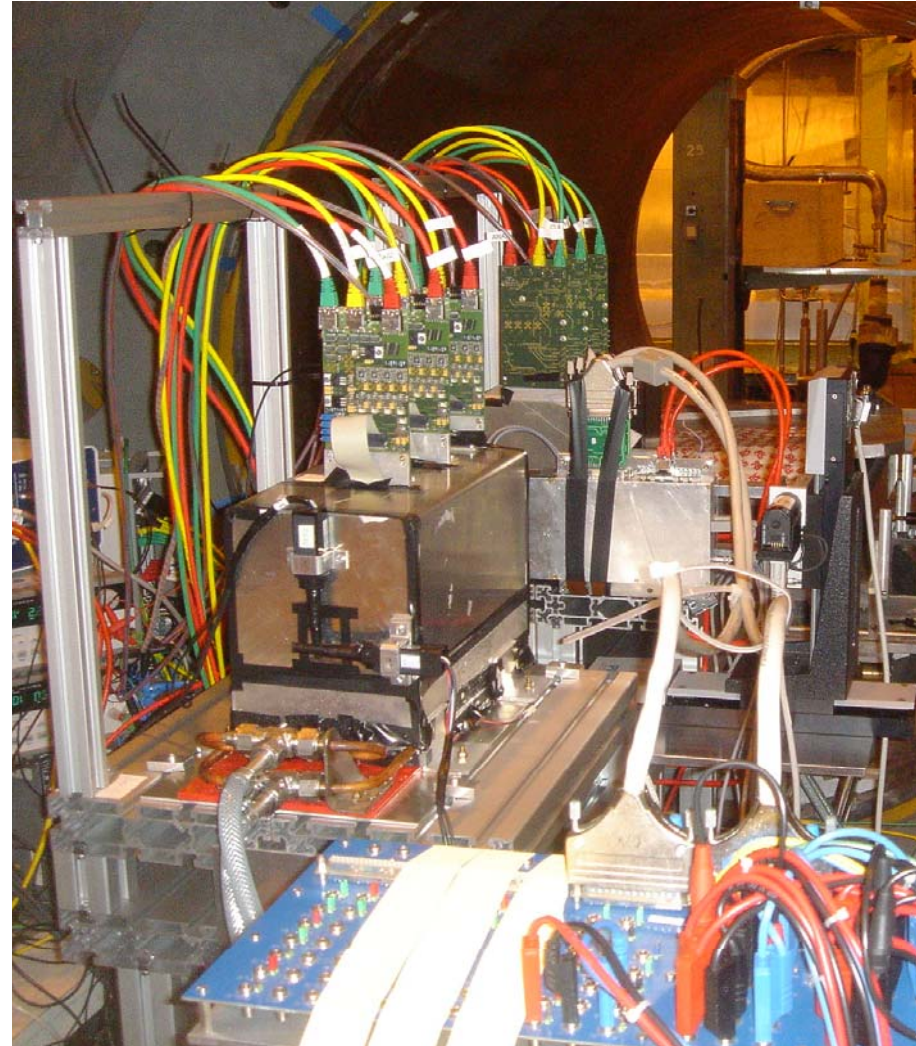
Ingrid-Maria Gregor, DESY  
EUNET Annual Meeting  
Paris, October 2007





# Outline

- Introduction
- Milestones for final telescope
- Next steps for the PCMAG
- Summary





# JRA1 Schedule

## Phase1: "Demonstrator"

- First test facility will be available quickly for the groups developing pixels
- Use established pixel technology with analogue readout and no data reduction
- From now on: support for telescope users

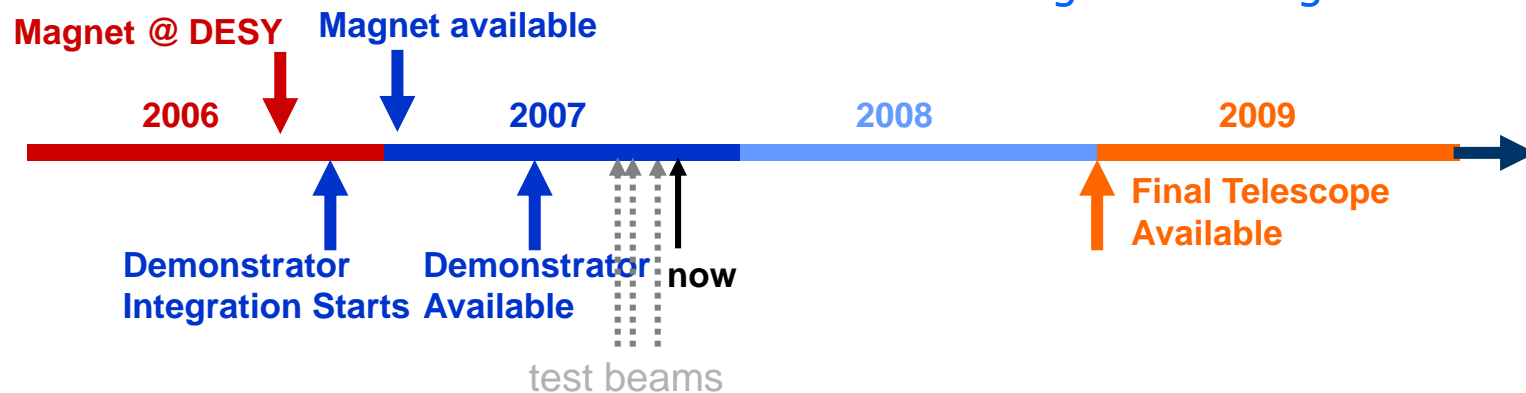


## Phase2: Final telescope

- Use pixel sensor with fully digital readout, integrated Correlated Double Sampling (CDS), and data sparsification
- The beam telescope ready at the end of 2008



+ Large bore magnet





# JRA1 Milestones

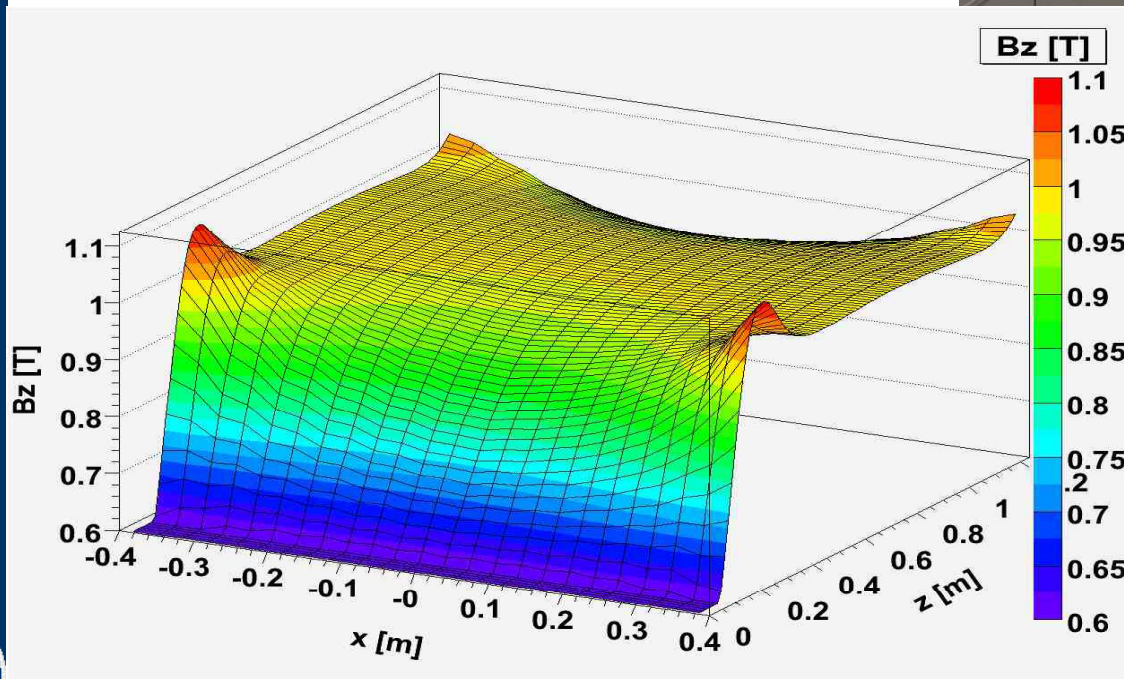
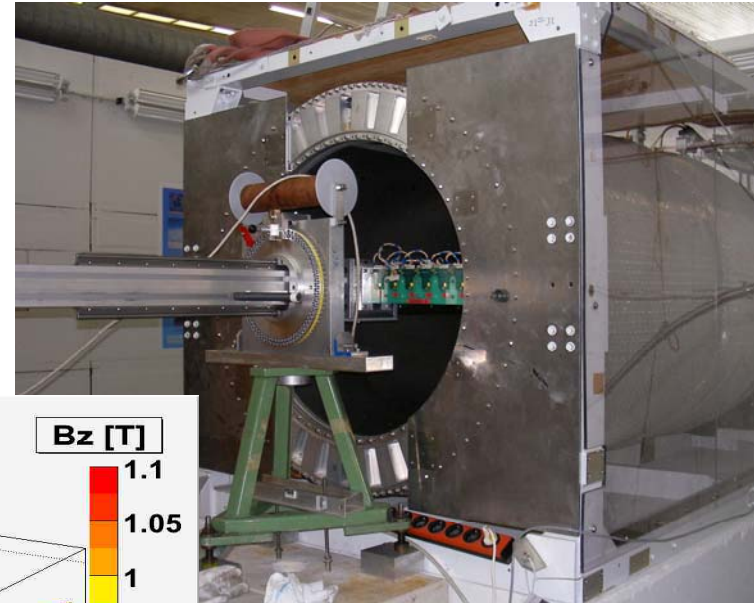
Milestone	Description	Date	Status
JRA1-1	SDC Prototype 1 ready (Mimosa17)	9	completed
JRA1-2	Magnet available	12	completed
JRA1-3	SDC Prototype 2 ready (Suze01)	18->24	soon available
JRA1-4	Field map available	18->24	soon available
JRA1-5	Analog Telescope integration in beam	18	completed
JRA1-6	Readout for prototype available	18	completed
JRA1-7	IDC prototype ready (Mimosa22)	27	
JRA1-8	Final pixel telescope integrated in beam	36	
JRA1-9	TC ready (Mimosa 22+)	36	
JRA1-10	Final readout ready	36	
JRA1-11	Tracking software available	36	
JRA1-12	Test report analog telescope available	36	
JRA1-13	Final project reports	48	





# JRA1-4 PCMAG Field map available

- ❑ Field mapping done at DESY by CERN-PH group this summer
- ❑ Accuracy of measurement in the range of  $10^{-4}$ .
- ❑ Analysis of 100.000 points @ 1 T under way



Raw fieldmap without any corrections applied

See also:  
Fabio Formenti and  
Christian Grefe  
JRA1 Parallel Session





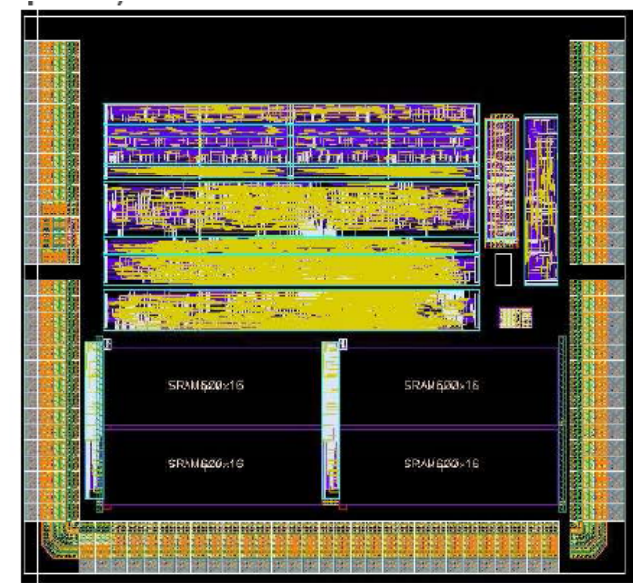
## JRA1-3 SDC Prototype 2

Prototype 2 = SUZE01

1st chip (SUZE-01) with integrated zero suppression and output memories (no pixels) :

2 step, line by line, logic :

- ❑ step-1 (inside blocks of 64 columns): identify up to 6 series of  $< 4$  neighbour pixels per line delivering signal  $>$  discriminator threshold
- ❑ step-2 : read-out outcome of step-1 in all blocks and keep up to 9 series of  $< 4$  neighbour pixels
- ❑ 4 output memories (512x16 bits) taken from AMS I.P. library
- ❑ Surface  $\sim (3.9 + 0.24) \times (3.6 + 0.24) \text{mm}^2$
- ❑  $\sim 10.3$  keuros (EUDET budget)
  
- ❑ sent for fabrication end of July
- ❑ back from foundry end of Sept -> tests are still getting prepared
- ❑ test completion and first report expected by end of year



See also: Marc Winter JRA1 Parallel Session



# JRA1-7 IDC Prototype Ready

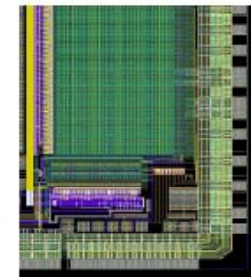
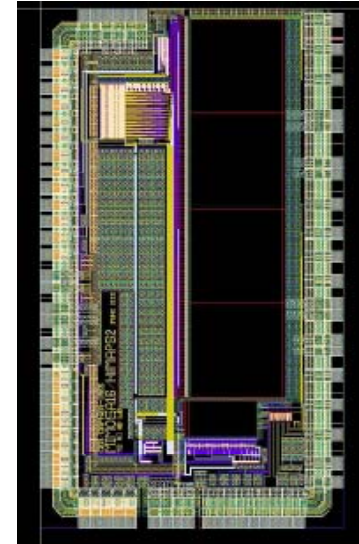
IDC = Intermediate Digital Chip  
= Mimosa22

Spring 2008

## Mimosa22: Extension of MIMOSA-16

### MIMOSA-16 design features:

- ❑ AMS-0.35 OPTO translation of MIMOSA-8:
  - 11–15  $\mu\text{m}$  epitaxy instead of  $<7 \mu\text{m}$
  - ❑ 32 // columns of 128 pixels (pitch: 25  $\mu\text{m}$ )
  - ❑ on-pixel CDS
  - ❑ 24 columns ended with discriminator
- ❑ 4 sub-arrays :
  - ❑ S1 : like MIMOSA-8 (1.7x1.7  $\mu\text{m}^2$  diode)
  - ❑ S2 : like MIMOSA-8 (2.4x2.4  $\mu\text{m}^2$  diode)
  - ❑ S3 : S2 with ionising radiation tol. Pixels
  - ❑ S4 : with enhanced in-pixel amplification (against noise of read-out chain)
- ❑ MIMOSA-16 tests at the SPS very preliminary analysis results:
  - ❑ The column architecture works very well



Ingrid-Maria Gregor, JRA1: Next Steps

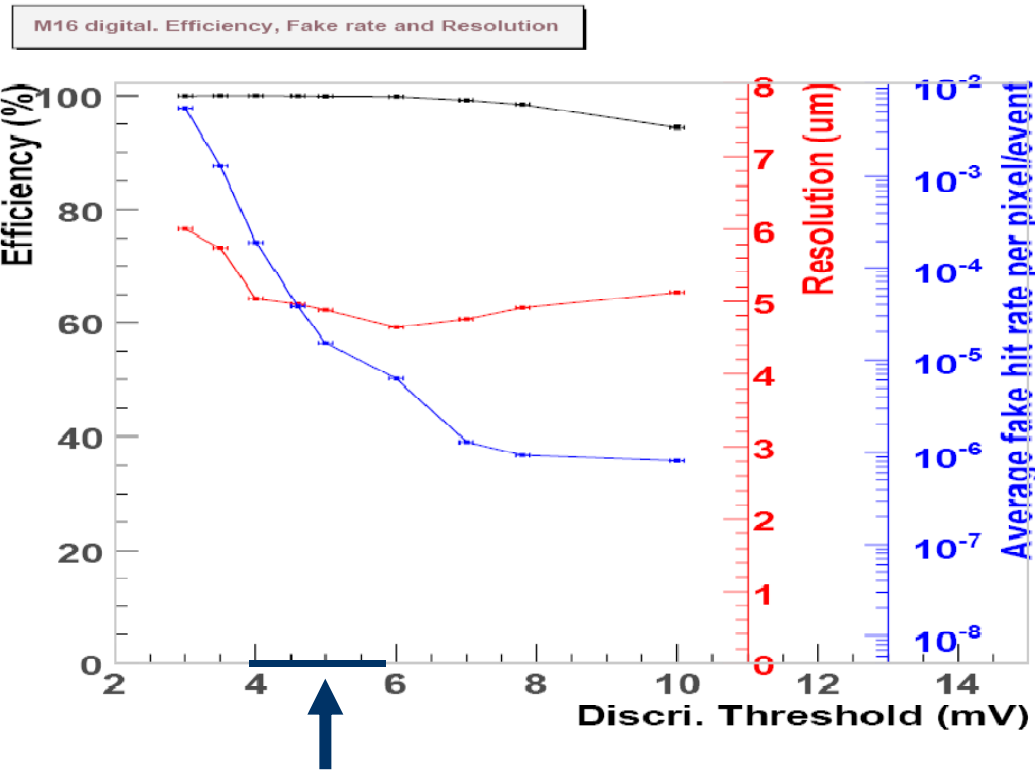


See also: Marc Winter JRA1 Parallel Session



# JRA1-7 IDC Prototype Ready

Mimosa 16: Summary of results obtained with S4 sub-array (epi-14) :



Good compromise between efficiency, resolution and occupancy

- There is at least one pixel architecture which works fine (SNR>16,  $\epsilon=99.9\%$ )
- Complementary info expected from the analysis of the other pixel architectures







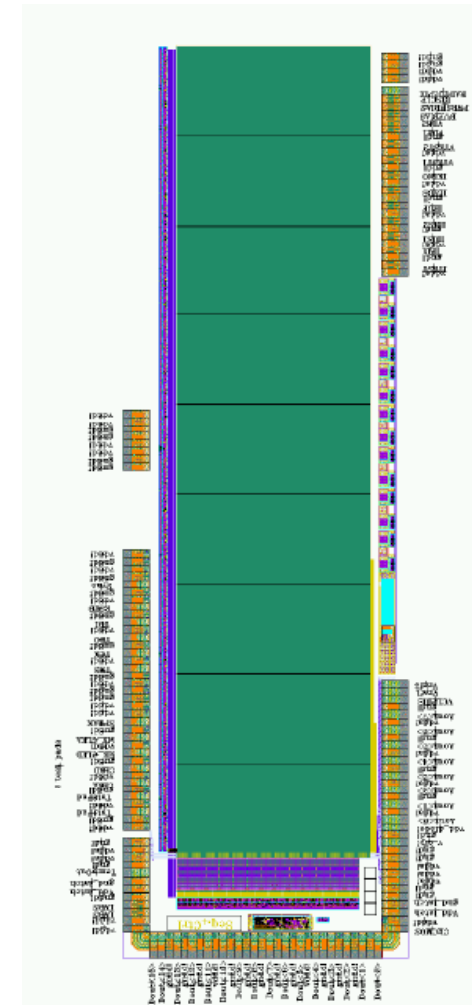
# JRA1-7 IDC Prototype

IDC = Intermediate Digital Chip

Spring 2008

## Mimosa 22: larger surface, smaller pitch, optimised pixel, JTAG, more testability

- ❑ Pixel characteristics :
  - ❑ pitch : 18.4  $\mu\text{m}$
  - ❑ diode surface: 10–15  $\mu\text{m}^2$  to optimise charge coll. & gain
  - ❑ active digital area : 128 x 576 pixels ( $\sim 25 \text{ mm}^2$ )
  
- ❑ Testability :
  - ❑ JTAG + bias DAC -> programmable chip steering
  - ❑ 2 additional DC voltages to emulate pixel's output for independent discriminator performance assessment
  
- ❑ Status :
  - ❑ Design close to completion: submission by end of Oct. '07
  - ❑ Funding ( $\sim 50 \text{ mm}^2$ ):  $\sim 40$  keuros->EUDET ( 27 keuros) & DAPNIA resources



Ingrid-Maria Gregor, JRA1: Next Steps



on track

See also: Marc Winter JRA1 Parallel Session

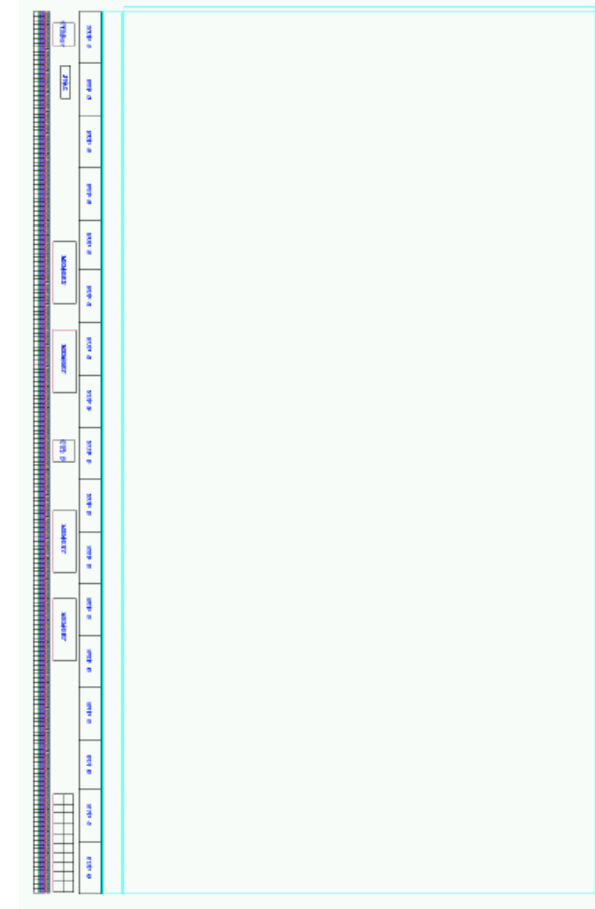


# JRA1-9 TC (Telescope Chip) ready

End 2008

## Roadmap towards the Final Chip

- ❑ Autumn 2008 : MIMOSA-22+ = Final Sensor
  - ❑ MIMOSA-22 complemented with zero suppression micro circuit (SUZE-01)
  - ❑ 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
  - ❑ Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm<sup>2</sup>)
  - ❑ Read-out time 100  $\mu$ s
  - ❑ Chip dimensions : 20 x 12 mm<sup>2</sup>
  
- ❑ Engineering run : ~120 keuros for 6 diced and thinned wafers
  
- ❑ funding : EUDET (70 keuros) & IPHC/DAPNIA (50 keuros)



on track

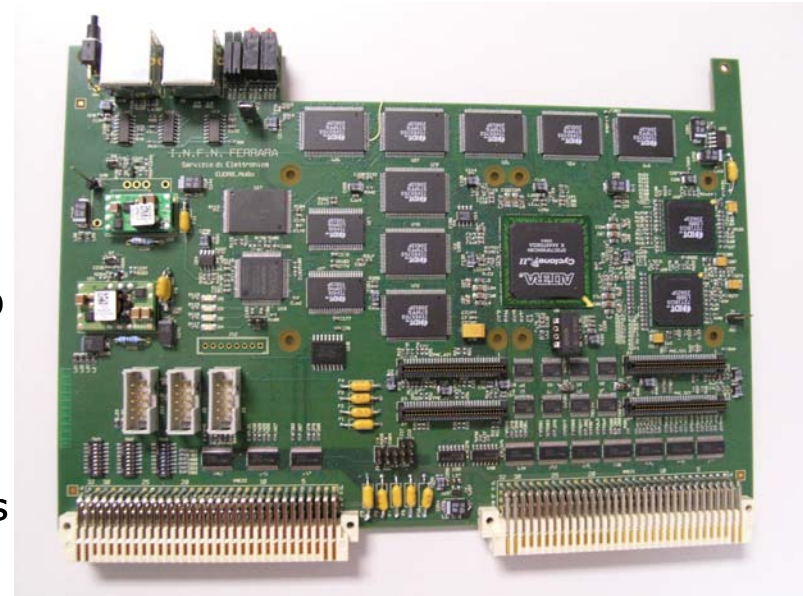
See also: Marc Winter JRA1 Parallel Session



# JRA1-10 Final readout ready

End 2008

- ❑ Readout = from AUX boards to GRID (EUDRB + EUDAQ)
- ❑ EUDRB completely tested and runs well with MimoTel chip
- ❑ Next steps: readout speed needs to be optimised
  - ❑ Mainly software side such as VME libraries
  - ❑ Implement MBLT for initial pedestals and noise
  - ❑ in zero suppression: want more events in buffer
- ❑ Final Telescope: modify the EUDRBs to be able to read out Mimosa22
  - ❑ New design of daughter cards is necessary to digest digital data
  - ❑ Mimosa 22 specifications will be given to INFN
  - ❑ Design of new hardware and software (FPGA programming) will start as soon as possible



Ingrid-Maria Gregor, JRA1: Next Steps



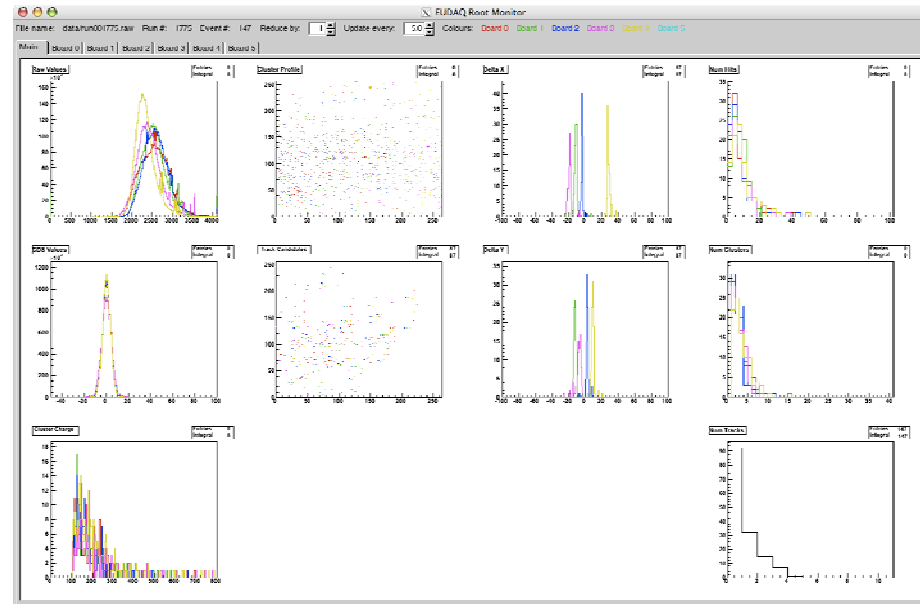
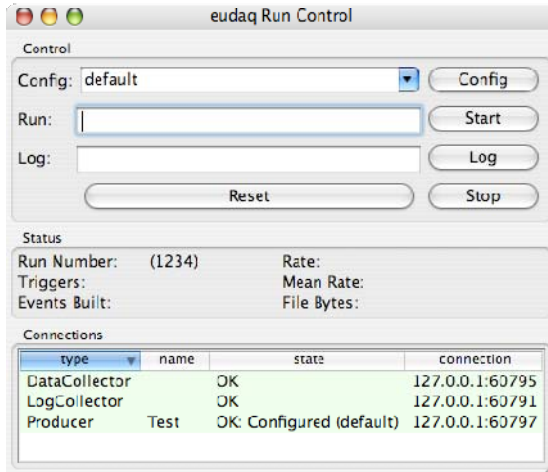
on track

See also: Concezio Bozzi JRA1 Parallel Session



# JRA1-10 Final readout ready

End 2008



- ❑ **EUDAQ:** Already have a reasonable usable DAQ system, but a few remaining issues
  - ❑ Improve speed and stability
  - ❑ Run Control: GUI for configuration
  - ❑ Data Collector: Processing - what/where?
  - ❑ Documentation

on track

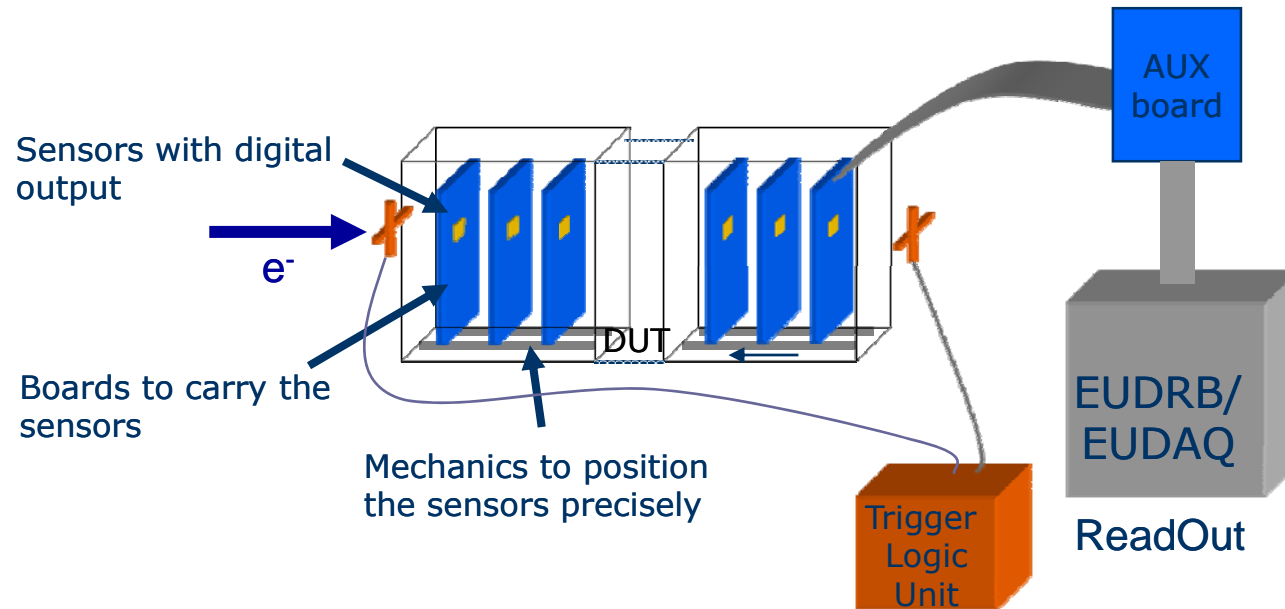
See also: Emlyn Corrin JRA1 Parallel Session



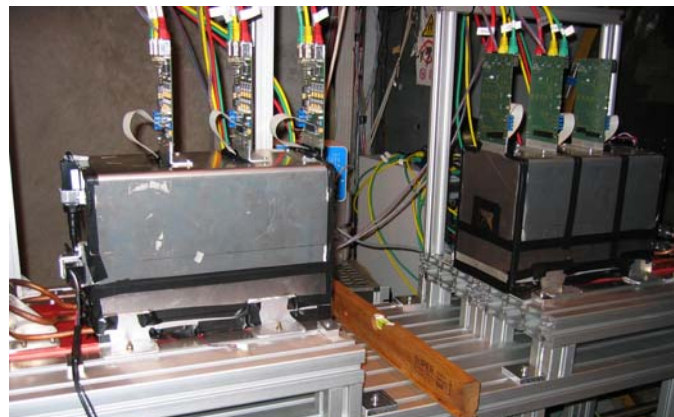


# JRA1-8 Final pixel telescope integrated in beam

End 2008



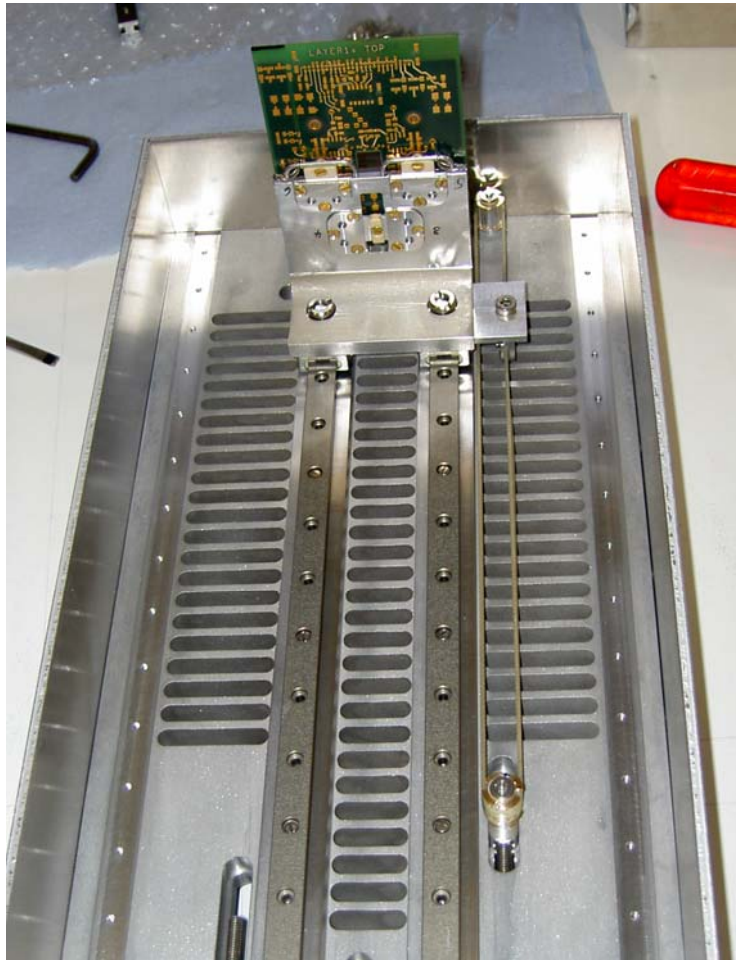
- All building blocks ready or on track, details were discussed in JRA1 parallel session





# JRA1-8 Final pixel telescope integrated in beam

End 2008



- Mechanics for final telescope:
  - First version of mechanics used at CERN during testbeam
  
- New design of L-pieces (sensor board support) under way

on track

See also: Ingrid Gregor JRA1 Parallel Session





# JRA1-11 Tracking software available

End 2008

- ❑ Tracking software EUTelescope is working!
  - ❑ The results obtained from the three data taking periods are proving that it is well behaving...
  - ❑ A lot of work has been done and the milestone foreseen for the end of 2008 will be easily achieved.

## Towards final tracking software:

- ❑ include the **LCIO format** in the DAQ software to avoid the conversion step.
- ❑ improve the alignment processor:
  - ❑ use **Millipede** and therefore include it into MarlinUtil
- ❑ improve the integration with the DUT user. A good exercise will be the integration of the **DEPFET sensor** and will start with the next month.
- ❑ improve the currently available **event display**.
  - ❑ In contact with other JRA members



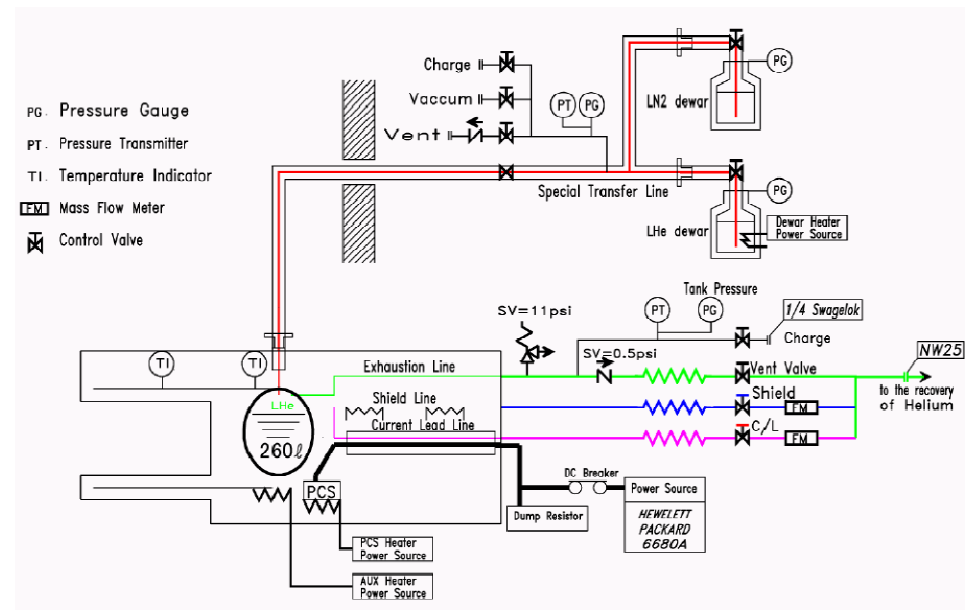
on track

See also: Antonio Bulgheroni JRA1 Parallel Session



# Next Steps for PCMAG

- Improvement of the cryogenic system is necessary for safer and easy operation of the PCMAG in the DESY experimental area.
- The new safety regulations at DESY forbid any work higher than 2m without proper protection and training.
- a new transfer tube with a cold helium-gas vent to minimize the heat flow into the reservoir and minimize the work on the top of magnet.
- More important: new transfer line would ease He filling of magnet
- No dewar exchange necessary







# JRA1 Milestones

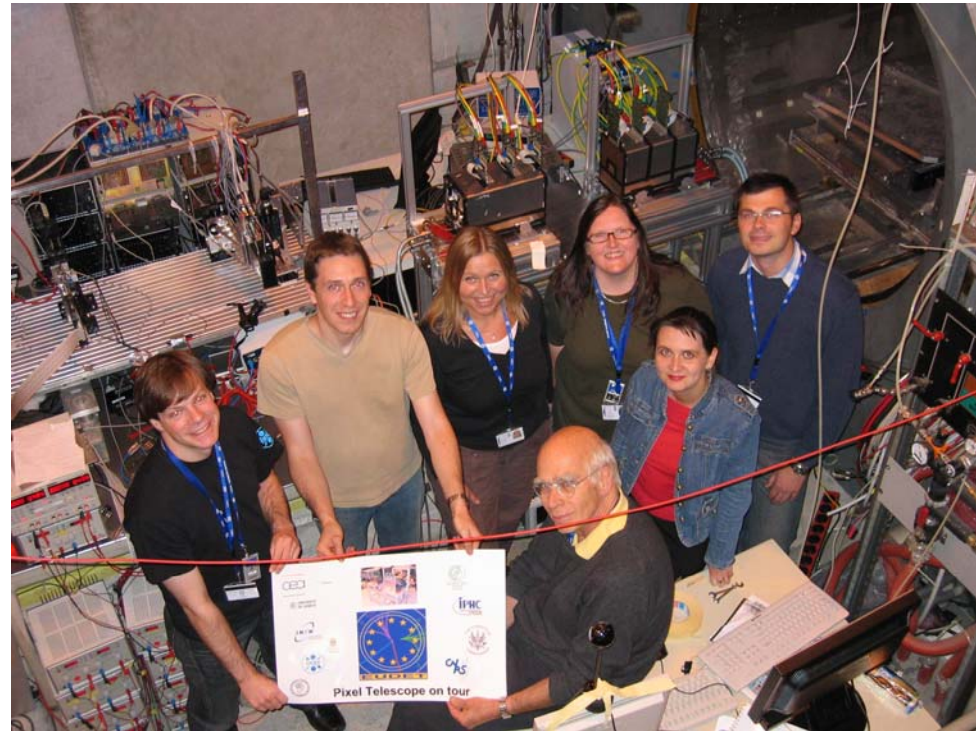
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JRA1-9	TC ready	36	C	on track
JRA1-10	Final readout ready	36	D	on track
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JRA1-12	Test report analog telescope available	36	E	
JRA1-13	Final project reports	48	A,B,C,D,E	





# Summary

- ❑ JRA1 group build and tested in the recent months the Demonstrator telescope and is happy about the status of the project
- ❑ Next steps will concentrate on the final telescope, using the final telescope chip (integrated discriminator), final readout and newly improved mechanics
- ❑ Softwarewise (DAQ, Tracking Software) also very well on track



- ❑ Preparation to meet all the milestones are well under way and we are optimistic that we will meet all future milestone

