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Demonstrator Status

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Outline

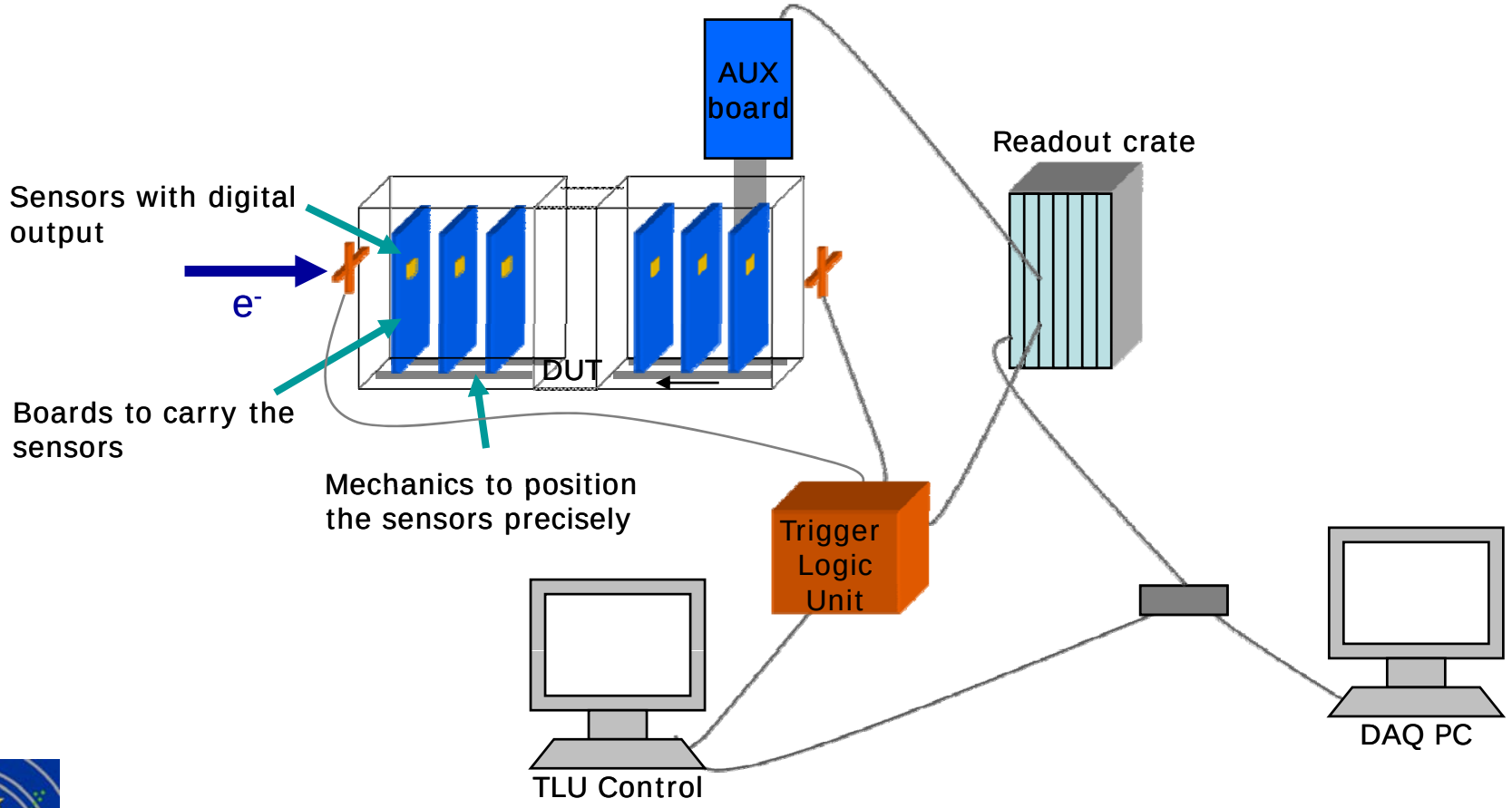
- Overview of the Telescope
- Hardware
- Mechanics
- Readout Electronics: EUDRBs
- Software
- Remaining Issues
- Conclusions

Telescope

- 6 telescope planes
- DUT movable
  via X-Y table
- Cooling can be provided
- Flexible geometry
- High-resolution planes
  close to DUT possible

QuickTime™ and a
TIFF (LZW) decompressor
e needed to see this picture.

Telescope Readout



Hardware

- MimoTEL sensors
  256x256 pixels, 30 μm pitch
  (developed at IPHC Strasbourg)
- EUDRB readout boards
  (developed at INFN Ferrara)
- MVME6100 VME CPU
- Trigger Logic Unit
  (developed at Bristol)
- Linux PC for TLU Control
- DAQ Computer: Mac Pro with
  4x1TB RAID array for data

QuickTime™ and a
TIFF (LZW) decompressor
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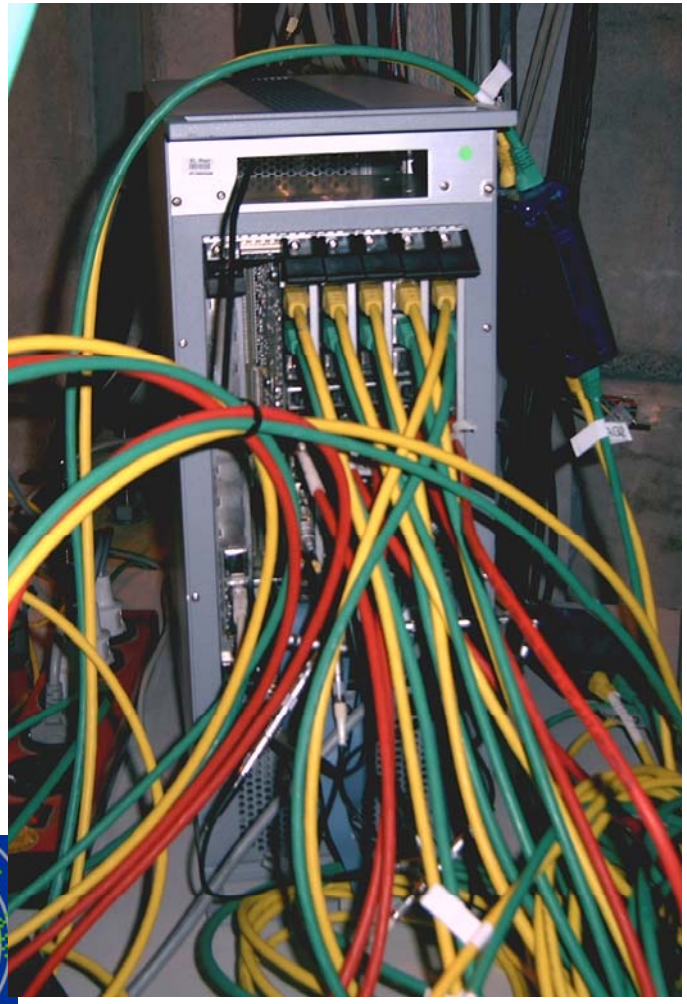
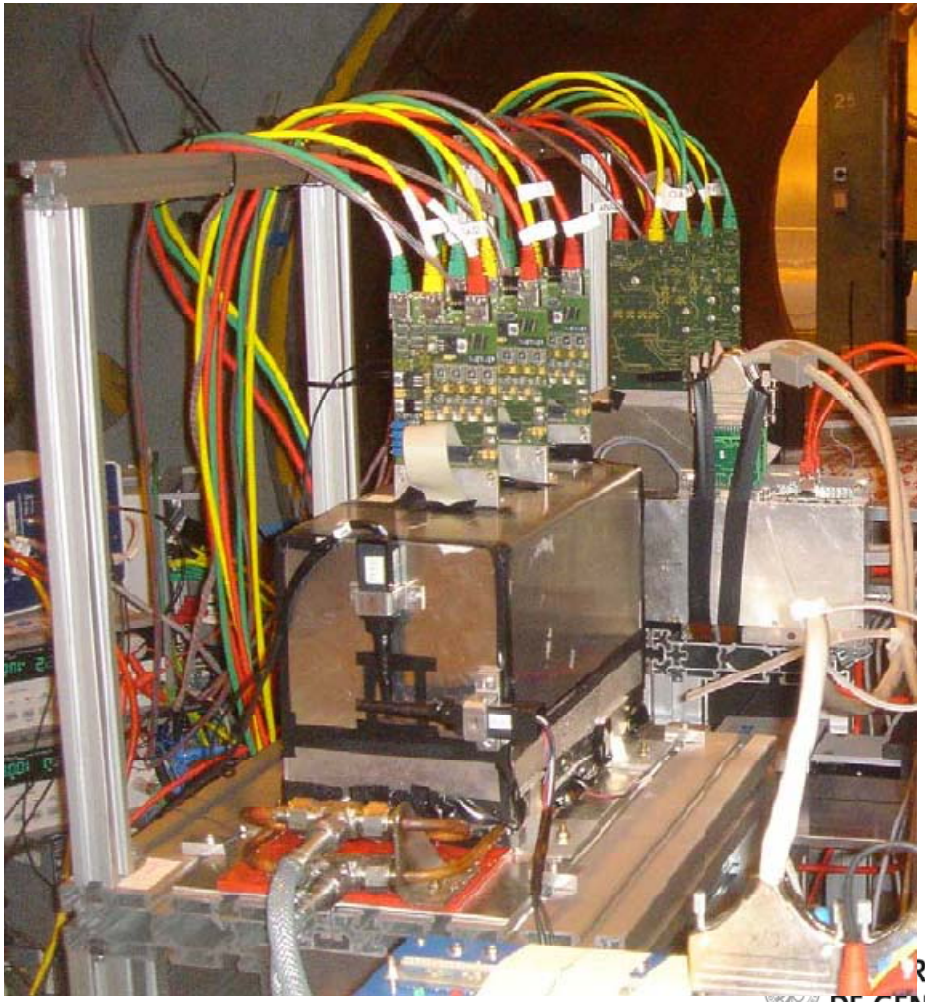
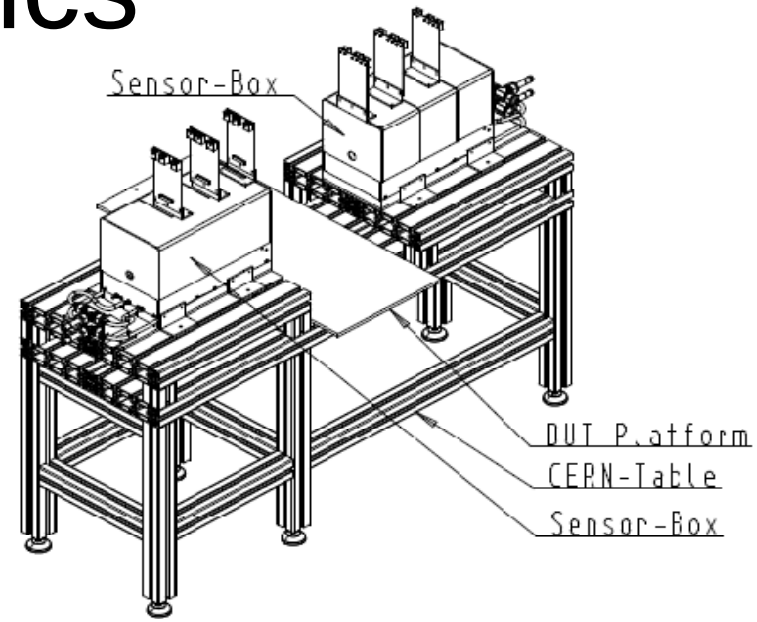
Telescope in H8 (CERN)



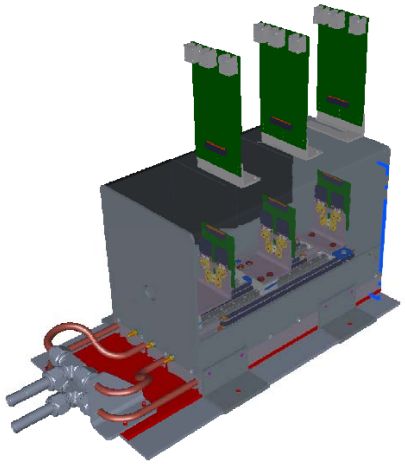


Mechanics

- For CERN Testbeam the original mechanics was used for the first time

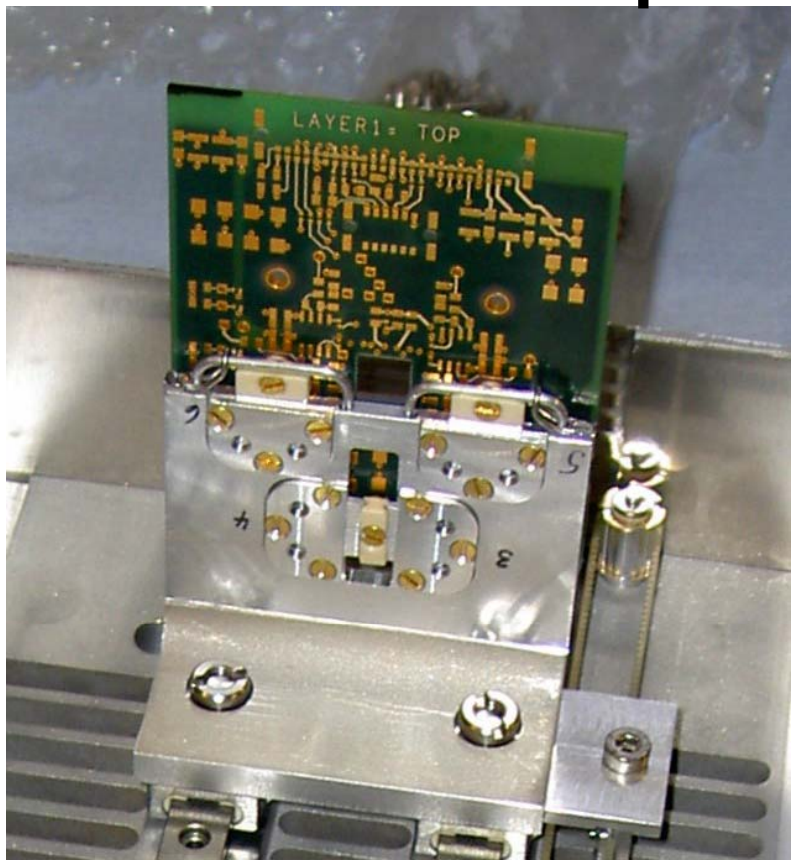


- Two boxes with 3 sensors each
- Distances 10 cm within one box, 34 cm from one box to the next
- Big gap for users DEPFET and SiLC



- Features:
  - Cooling from below -> no risk of watering the sensors
  - Positions adjustable

Close-up of mechanics



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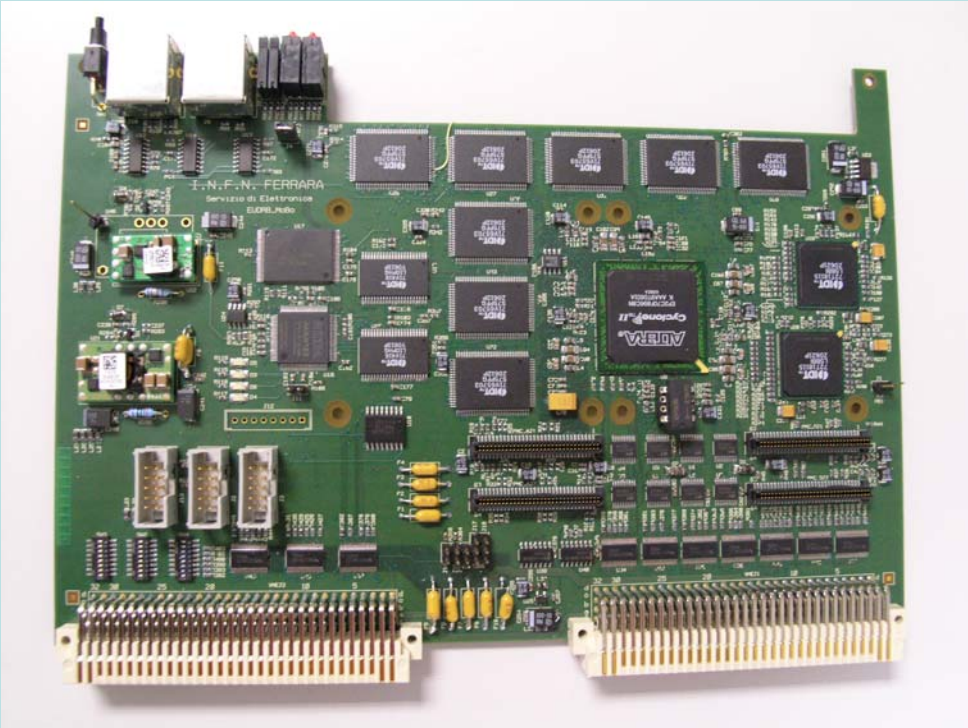
A VME64x/USB2.0-based DAQ card for pixel sensors



mother board built around an ALTERA CycloneII FPGA (clock rate: 80MHz) and hosting the core resources and Interfaces (VME64X slave, USB2.0, EUDET trigger bus)

NIOS II, 32 bit "soft" microcontroller (clock rate: 40MHz) implemented in the FPGA for

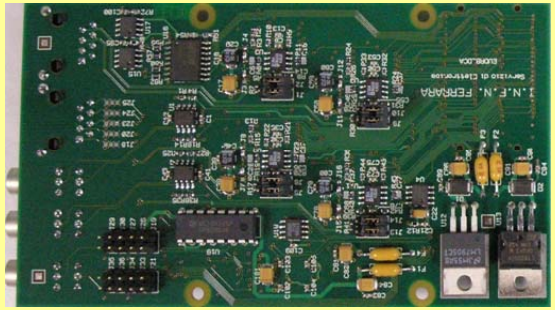
- on board diagnostics
- on-line calculation of pixel pedestal and noise
- remote configuration of the FPGA via RS-232, VME, USB2.0

Two readout modes:

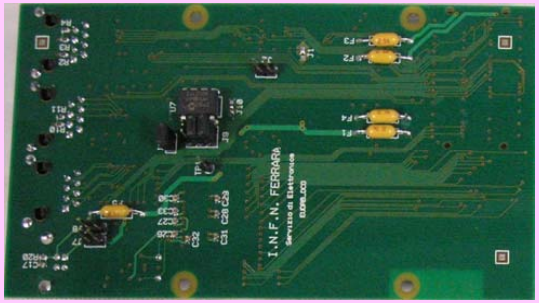
Zero Suppressed readout to minimize the readout dead-time while in normal data taking.

Non Zero Suppressed readout of multiple frames for debugging or off-line pedestal and noise calculations

analog daughter card based on the successful LEPSI and SUCIMA designs



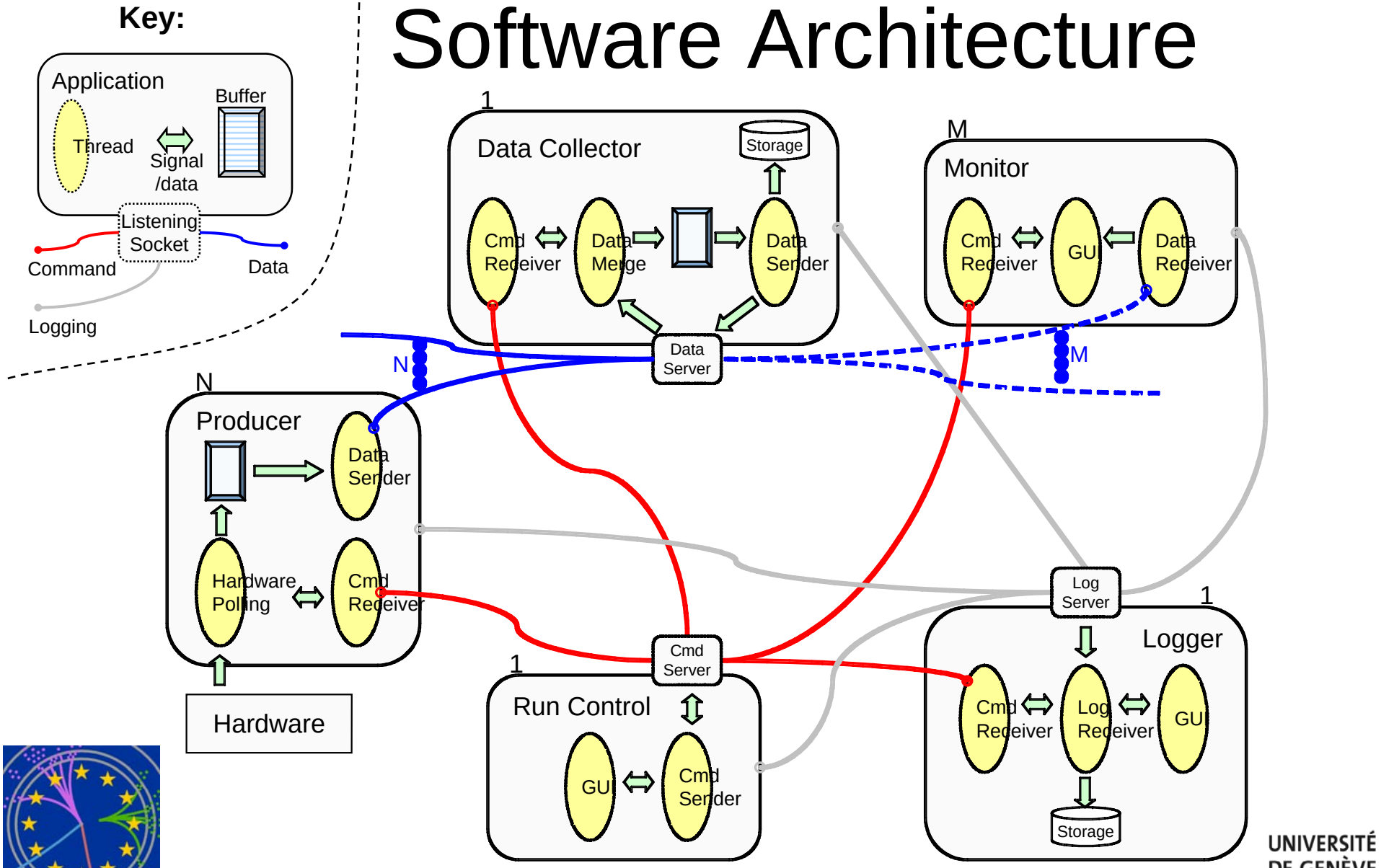
digital daughter card drives/receives control signals for the detectors and features a USB 2.0 link



EUDRB - Characteristics

- On board sparsification of data
- VME and USB2 readout
- Data transfer 40 MB/s over VME (burst) today
- Mother and daughter board architecture for maximum flexibility

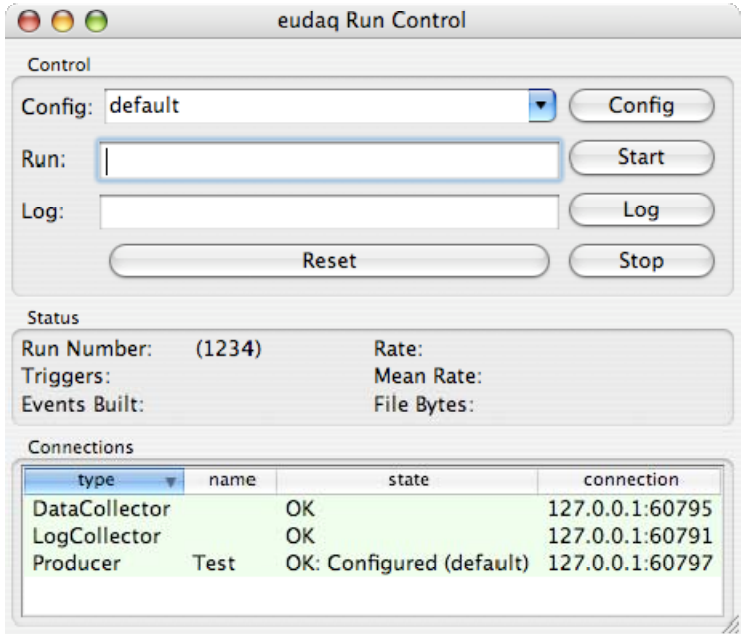
Software Architecture

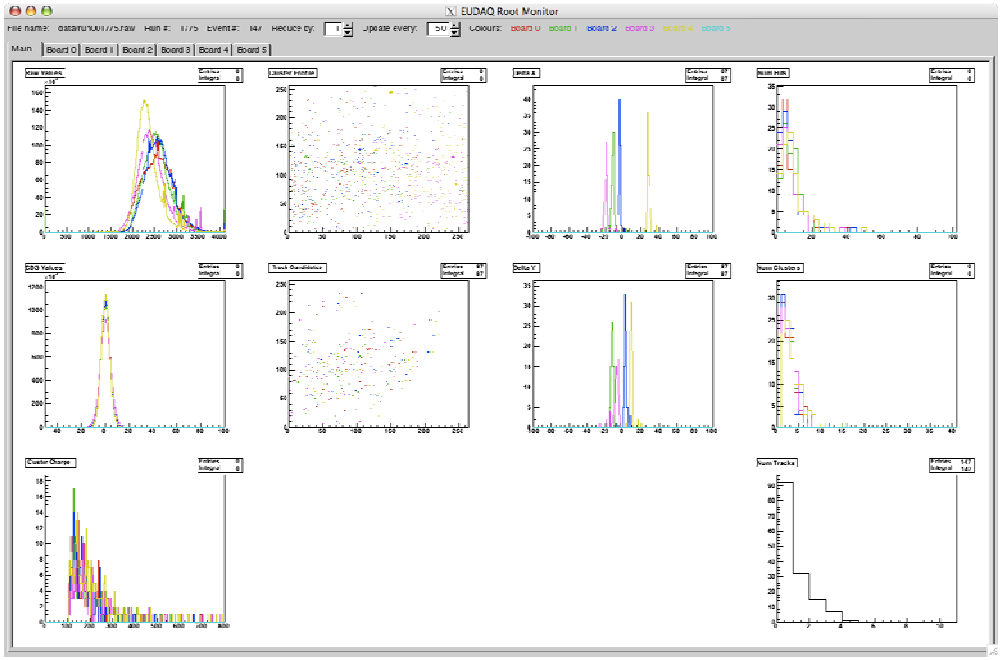


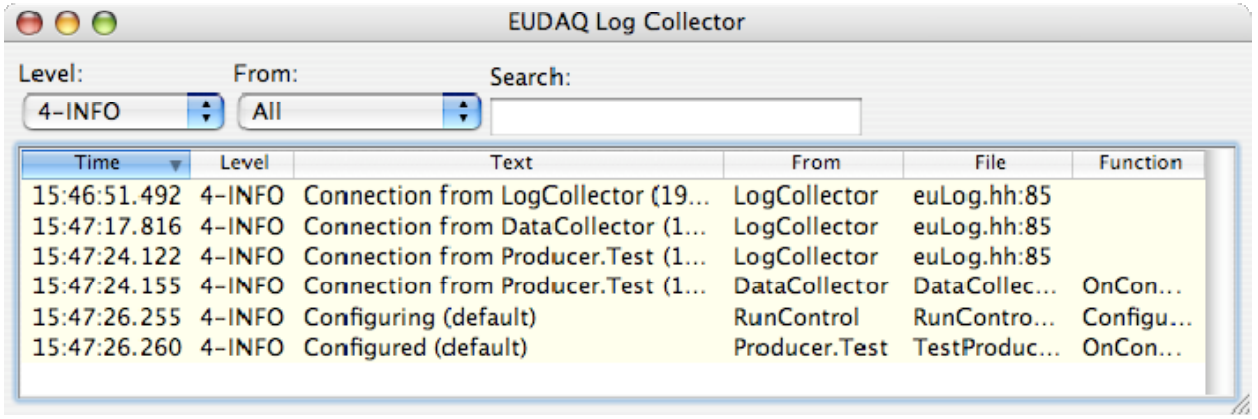
Software

- Custom DAQ software written in C++
- Uses POSIX for threads and sockets
- Run Control GUI using Qt
- Online Monitor using Root
- Runs on Mac OS X, Linux, and Windows (using cygwin)
- Highly modular, allowing DUTs to be easily integrated into the framework
- Software available at: http://eudet.unige.ch (or currently http://eudetmac001.cern.ch)

Graphical Interface







Data

- Data is read out and stored in custom binary format on local RAID array
- Manually copied to GRID for conversion to LCIO, then clustering and tracking
- Now that conversion is validated we can think about writing directly in LCIO
- Then automate copying to GRID and initiation of processing

Remaining Issues

- Optimisation of sensor board supports
- Readout speed needs improving, mainly in VME library
- Software documentation

Conclusions

- Mechanics approaching final version
- Readout working well, with some speed optimisation needed
- Software reasonably usable and stable
- Demonstrator has been successfully used in 3 test beams, 1 with an integrated DUT, and is currently at CERN for the SiLC testbeam