JRA3: DAQ Overview

Objectives

System Overview

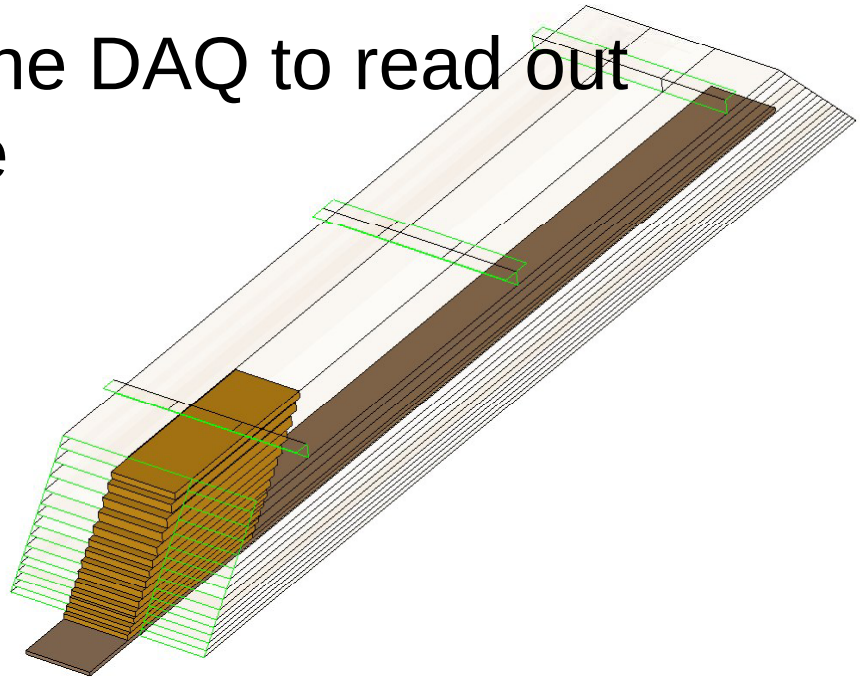
Status of DAQ Components

Outlook

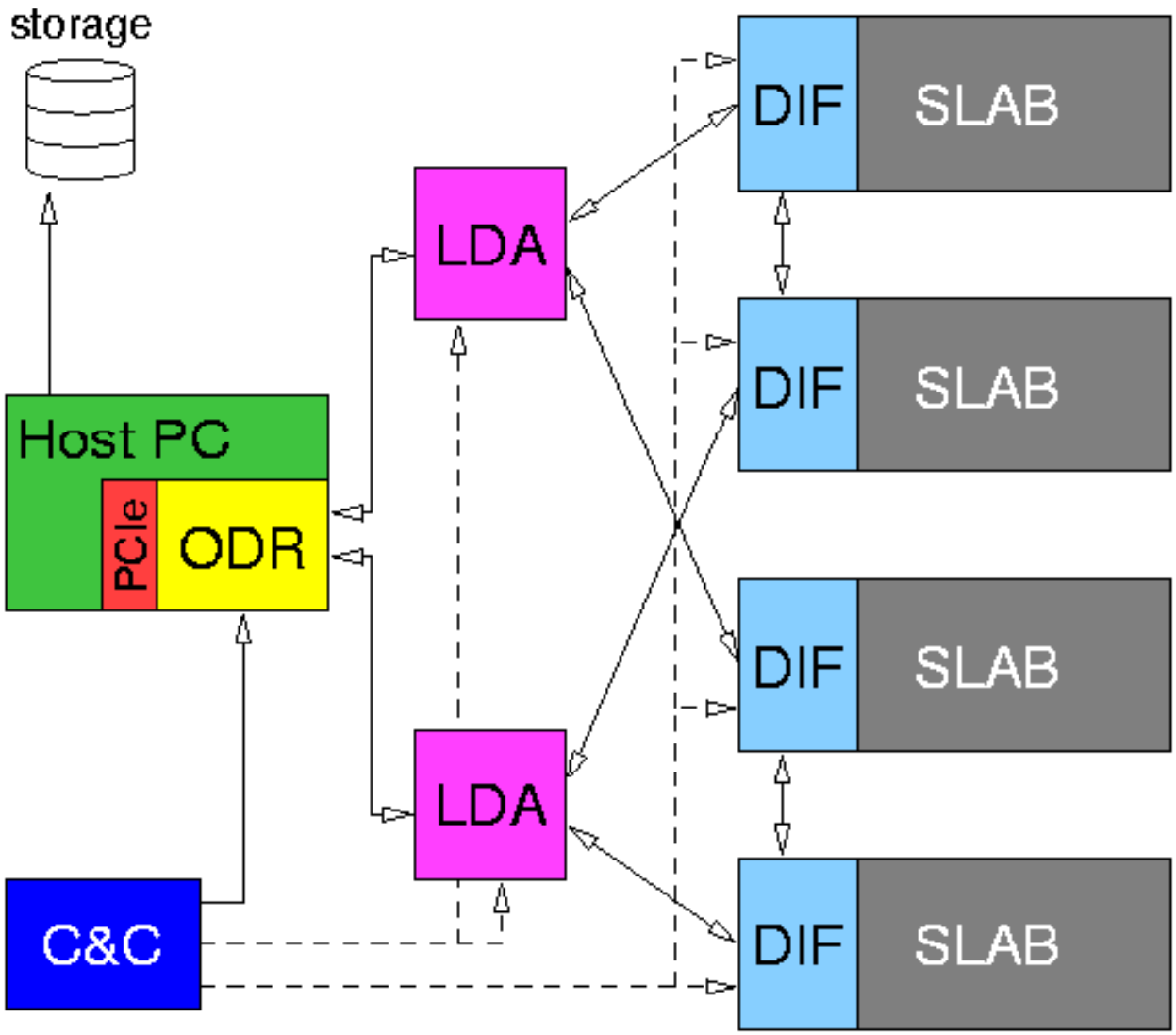
DAQ objectives

- Perform DAQ tasks for a ILC Calorimeter Detector using a scalable system built from commercial off-the-shelf components

- Build a small-scale version of the DAQ to read out the EUDET calorimeter module



DAQ architecture



DIF: Detector InterFace

LDA: Link/Data Aggregator

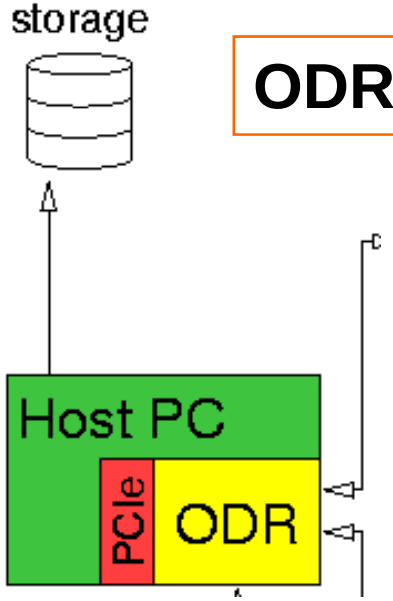
ODR: Off-Detector Receiver

C&C: Clock & Controls

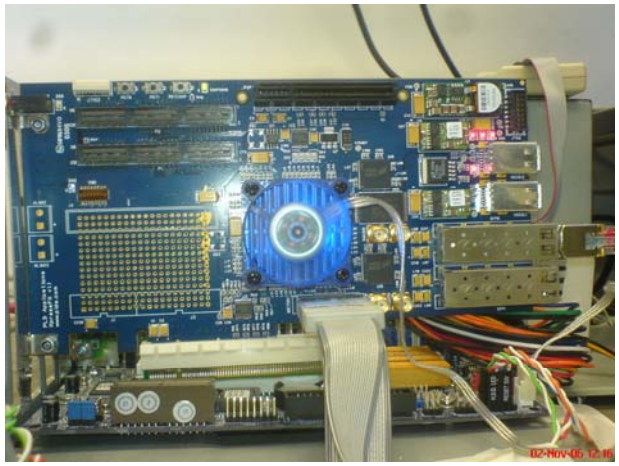
PCIe: PCI-Express

- Slab hosts VFE chips
- DIF connected to Slab
- LDA servicing DIFs
- LDAs read out by ODR
- PC hosts ODR, through PCIe
- C&C routes clock, controls

Off-Detector Receiver

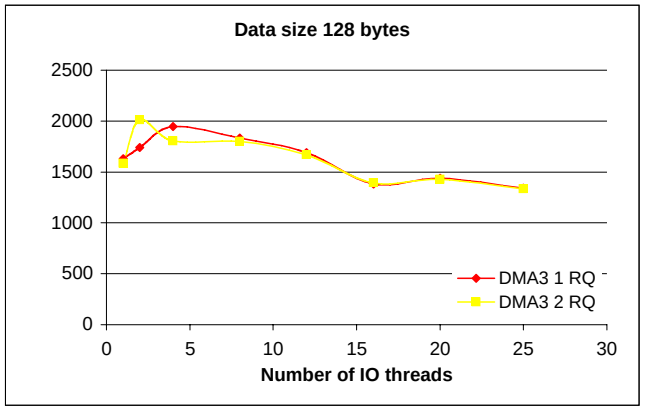


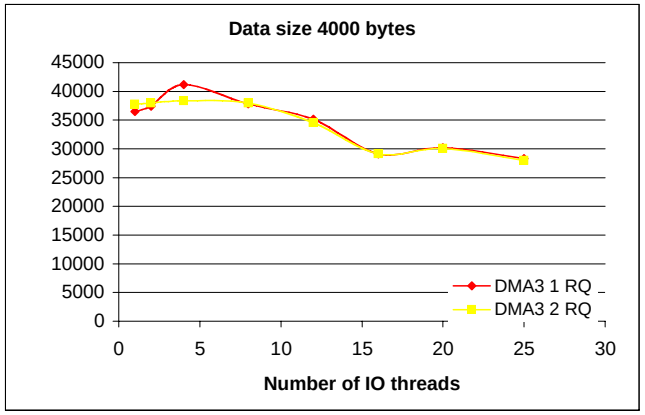
ODR is the interface between DAQ and the 'PC-world'



- ODR is a commercial FPGA board with high speed serial interfaces and a PCIe host bus
  (Virtex4-FX100, PCIe 8x, etc.)
- Customised firm- and software:
  DMA driver pulls data off the onboard RAM, writes to disk

ODR Data Rate Studies

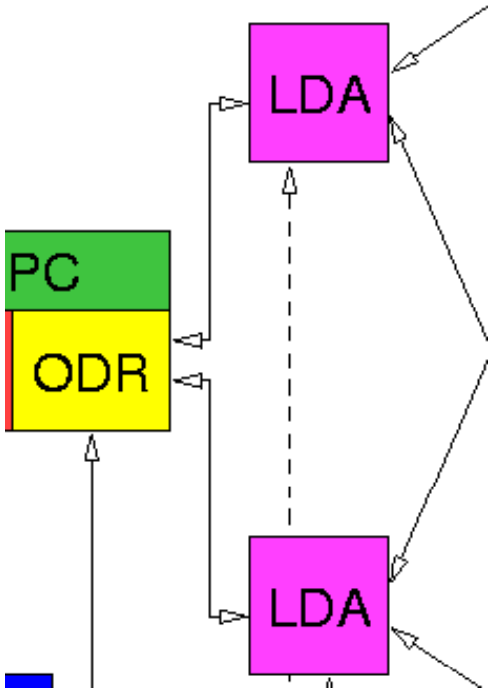




- Data rate studies lead to identification of bottlenecks
- Re-iterate on firmware, software
- Firmware update to full-width (and speed) data path
- Plans: firmware development and integration of
  - High-Bandwidth DDR2 RAM controller
  - Hi-Speed data links (Gbit Eth/TLK2501)

Link/Data Aggregator

LDA interfaces many DIFs with few high-speed links

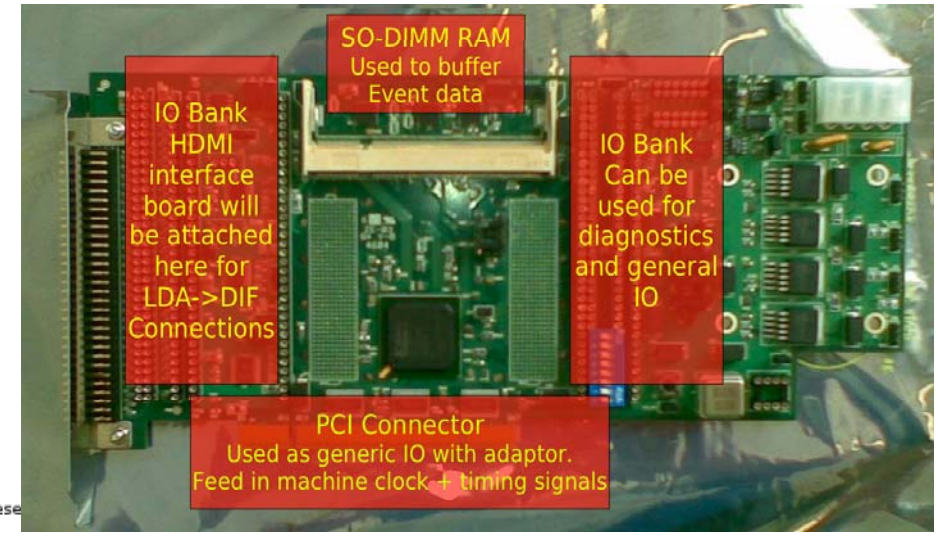


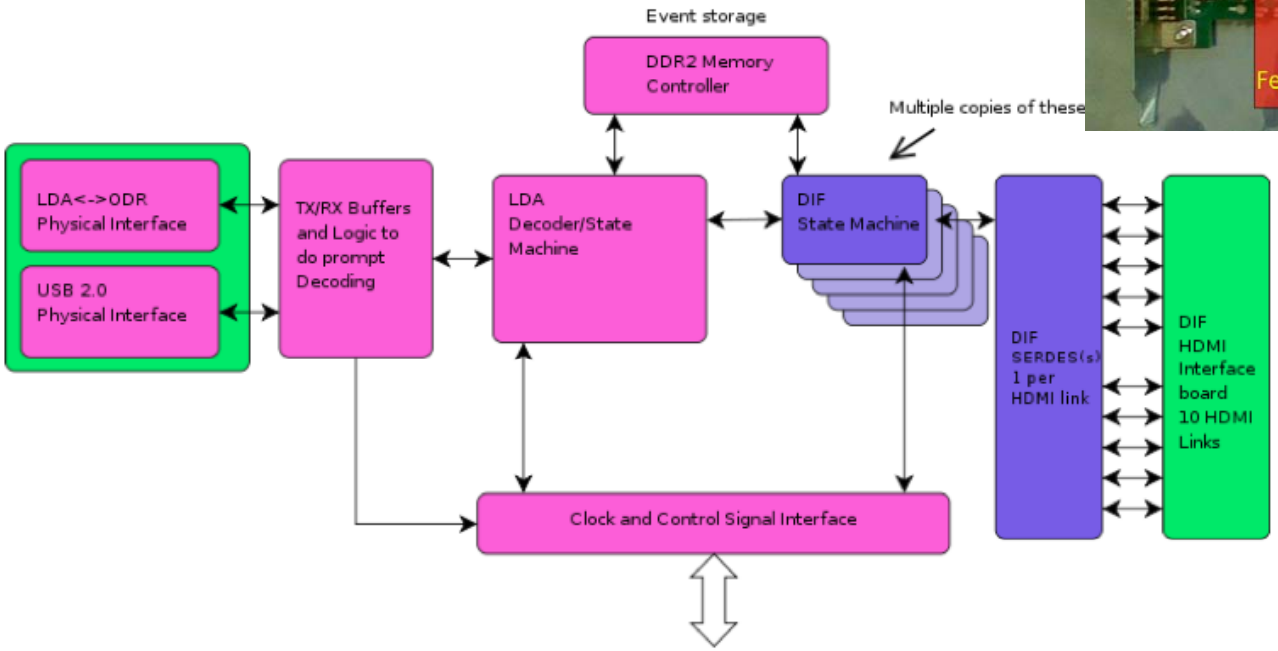
- Handles dataflow from DIFs
- Manages commands to & from both DIFs and ODRs
- Robustness through simplicity:
  - Unaware of exact data content
  - Abuse-resistant through design

LDA prototype

Prototype is a commercial FPGA board with customised firmware and hardware add-ons:

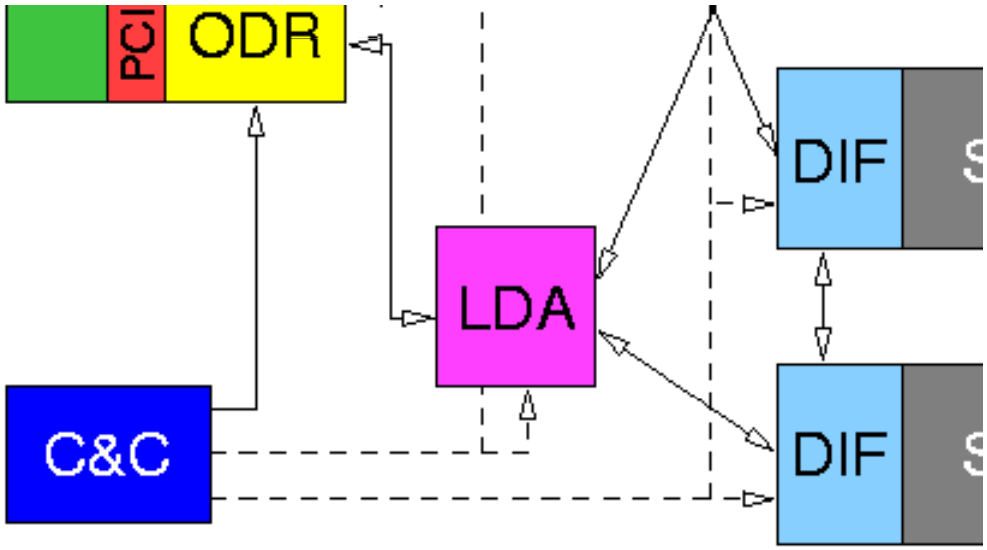
- High-bandwidth link to ODR
- Many links towards DIFs





- Enterpoint Xilinx Spartan3 based dev. board
- RAM & lots of I/O (including PCI)

Clock & Controls Distribution

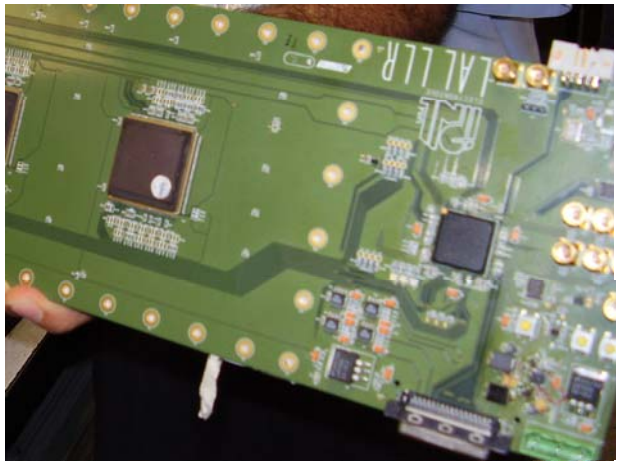


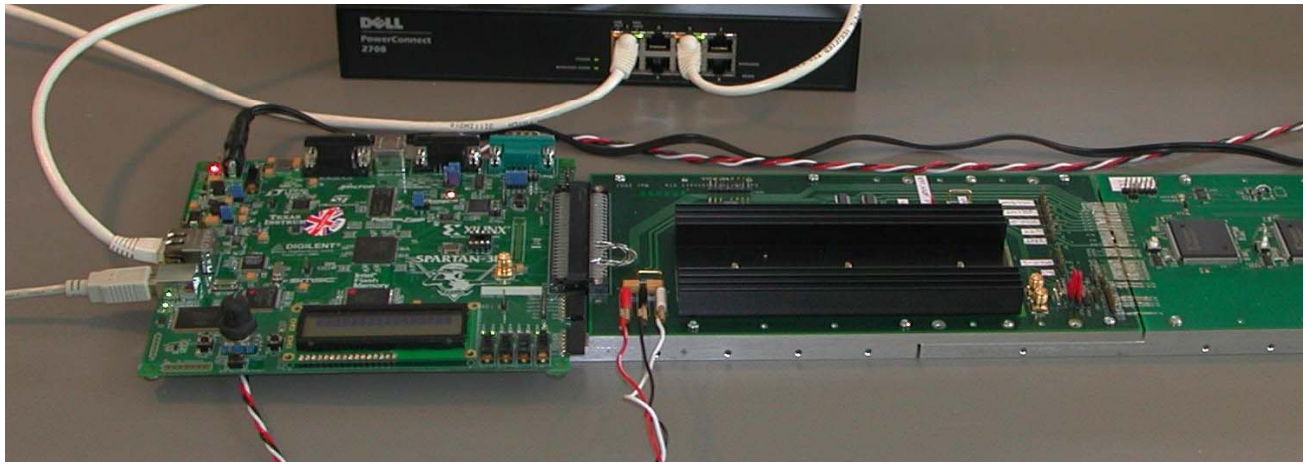
- C&C unit provides machine clock and fast commands through ODR and LDA towards DIF
- Possibly partial integration with ODR

- Fast Controls: encoded commands on the LDA-DIF link
- Slow Controls/Configuration: block transfers on LDA-DIF link
- Low-latency fast signals: distributed ‘directly’

Detector InterFace

- Sits at the end of detector slab PCB
- Directly connected to the Front-End chips
- Integral part of the detector





- Various prototypes developed for specific tasks

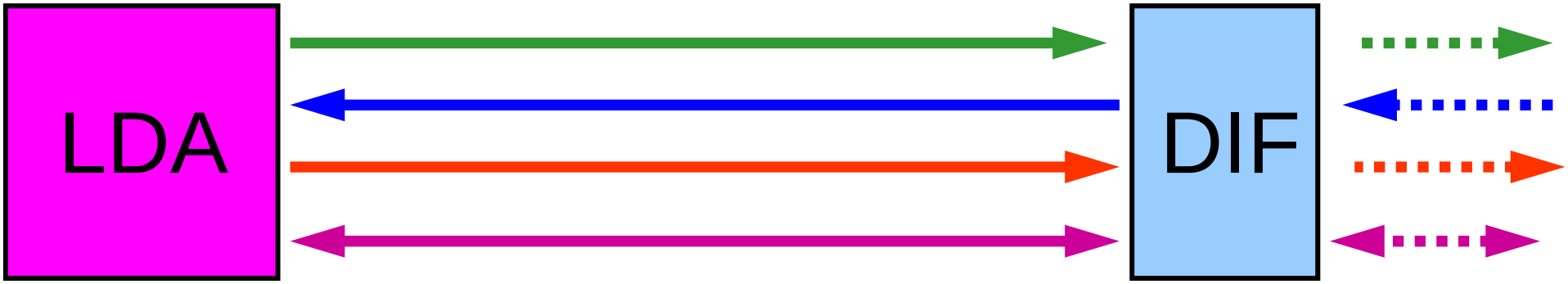
LDA-DIF communication

Clock: provide machine clk + synchronisation

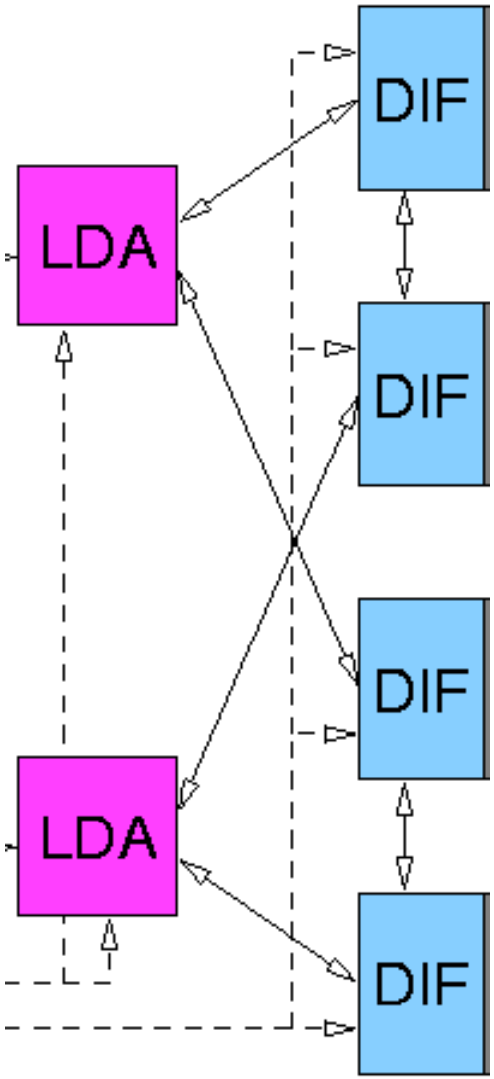
Data: large block transfers from DIF to LDA

Fast control commands: immediate action

Block transfers for confguration of VFE chips



LDA-DIF link



LDA-DIF link:

- Serial link running at multiple of machine clock
- 50Mbps (raw) bandwidth minimum
- robust encoding (8B/10B or alike)
- anticipating about 10 DIFs on an LDA
- LDAs serve even/odd DIFs for redundancy

	Gnd	2	1	Clk+	Pair1 (STP)
			3	Clk-	
Pair2 (STP)	DL2D+	4	5	Gnd	
	DL2D-	6	7	DD2L+	Pair3 (STP)
	Gnd	8	9	DD2L-	
Pair4 (STP)	SpD2L+	10	11	Gnd	
	SpD2L-	12	13	Pow1	
	Pow2	14	15	SpL2D+	Pair5 (UTP)
	SpL2D-	16	17	Gnd	
	Pow3	18	19	Pow4	

Possible Pinout for HDMI
(Based on SAMTEC HPDPI cable signal designation)

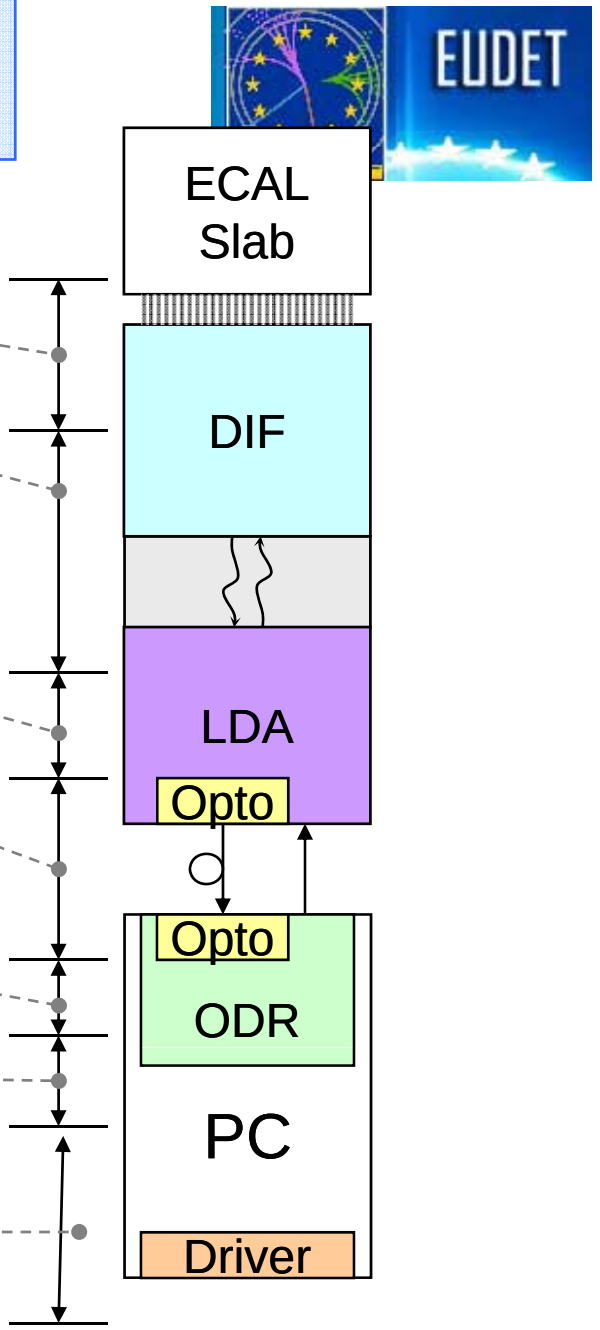
DIF implementation

- The Slab is an integral part of the detector
- The LDA and ODR are transparent wrt detector type

- The DIF and its interface to the slab is detector-specific
- Large parts of the DIF firmware must be generalised
- *DIF hardware should support firmware* to profit from common developments
- DIF working group: AHCAL, ECAL, DHCAL + DAQ
- DIF wg to address common problems and share knowledge, experience, and VHDL code

UK Read-out work (ECAL FE)

- Detector Interface (Cambridge, Imperial College)
  - Spec + hardware
- DIF to Link/Data Aggregator (Cambridge, Manchester)
  - Spec + hardware
- Data aggregate, format (Manchester)
  - Hardware + firmware
- LDA to ODR opto-link (Manchester, UCLondon)
  - Hardware + firmware
- ODR (Royal Holloway, UCLondon, Cambridge)
  - firmware
- ODR to disk (Royal Holloway)
  - Driver software
- DAQ Software (Royal Holloway, UCL, Imperial College)



DAQ Software

- Aim for modular, upgradeable software components
- Compilation of list of EUDET DAQ requirements
- Investigation of existing frameworks used, both in HEP and industry:
  - EPICS
  - ACE
  - DOOCS
- So many nice features to choose from…. not easy!

JRA3: DAQ Outlook

- Hardware and firmware development ongoing in many areas, software is being investigated
- DIF working group formed to address common issues, centralize VFE-DAQ discussion and avoid triplication of work
- Development ongoing for all components in a full system chain:

  Software, ODR, LDA, DIF, Slab