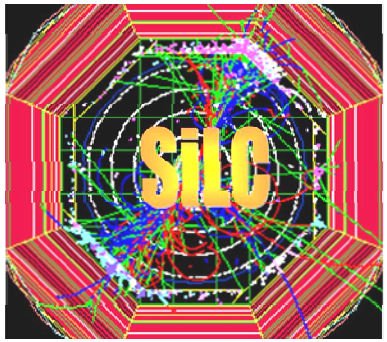


JRA2/SiTRA report

EUDET Annual Meeting

9 October 2007

Zdenek Dolezal

Charles University Prague

On behalf of the SiTRA activity in EUDET:

HIP-Helsinki, LPNHE-Paris, Charles U. Prague, IFCA/CSIC Santander

and

IMB-CNM/CSIC Barcelona, Liverpool University,

OSU Obninsk, IFIC/CSIC-Valencia, HEPHY Vienna

(associated Institutes)

The work reported here is also part of the SiLC R&D Collaboration

Outline

- Large size prototypes
- Cooling prototype
- Alignment prototype
- Front end electronics
- Test beams
- Status of deliverables
- Conclusions

Construction of large structure
Silicon tracking prototypes for test beam

- New sensors
  - ► New μstrip sensors from HPK, including test structures and special treatment for alignment.
  - ► Thinning tests by LPNHE with Edgetek
  - ► Direct wiring of the FEE onto μstrips (LPNHE, HPK)
  - ► Prospects: New Firms (apart from HPK), New technology
- Developing tooling for a new module construction
  - ►Based on already existing one: IEKP
  - ► Starting expertise: LPNHE (plus collaboration with CERN)
- Design and construction of large prototypes
  - ►Two main cases:
    - plans of Si layers for central or XUV Forward (1st by end 2007)

(can be used for combined tests with μvertex or calorimeter prototypes)

- and prototype for LCTPC combined test (2008)

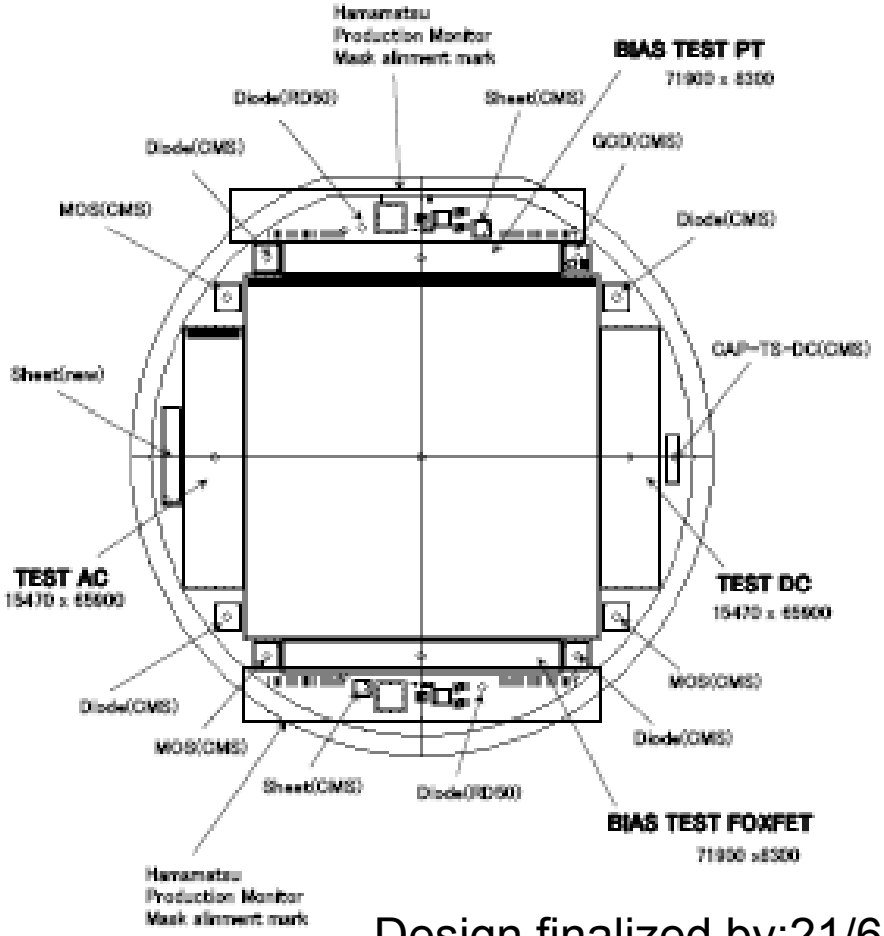
N.B. NO EU funds for construction of large size Si structures/prototypes

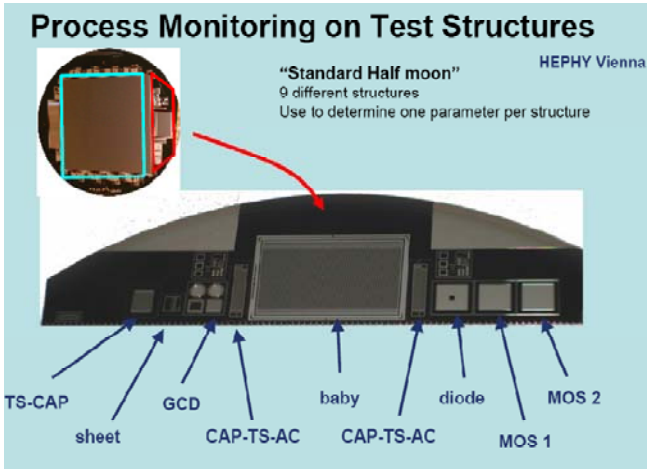
SiIC work program for sensor R&D 2007-2008

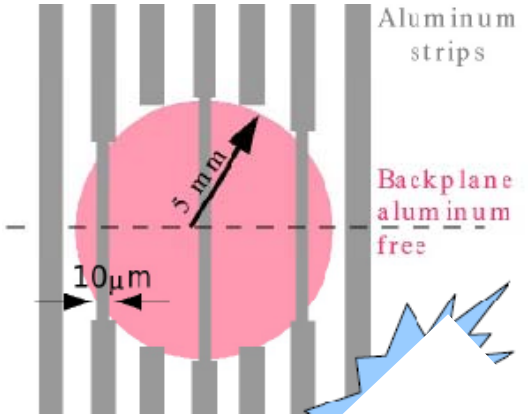
IEKP Karlsruhe, HEPHY Vienna, LPNHE, IFCA+IMB/CSIC, HPK

- Step 1 (2007)
  - ✓ Wafer thinning (100, 200, 300µm)
  - ✓ Strips larger wafer (50 µm pitch)
  - – Test new readout chips (DC coupling, power cycling)
  - ✓ Improve standardized test structures and test setups
- Step 2a (2008-)
  - ✓ Move from pitch adapter to in-sensor-routing
  - – Test crosstalk, capacitive load of those sensors
- Step 2b (2008-)
  - ✓ Test 6” double sided sensors (LPNHE + Canberra)
- Step 2c (2008-)
  - 8” (12”) single sided DC wafer
- Step 3 (2007-)
  - New firms (Liverpool+Micron & E2V)
  - New technology (IMB-CNM, HIP, VTT, HEPHY, LPNHE)

New 6'' μstrip wafers (HPK), tests structure(HEPHY) designed and produced: sensors are 9.05x9.05cm^2, 320μm thick, 50μm pitch; 5 sensors out of 35 ordered are speciall treated for alignment with laser; Delivered last week so (hopefully) available for Oct 07 and for sure for LCTPC 08.







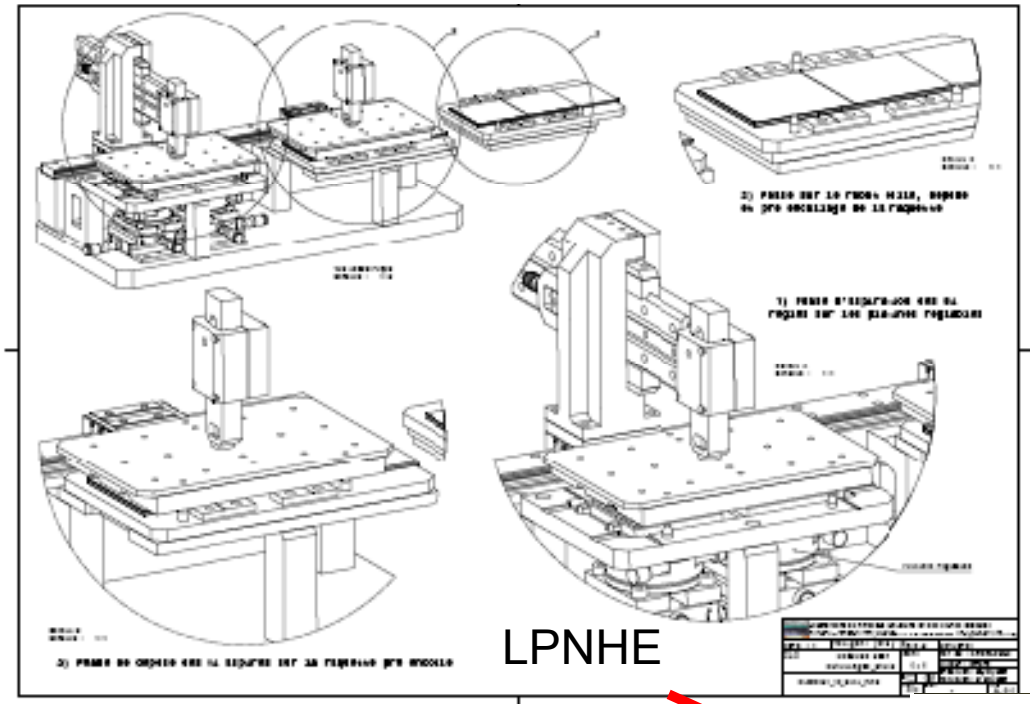
Design finalized by:21/6/07

More details at T. Bergauer's talks at JRA2 parallel session

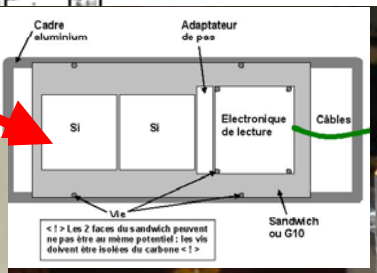
5 wafers treated for alignment (hole on the back side)

N.B.: NO E.U. funding for Si sensors

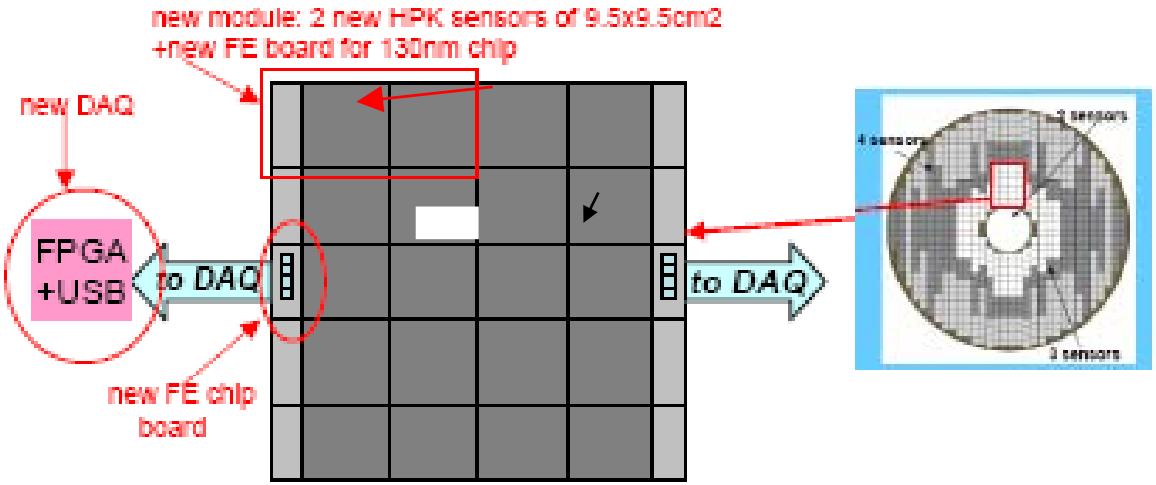
Tooling for construction of modules:



- Need for developing new expertise and tooling at LPNHE (well in progress)
- and use of already existing expertise and tooling: IEKP Karlsruhe
- Bonding Lab at CERN (A. Honma, I. McGill, M. Moll)

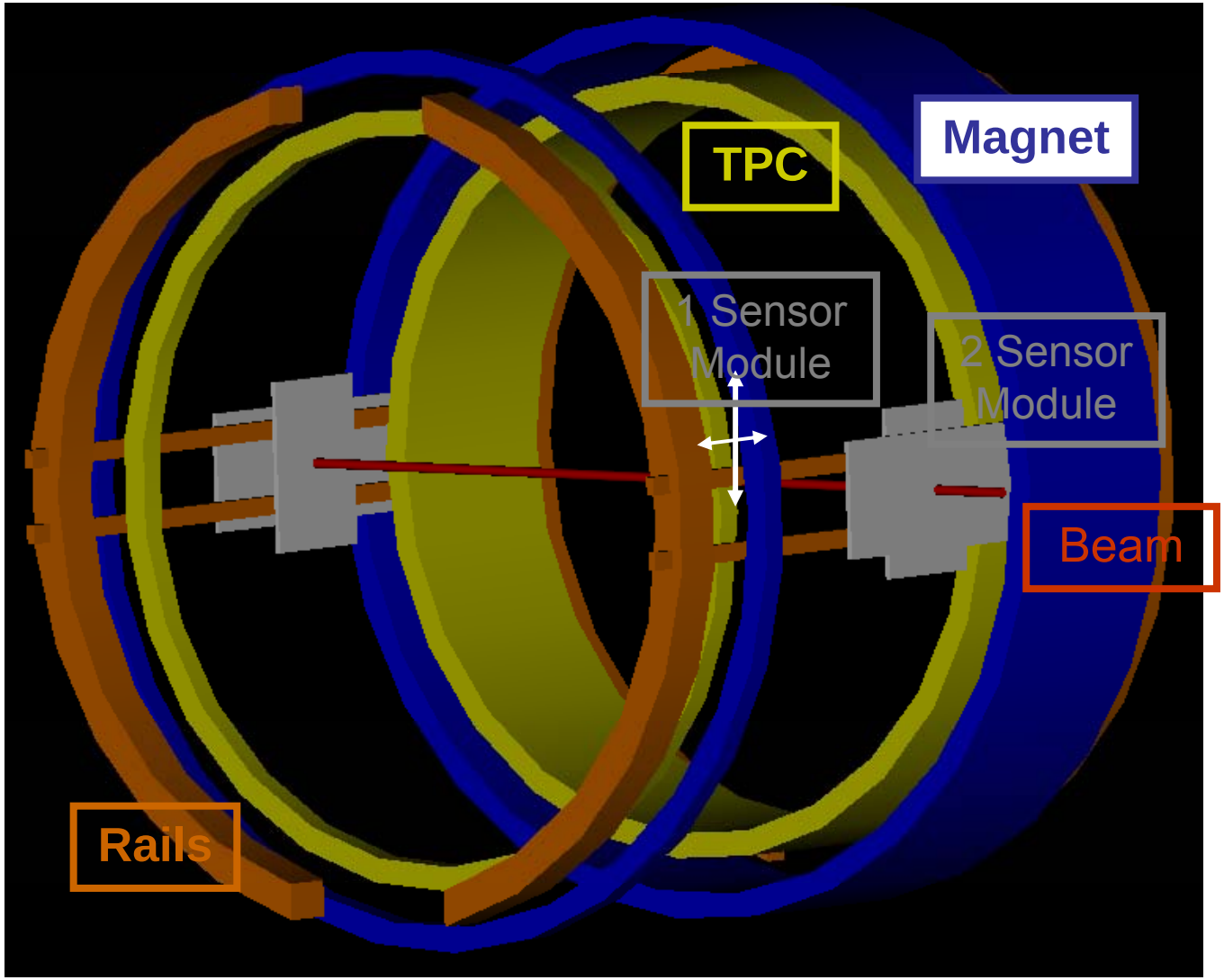


Large size Si prototypes:



✓First prototype of large size (mechanical structure ready end of 2007). Evolutive system.
✓2 first modules will be tested in CERN T.B. in Oct 2007.
✓4 planned to be built and equipped (sensors and FEE) for 2008-2009 T.B.
✓Will provide 2 XY/track or 1 XUV if FWD.
✓Cooling prototype will be adapted to it.
✓System available for combined test beam with μvertex prototypes and/or Calorimeter prototypes
✓Alignment system prototype (IFCA) will be included to it.

Tests with LP TPC
(IEKP, HEPHY, LPNHE)



Tests with LP TPC

Sensors: HPK 6’

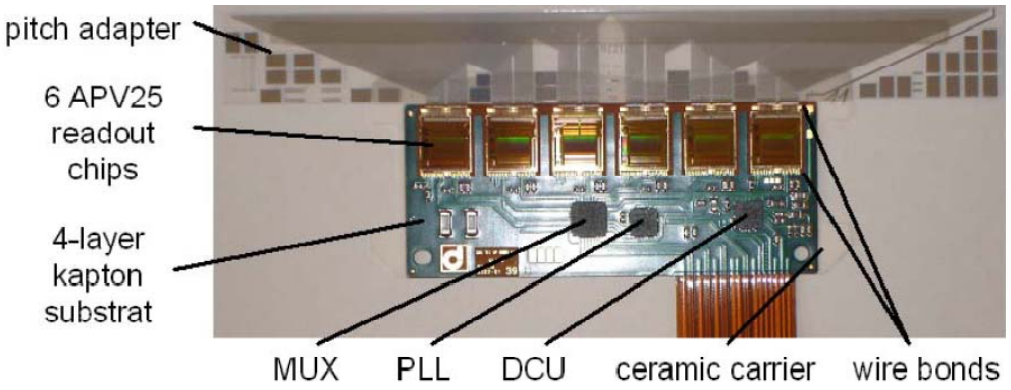
FE electronics:

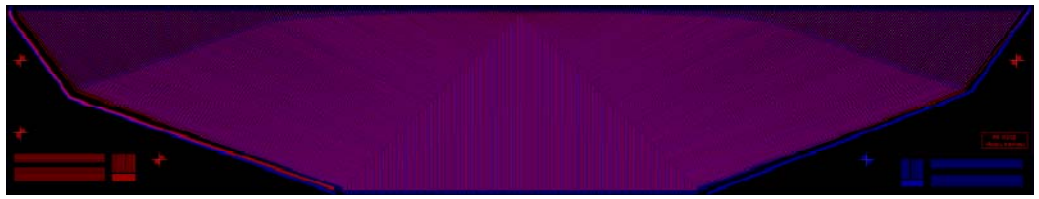
- Short term (2008):

  CMS ASICs + CMS hybrid
  CMS R/O

- Long term: SITR 130_128

Pitch-adapter: specially designed





SITRA-LP TPC Plans

1st half of 2008: Cosmic Run:

- Limited readout area: 38,4 cm^2
- 18 muon coincidences expected per day
- Too much effort for this? No, first system test of TPC+Si readout systems

Support structure for Cosmic Run

- has to be rotated by 90°
- Problem of space with field cage support (half-shells), which are in this region (top/bottom of TPC)
- Half-shells have been/will be replaced by array of round bars

2nd half of 2008: Beam test

- Eventually with new hardware from LPNHE Paris
- Mechanics under development

More details at T. Bergauer's talk at JRA2 parallel session

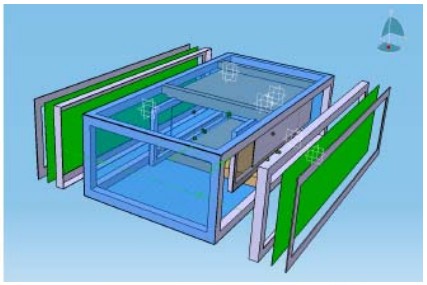
COOLING PROTOTYPE *(LPNHE +OSU+Torino U.)*

Cooling and insulating frame

prototype expected to be ready for October 2007

Insulating cage for DESY test beam

N.B. almost NO funding



Final prototype in composite material will be made with help of OSU &Torino U.

Actual FEE results: ~ 0.6mWatt/ch
No Power cycling included yet
→Main problem: power dissipation from neighbours

	Preamp	Shaper	Zero suppr.	Pipe-line	Total Analog	ADC	Logic	Total Digital
180nm/ch	90	180			270			
130nm/ch	148	148	198	10	575	66		
Common				100		5	96	101

Alignment prototype

IMB-CNM & LPNHE
New sensors (FEE)

Basic idea (developed first by AMS & CMS):

Use laser beam in the IR region ("pseudo-track" of infinite momentum) to cross several sensors consecutively. Main advantages:

- **No mechanical transfer errors between fiducial marks and the modules**
- **Minimum impact on system integration and none on DAQ**

Two-fold approach:

1) Integration with SiTra:

1.1) Mandatory change in the module:

∅~10 mm window where Al back-metalization has been removed (requires 1 new mask and sensor backprocessing)
(This is included in new HPK sensors)

1.2) Optional changes in alignment window

Strip width reduction
Alternate strip removal
Thickness optimisation

→ Transmittance improved

2) R&D on transparent Silicon µstrip sensors:

- IFCA with IMB-CNM (Barcelona) develops prototypes of new sensors that can achieve maximum transmittance in a wavelength range
- Study utilization of semi-transparent electrodes as strips as an alternative to Aluminum
- Wide margin for changes and experimentation to obtain best optical and electrical sensor

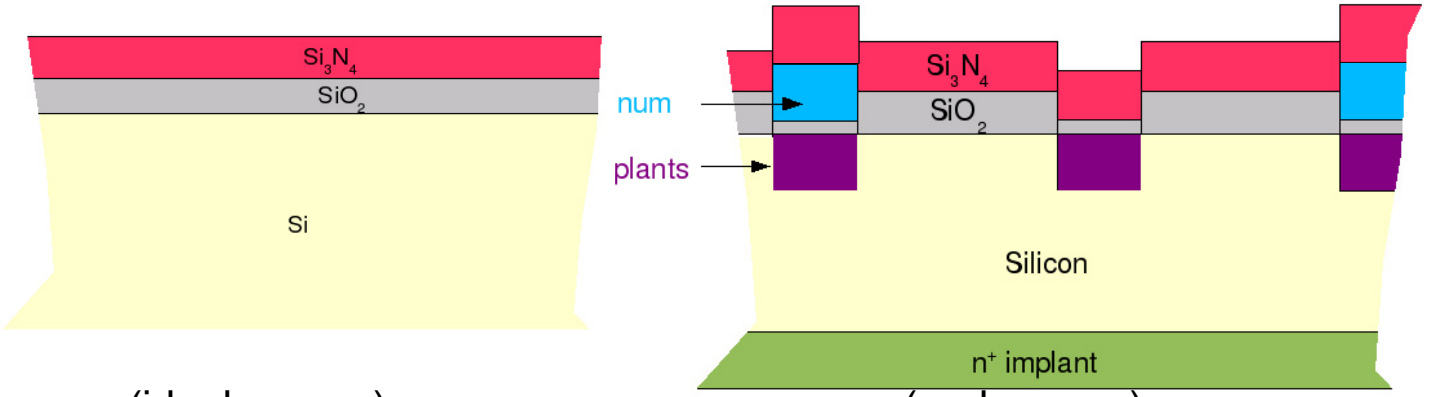
Status

SiTra prototype:

Ordered 5 sensors to HKP with alignment window (to be tested on optical test bench & test beam)

R&D IFCA-Santander&CNM-Barcelona:

- Scalar simulation of multiple reflections inside the multilayer of the sensor **… done**
- Optimization of multilayer design to achieve maximum T at λ_{IR}±5nm (laser spectral width) **… done**
- Vectorial simulation of diffraction processes due to strip segmentation ... **in progress**



(ideal sensor) (real sensor)

Basic samples will be produced by IMB-CNM on September to:

- characterise each layer individually (refraction indexes)
- study the effect of Silicon doping on transmittance
- Validate scalar and vectorial simulation

Optical testbench

Lab testbench for sensor characterization commissioned at IFCA

Component status:

Focusing & steering optics already received
DAQ electronics available and currently under programming
Automated 3D stages by the end of September
Beta source for testing by the end of the year
Black-box under construction
IR laser @ 1060 nm

N.B. NO Funding from E.U. except for F.E.E.

More details at I. Villa's talk at JRA2 parallel session

3D Motorised Test Bench

All components acquired (DAQ and trigger electronics, large range XYZ stages, laser source)

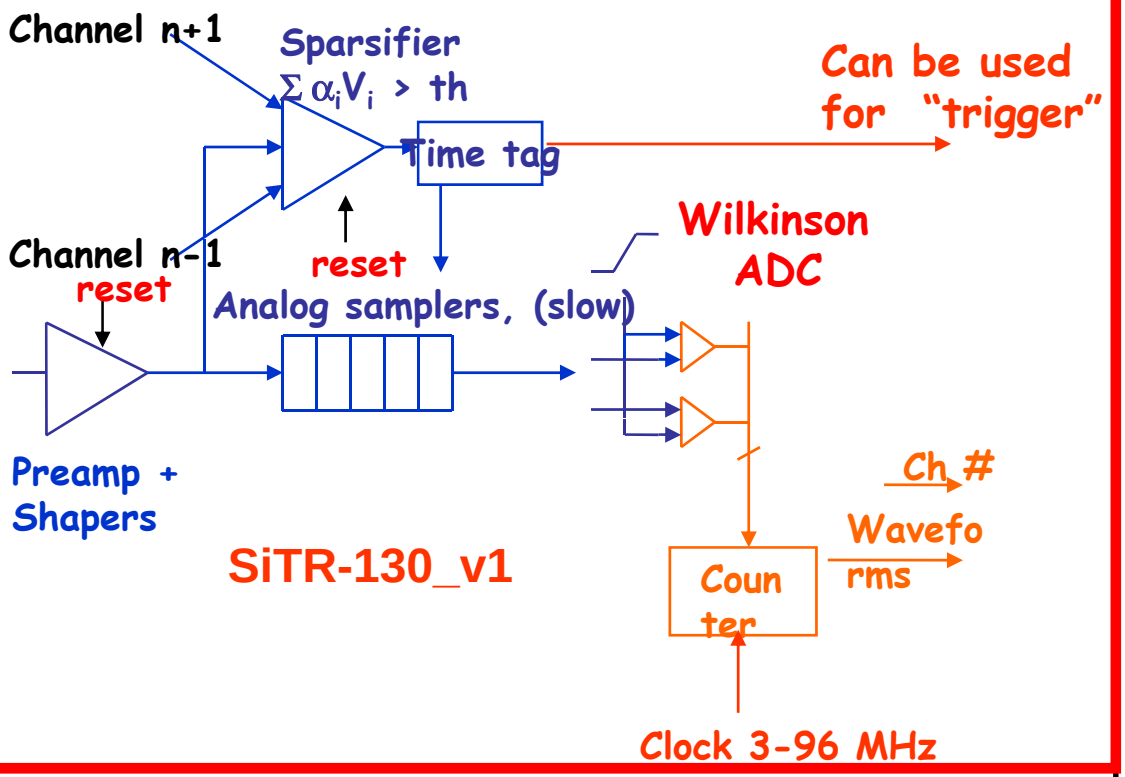
Currently working on mechanics and DAQ programming.

To achieve a maximum positioning accuracy we want to integrate a interferometer head for measuring the stages displacement with submicron accuracy.

First test with newly acquired HPK sensors.

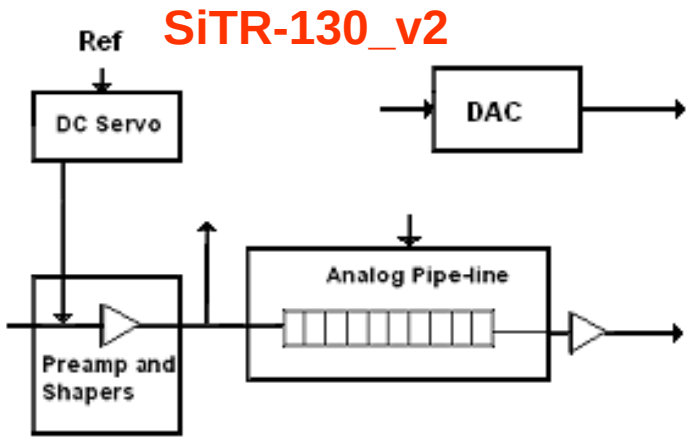
FE Electronics: *(LPNHE + LAPP (SiLC))*

- **Tests of 2 versions SiTR-130_v1 et _v2 sent to foundry in 2006**
- **Design of SiTR-130 for mini production and equipment of prototypes in 2008**



Version 1: LPNHE *Received end 2006*

Functionality tests: OK, tests with Si detector & detailed characterisation: in progess



Version 2: LAPP

(D. Fougeron +R . Hermel)

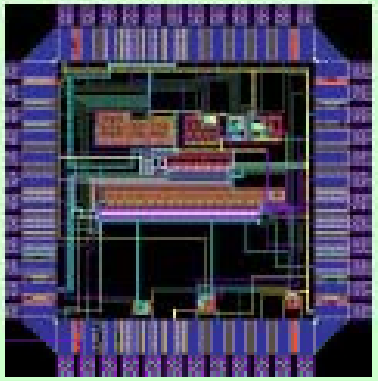
DC servo adapted to sensors with DC coupling

DAC: calibration

Pipeline improved wrt version v1.

Received 5/1/07: test at LAPP

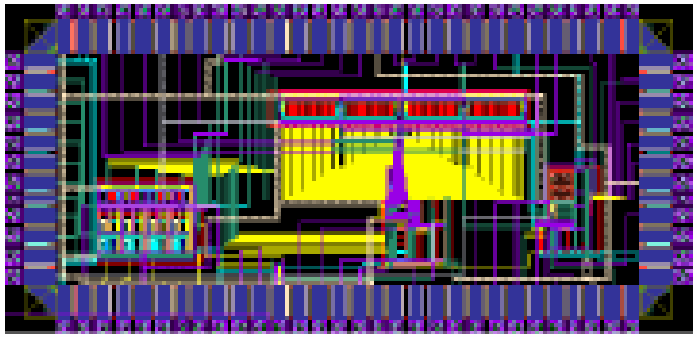
Layout & photographs of the chips SiTR-130_1 and _2



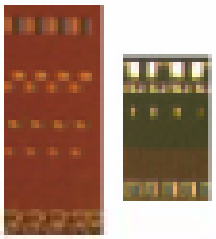
Layout

Picture

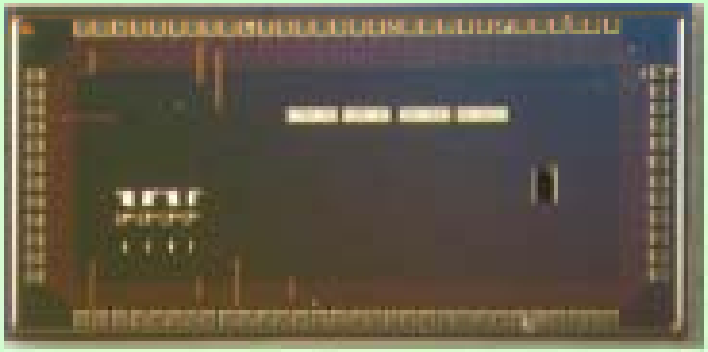
One channel 1.5 x 1.5 mm^2



Layout of the 130nm chip including sampling and A/D conversion



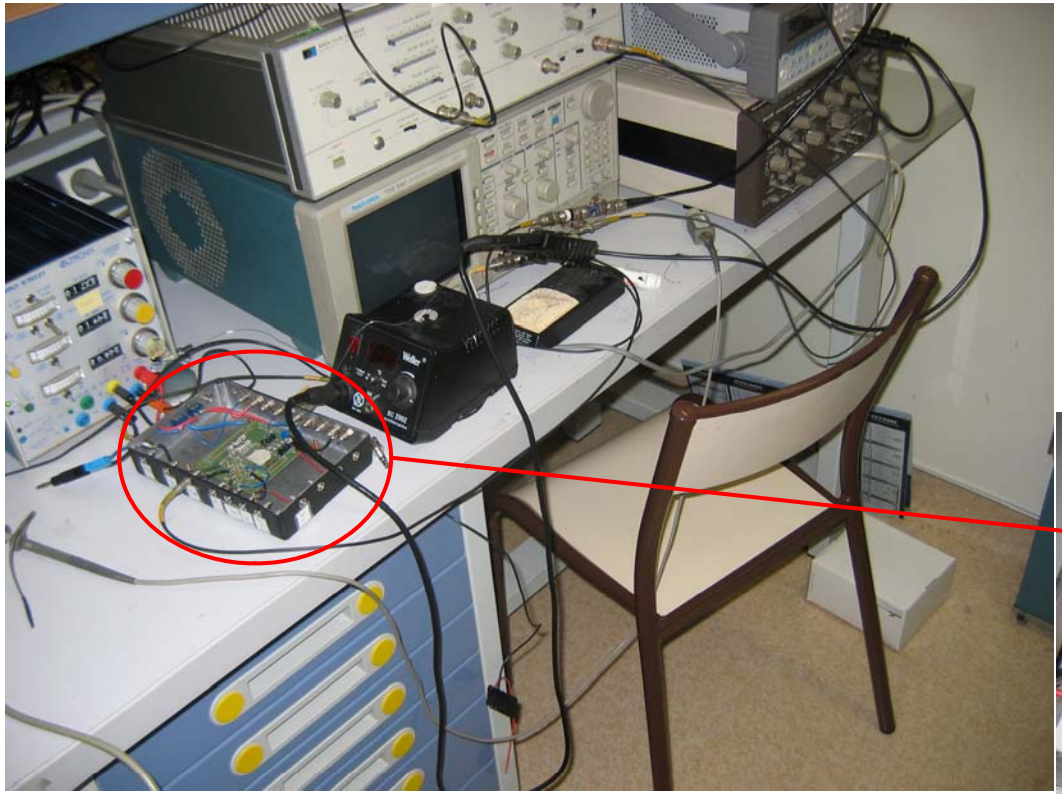
180nm 130nm



Picture

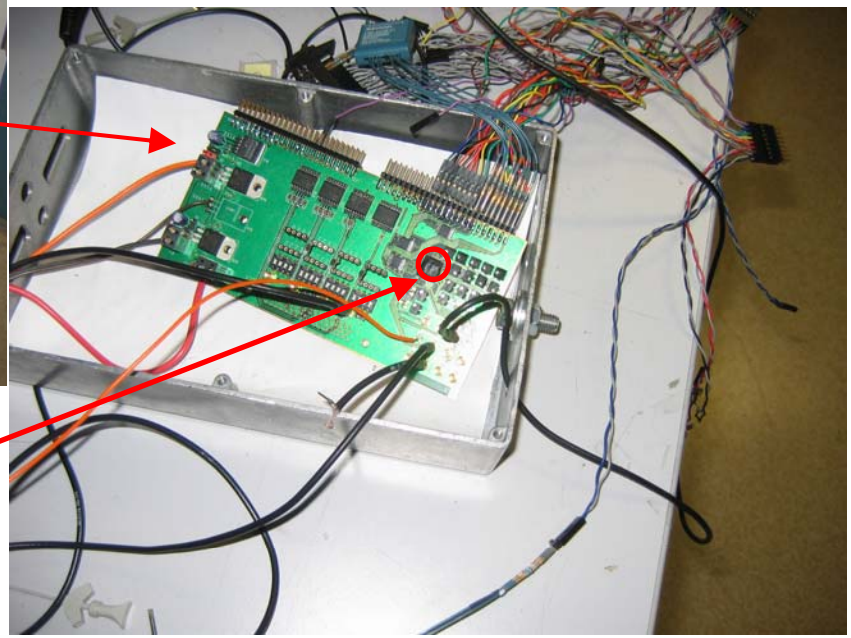
Chips received end 2006 and beginning 2007. Both tested in 2007

Functionality tests of SiTR-130_v1



Lab test bench at LPNHE

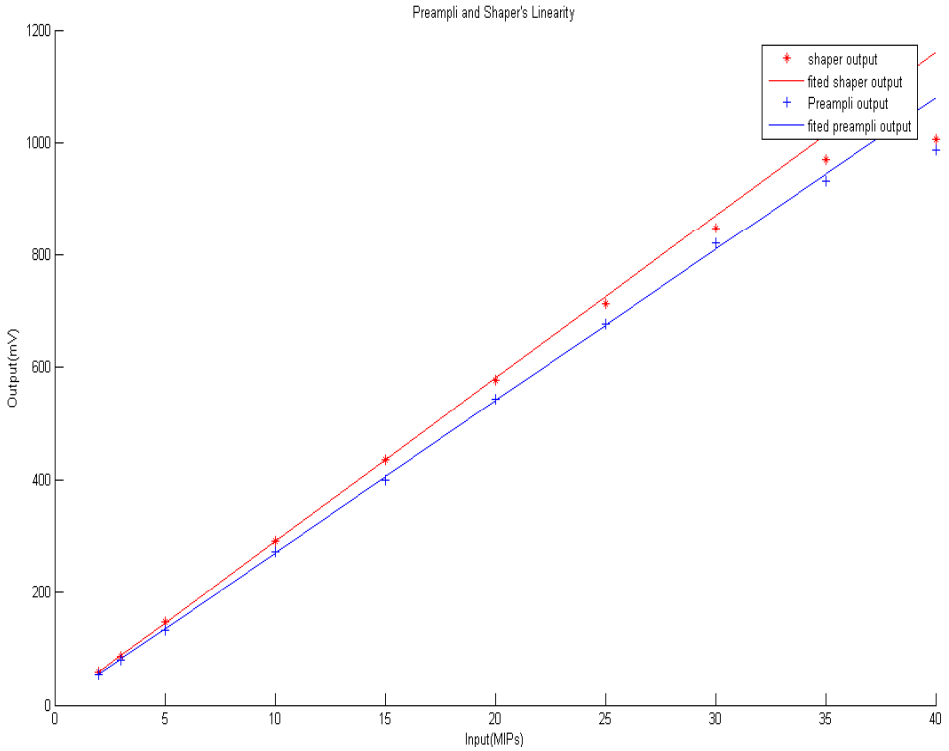
Test board for SiTR-130_v1

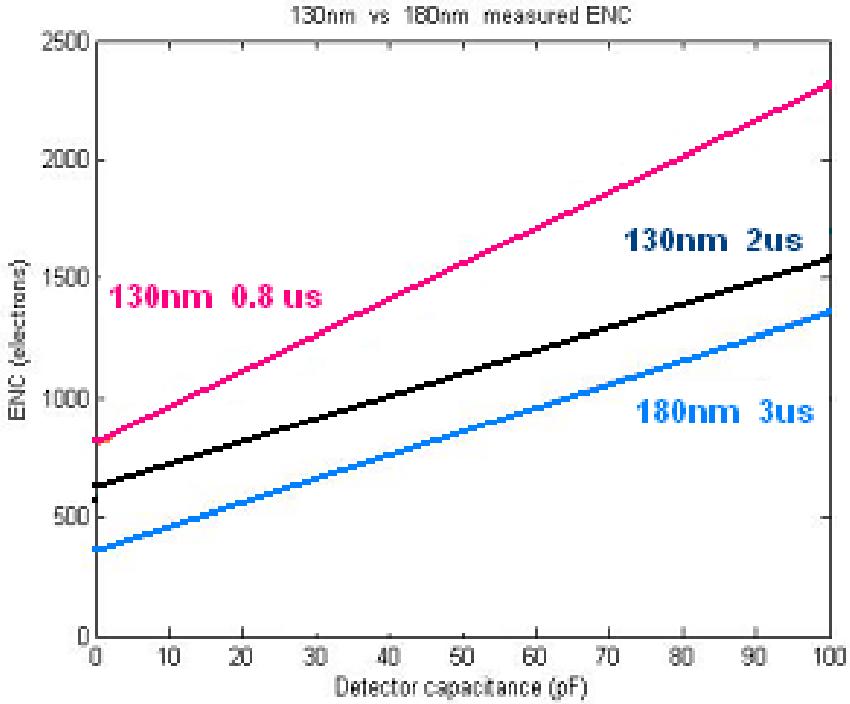


Chip SiTR-130_v1

Another test bench system is being installed at LAPP in order to fully test SiTR-130_v2 . This test bench will be fully automatized.

Results in functionality of SiTR-130 v1





Preamplifier :

Gain = 27mV/MIP

Dynamics = 25MIPs (<1%)

= 30MIPs(<5%)

Shaper :

Gain = 29mV/MIP

Dynamics = 20MIPs(<1%)

= 30MIPs(<5%)

Performance (noise):

130nm @ 0.8 **µs** : 850 + 14 e-/pF

130nm @ 2 **µs** : 625 + 9 e-/pF

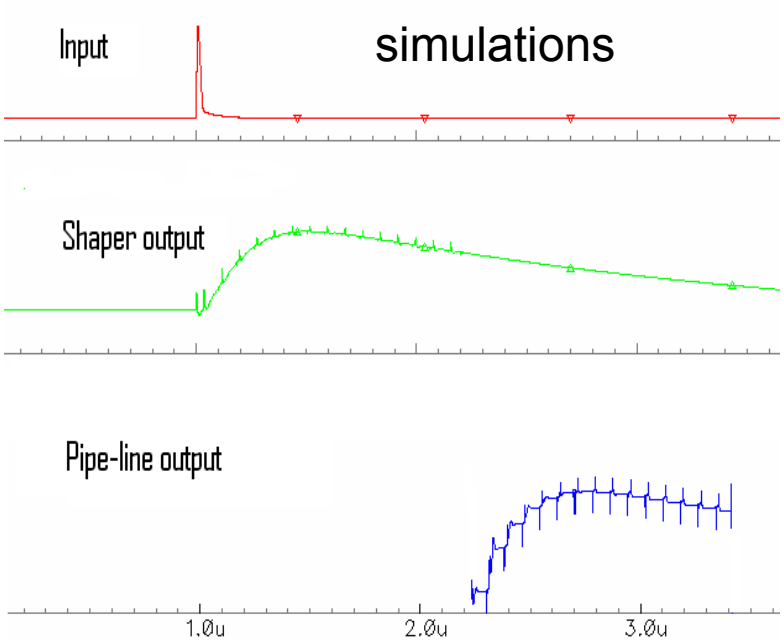
625*sqrt(2/3)=510 **e-/pF**

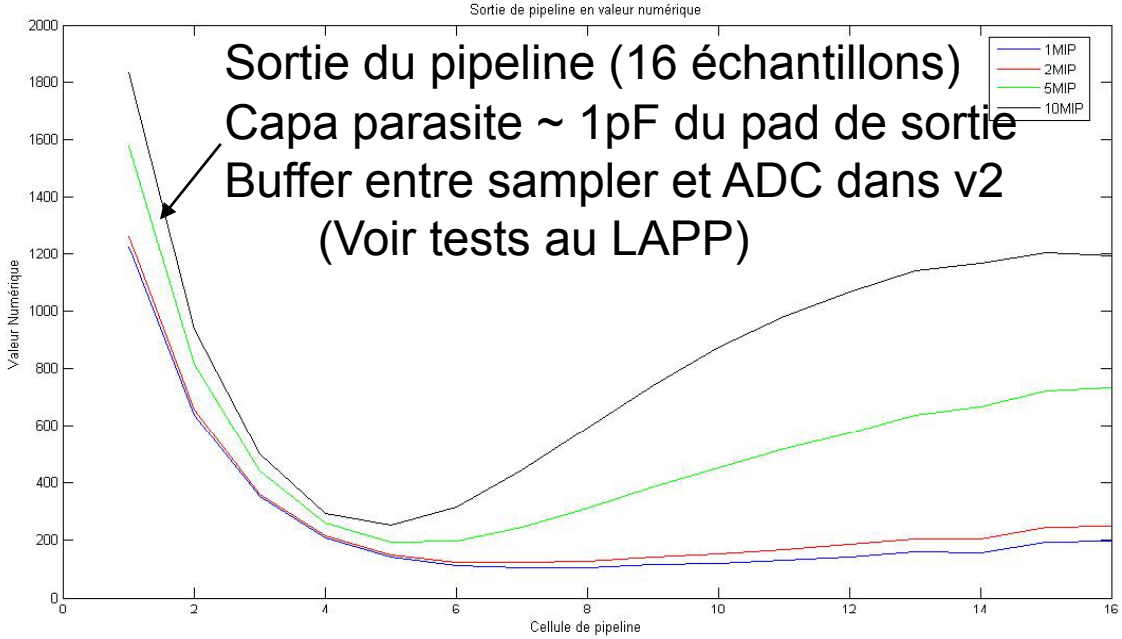
180nm @ 3 **µs** : 375 + 10.5 e-/pF

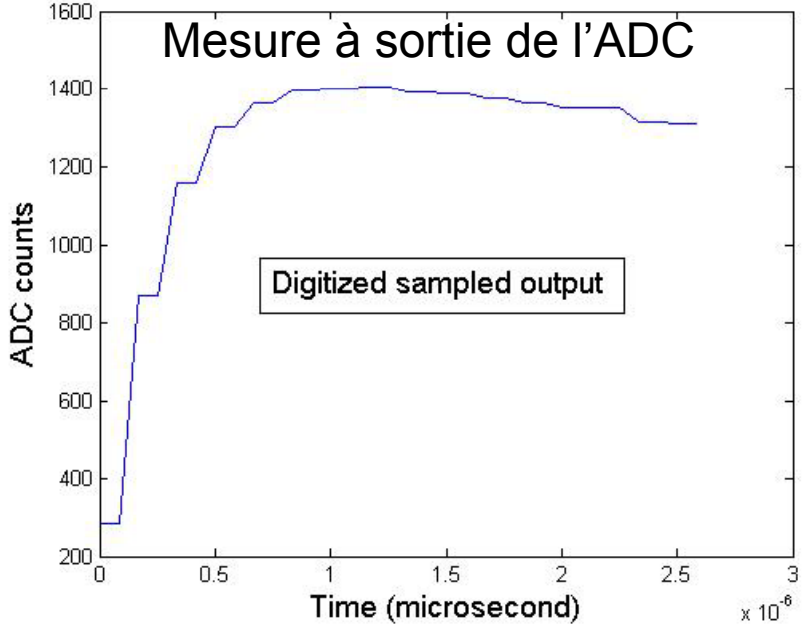
Power consumption

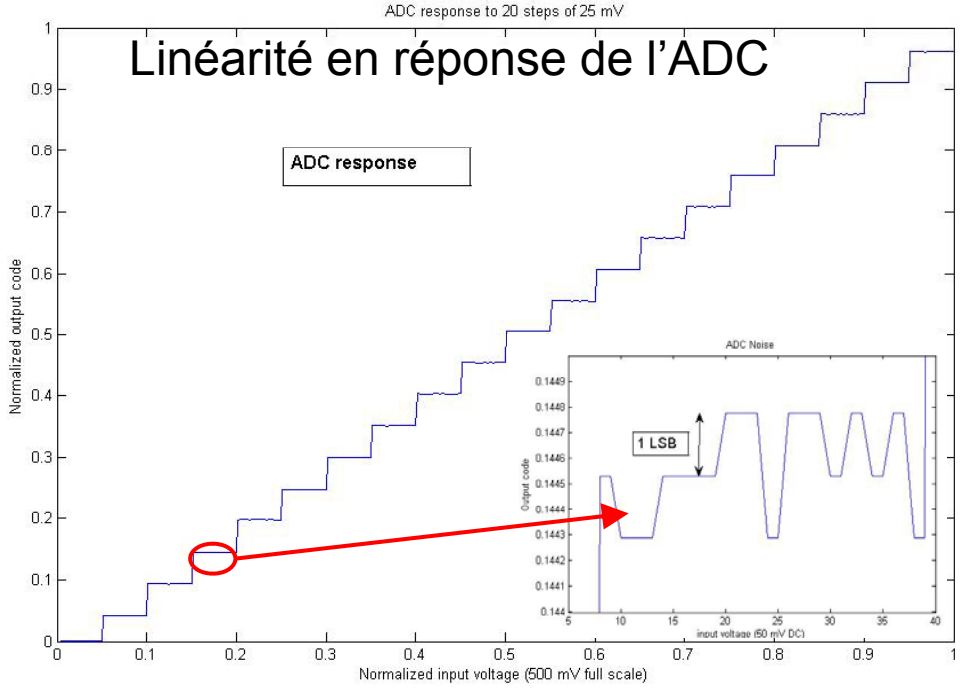
(Preamp+ Shaper) = 290 **m**W

Results in fonctionality of SiTR-130_v1=> OK







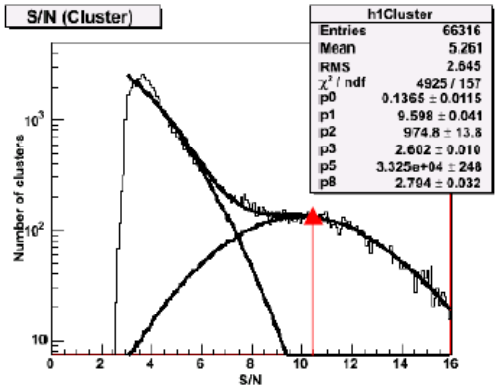


SiTR-130_v1 et v2: still to be done

Detailed characterisation of the A/D converter

- Linearities — integral, differential
- Noise — fixed pattern, random
- Speed — Maximum clock frequency

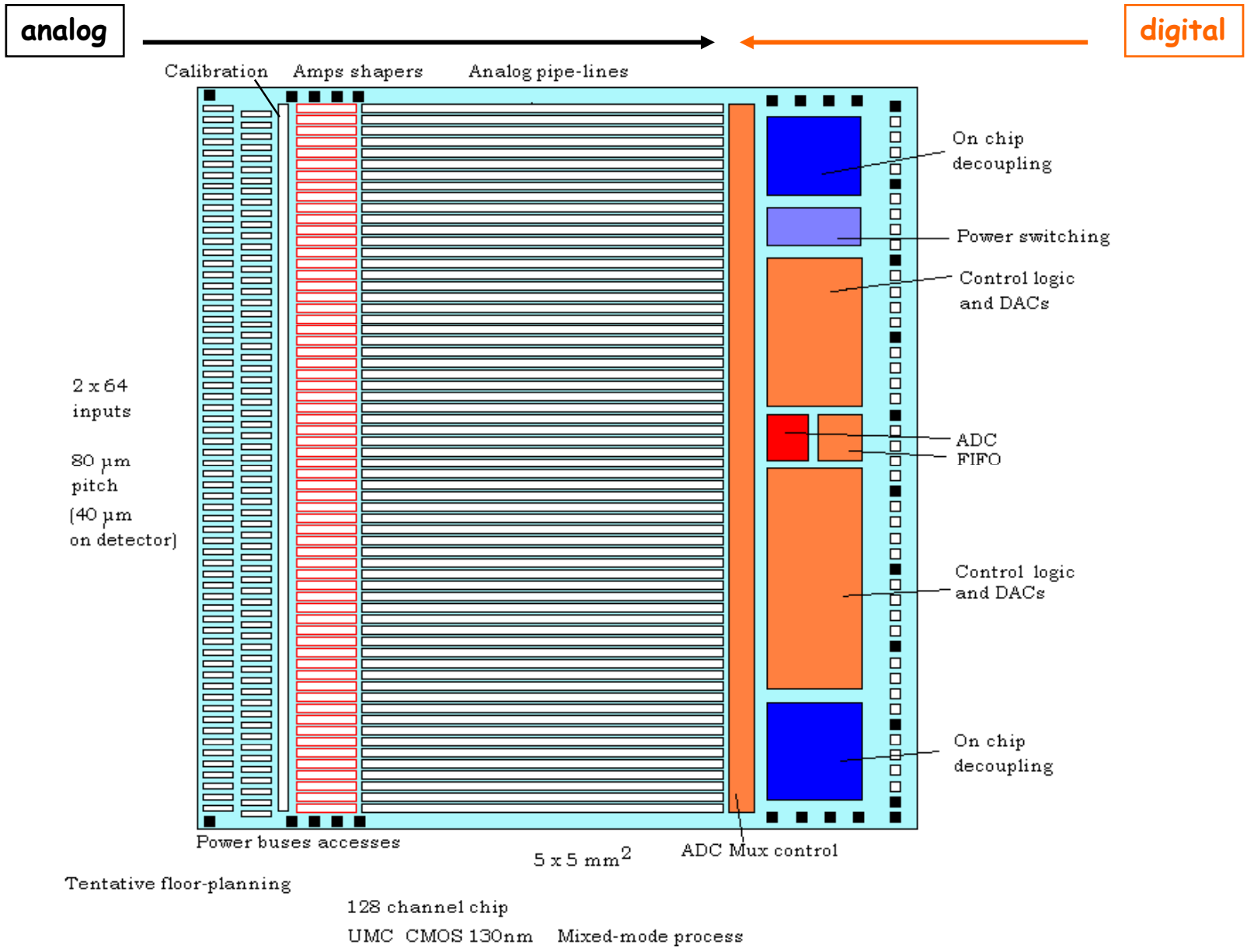
Number of effective bits (ENOB)
and full caracterization of SiTR-130_v2 autLAPP



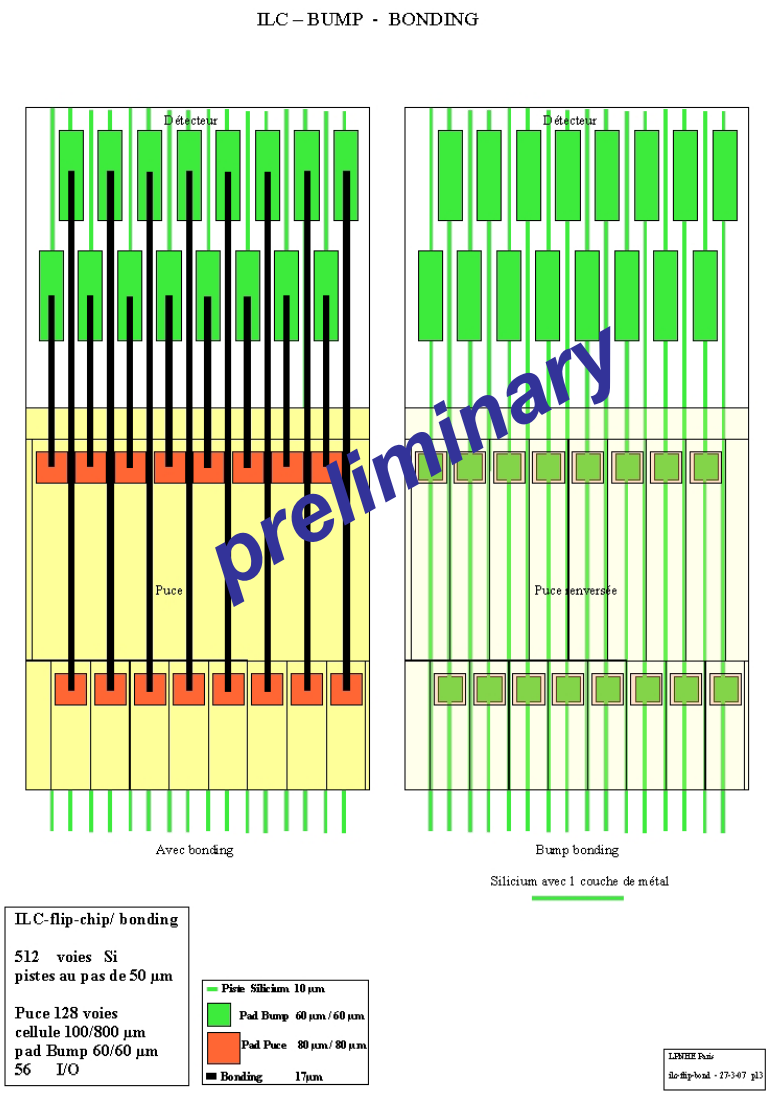
Tests of SiTR-130_v1 mounted on FE board connected to a Si module made of one CMS sensor (9,45cm strip long, 125µm pitch) made by IEKP, are underway at the Lab test bench in Paris before testbeam at CERN.
Tests with LD1060nm ➔ The electronic chain works fine
Tests with radioactive source have just started
These tests are in preparation of CERN t.b. in October.

These tests are crucial for the new SiTR-130_128ch, based on same design, but with 128 ch/chip and power cycling; New chip will be sent in foundry January 8 (EUDET).

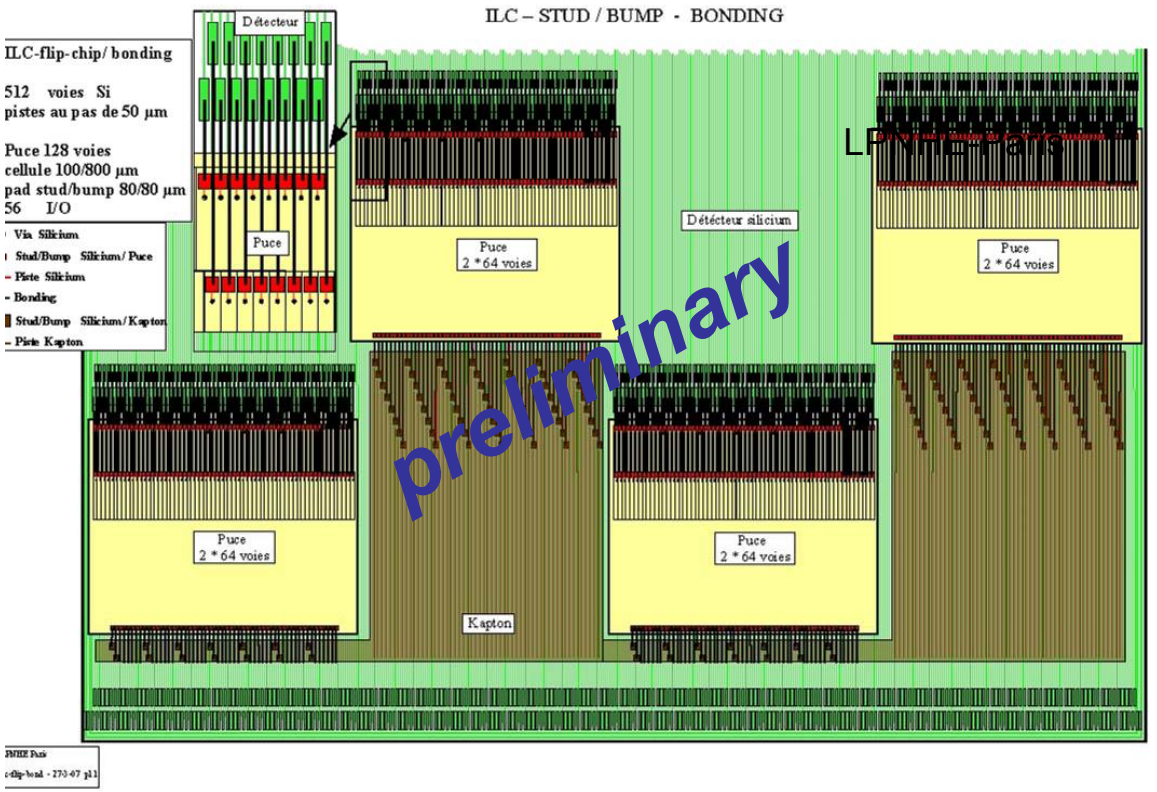
128-channel chip



“Inline pitch adapter” of SiTR chip for SiLC

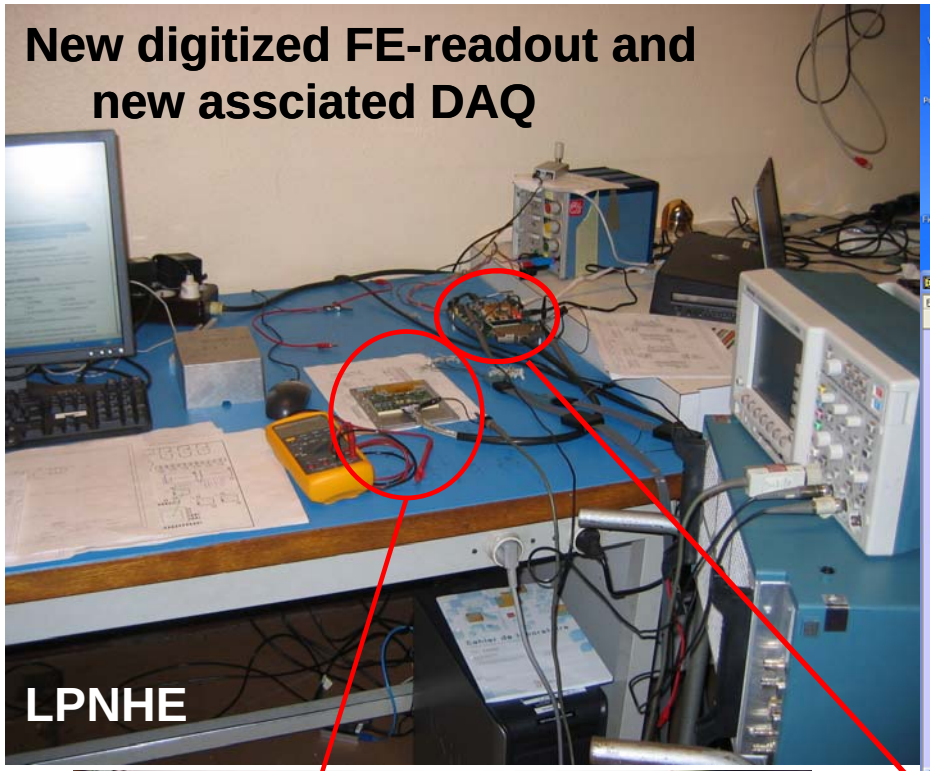


LPNHE + HPK

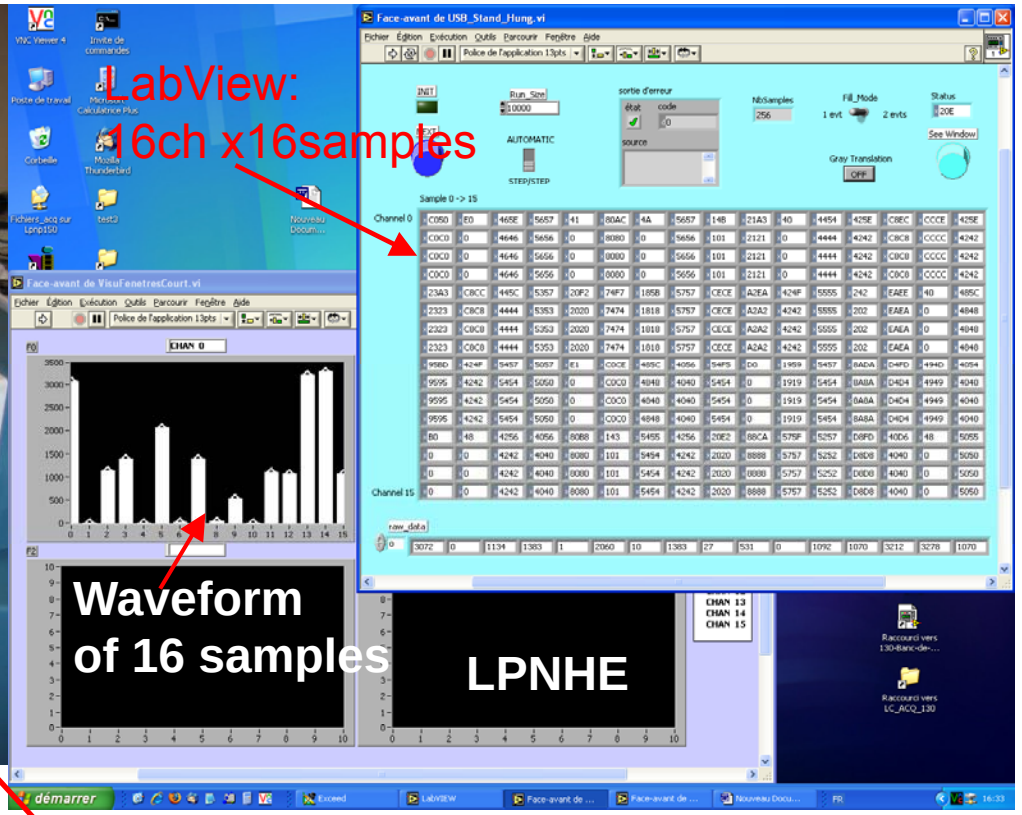


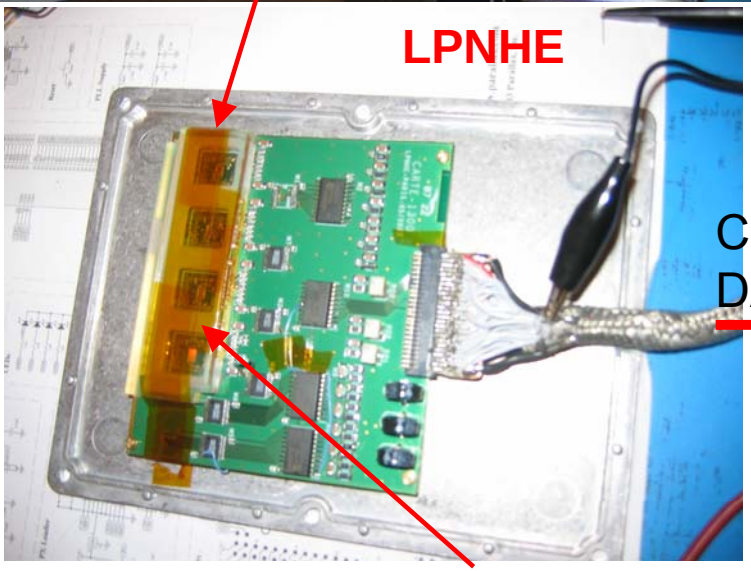
- LPNHE produces the chips (SiTR-130_128v)
- HPK does the bump bonding of the chip on the detector in: Bump
  Flipchip
  Stud-bonding
  (MoU & NdA in preparation)
- Foreseen tests and mini production in 2008

New digitized FE-readout and new assciated DAQ



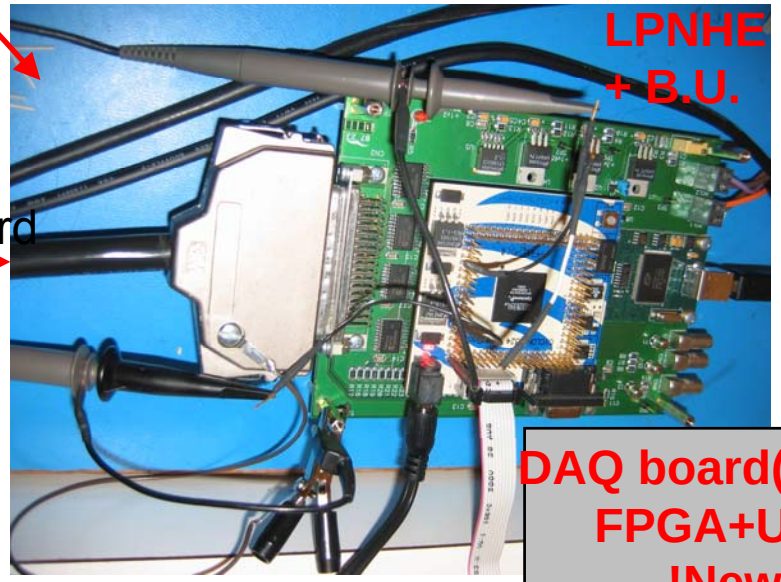
LabView:
16ch x16samples





FE hybrid with 4 SiTR-130_v1
→ Total number of channels = 16

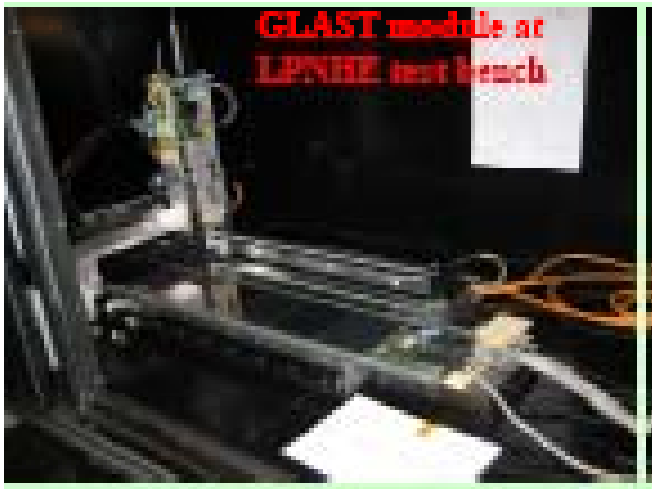
Cable to
DAQ board

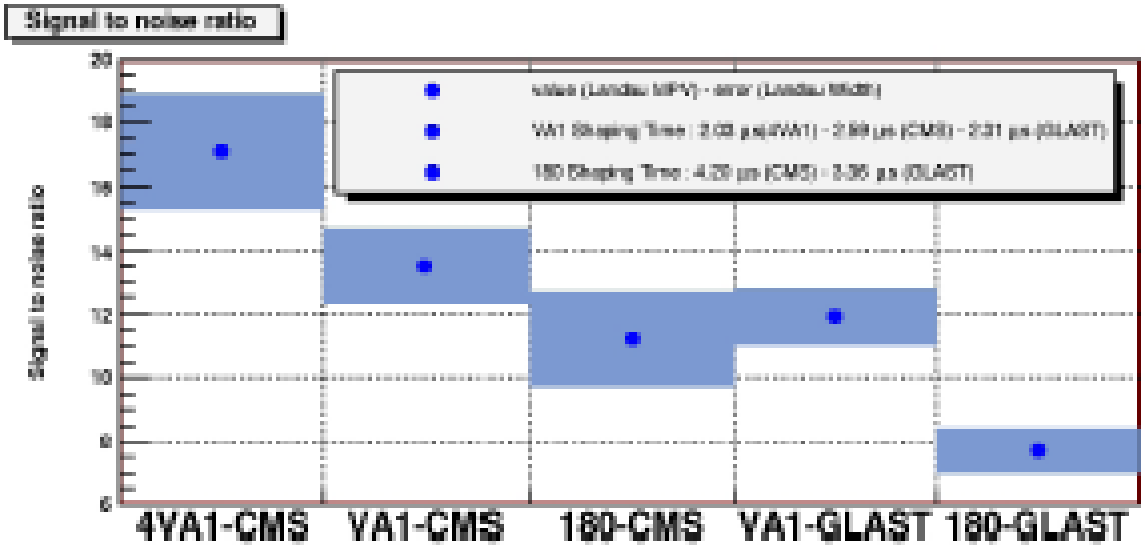


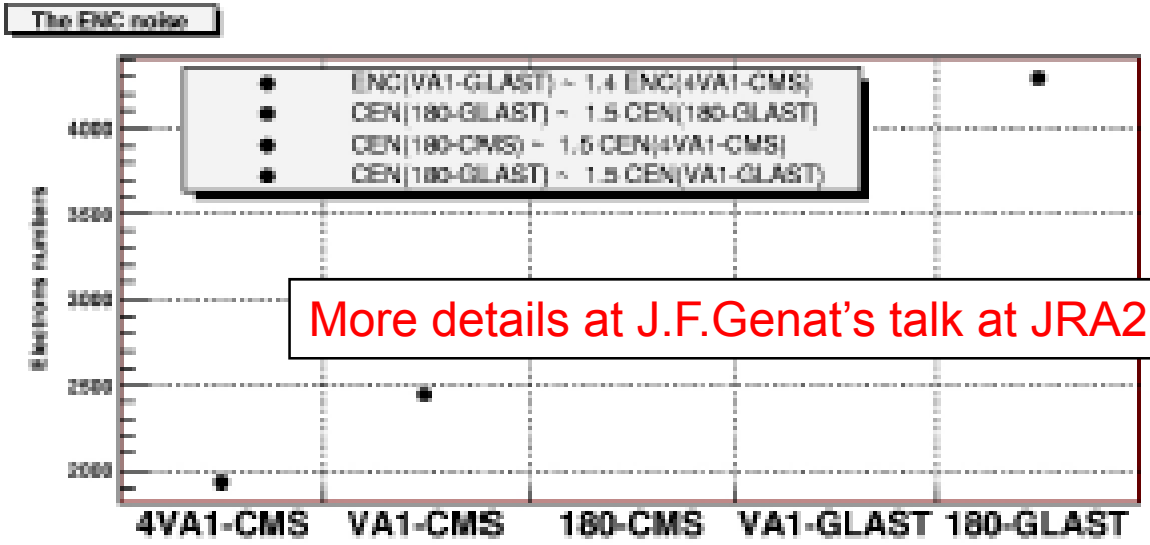
DAQ board(VHDL)
FPGA+USB
!New!

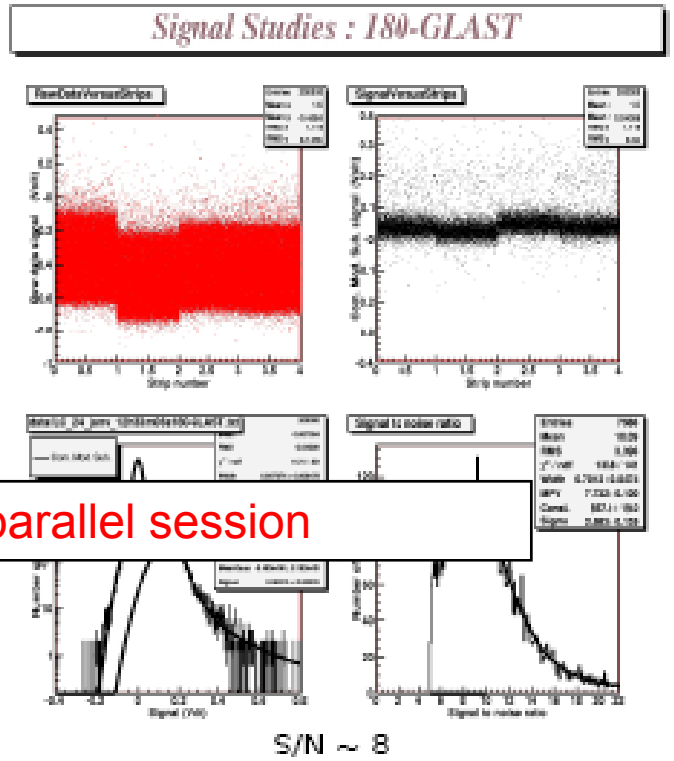
Characterization of Si detectors & FEE

Measurements S/N (MPV) and noise (ENC) at Lab test bench, on modules with 3CMS & 10 GLAST, read out by VA1 (ref) and SiTR-180





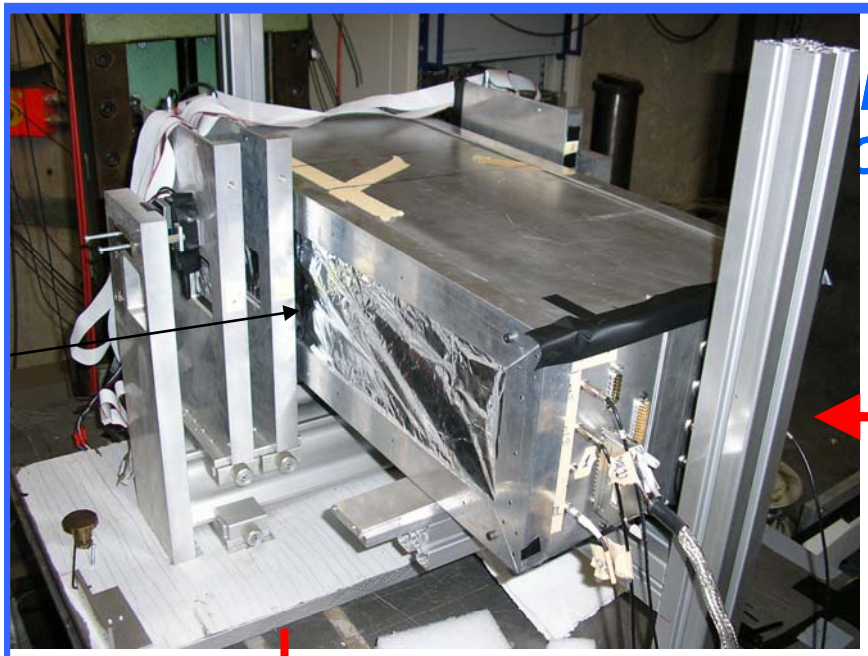


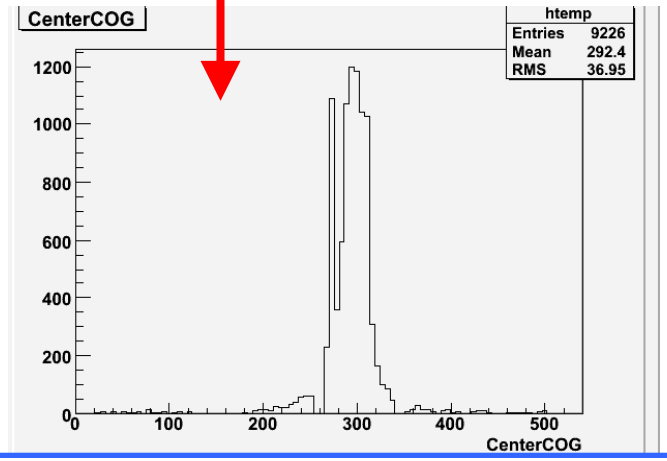


More details at J.F.Genat's talk at JRA2 parallel session

Beam Tests *(CU Prague, IFCA, IEKP, LPNHE, HIP & more joining)*

- Tests at DESY 4/6 → 17/6, TB22, in preparation of:
- Tests at CERN 10/10 → 22/10, TB H6 at SPS
- Preparation of test with LCTPC: foreseen Fall 08.





DESY T.B:
BU, DESY, IEKP, LPNHE, Prague, IFCA
Coordinator SiTRA DESY T.B.: Z. Dolezal,
Contact person: V. Saveliev

→Pursuing on tests at DESY (Nov06) & new Lab tests from testbench at LPNHE with CMS-180nm vs VA1 (ref)

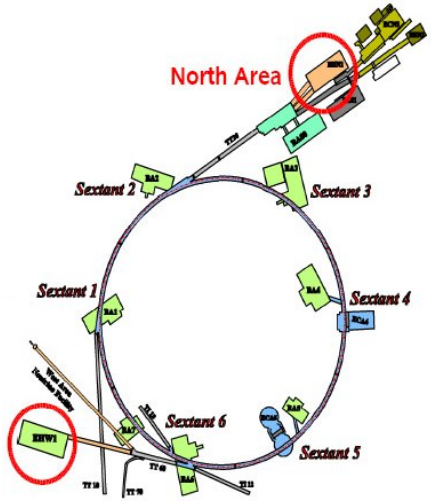
→Attempt to test S/N with Si module: 3CMS & 16ch of SiTR-130_v1prototype

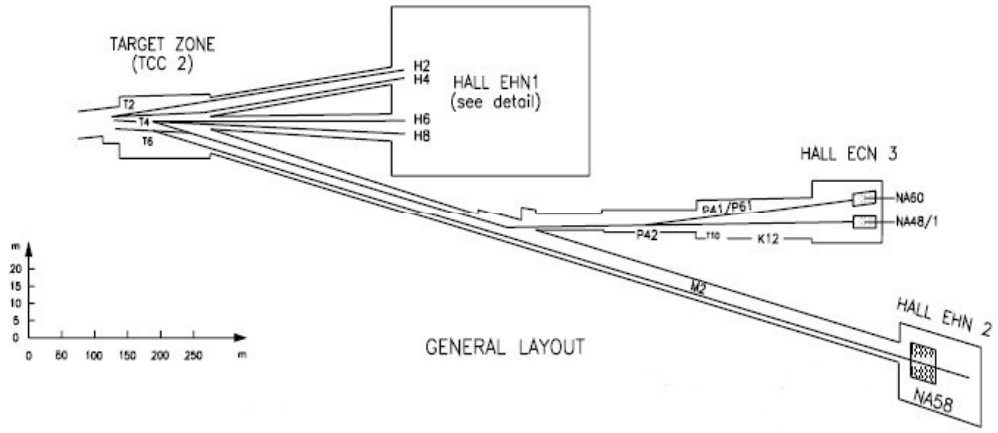
- New DAQ Hardware: digitized FE+ FPGA + USB interface
- New DAQ software (VHDL + LabView)
- New FE board
- New cabling
- Preliminary tests at the Paris Lab test bench DAQ hard + soft, new chip on FE board connected to Si module

Overall new 130nm-system could not be ready for June tests thus tests were pursued at Lab.

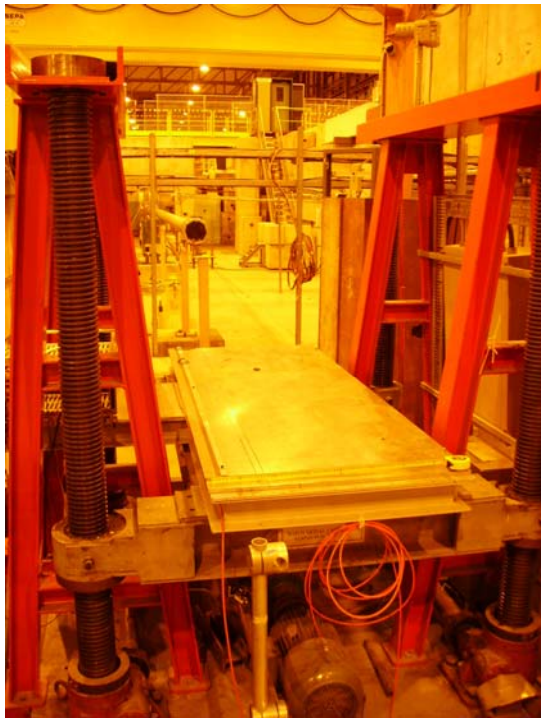
Contact person at CERN: Marcos Fernandez Garcia (IFCA & E.U. postdoc)

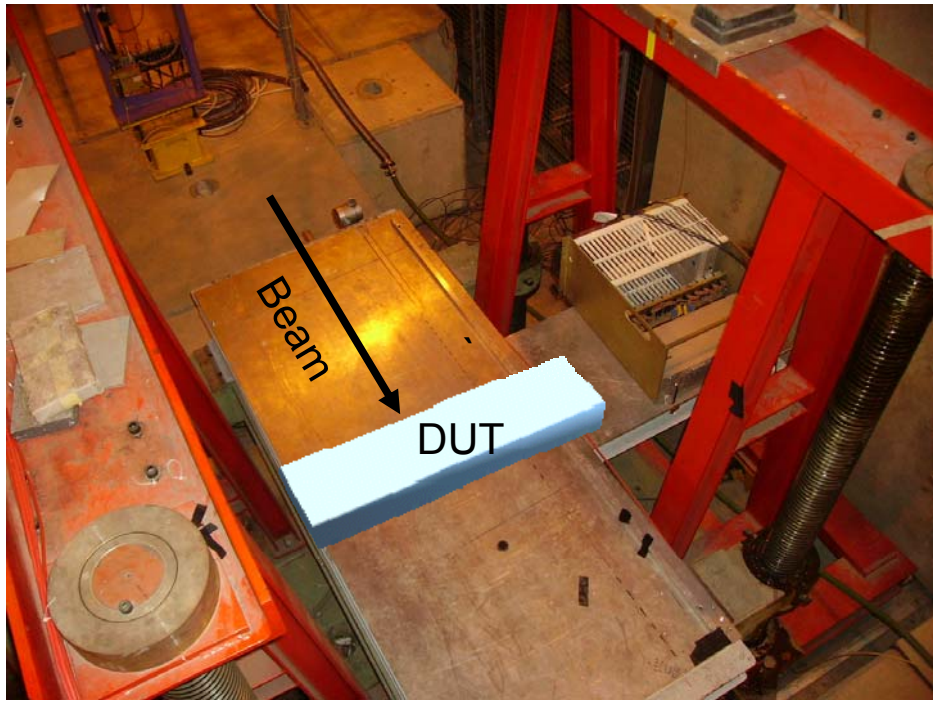
Coordinator SiTRA CERN T.B.: A. Savoy-Navarro





Test Beam at CERN: October 10-22, 2007





Objectives of CERN T.B.

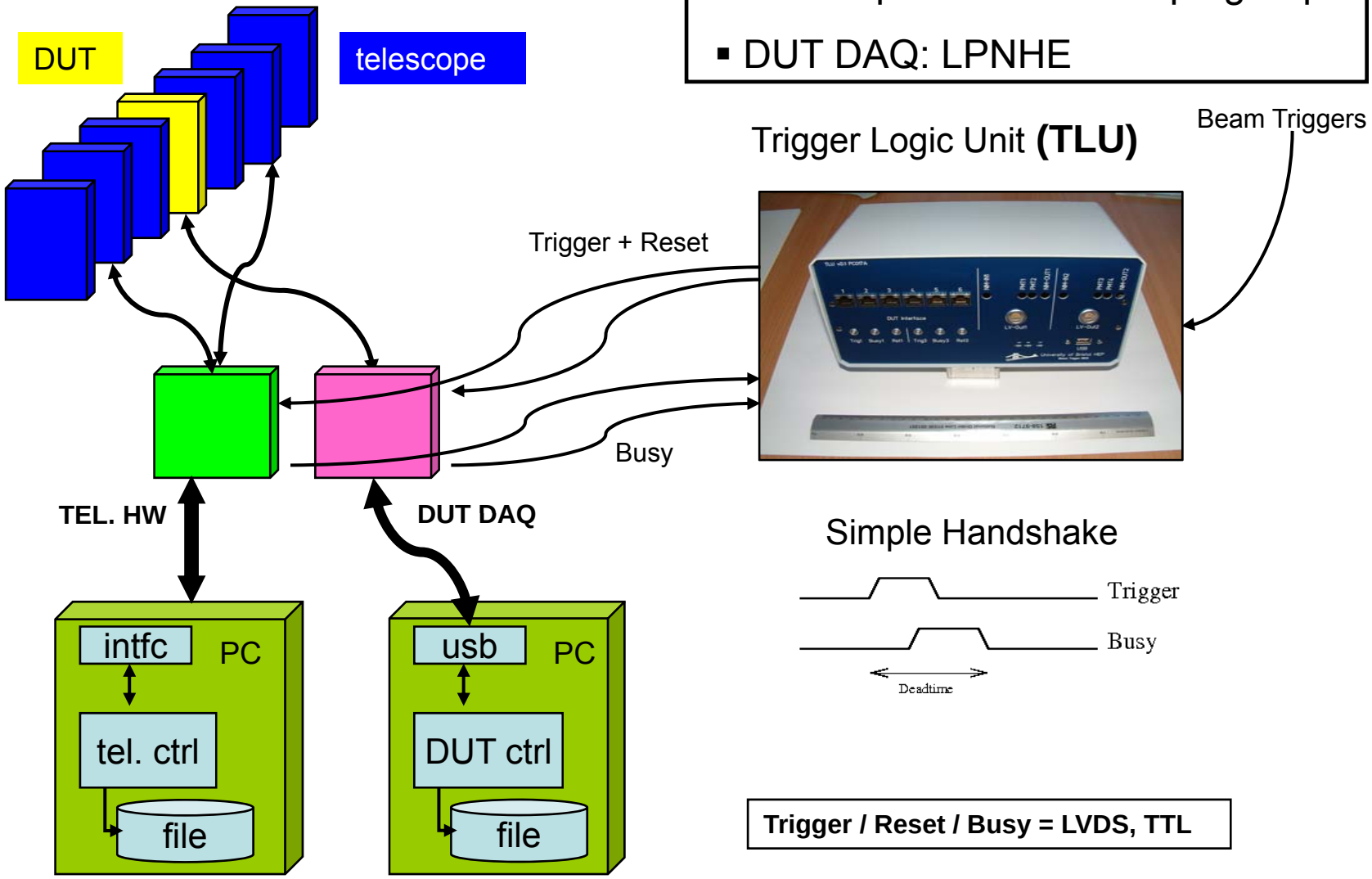
- A new module made of 2 new Si HPK sensors and SITR-130 chips that will be used for making large size prototypes (SiTRA deliverable) for next year test beams will be tested
- Compared with 2 modules read out with VA1

  (reference readout) and 2 modules with CMS sensor and SITR-130 chips
- New FE electronics prototype of the readout chip (SiTRA deliverable major funding component)
- New DUT DAQ and new overall Si-DAQ adapted to common EUDET-ILC DAQ

TELESCOPE + DUT TESTBEAM

- Overall DAQ + Beam & trigger:

  IFCA + CU Prague
- Telescope DAQ: Telescope group
- DUT DAQ: LPNHE



Simple Handshake

Trigger / Reset / Busy = LVDS, TTL

SiTRA: Appointments status

The 3 job positions are being filled

CU Prague: since August 2006 (Peter Kvasnicka)

IFCA Santander: since September 2006 (Marcos Fernandez Garcia)

LPNHE-Paris: First candidate, starts October 1st 2007

The 32 months are split into 2 positions. The 2nd candidate: end 07.

Milestones and Deliverables (J.M. slide)

Milestone Deliverable	Deadline	Status
Convection cooling system prototype	22	In progress
Motorised 3D table	24	
Central tracker prototype	24	
FE chip version 1	24	

Milestones and Deliverables (J.M. slide)

Milestone Deliverable	Deadline	Status
Convection cooling system prototype	22	In progress
Motorised 3D table	24	HIC SUNT LEONES
Central tracker prototype	24	
FE chip version 1	24	

Milestones and Deliverables Reality

Milestone Deliverable	Deadline	Status
Convection cooling system prototype	22	In a good shape
Motorised 3D table	24	In a good shape
Central tracker prototype	24	In a good shape
FE chip version 1	24	In a good shape

In a good shape = Work in progress, very likely to be matched, documentation lags behind, but more effort will be put into its timely finishing

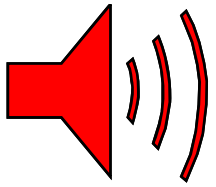
Critical points:
(*not only for SiTRA)*

- **Financing**

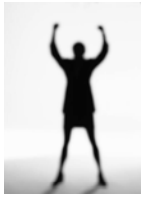
  Non E.U. funds are needed for: Silicon sensors, detector prototypes, part of cooling system, all the alignment system, DAQ and related electronics (FE boards etc…)

- **Collaboration with industry** on some of the high tech aspects is crucial (new sensors; wiring /packaging, VDMS foundries, new materials) and needs funding as well.

- **Test beam:** longer and far away (CERN & FNAL), thus increasing needs for travelling money



SiTRA positive points



- Important progress in 2007 on:
- New large area Si tracking prototypes: IEKP, HEPHY, LPNHE and fuitful colaboration with CERN.
- Front end chips
- Alignment prototype & cooling prototype as well.
- Collaboration started with other sub detectors:TPC & µvertex
- Valuable T.B. facility in DESY+ starting T.B. at CERN
- Non E.U. SiLC teams join beam tests(prepa & construction)
- Industrial firms starting active contributions on crucial aspects: new sensors & inline pitch adapter (new Si modules).
- Non E.U. financing increase for some teams (Spain, Vienna, France….); but not yet enough for the next years needs .
- R&D SiLC collaboration developing well: regular meetings of the whole collaboration or on dedicated topics + good visibility

=> valuable help for SiTRA

List of people contributing to SiTRA in 2007

SiTRA partners

- **HIP and VTT Helsinki:**

S. Eranen (VTT), R. Orava,
N. Van Remortel

- **LPNHE Paris:**

W. Dasilva, G. Daubard, J. David,
M. Dhellot, C. Evrard, J.F. Genat,
P. Ghislain, J.F. Huppert, D. Imbault,
F. Kapusta, H. Lebbolo, T.H. Pham,
Ph. Repain, F. Rossel, A. Savoy-N.,
R. Sefri + D. Fougeron, R. Hermel
(LAPP/IN2P3)

- **CU Prague**

Z. Dolezal, Z. Drasal, P. Kodys,
P. Kvasnicka (E.U. postdoc),
D. Scheirich

- **IFCA Santander**

M. Fernandez-Garcia(E.U. postdoc),
F.J.Gonzalez-Sanchez, R. Jaramillo,
C. Martinez-Rivero,A. Ruiz-Jimeno,
Ivan Vila

SITRA Associated

- **IMB-CNM Barcelona:**
  E. Cabruja, M. Lozano, G. Pellegrini, L.Teres
- **Liverpool Uni.:** Ph. Allport, T. Greenshaw
- **OSU, Obninsk:** V. Saveliev
- **IFIC Valencia:** A. Faus-Golfe, J. Fuster,
  C. Lacasta, P. Modesto, M. Vos
- **HEPHY Vienna:** T. Bergauer,
  M. Krammer, W. Mitaroff, M. Regler

Other institutes:

- **IEKP Karlsruhe:** P. Bluem, M. Frey,
  F. Hartmann, P. Lederman, T. Muller

Collaboration of CERN bonding Lab
A. Honma, I. McGill, M.Moll

DESY: test beam+ telescope
N. Meyers, T. Hass & al.

HPK Hamamatsu
and SiLC R&D collaboration