Silicon Wafers for EUDET module design and test bench

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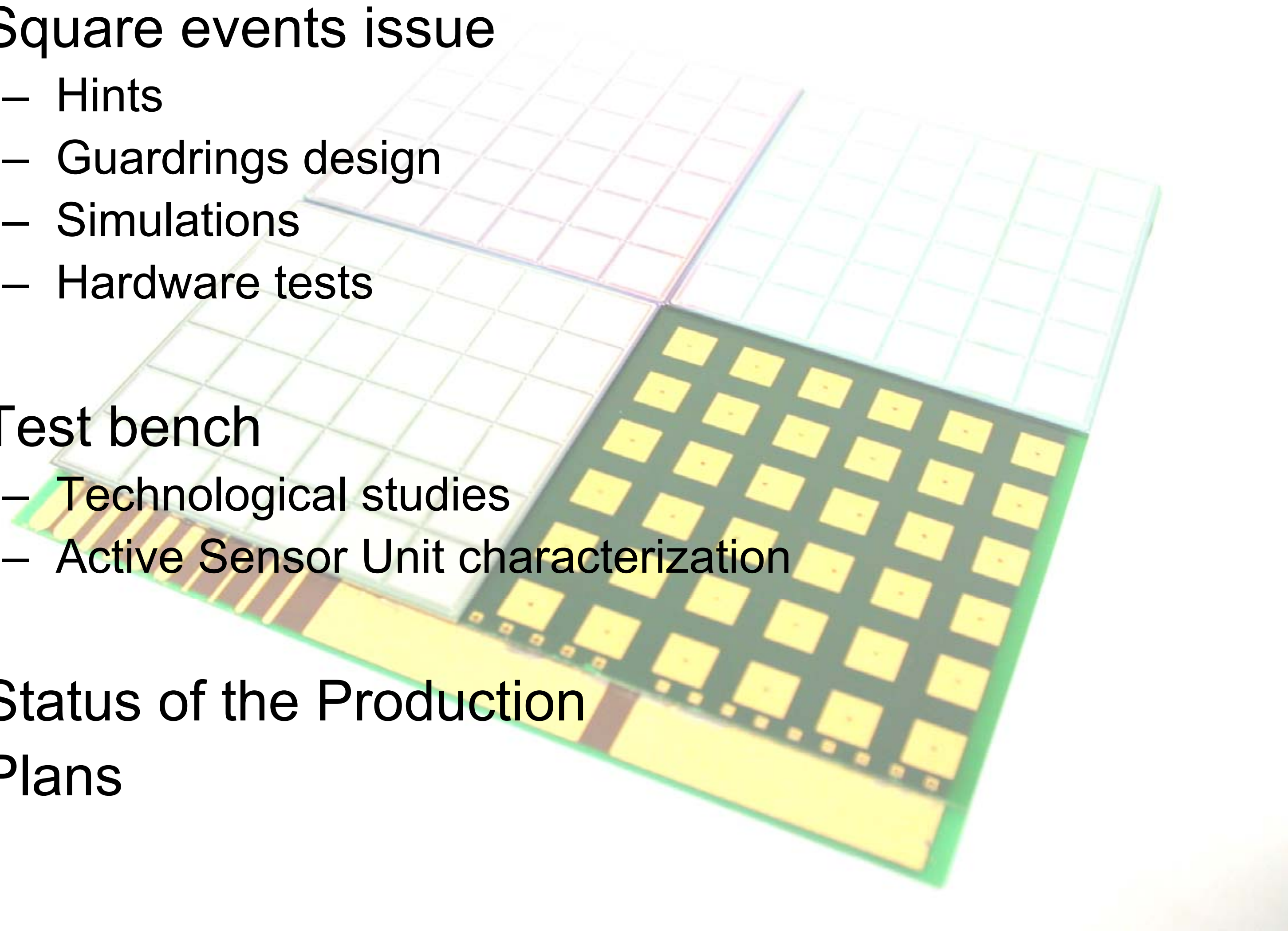
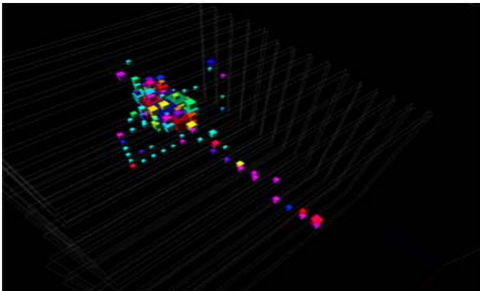
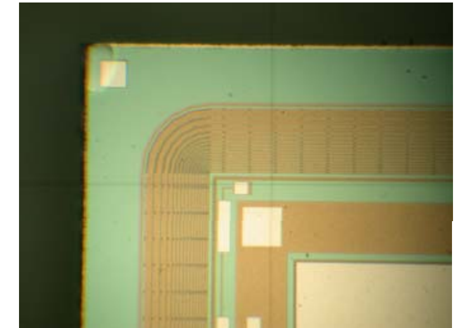
Overview



- Square events issue
  - Hints
  - Guardrings design
  - Simulations
  - Hardware tests
- Test bench
  - Technological studies
  - Active Sensor Unit characterization
- Status of the Production
- Plans



Understand the origin of Square events

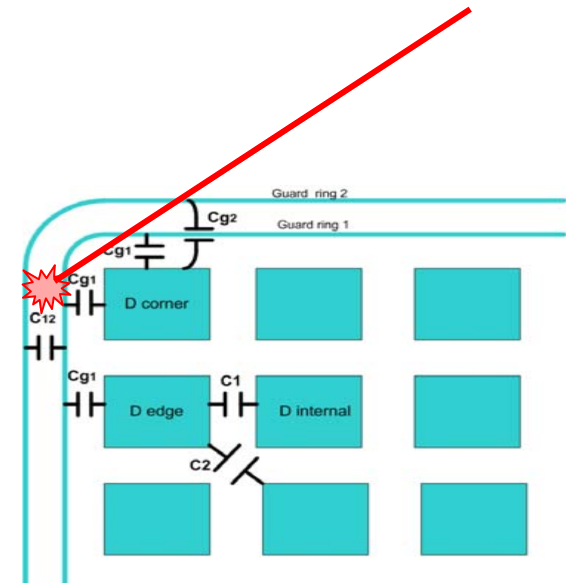


Guard-rings are needed to avoid high leakage current at the wafer border…

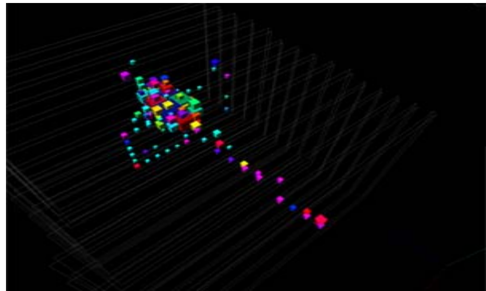
The square shape corresponds to guard-rings location

Effects of a particle hit on guard-rings could be propagated to every bordering pixels

= cross-talk effect



Other source effects ?
Need to check and crosscheck…

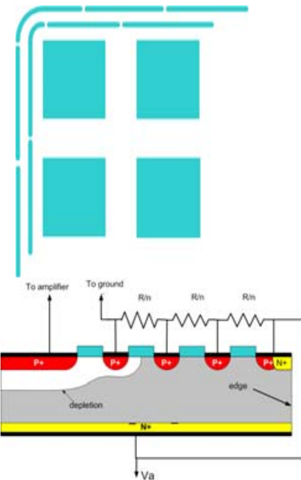


Find a turnaround

Square event issue must be solved

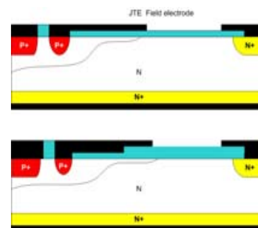
Many possibilities to explore
• Guardring implementation
• Guardring technology
• Others ?

Guardring implementation
• continuous (baseline)
• segmented
• polarized
With various spacing and V

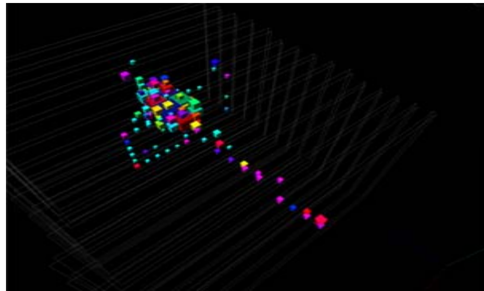


See Akli's talk @ Seoul

Guardring technology
• P+ implant (standard)
• progressive doping
• MOS
• brutal etching
• new ?



Others ?
• Priority given to crosstalk as it is most probable and "easy" to test segmented topology

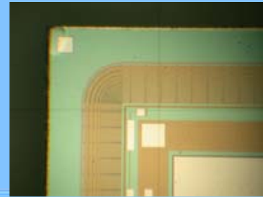


Crosstalk hypothesis verification

Method

Square event

Understand		Try to reproduce the phenomenon	Characterize
Simulation			Measurment Bench
SILVACO	SPICE		Samples
Guardring design: Splited, Polarized, Progressive	Pure crosstalk	Physical Model	Find out best candidate
Charge Injection: Photon, Electron	Electrical level	Splited guardring impact on pure crosstalk	Test new designs • layout • technologic improvements
Effects on: Leakage, Capacitance			
Current flow			

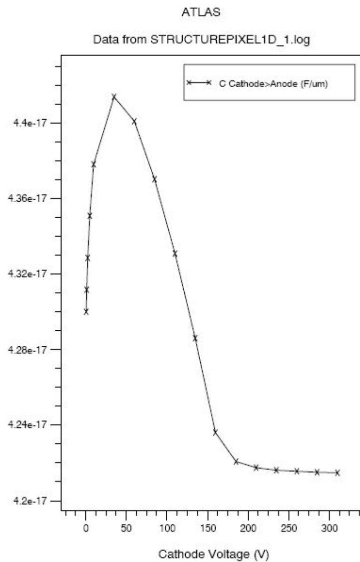


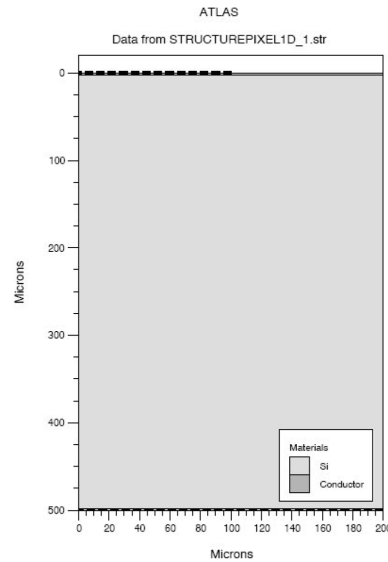
Simulation bench

Cu-Epo “wafer”

Various 3x3 test wafer to be produced by OnSemi
As result, select the best design technique…

Simulations with SILVACO





C(V) between pixel and common bias and C(V,a,b,c,d…)

First step to verify capacitance values between pixels, guardrings, substrate

Then back annotate to SPICE simulation

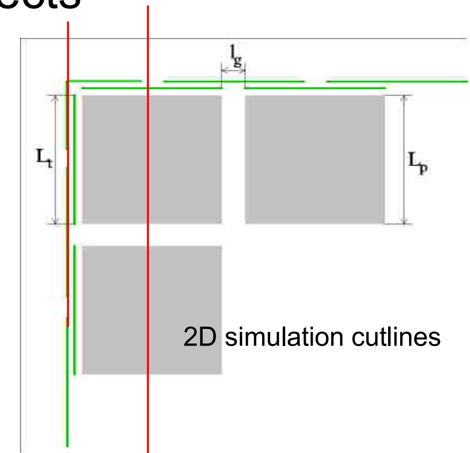
Simulated Cap. Values are within a 20% range from expected values calculated with first order formula

See Akli's talk @ Seoul

3D simulation are ongoing to take into account border effects

Second step to simulate ionization effects (electron or photon) or SEE/SEU events

Third step (following months) to evaluate design parameters impact on C and explore new designs of guardrings from crosstalk point of view



Segmented guard-rings technique may prevent Xtalk by a factor 3

diaphonie pixel – 3x3 matrix

Cgb = 4 pF Cgg=24pF Cpg = 1 pF

Simulations with SPICE

Plain guardring

5.6		5.6		5.6
	1	100	1	
5.6	0.3		0.3	5.6
	0.5	0.3	0.5	
5.6		5.6		5.6

Segmented guardring 160 fF

2		42		2
	0.3	100	0.3	
2	0.1	-	0.1	2
	0.15	0.08	0.15	
2		2		2

Guardring **non segmenté, Signal at G1**

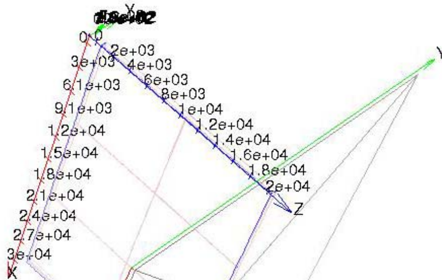
		100		
	20	5.6	20	
	5.6	-	5.6	
	20	5.6	20	

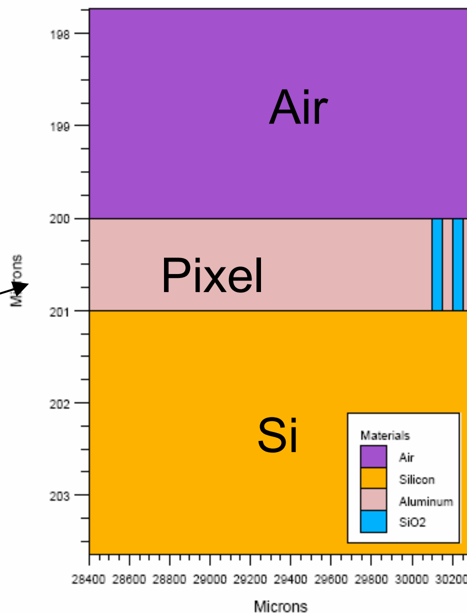
Guardring 1 segmenté, **Signal at G1_2 segment**, Css=160 fF

6		100		6
	1	5.6	1	
4	0.2	-	0.2	4
	0.4	0.2	0.4	
4		4		4

Simulations with SILVACO 3D

6 pixels and guard-rings





3D simulations enabled

3D simulation are ongoing to take into account border effects

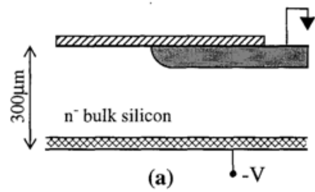
3D caps extracted : same range as for 2D

Next steps :

- SPICE simulations with extracted parameters

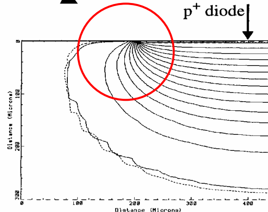
- radiation induced effect (photon and ionizing particles)

Angle etched wafers



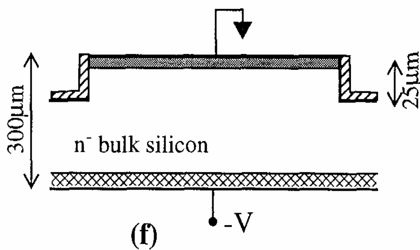
n-type diffusion
p-type diffusion
thermally grown oxide
polysilicon

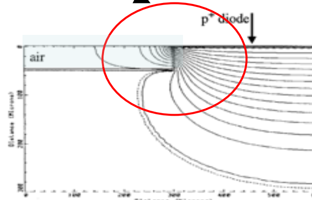
High $\vec{E}$ region



Critical field at breakdown 2E5 V/cm *(Ref: Semiconductor Devices S.M.SZE)*

Lower $\vec{E}$





Fine for breakdown = guard-ring replacement
No capacitance induced crosstalk

A vertical high voltage termination structure for high-resistivity silicon detectors

Segal, J.D.; Kenney, C.J.; Aw, C.H.; Parker, S.I.; Vilkelis, G.; Iwanczyk, J.S.; Patt, B.E.; Plummer, J.
Nuclear Science Symposium, 1997. IEEE
Volume , Issue , 9-15 Nov 1997 Page(s):299 - 303 vol.1

http://ieeexplore.ieee.org/iel4/5472/14772/00672589.pdf?arnumber=672589

Courtesy of Akli Karar (LLR)

Table 1: Comparison of high voltage termination structure simulation results for 300µm thick 1e12/cm^3 n-type bulk requiring 70V to deplete, with 2µm deep p-type junction,

junction termination structure	peak electric field for $Q_f=0$	peak electric field for $Q_f=1e11/cm^2$
un-improved diode	3.9E4 V/cm	8.0E4 V/cm
three floating rings (optimized) But square events	1.3E4 V/cm	3.1E4 V/cm
poly field plate extension (at uniform bias)	2.8E4 V/cm	5.8E4 V/vm
poly field plate extension (with linear voltage gradient)	0.8E4 V/cm	1.0E4 V/cm
linear implant gradient	1.5E4 V/cm	2.3E4 V/cm
vertical etch junction termination	2.0E4 V/cm	4.7E4 V/cm
angled etch junction termination	2.5E4 V/cm	6.0E4 V/cm

Critical field at breakdown 2E5 V/cm *(Ref: Semiconductor Devices S.M.SZE)*

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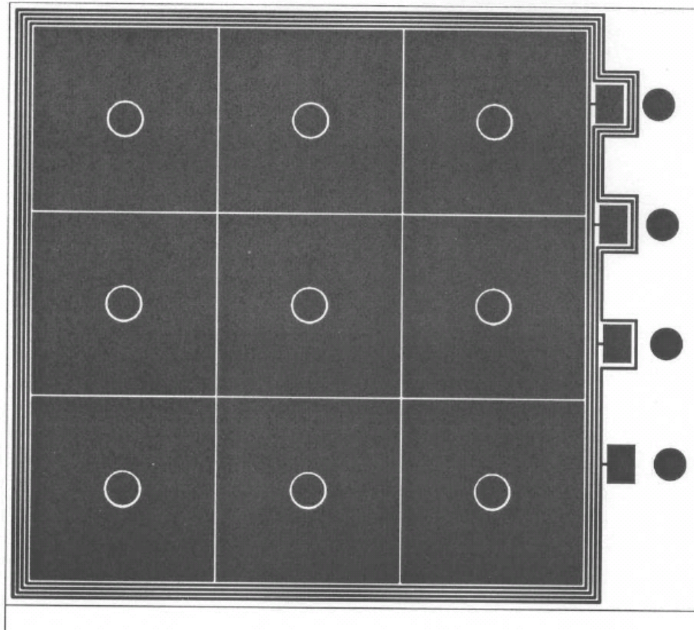
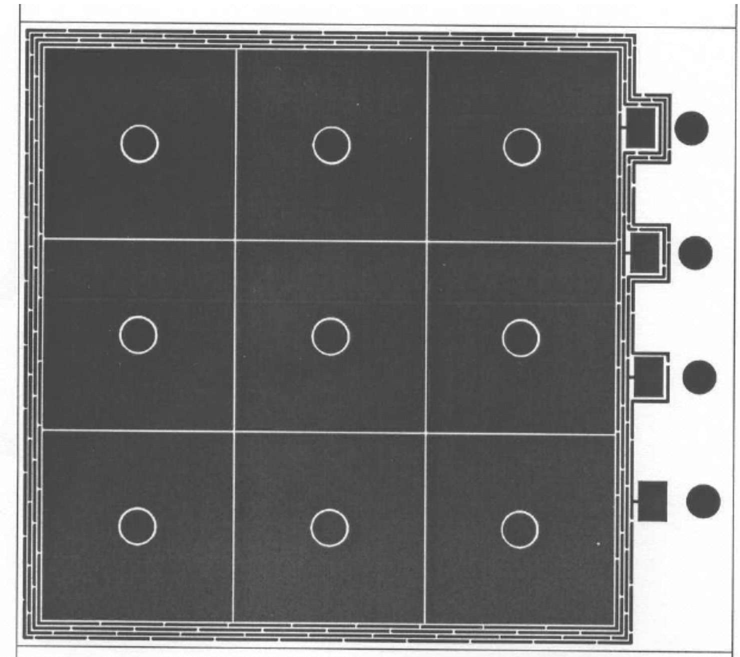
All these techniques can be simulated in accordance with ECAL wafer characteristics

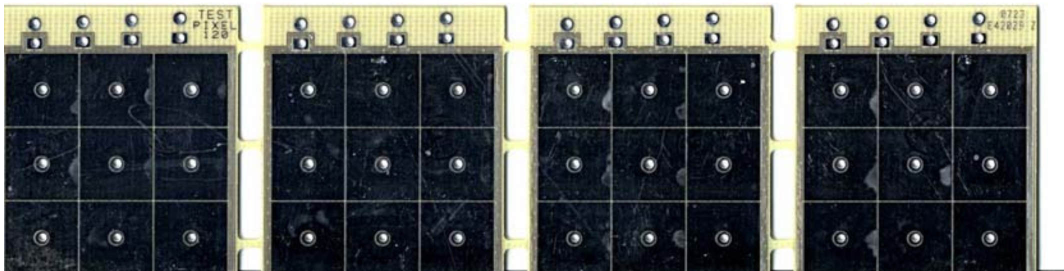
Physical Model : Cu-Epoxy

- Study pure crosstalk effects (various configurations)
- Measurement method validation
- Test bench calibration



Continuous guardring



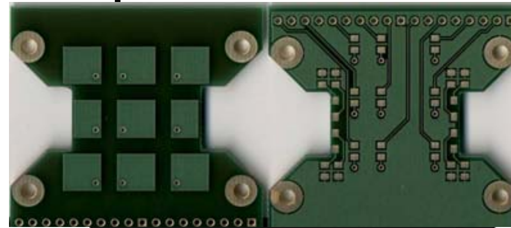


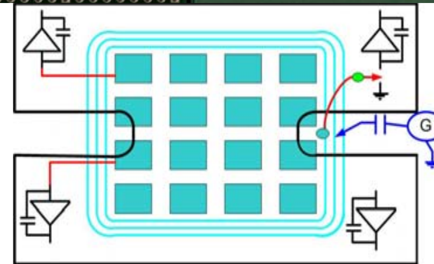
Splited guardring
- 4 @ 1 cm
- 4 @ 3 mm
- 2 @ 1 cm + 2 unsplited

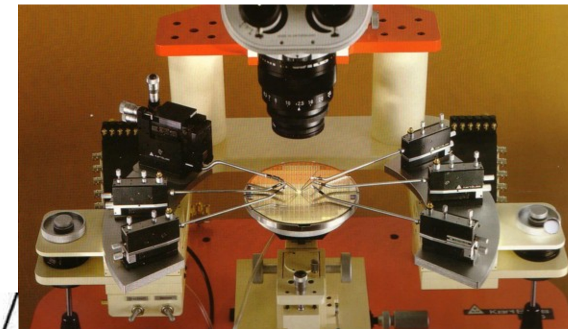
Hardware Test bench

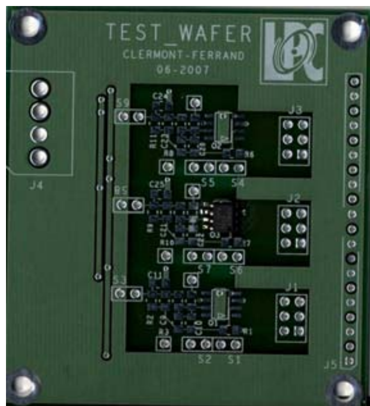
Setup and tools

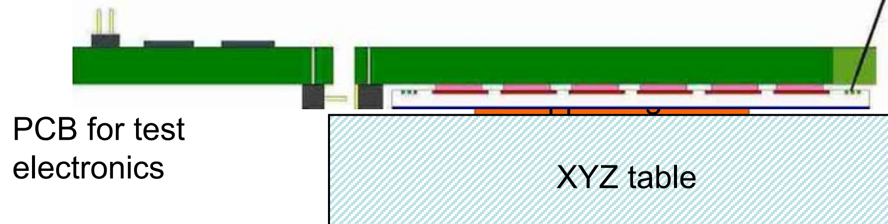
- pulse generator
- micro-positioner & probes
- shaper + scope











PCB for test electronics

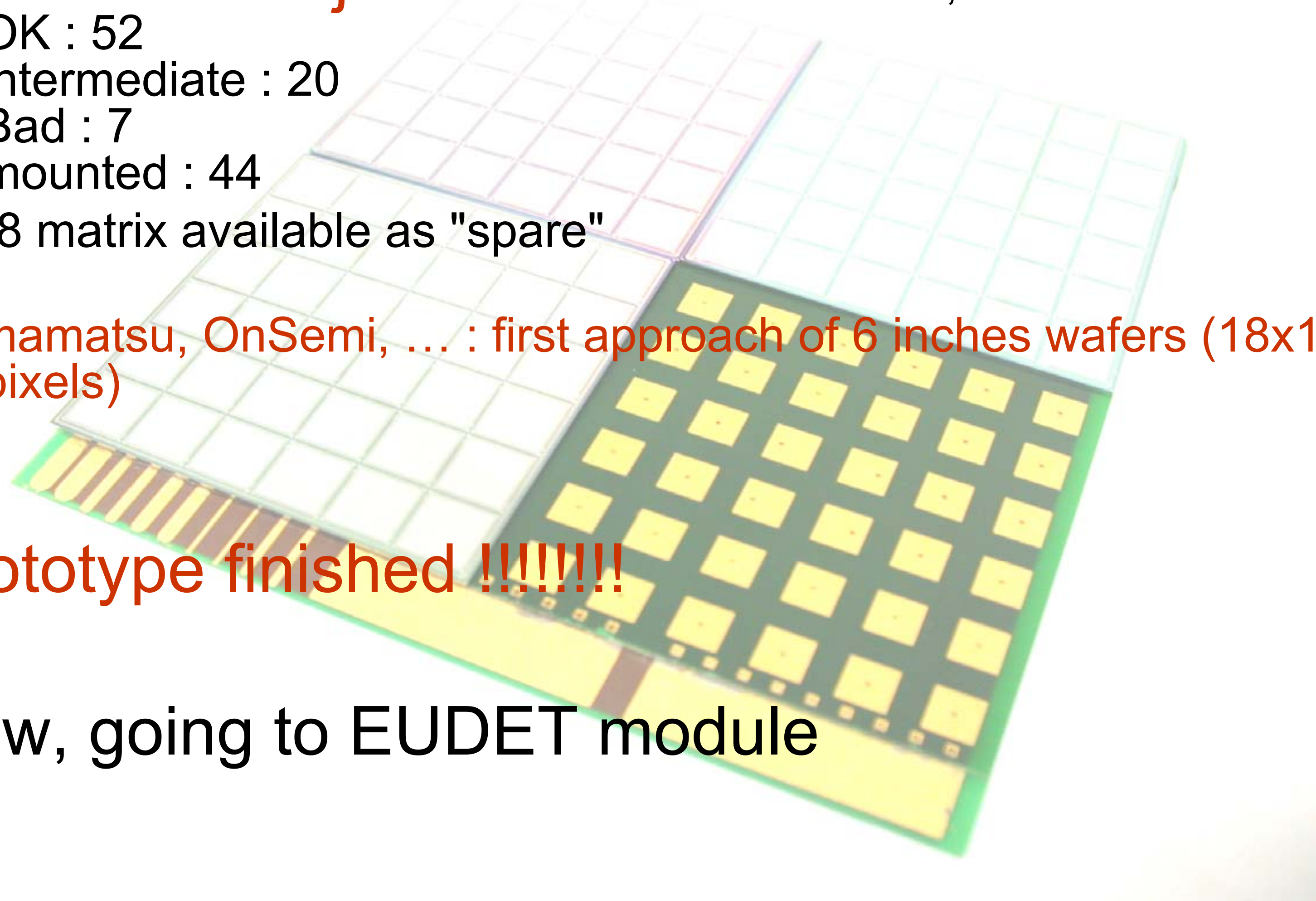
Characterization
- Charge injection
- pixel signal analysis

Includes 3 OPA (OPA380 or OPA657) for signal shaping and trans-impedance adaptation to a scope

Nd:YAG laser could be used to inject signal (or by simulations)

Wafer Production Status

Jean-Charles Vanel (LLR)



Production of june'07 : Total of 79 matrix, tested at LLR

- OK : 52
- intermediate : 20
- Bad : 7
- mounted : 44

28 matrix available as "spare"

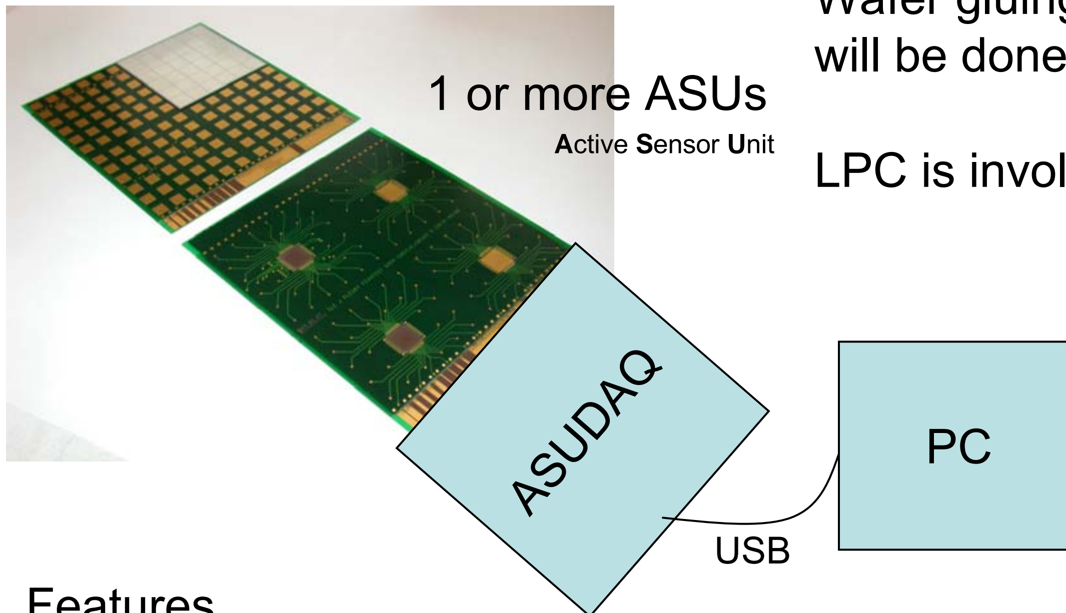
Hamamatsu, OnSemi, … : first approach of 6 inches wafers (18x18 pixels)

Prototype finished !!!!!!!

Now, going to EUDET module

ASUDAQ for ECAL

R&D on ASU



Wafer gluing and production tests will be done at Manchester

LPC is involved in the test bench development

Cosmic test bench for ASU characterization.

First R&D step towards EUDET production tests

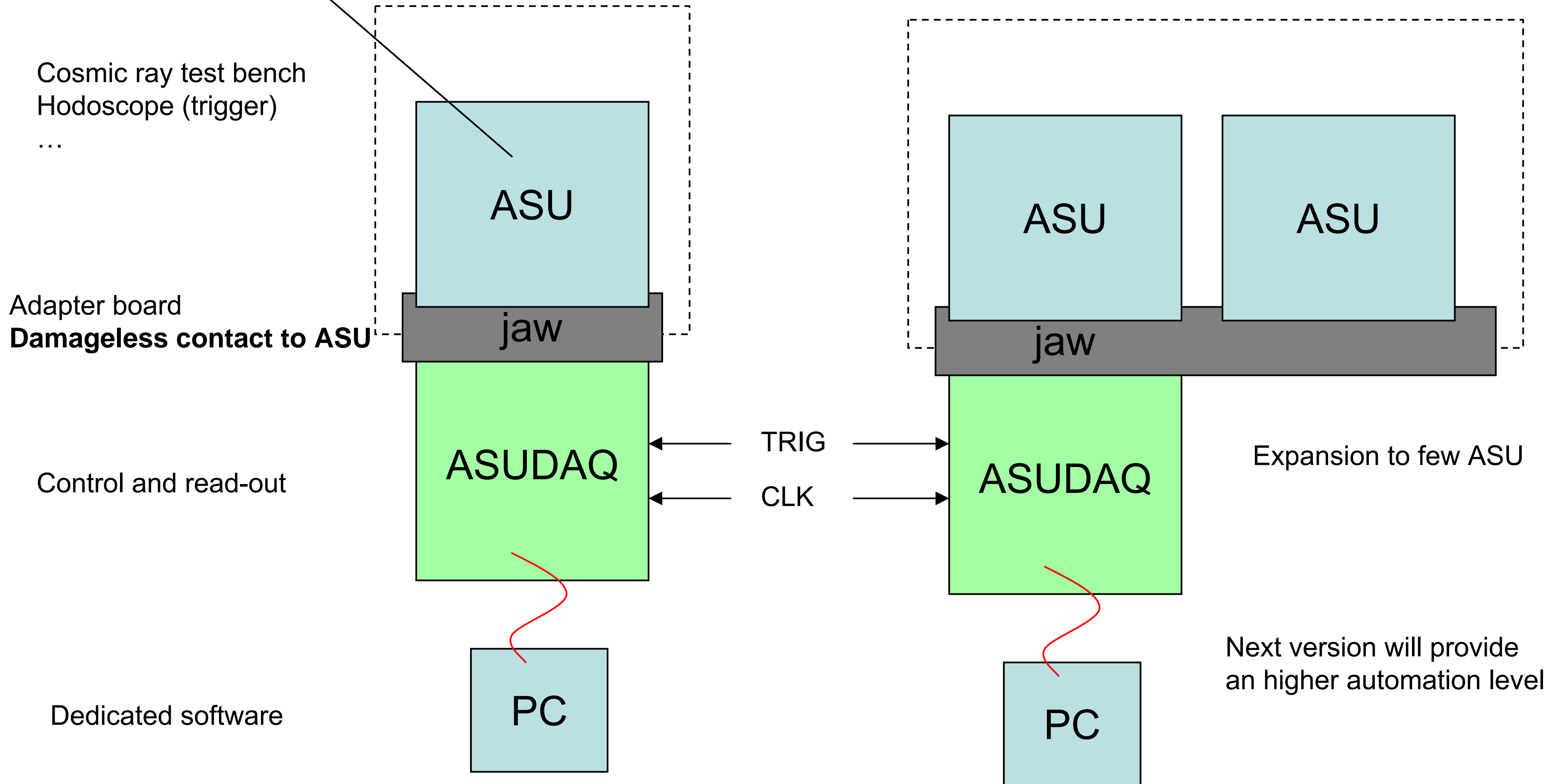
Features

- full **slow control** including internal probing system control
- access to analog test points (embedded ADC)
- **read out** of 4 SKiROC through USB & PC
- cosmic bench environment support (triggers)
- mechanical jaw providing damageless contacts to ASU

A board is being designed at LPC

ASUDAQ for ECAL

usage



Plans & Conclusion

Visit to OnSemi (Roznov, Cz) on 14 september 07

- 3x3 wafers specs and manufacturing

Simulations : on going

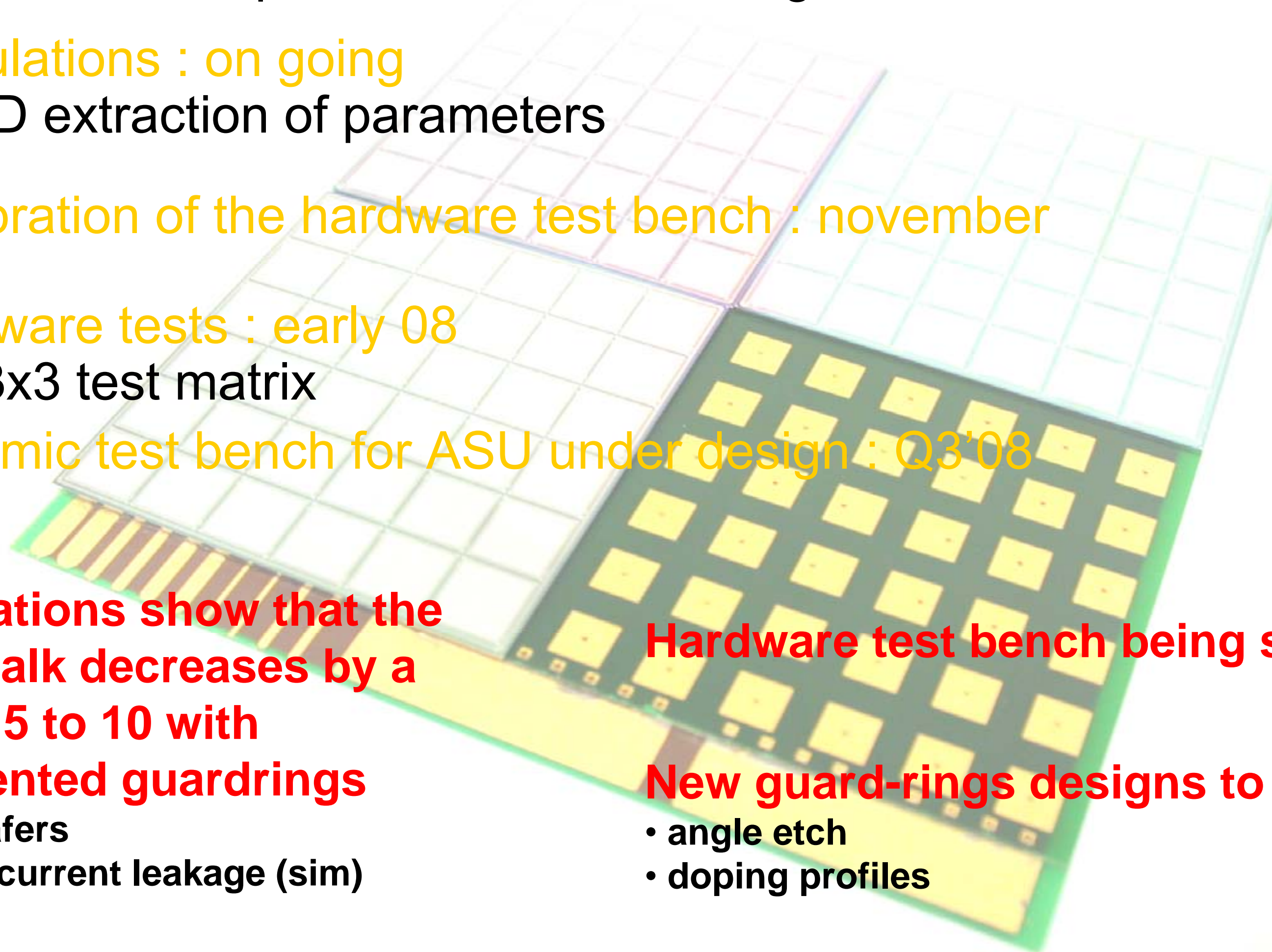
- 3D extraction of parameters

Calibration of the hardware test bench : november

Harware tests : early 08

- 3x3 test matrix

Cosmic test bench for ASU under design : Q3'08



Simulations show that the crosstalk decreases by a factor 5 to 10 with segmented guardrings

- **3x3 wafers**
- **check current leakage (sim)**

Hardware test bench being set up

New guard-rings designs to explore

- **angle etch**
- **doping profiles**