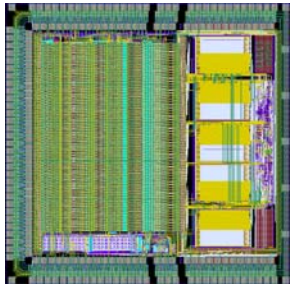
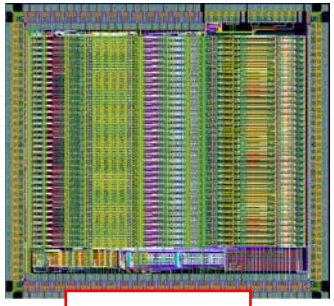
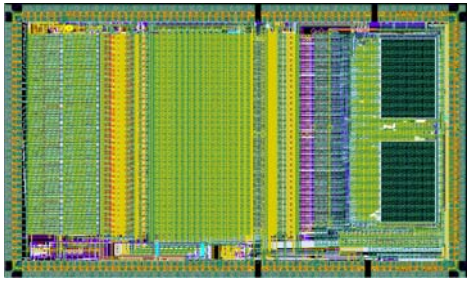


HaRDROC



SKIROC



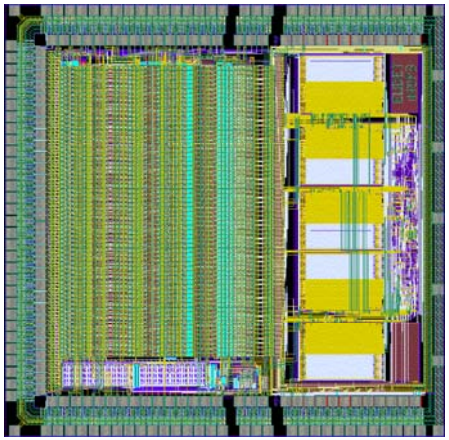
SPIROC

EUDET JRA3 Front-End electronics in 2007

C. de La Taille
IN2P3/LAL Orsay

Tasks for CALICE/EUDET in 2007

- **Complete physics prototype**
  - Add and test DHCAL, complete physics program
  - Test effect of em shower on ASIC



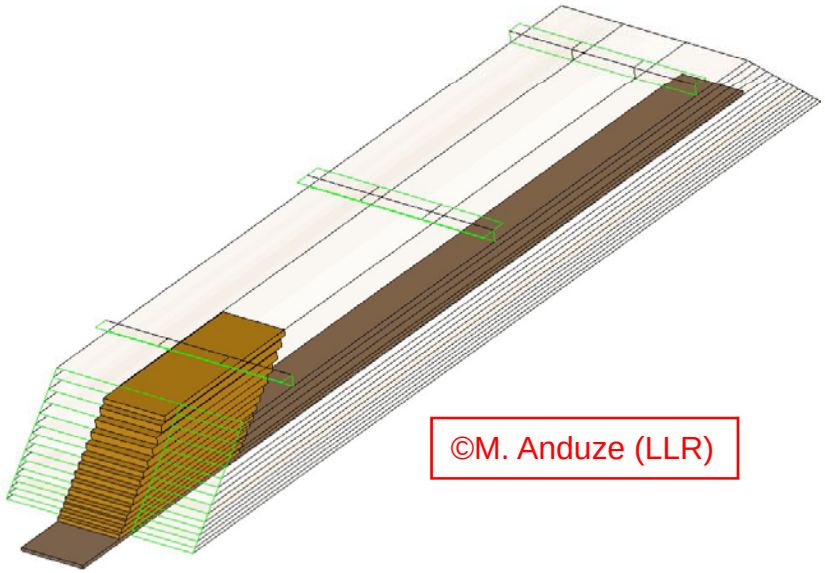
- **Measure performance of 2nd generation ASIC**
  - On testbench in different labs
  - DHCAL ECAL, AHCAL
  - Test 2nd generation DAQ (UK)

- **Design Very Front-End boards with integrated ASICs**
  - DHCAL board with HARDROC
  - AHCAL board with SPIROC
  - ECAL board with SKIROC (or SPIROC)

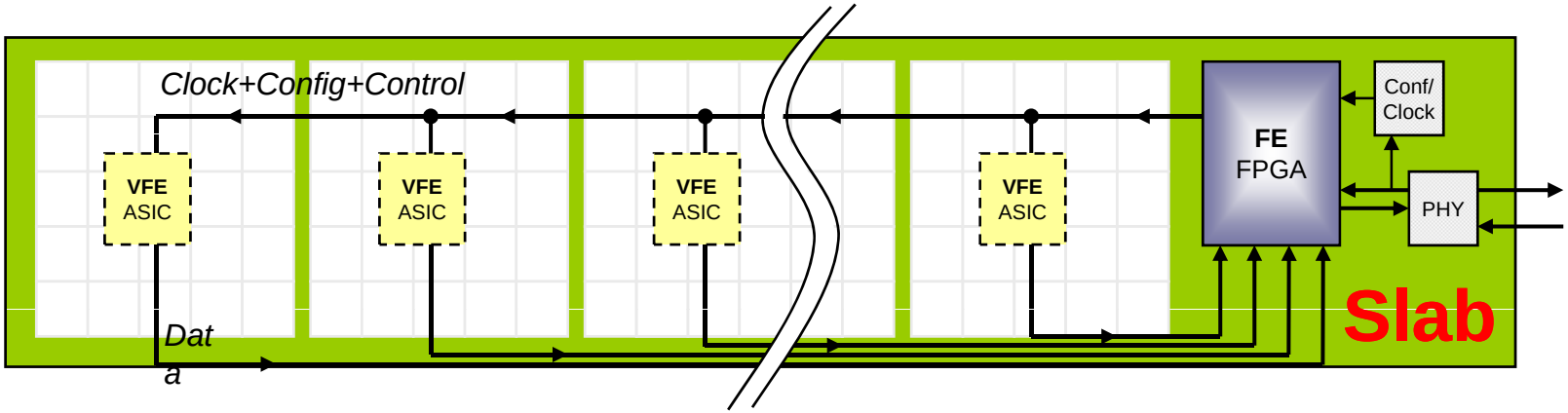
- **Design EUDET module(s) (demonstrator)**
  - Identify responsibilities and organize schedule
  - Moving to monthly meetings (in common with CALICE)
  - Aim at completing the design of EUDET modules beg 08

EUDET : ECAL module

- **Electromagnetic calorimeter**
  - Prototype of a (~ 1/6) module 0 : **one line & one column**
  - 150 cm long, 12 cm wide 30 layers
  - 1800 + 10800 channels
  - Test full scale mechanics + PCB
  - Can go in test beam
  - Test full integration + edge communications
- **To be delivered in 2009**

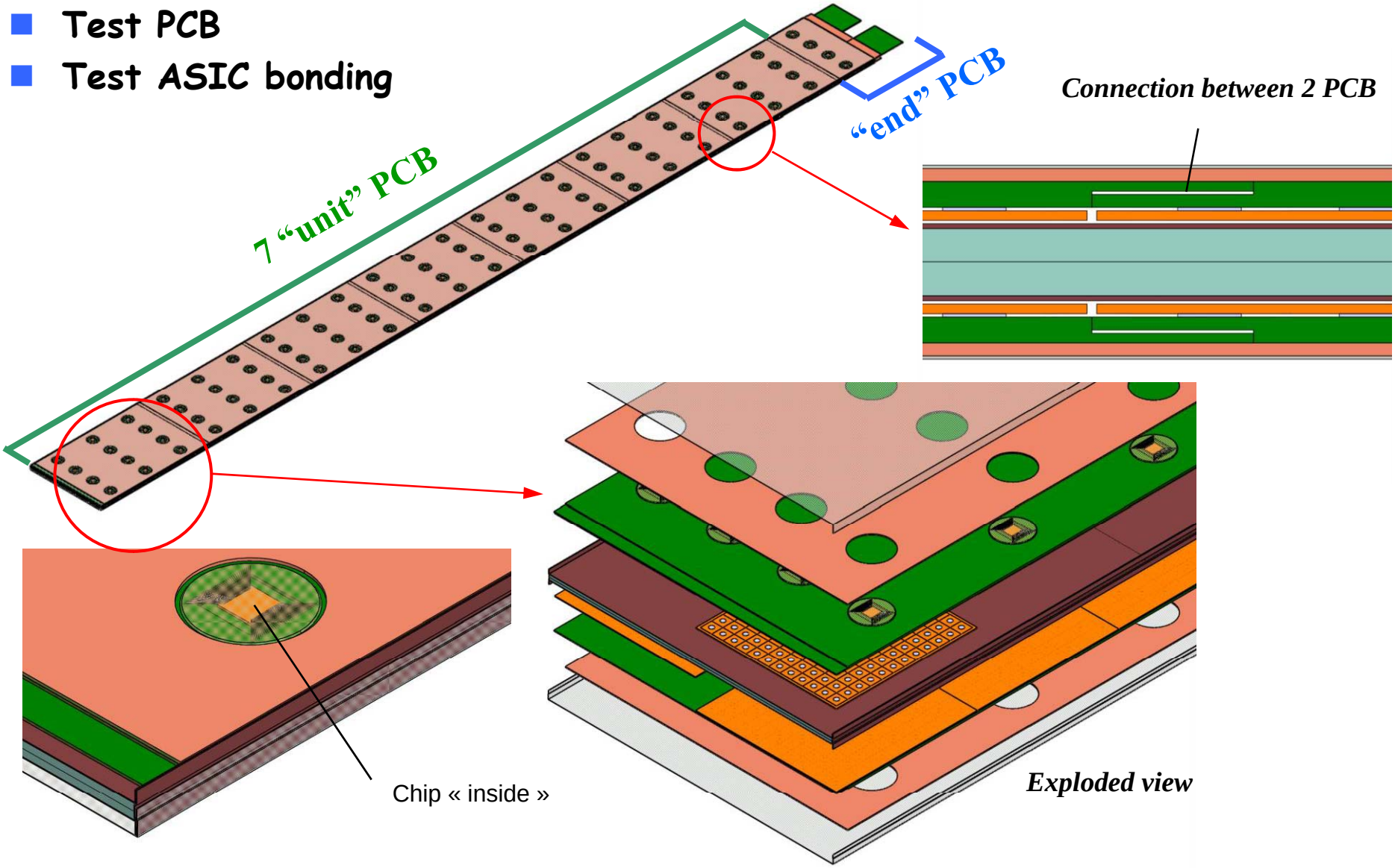


©M. Anduze (LLR)

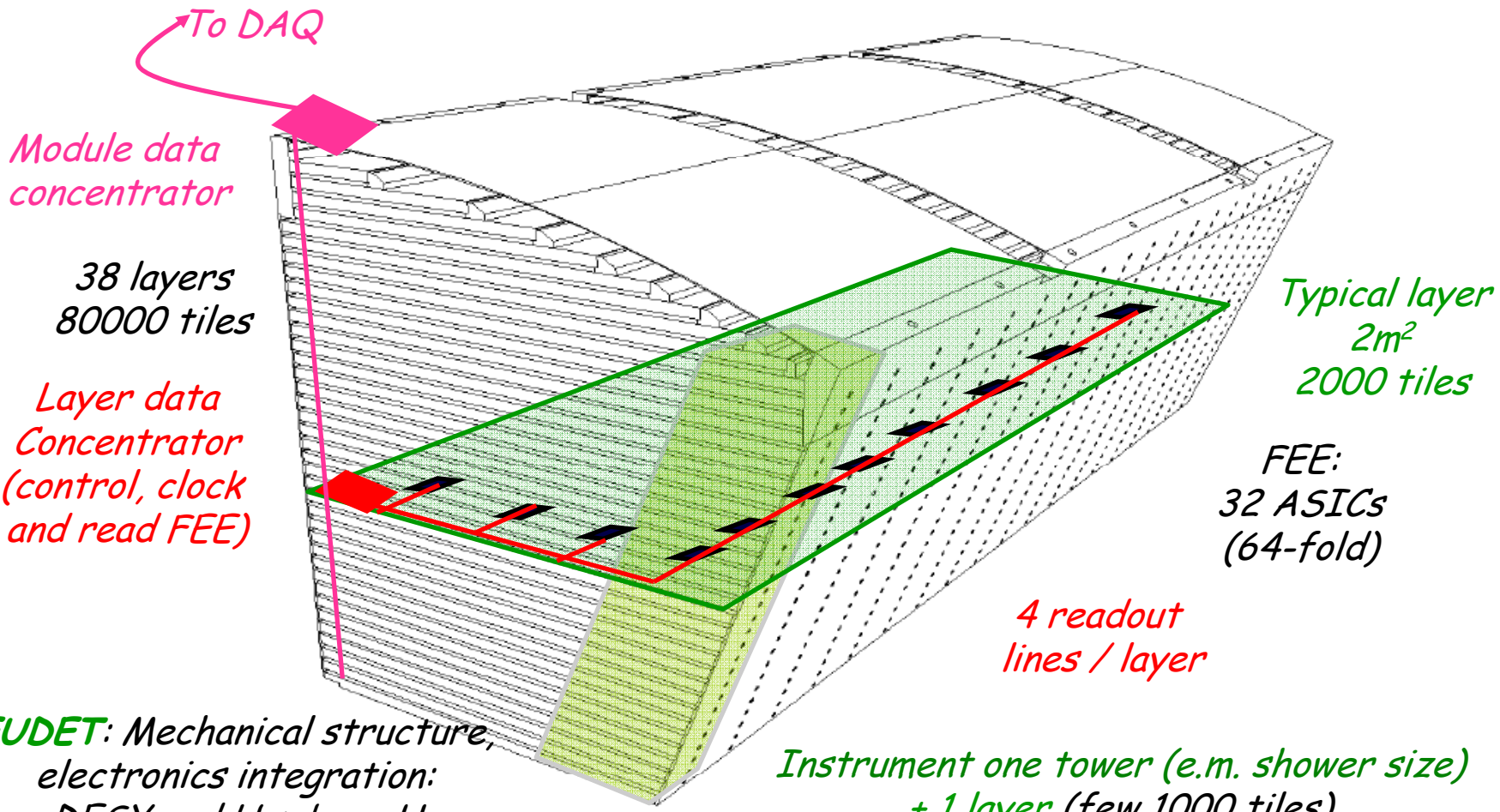


EUDET - Detector slab (2)

- Test PCB
- Test ASIC bonding

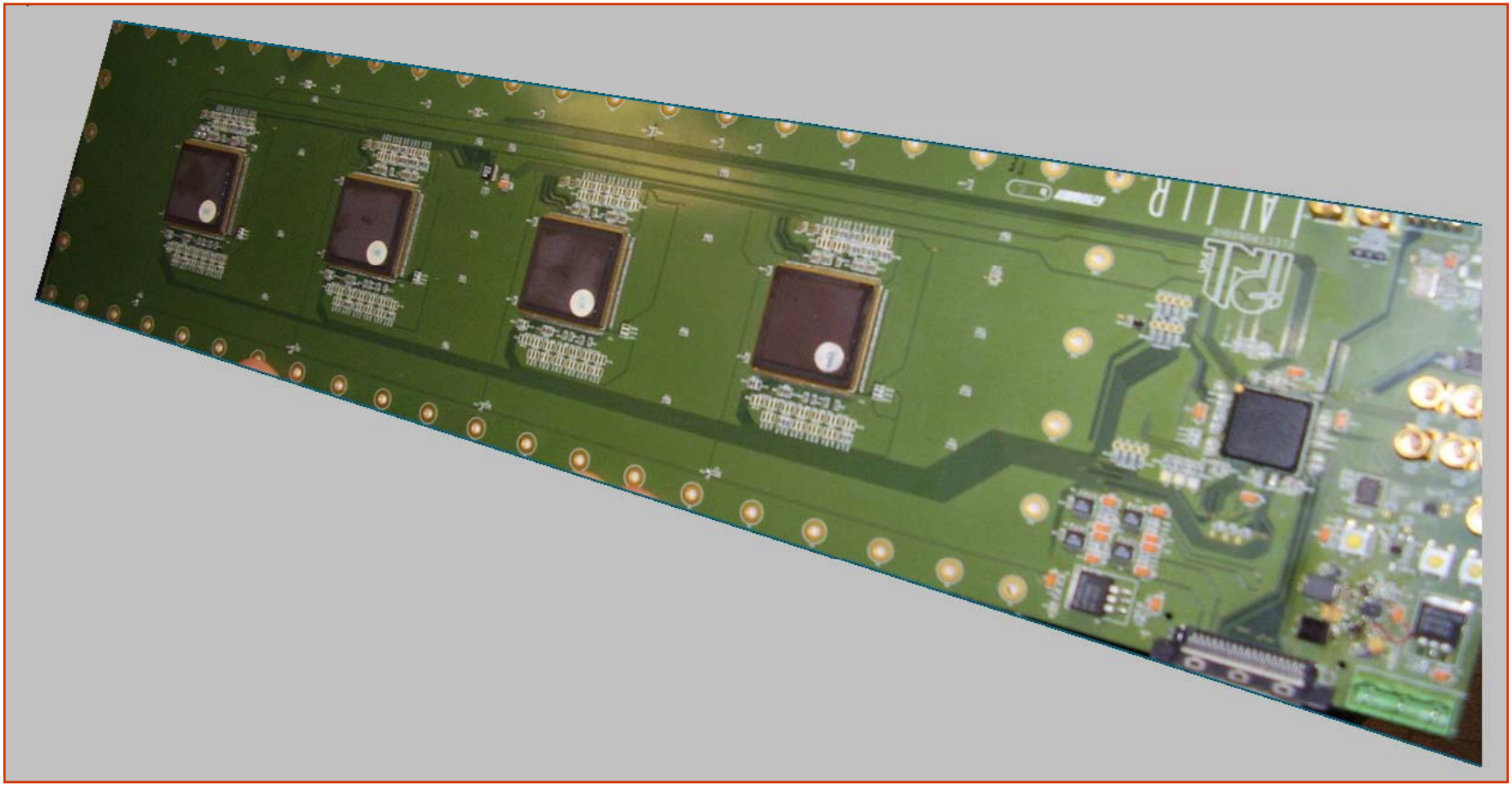


AHCAL architecture



DHCAL architecture

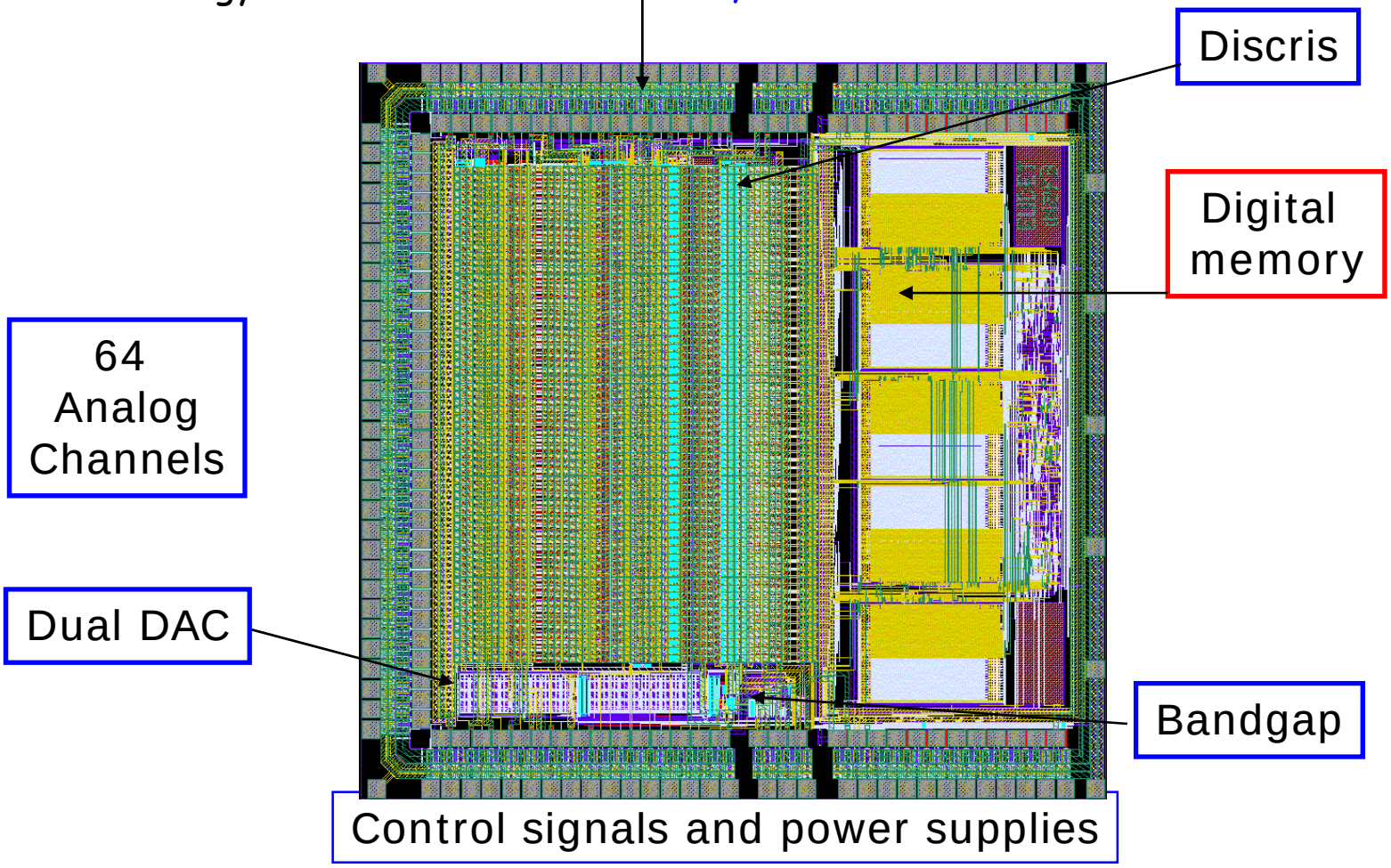
- First detector with 2nd generation ASCIs and 2nd generation DAQ
- Board received in june 07, tests starting



HaRDROC chip for DHCAL [LAL,IPNL]

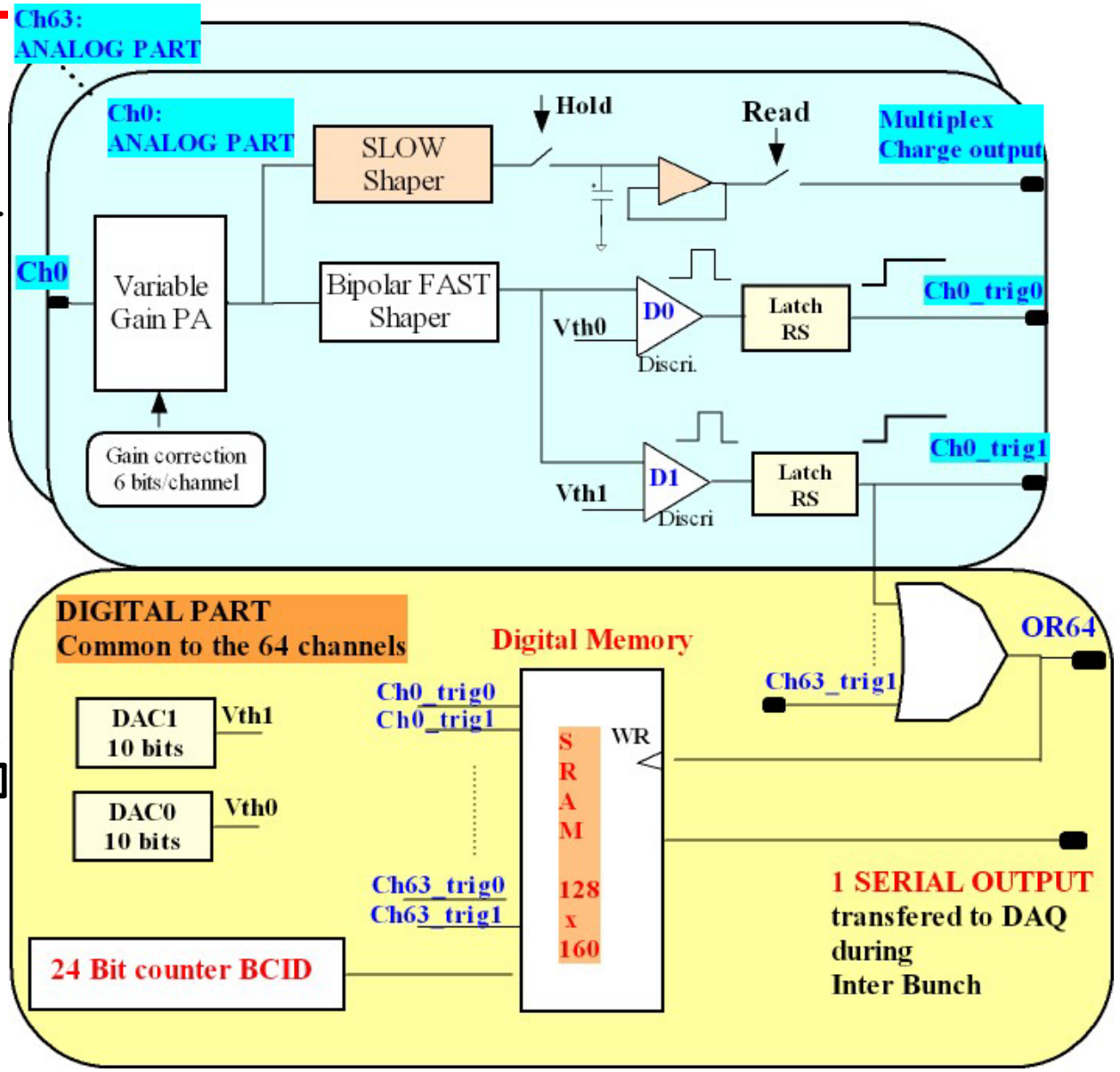
JRA3 Milestone

- **Hadronic Rpc Detector Read Out Chip (Sept 06)**
  - 64 inputs, preamp + shaper+ 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ : only 1 digital data output
  - Technology : AMS SiGe BiCMOS 0.35 µm



HaRDROC architecture

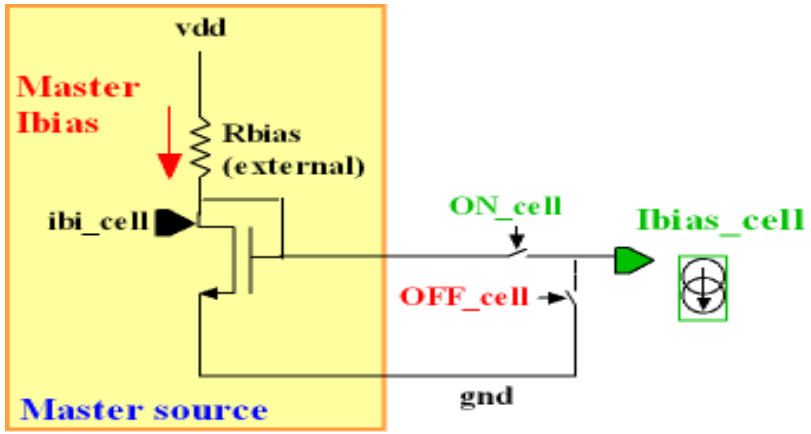
- Full power pulsing
- Digital memory: Data saved during bunch train.
- Only one serial output @ 1 or 5MHz
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- Based on MAROC ASIC, but several design changes



HARDROC POWER PULSING: Power dissipation (1)

- **Maximum power available:**
  - 10 µW/ channel with 0.5% duty cycle

  => 640µW/3.5V=**180 µA** for the entire chip
  - **OFF**= Ibias _cell switched off during interbunch:

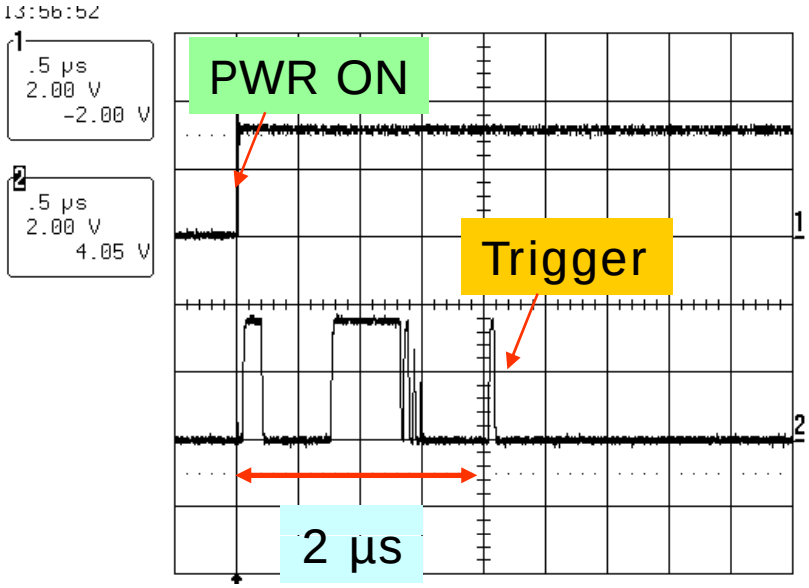


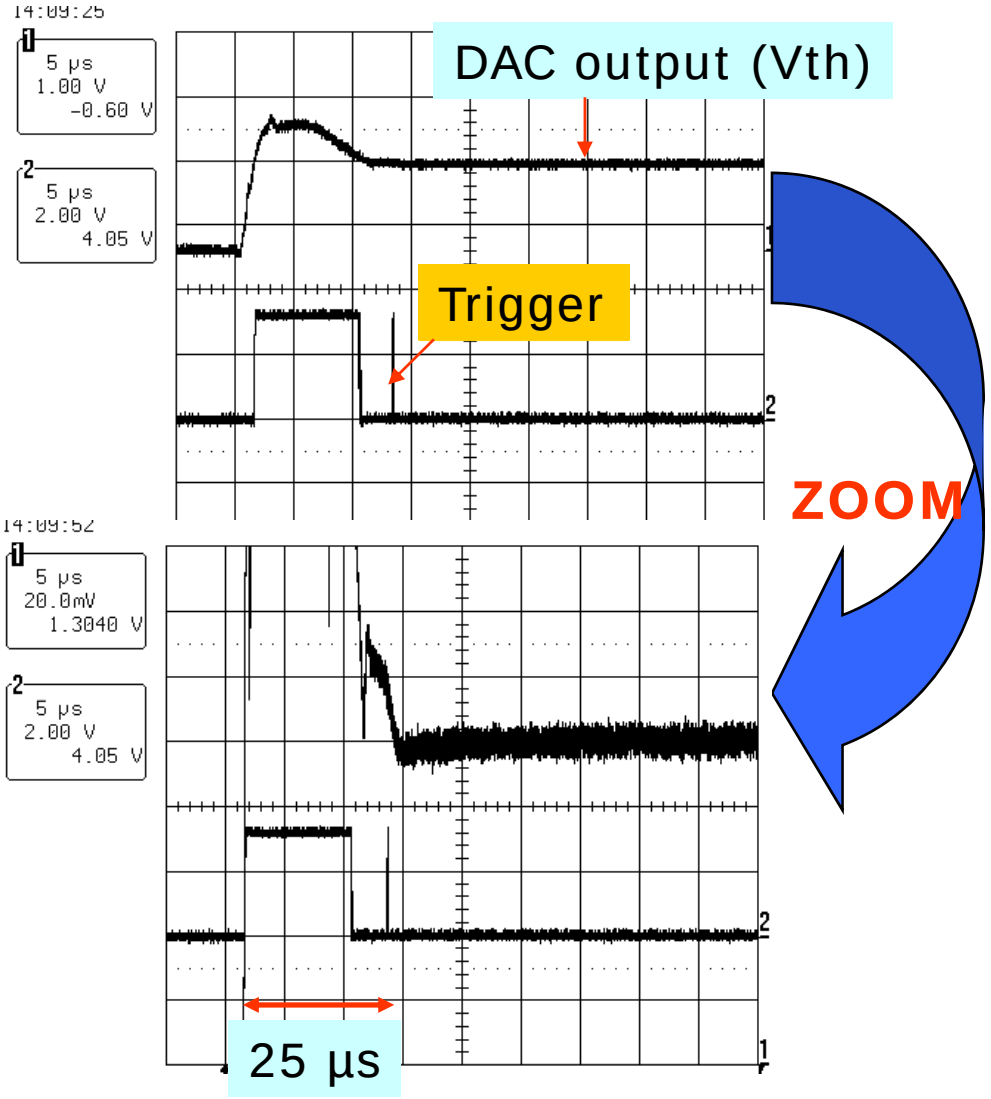
	ON	OFF
Vdd_pad	0	
Vdd_pa	5.8 mA	5.6 µA
Vdd_fsb	4.9 mA	65 µA
Vdd_d0	2.8 mA	78 µA
Vdd_d1	2.7 mA	0
Vddd+ vddd2	3.3mA	200µA + 0 (Clk OFF)
Vdd_dac	0.77 mA	218 µA
Vdd_bandgap	5.05 mA	2.73 mA
Total (noPP)	25.3 mA	3.2mA
Total with 0.5% PP	125 µA	0 hopefully

  - BUT a few forgotten switches…
    - Bandgap, some reference voltages not power pulsed
  - **Easy to fix in the production version**

SW to be added to switch off all the master Ibias, Vref, V_BG…

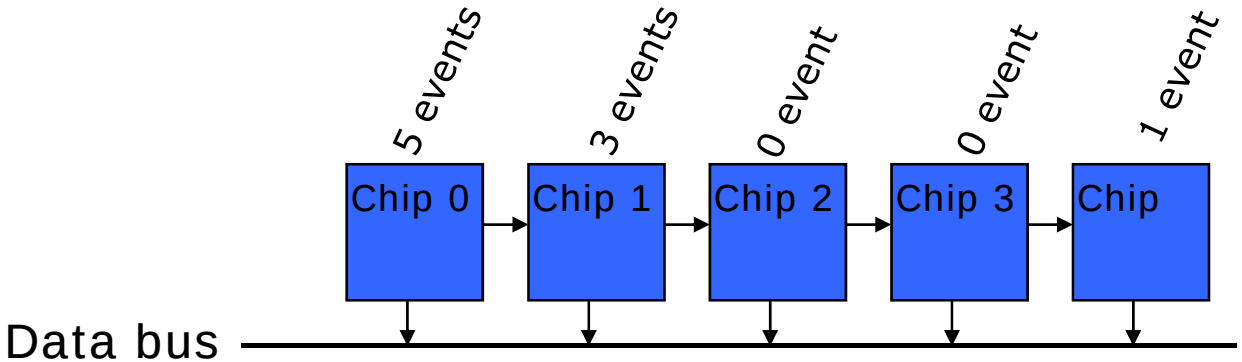
HARDROC Power pulsing: « Awake » time (2)

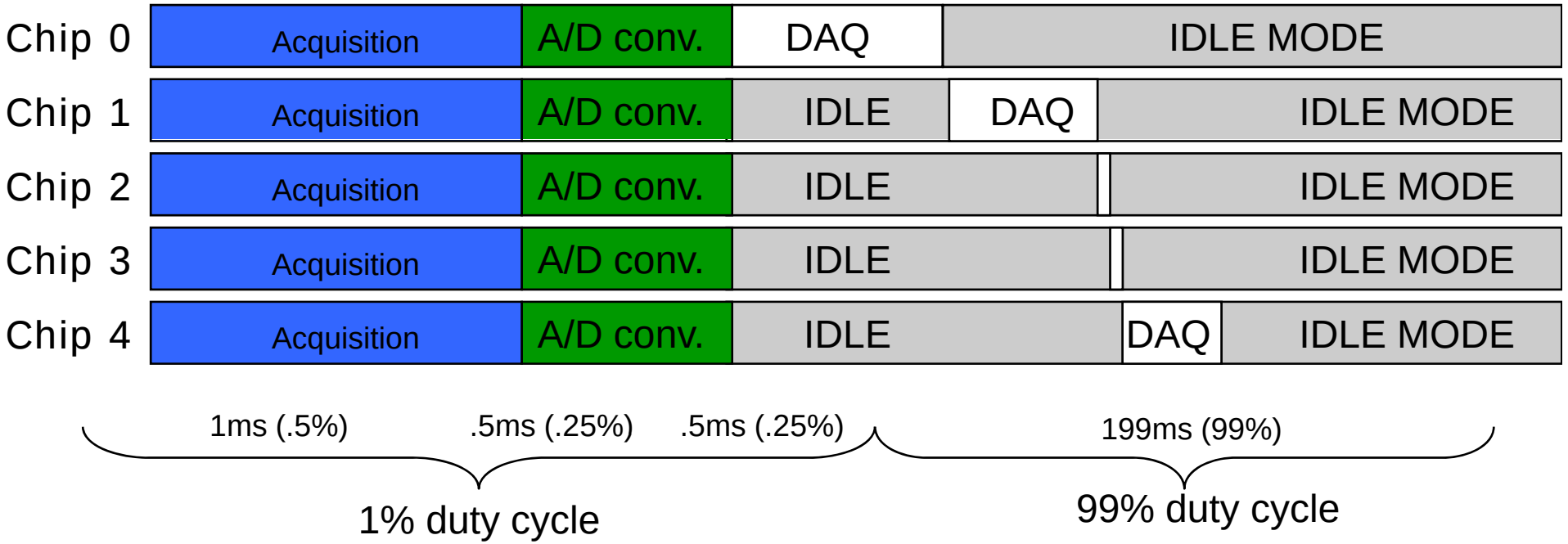




- **PWR ON: ILC like (1ms,199ms)**
- **All decoupling capacitors removed**
- **PP of the analog part:**
  - Input signal synchronised on PWR ON
  - Injection of 100fC, Threshold= 30fC
  - => **Awake time= 2 µs**
- **Power pulsing of the DAC:**
  - **25 µs (slew rate limited)**

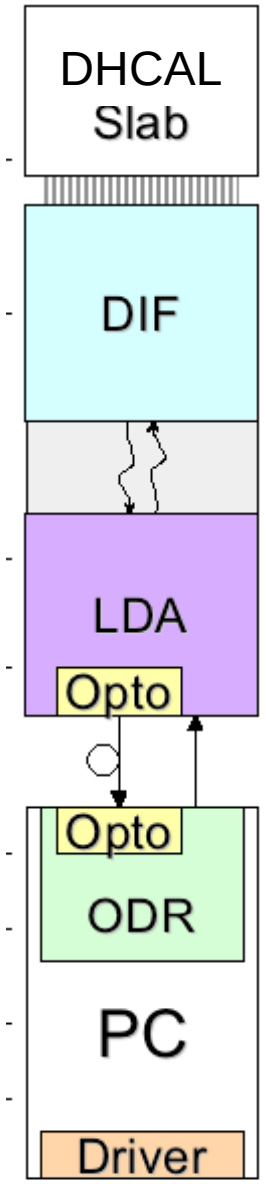
Read out : token ring





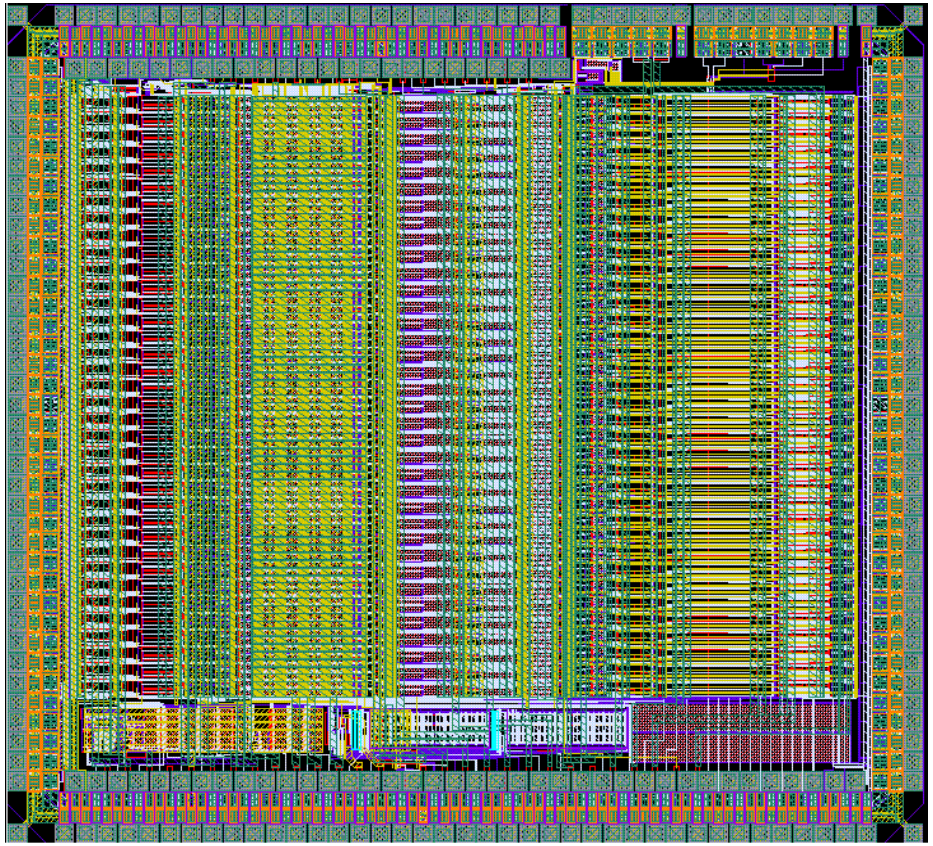
Digital part: DAQ2

- **DAQ and online system**
  - **Common to all detectors**
  - Crateless, non-custom, **ILC-like system** with readout directly into PCs
  - System-dependences isolated to single interface (LDA-DIF)
  - DIF task force to define interface to slabs and DAQ
- **Offline software**
  - Common and based on LCIO, Grid



SKIROC for W-Si ECAL

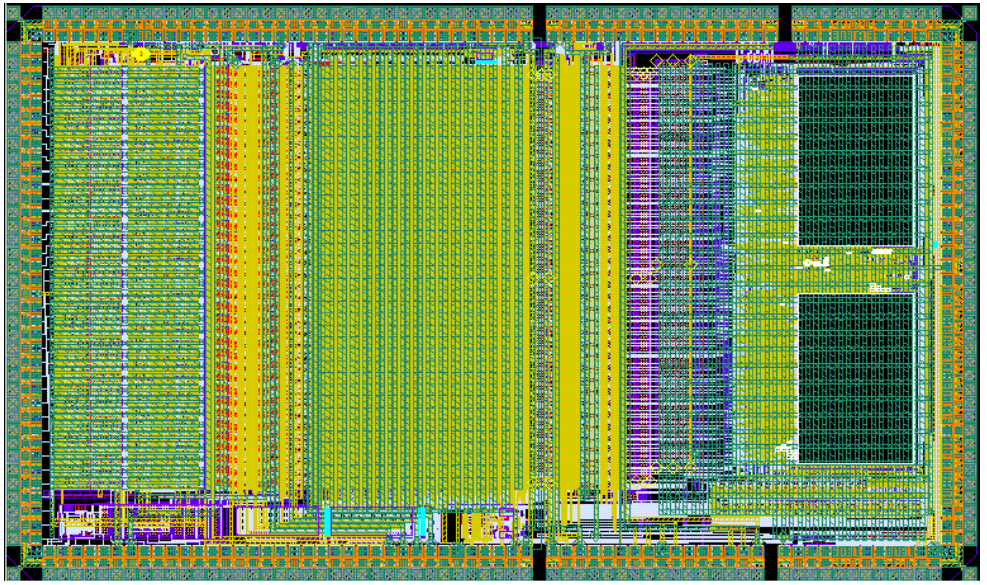
- **Silicon Kalorimeter Integrated Read Out Chip (Nov 06)**
  - 36 channels with 16 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07, tests starting

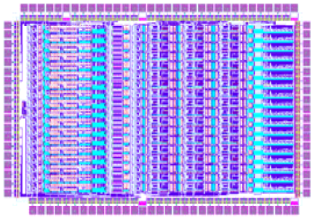


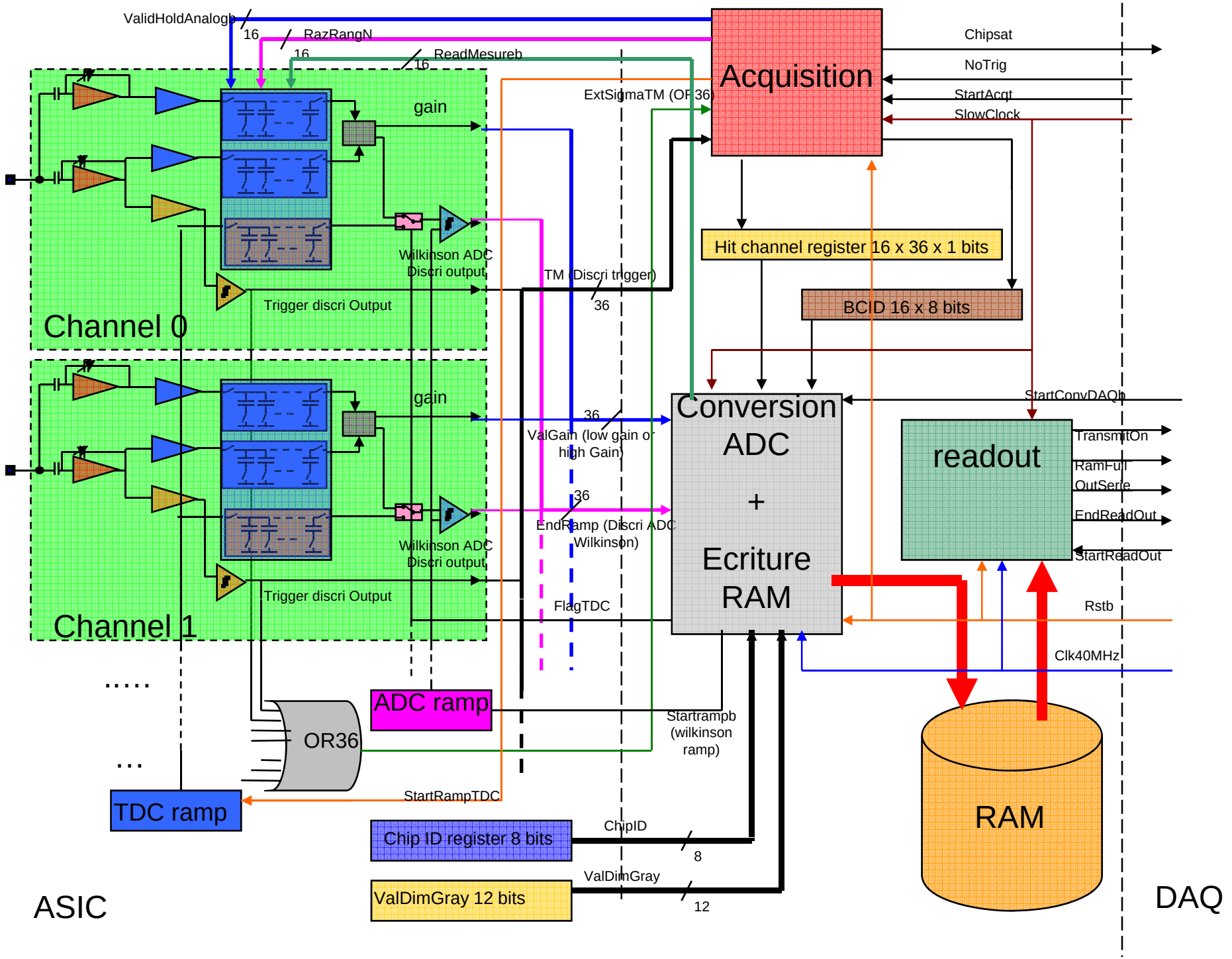
SPIROC overview

JRA3 Milestone

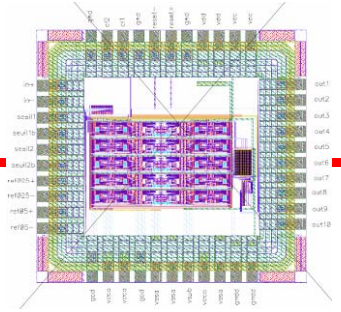
- Silicon Photomultiplier Integrated Read Out Chip
  - A-HCAL read out
- Silicon PM detector
  - G = 3 E5 to 1 E6
  - Same biasing scheme as TB
- 36 channels
  - Charge measurement (15bits)
  - Time measurement (< 1ns)
- Compatible with old & new DAQ
- Complex chip,, but many SKIROC, HARDROC, and MAROC features re-used
- Submitted june 11th
  - Expected september






ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

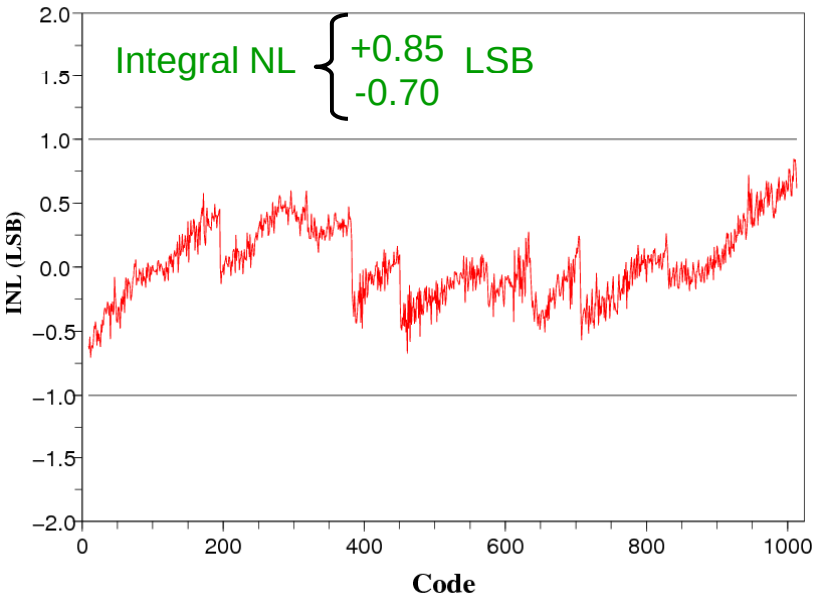
On-going R&D : ADCs, FCAL…

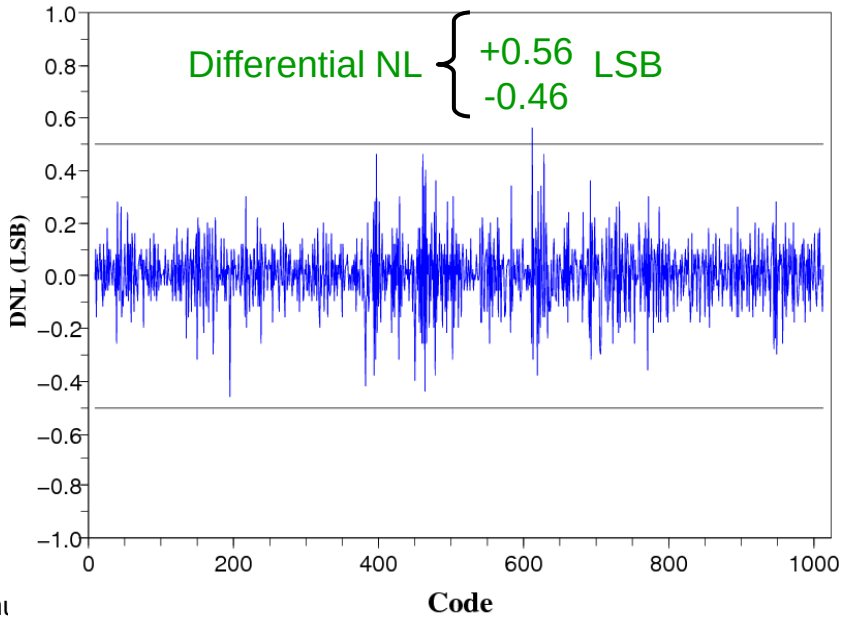


- **Characteristics:**
  - Technology: CMOS SiGe 0.35µm
  - Power supply: 5V (digital: 2.5V)
  - Clock frequency: 40 MHz
  - Differential architecture
  - 10 stages - 1.5 bit/stage
  - Die area: 1.2 mm²

- **Performance (measured):**
  - Resolution: 10 bits
  - Consumption: 35 mW
  - Conversion time: 0.25 µs (@ 40MHz)
  - Integrated cons.: (35mW * 0.25µs)/200ms= .044µW

Noise (measured):
< 0.47 LSB @ 68% C.L.



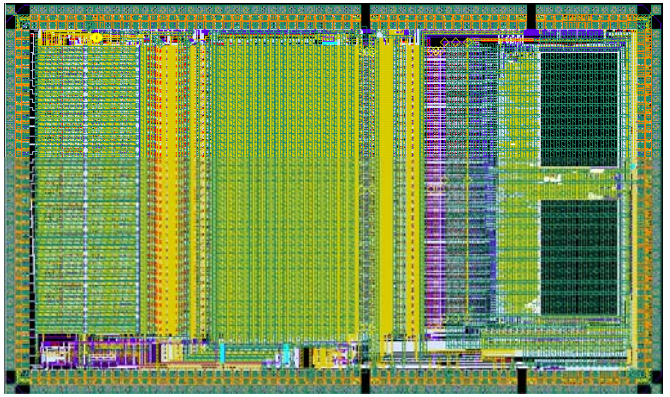


Common issues

- **Power pulsing studies**
  - Power management and distribution
  - Stability,
  - Clock distribution
- **DAQ**
  - Zero suppressed data
  - Minimum number of lines
- **ASIC technologies**
  - « Analog friendly » technologies : now mostly 0.35µm AMS SiGe
  - Sharing blocks, MPWs : in2p3, Krakow….

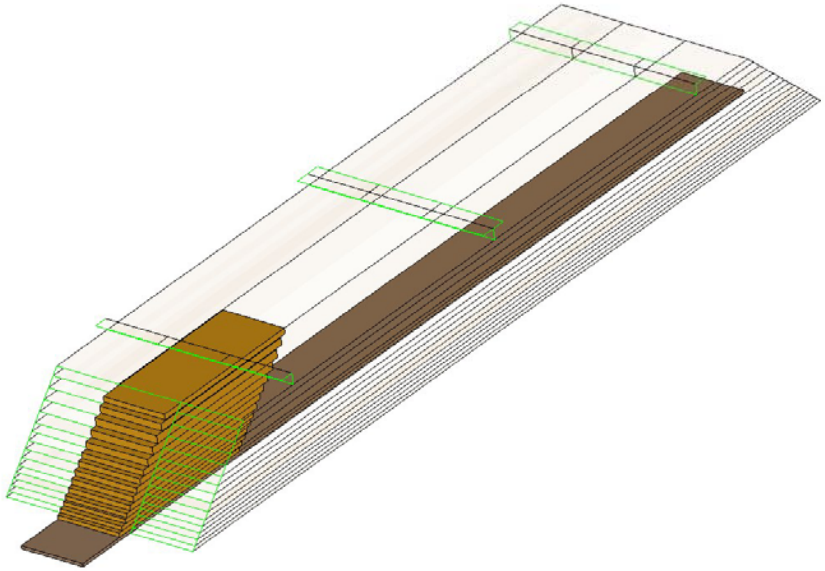
Conclusion

- **3 major second generation ASICs for technological prototypes submitted**
  - HARdROC submitted for DHCAL RPCs
  - SKIROC submitted for ECAL Si-W
  - SPIROC for AHCAL SiPM



- **System aspects now proceeding**
  - Power pulsing, Zero-suppress, Auto-trigger, 2nd generation DAQ…
  - On detector boards
  - Connection to DAQ : task force
  - EUDET repository for shared VHDL code

- **EUDET modules in 2009 is challenging !**
  - Production of all ASICs mid 2008 !
  - Organization coming in place

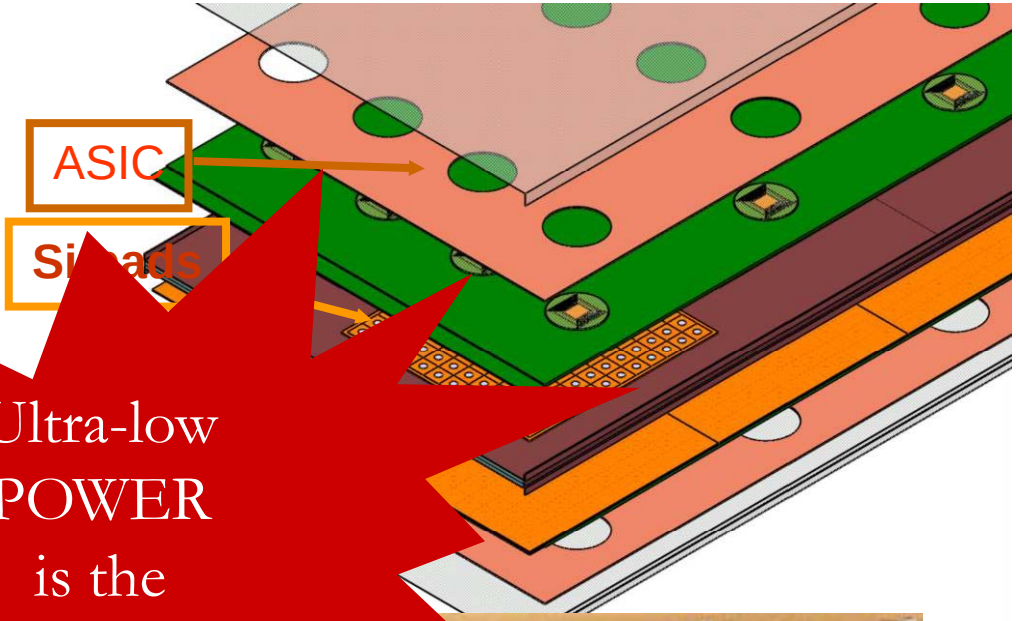


Milestone	Date	Task
Analogue ASIC prototype 1 available	6	E
PCI card prototype available	9	D
AHCAL FE board prototype ready	18	E
Modified stack available	18	B
DHCAL VFE conceptual design ready	18	E
Analogue ASIC prototype 2 available	19	E
Prototype of laser positioning system ready	24	C
Sensor test facility ready	24	C
Readout electronics design ready	24	C
Integrated ASIC available	30	E
Final DAQ system available	30	D
DHCAL VFE engineering design ready	36	E
Front-end electronics infrastructure available	36	E
AHCAL FE boards produced	39	E
Integrated system available	42	B
Detector test facility ready	48	C
Construction complete	48	A

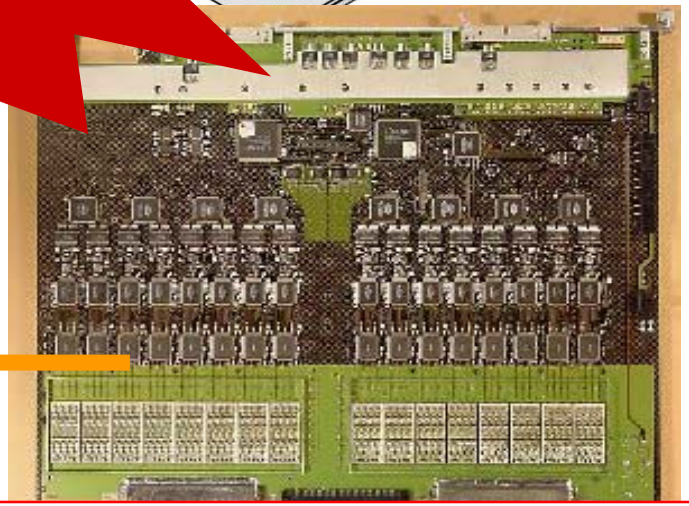
ILC Challenges for electronics

- **Requirements for electronics**
  - Large dynamic range (15 bits)
  - Auto-trigger on ½ MIP
  - On chip zero suppress
  - Front-end embedded in detec
  - **Ultra-low power : (« 100**
  - 10^8 channels
  - Compactness

- **« Tracker electronics wi**
  performance »



Ultra-low POWER is the KEY issue



ILC : **100µW/ch**

FLC_PHY3 18ch 10*10mm **5mW/ch**

ATLAS LAr FEB 128ch 400*500mm **1 W/ch**