JRA3: Calorimeter DAQ status

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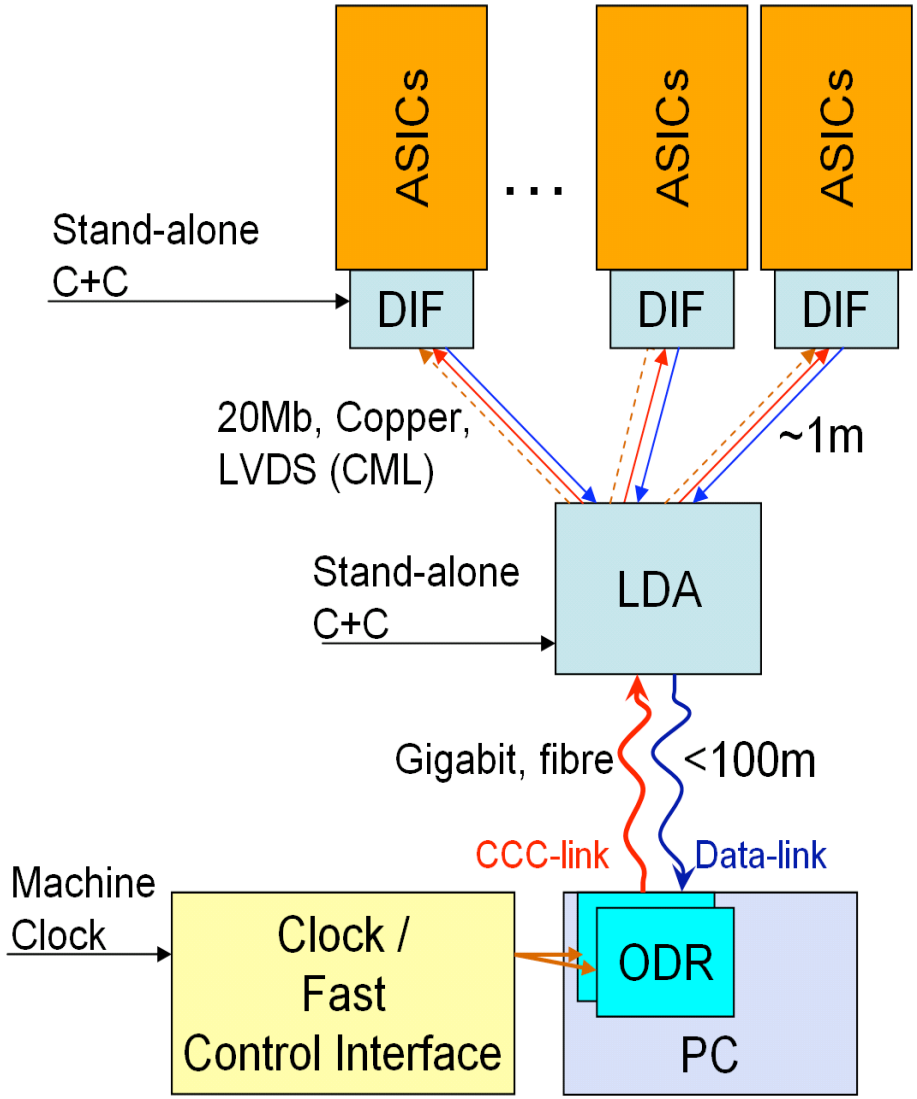
- General overview
- Some details of work
- Administration

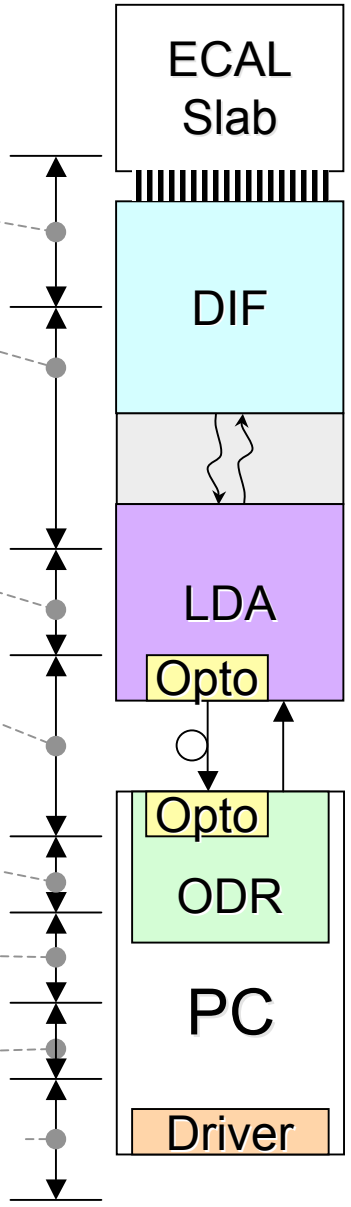
Ideal DAQ Structural Overview

- Detector ASICs on e.g. ECAL slab
- Front-End (FE)
  - FE-Interface (DIF): Detector specific
  - FE Link/Data Aggregator (LDA): Generic
- Data-link (FE to Off-Detector Receiver)
- CCC-link (Clock+Control+Config to FE)
- DAQ PC
  - Off-detector receiver/s (ODR)
  - Drives CCC-link
  - Data Store



UK Read-out work (ECAL FE)

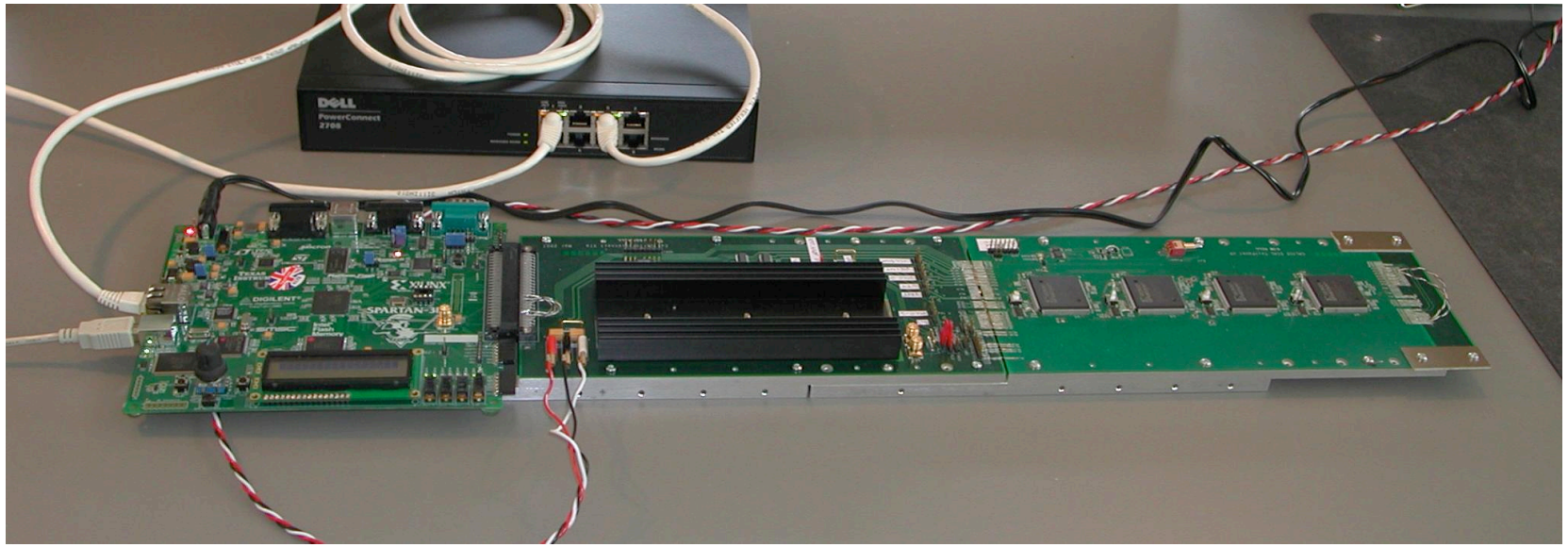
- Detector Interface (Cam, IC)
  - Spec + hardware
- DIF to Link/Data Aggregator (Cam/Man)
  - Spec + hardware
- Data aggregate, format (Man)
  - Hardware + firmware
- LDA to ODR opto-link (Man, UCL)
  - Hardware + firmware
- ODR (RHUL, UCL, Cam)
  - firmware
- ODR to disk (RHUL)
  - Driver software
- Local Software DAQ (RHUL)
- Full blown Software DAQ (RHUL, UCL, [IC])



General overview

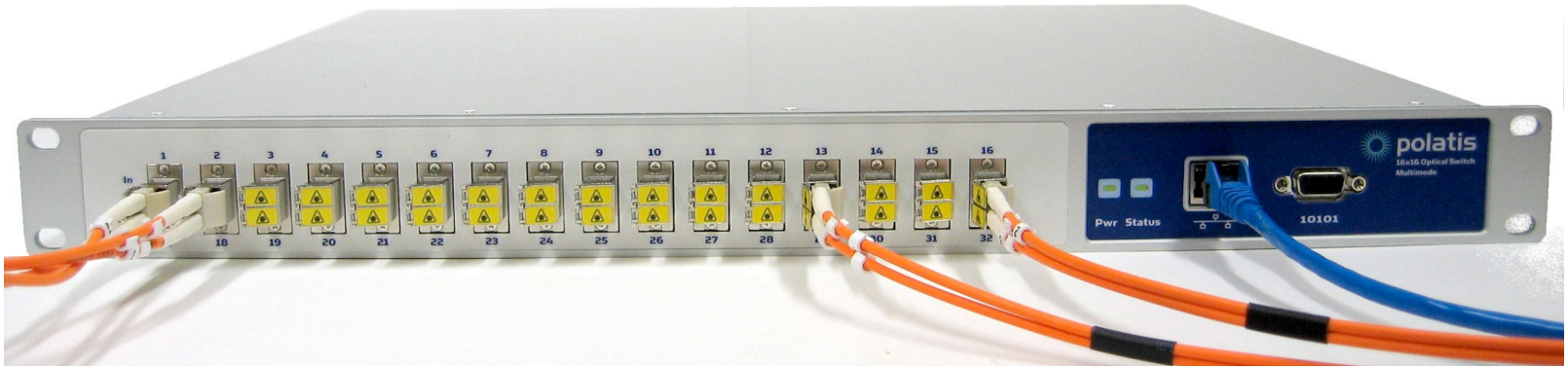
- A DAQ structure has been defined for all calorimeters - adopted by CALICE.
- Testing ASICs produced by LAL
- Development and tests of model 1.5 m slab
- High-speed and efficient networking
- Interfaces are being specified (e.g. LDA ➔ DIF) - needed by calorimeter builders
- Development of LDA and ODR hardware, firmware and test software
- A general structure for the DAQ software has been drawn up and work has started

Test slab



- Mock slab to test data paths over 1.5 m
- Single-panel slab (~25 cm) fully functional
- Leads to ideas on DIF design: ideas of functionality and schematics being drawn up
- Simulating full data stream, slab ⇔ ODR, to allow tests of e.g. a given detector/chip.

LDA and networking



- Optical switch between detector and ODR to reduce data loss for e.g. busy from ODR.
- High-speed networking, 10 Gbit, to reduce components.
- LDA-DIF interfaces crucial and document of our ideas exists.
- LDA connected to multiple DIFs. Considering hardware available for LDA.

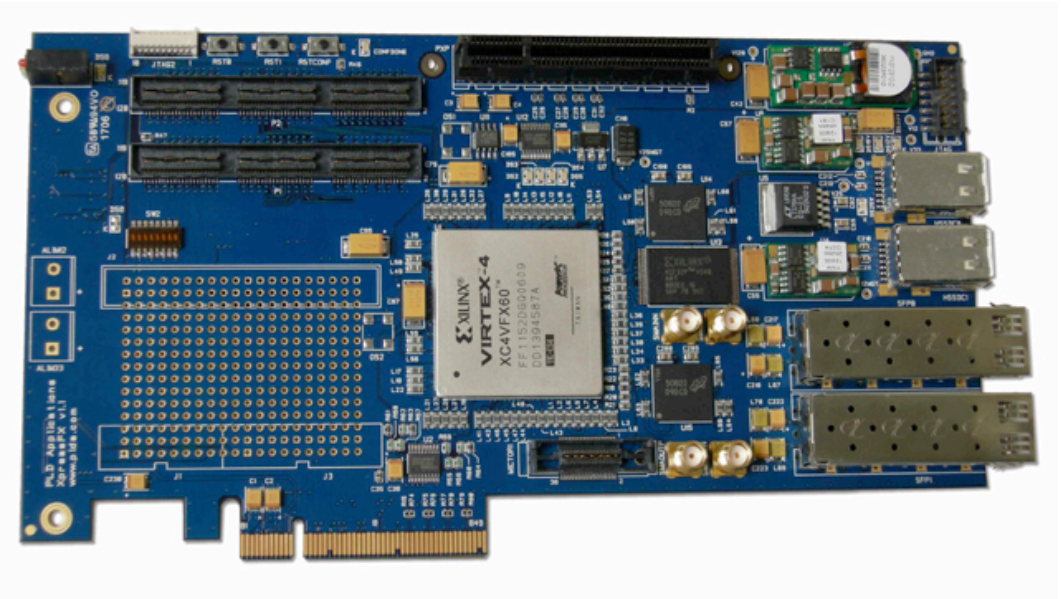
PCI prototype development

- Goal to have PCI prototype boards, housed in PCs, to act as an off-detector receiver (ODR)
- Use commercial components - flexible, easily upgradeable, cope with high rates and volume:
  - Optical and copper links, big FPGA, serial bus, etc.

Hosted in computers in our labs.

- Have a box diagram of a structure for passing data in such a system.
- Firmware essentially done for each box
- Can read data in (and out) of host memory
- Optimisation of performance

PCIe cards from PLD application (http://www.plda.com/



Administration

- PCI prototype available (June 2007) - complete, written up (briefly) in EUDET-Memo-2007-14
- DAQ system prototype available (September 2008)
- DAQ system available (June 2009)
- Finances okay.