VFCAL Report

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Infrastructure for sensor diagnostics FE Electronics Development Sensor test facilities Laser Alignment

Labs involved: Cracow UST, Cracow INP, Prague (AS), Tel Aviv Univ. DESY (Z.)

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Current design (Example LDC, 14 mrad):



Infrastructure for Sensor and FE Tests

Rooms (Cracow, DESY):

two rooms with filtered air (10k), stabilized temperature

- room 1: bonding and assembly
- room 2: all measurements without radioactive source

Upgrade of the probe station at DESY

- New voltage- current devices (Keithley 6487)
- Control software
- Amplifier test bench







Infrastructure for Sensor and FE Tests

Tel Aviv: Laboratory room is found and prepared

- Most components of the computer controlled silicon probe station are purchased
- LabView runs with a test circuit just ongoing
- Calibration with real but known Si pads in a few weeks

Prob Station in TA



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Infrastructure for Sensor and FE Tests

Design Flow for IC readout chip tests with the custom sequencer V1495





C.A.E.N. V1495 general purpose I/O module

w/ LVDS and NIM In/Out channels

Test Example: PHY3



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FE Electronics Development

Preamplifier for laband test-beam applications - Low noise (~200 e-) - 4 channels per board - Low cost (summerstudent contribution)



Prototyping of 12 channel Integrated FE (amplifier and ADC)

Charge sensitive variable gain
test mode: S/N ~ 10 physics mode: ~ 10 bit
Tpeak: 50-70 ns



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Mokka (Geant 4) simulation of LumiCal Digitisation

- 1. 500 GeV electrons for 8-Bit & 10-Bit schemes.
- Energy MPV of a MIP in
 0.3 mm thick silicon is 93.8 KeV.
- 3. The maximal number of MIPs in a single cell is 3,010.
- 4. 95% of the signal is below 10,575 pC = 2,586 MIPs







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FE Electronics Development



No change with regard to the non-digitized case (The same goes for 10-Bits...).



First (few 10) pieces of FE ASICS Produced and prepared for tests Tests complete in December 2007 Submission based on a refined design beginning of 2008 Pad Pitch 100 µm

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DESY-HF

FE Electronics Development

Pipeline ADC concept



- 9 stages for 10 bit
- A stage produces 2 bits and multiplies signal by 2
- Digital correction relaxes comparator requirements



- 8 stages of 1.5 bit
- Size 1.<u>15x1.11 mm</u>
 - •First Prototypes of the ADC functional blocks are produced
 - Test will start soon and completed in December 2007
 - •Submission of a 'second generation' prototype beginning of 2008

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Test Beam Equipment



collimator (I_{Coll})

 $Faraday cup (I_{FC}, T_{FC})$ sensor box (I_{Dia}, T_{Dia}, HV)

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Testbeam



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Example: Silicon pad sensors from BNL

Data analysis is ongoing, preliminary results expected for the EUDET annual meeting in Octobre

Silicon Sensors for LumiCal

- Sensor prototypes designed
- Contacts to several manufacturers
 - Tower Semiconductors Israel Hamamatsu Canbera



Half plane - 24 sectors, 96 cylinders (36 silicon tiles, 2304 pads)



Laser alignment system





Wojciech Wierba et al., INP Cracow

Two laser beams (one perpendicular, second with 45° angle to the sensor plane) allows to measure XYZ translation in one sensor



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Results and Status



Camera has been moved in steps of 50 μ m. The distance have been measured with Renishaw RG-24 optical head with the resolution of ±0.1 μ m

It is necessary to stabilize the temperature of camera (stabilized chamber is under design)

Main effect is traced to the self heating of the camera.

Collimator and laser optics should be improved

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Plans and Summary

- Laboratory infrastructure is created/improved
 Testbench for FE ASICS prepared
- First design FE ASICS produced
- Testbeam equipment for rad. hard tests completed and used
- Laser positioning system studies are ongoing

Next steps:

- Test of prototype ASICS
- Submission of improved/refined versions beginning
 2008
- Analysis of testbeam data (rad. Hardness)
- Preparation of tests for Si sensors (LumiCal)