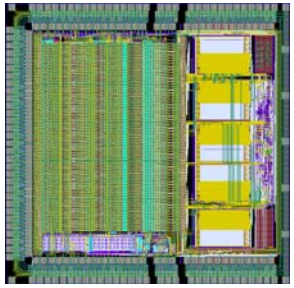
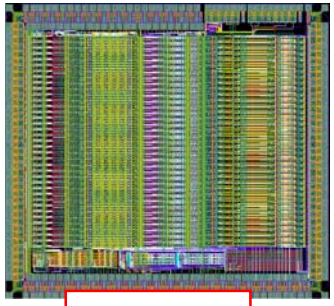
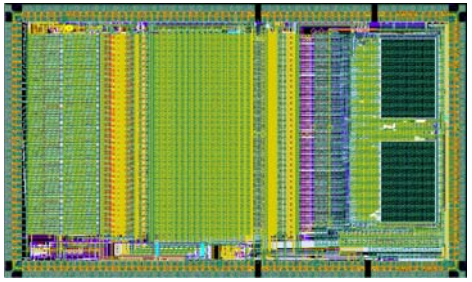


HaRDROC



SKIROC



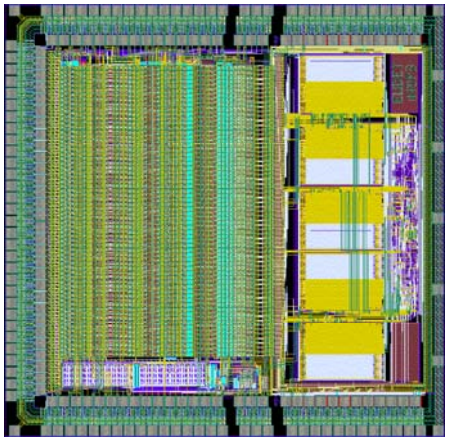
SPIROC

EUDET Front-End electronics in 2007

C. de La Taille
IN2P3/LAL Orsay

Tasks for CALICE/EUDET in 2007

- **Complete physics prototype**
  - Add and test DHCAL, complete physics program
  - Test effect of em shower on ASIC



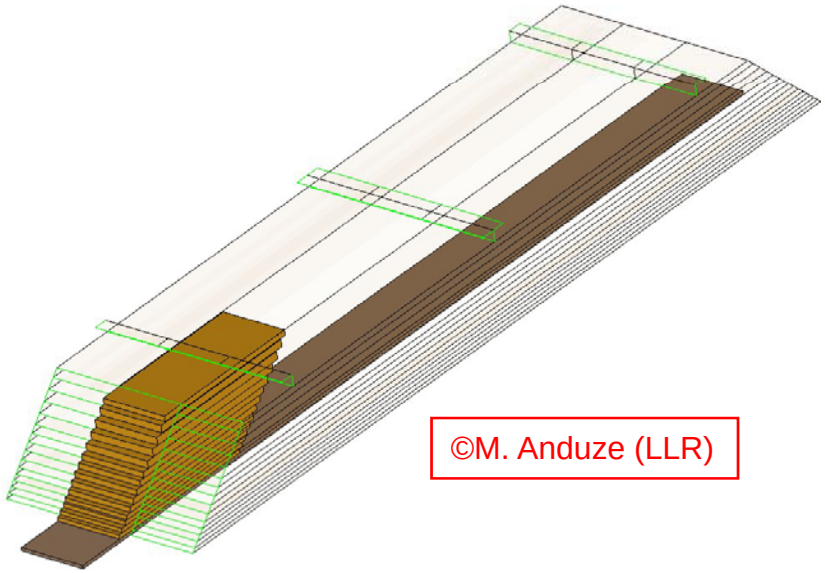
- **Measure performance of 2nd generation ASIC**
  - On testbench in different labs
  - DHCAL ECAL, AHCAL
  - Test 2nd generation DAQ (UK)

- **Design Very Front-End boards with integrated ASICs**
  - DHCAL board with HARDROC
  - AHCAL board with SPIROC
  - ECAL board with SKIROC (or SPIROC)

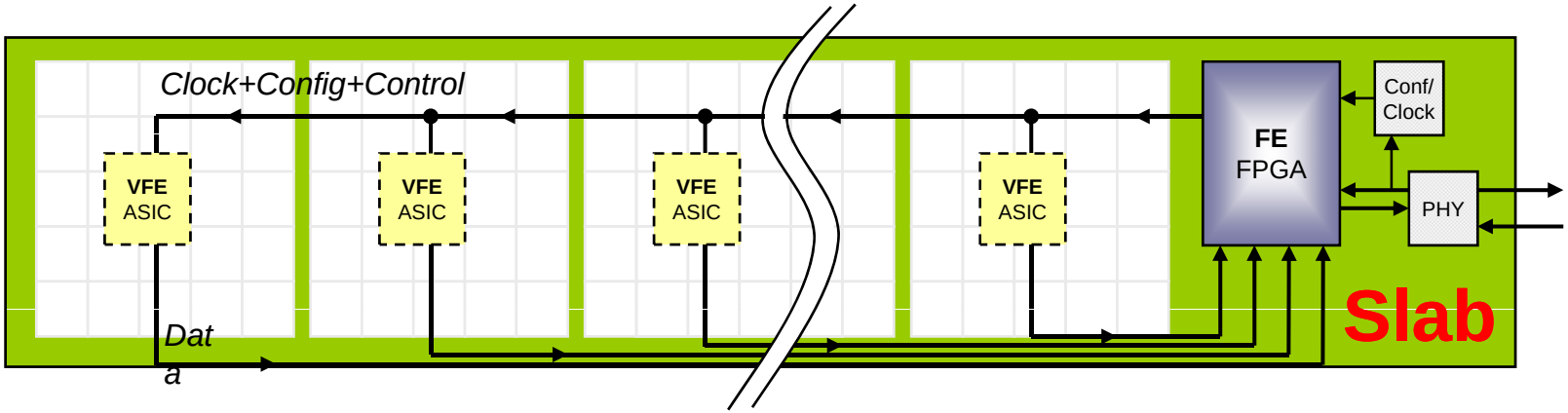
- **Design EUDET module(s) (demonstrator)**
  - Identify responsibilities and organize schedule
  - Moving to monthly meetings (in common with CALICE)
  - Aim at completing the design of EUDET modules beg 08

EUDET : ECAL module

- **Electromagnetic calorimeter**
  - Prototype of a (~ 1/6) module 0 : **one line & one column**
  - 150 cm long, 12 cm wide 30 layers
  - 1800 + 10800 channels
  - Test full scale mechanics + PCB
  - Can go in test beam
  - Test full integration + edge communications
- **To be delivered in 2009**

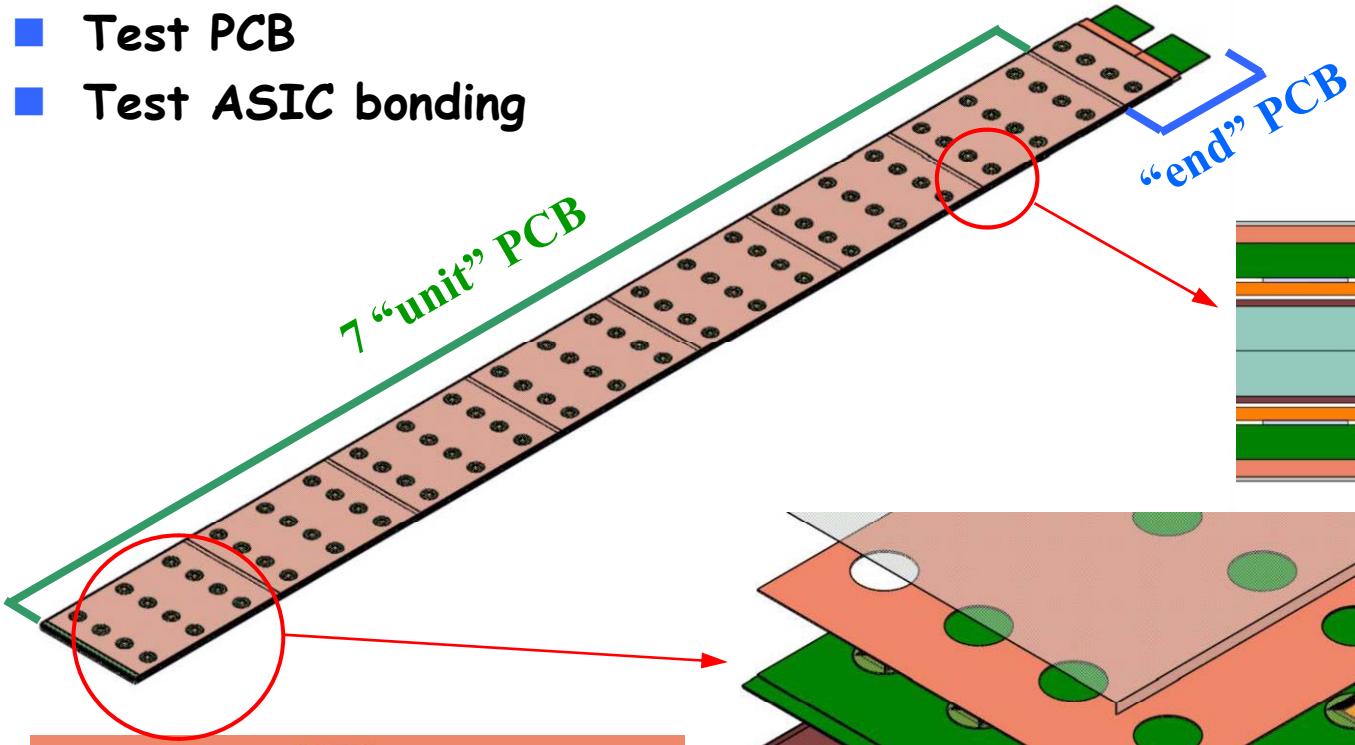


©M. Anduze (LLR)

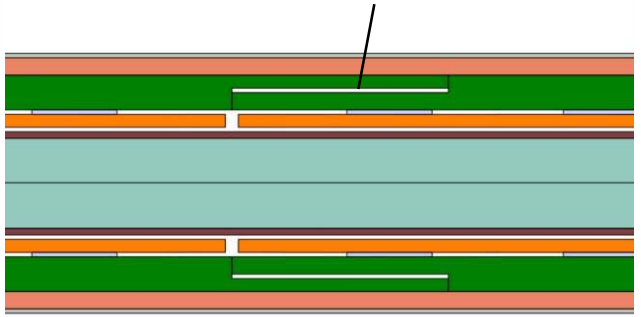


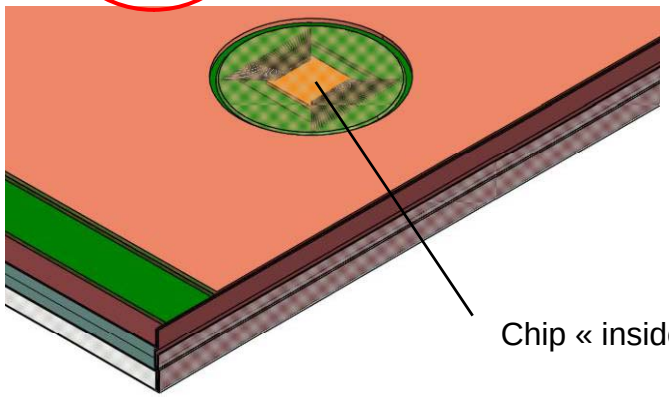
EUDET - Detector slab (2)

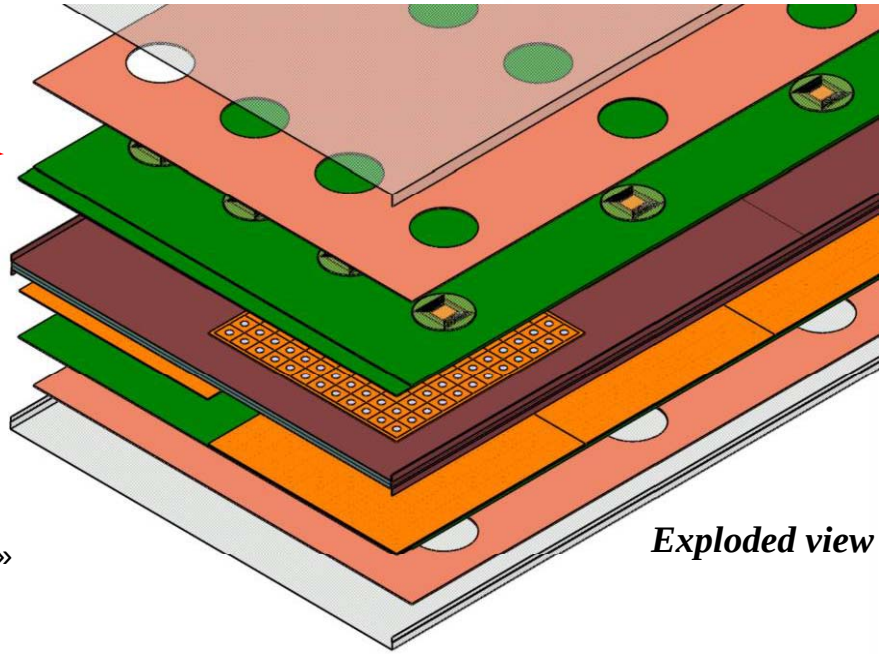
- Test PCB
- Test ASIC bonding



Connection between 2 PCB

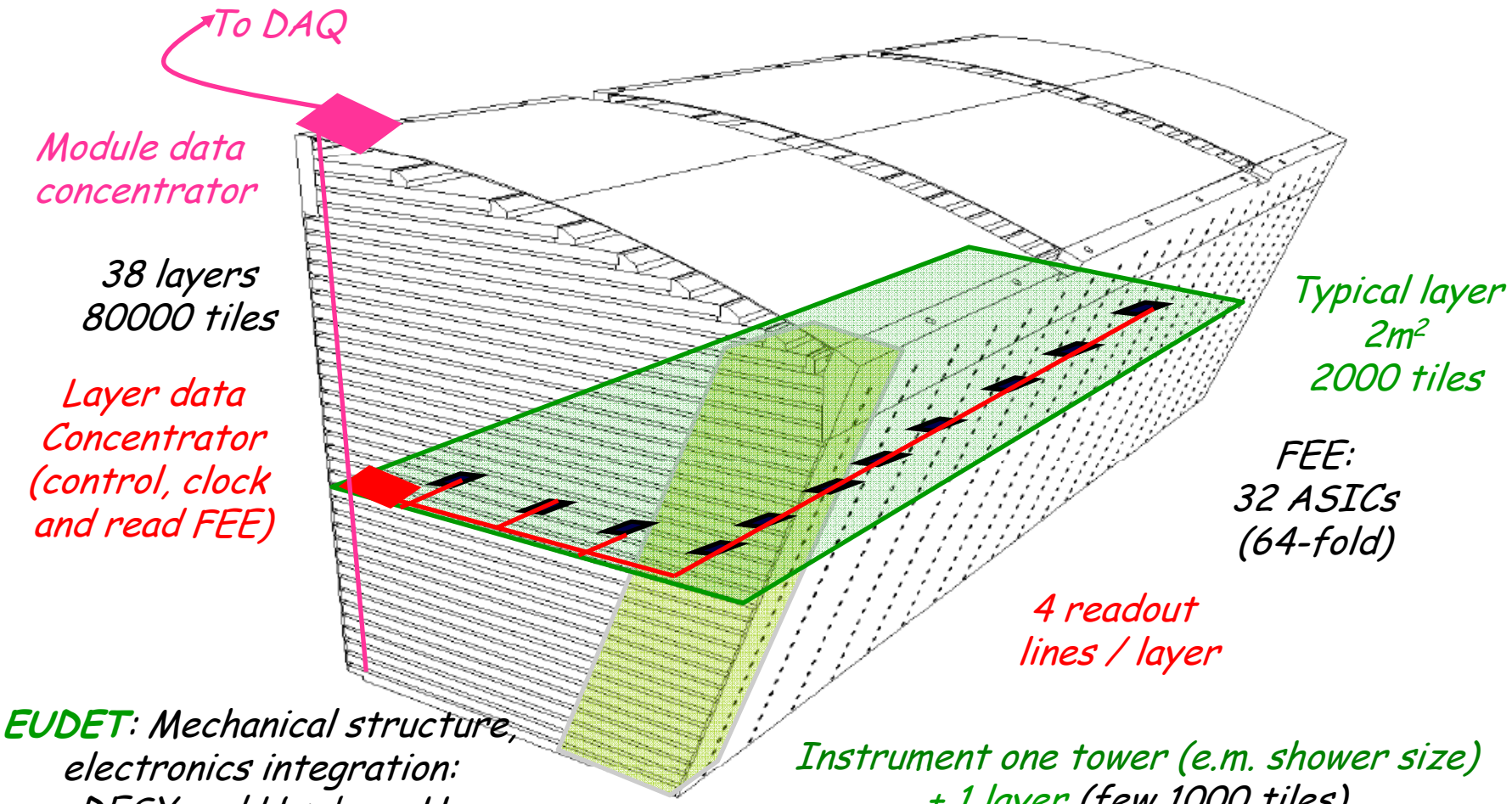






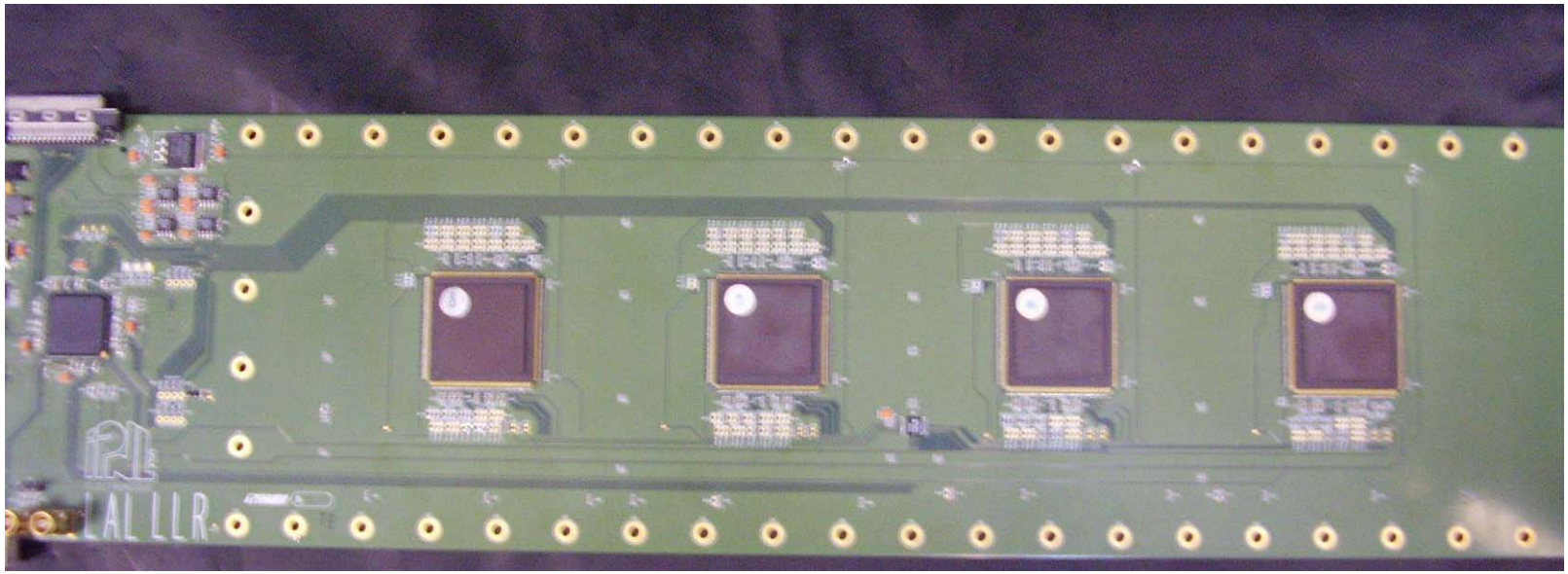
Exploded view

AHCAL architecture



DHCAL architecture

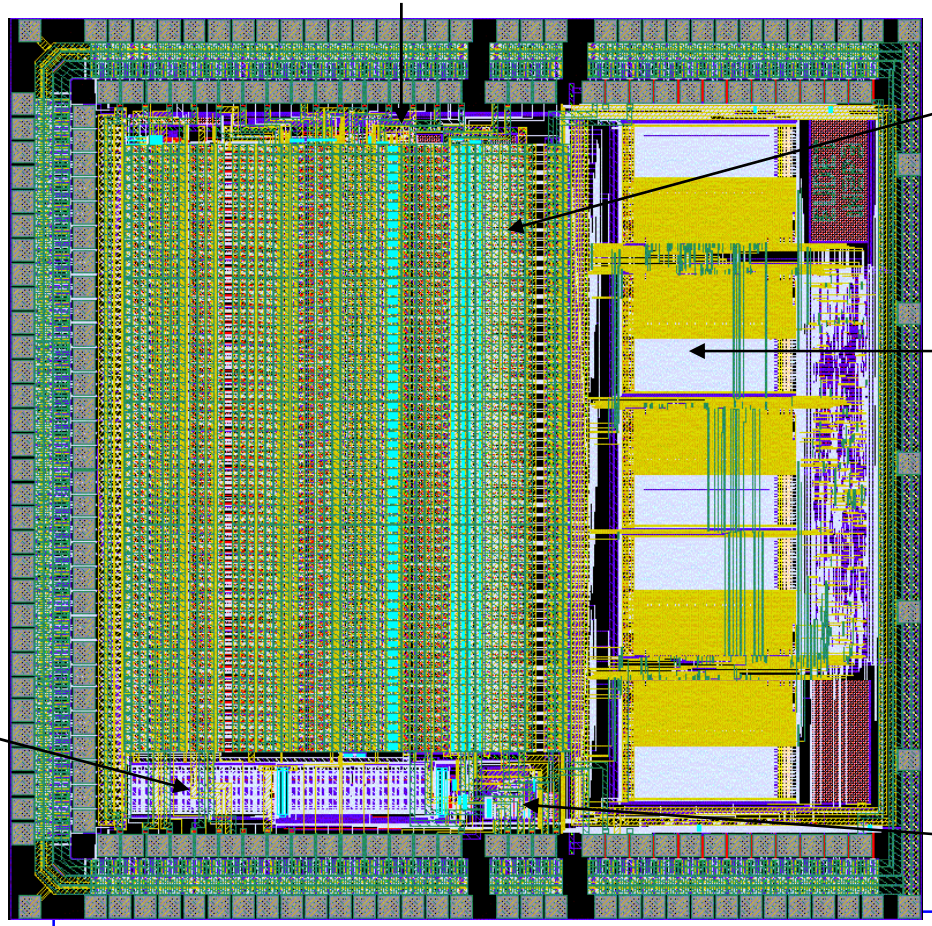
- First detector with 2nd generation ASCIs and 2nd generation DAQ
- Board received in june 07, tests starting



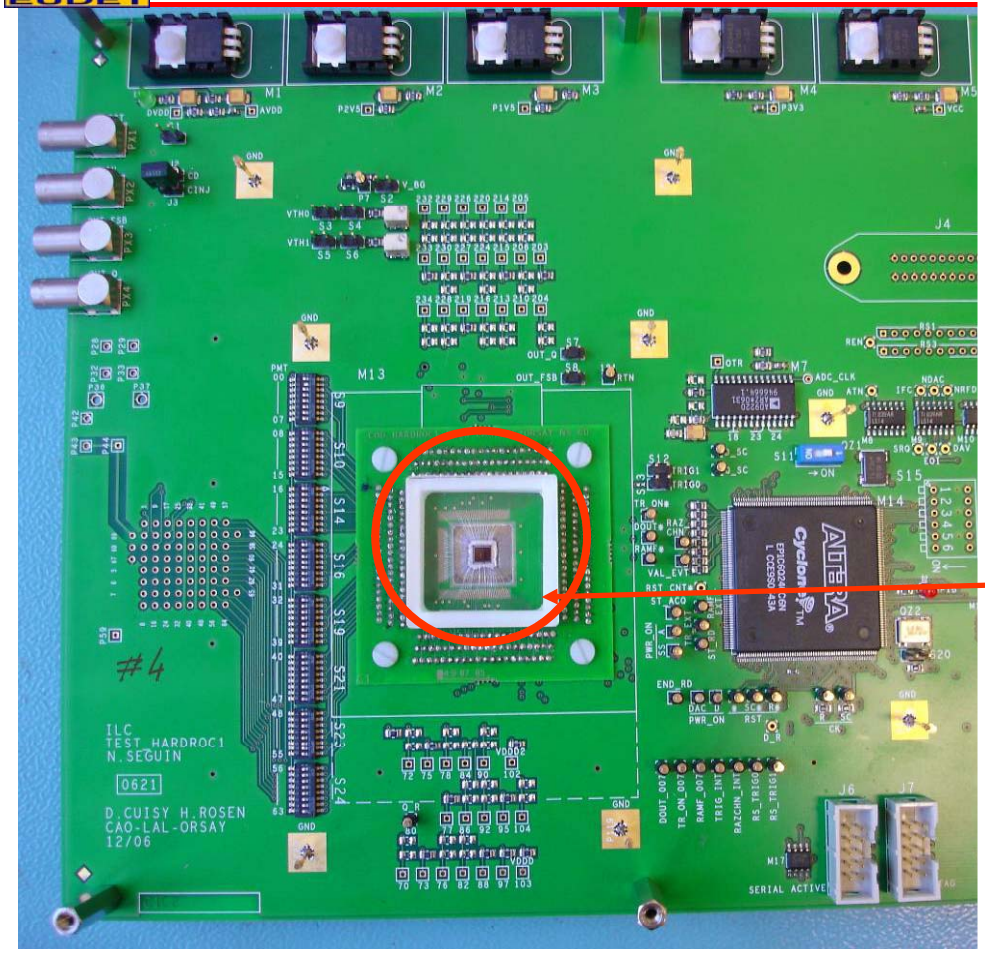
HaRDROC chip for DHCAL [LAL,IPNL]

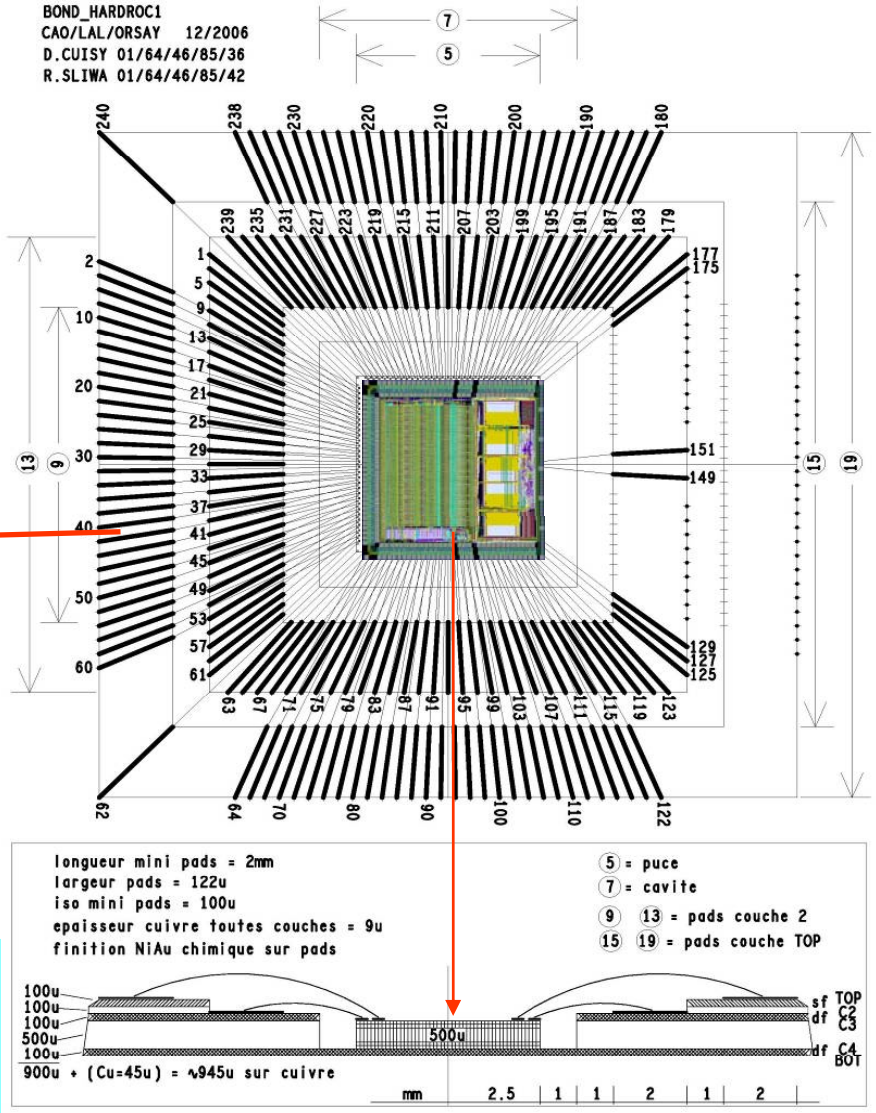
JRA3 Milestone

- **Hadronic Rpc Detector Read Out Chip (Sept 06)**
  - 64 inputs, preamp + shaper+ 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ : only 1 digital data output



HARDROC1: TESTBOARD with Chip On Board





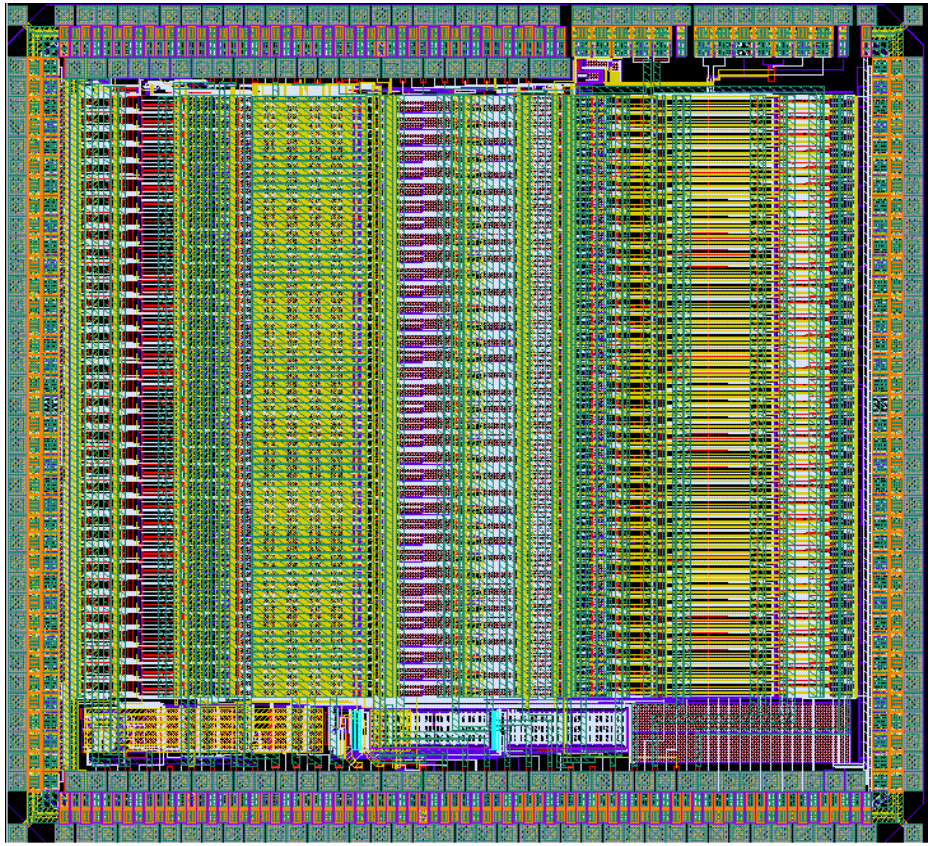
PCB for COB: to estimate feasability (ECAL)
6 layers, COB on Layer 5
2 steps to facilitate the bonding

HARDROC1 PERFORMANCE SUMMARY

Number of inputs/outputs	64 inputs, 1 serial output
Input Impedance	50-70Ω
Gain Adjustment	0 to 4, 6bits, accuracy 6%
Bipolar Fast Shaper	≈3.5 mV/fC tp=15ns
10 bit-DAC	2.5 mV/fC, INL=0.2%
Trigger sensitivity	Down to 10fC
Slow Shaper (analog readout)	≈50 mV/pC, 5fC to 15pC , tp= 50ns to 150ns
Analog Xtk	2%
Analog Readout speed	5 MHz
Memory depth	128 (20kbits)
Digital readout speed	5MHz or more
Power dissipation (not pulsed)	100 mW (64 channels)

SKIROC for W-Si ECAL

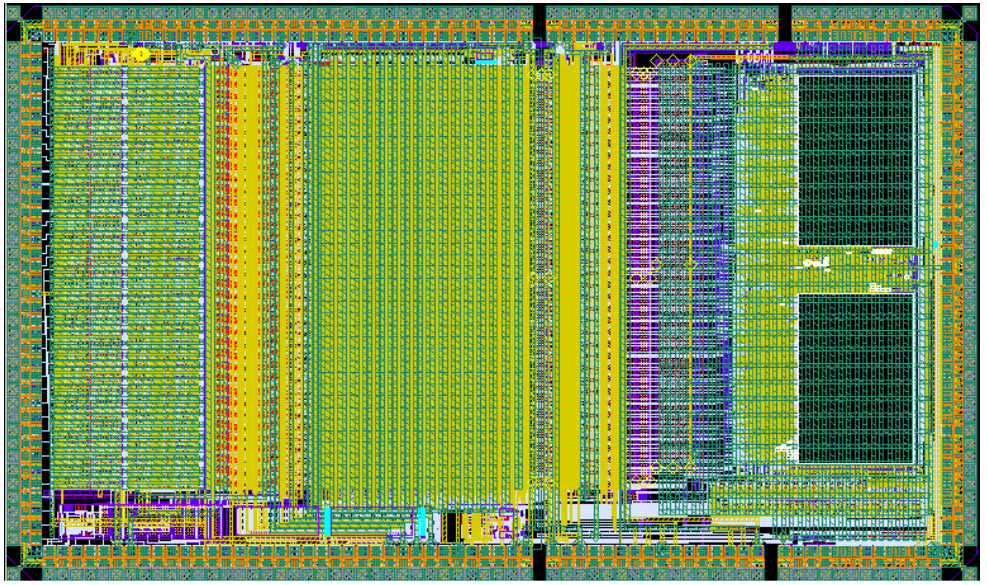
- **Silicon Kalorimeter Integrated Read Out Chip (Nov 06)**
  - 36 channels with 16 bits Preamp + bi-gain shaper + autotrigger + analog memory + Wilkinson ADC
  - Digital part outside in a FPGA for lack of time and increased flexibility
  - Technology SiGe 0.35µm AMS. Chip received may 07, tests starting

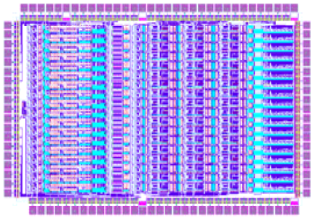


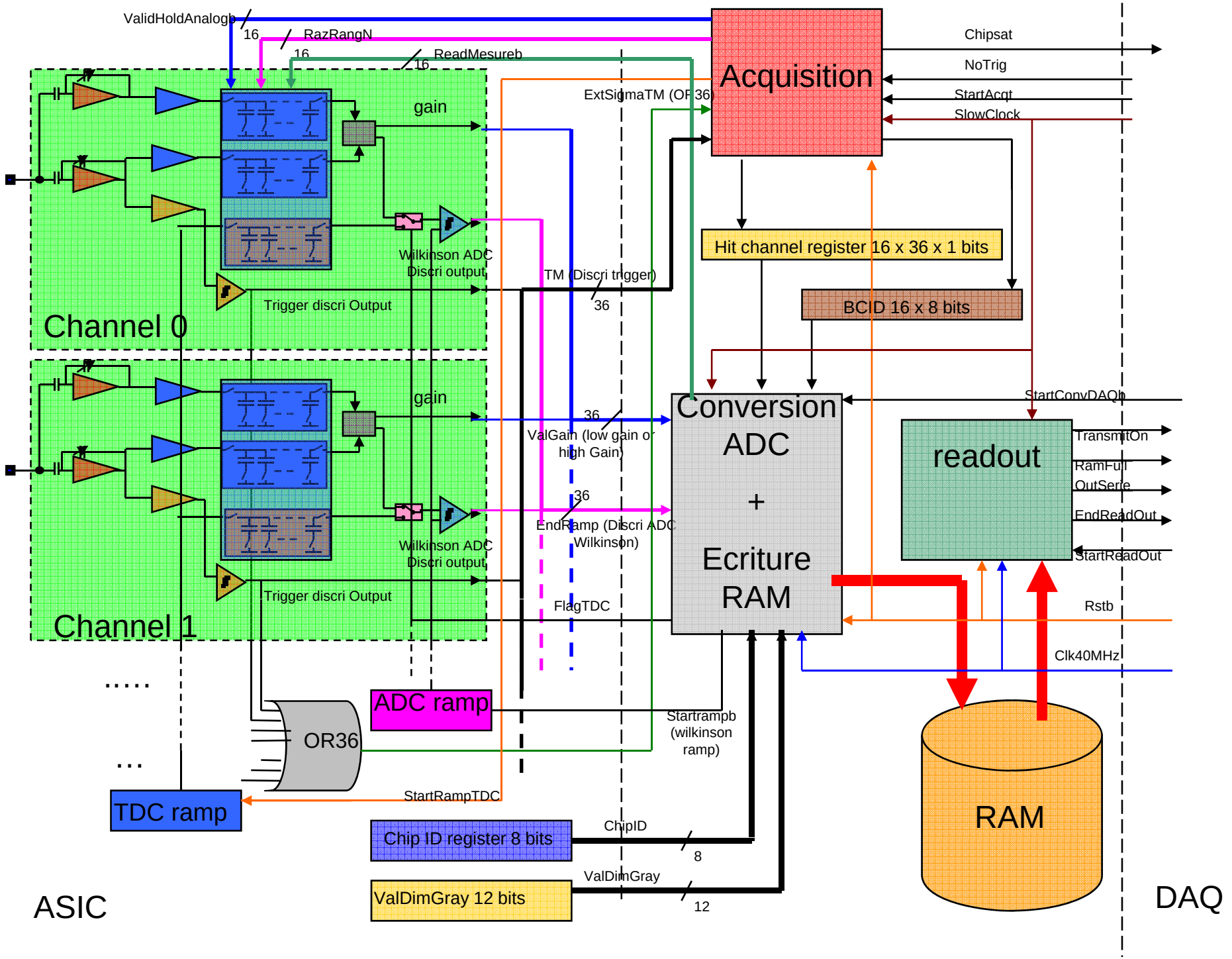
SPIROC overview

JRA3 Milestone

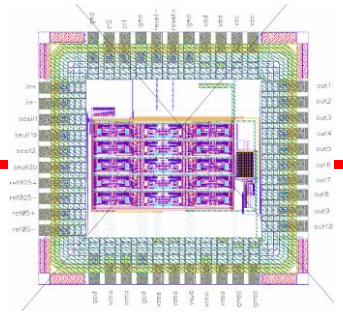
- Silicon Photomultiplier Integrated Read Out Chip
  - A-HCAL read out
- Silicon PM detector
  - G = 3 E5 to 1 E6
  - Same biasing scheme as TB
- 36 channels
  - Charge measurement (15bits)
  - Time measurement (< 1ns)
- Compatible with old & new DAQ
- Complex chip,, but many SKIROC, HARDROC, and MAROC features re-used
- Submitted june 11th
  - Expected september






ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR 36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
Conversion ADC + Ecriture RAM
StartConvDAQb
readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
ADC ramp
OR36
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
ASIC
DAQ

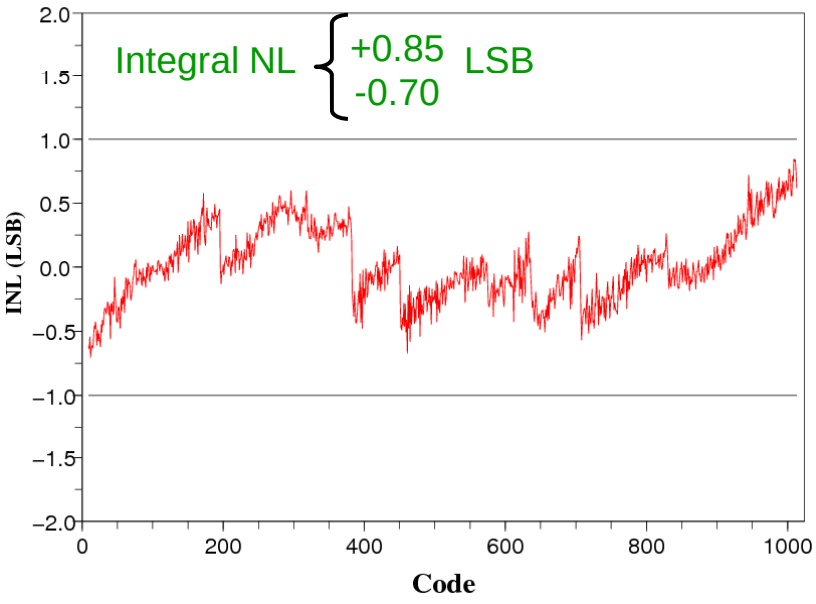
On-going R&D : ADCs

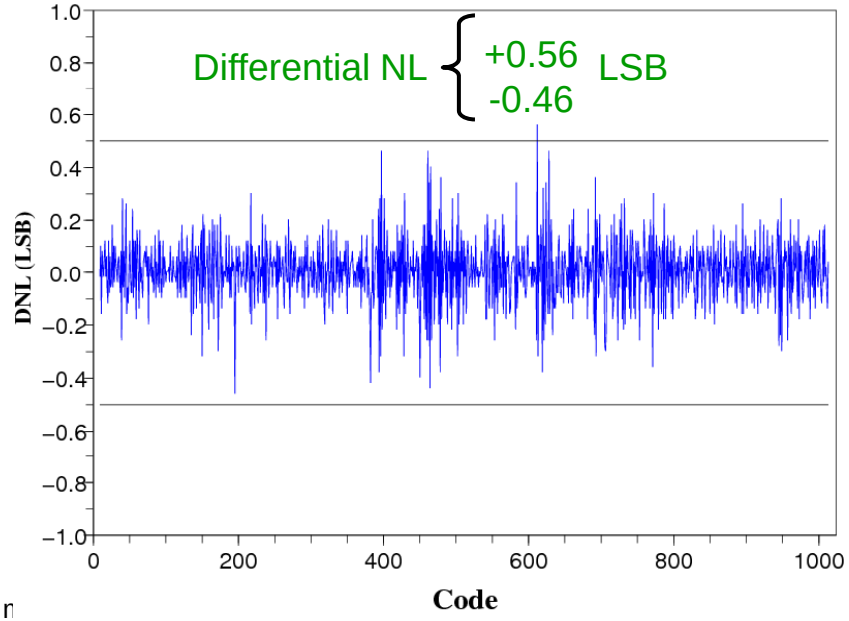


- **Characteristics:**
  - Technology: CMOS SiGe 0.35µm
  - Power supply: 5V (digital: 2.5V)
  - Clock frequency: 40 MHz
  - Differential architecture
  - 10 stages - 1.5 bit/stage
  - Die area: 1.2 mm²

- **Performance (measured):**
  - Resolution: 10 bits
  - Consumption: 35 mW
  - Conversion time: 0.25 µs (@ 40MHz)
  - Integrated cons.: (35mW * 0.25µs)/200ms= .044µW

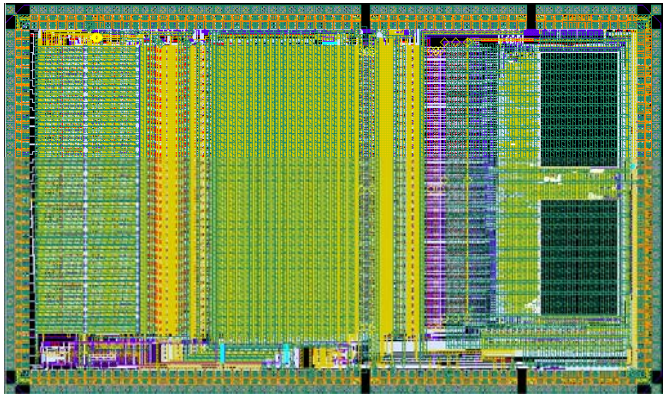
Noise (measured):
< 0.47 LSB @ 68% C.L.





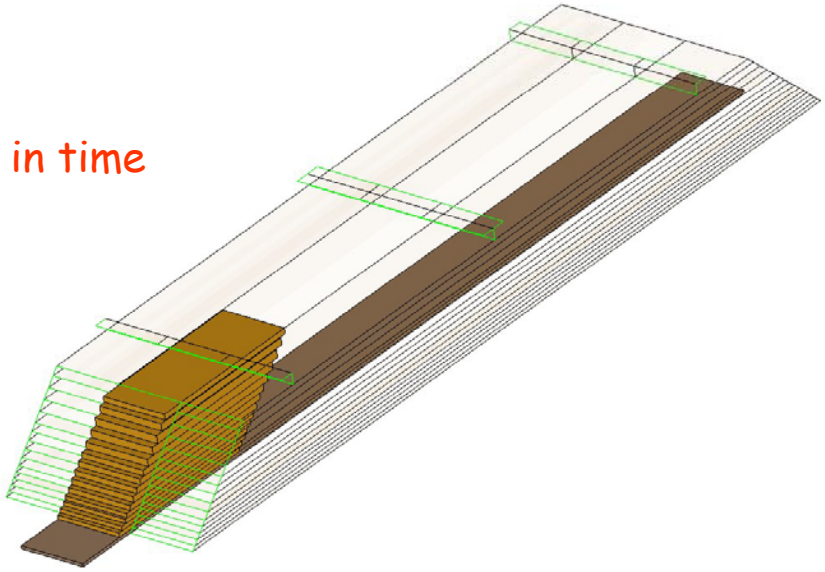
Conclusion

- **3 major second generation ASICs for technological prototypes submitted**
  - HARdROC submitted for DHCAL RPCs
  - SKIROC submitted for ECAL Si-W
  - SPIROC for AHCAL SiPM



- **System aspects now proceeding**
  - Power pulsing, Zero-suppress, Auto-trigger, 2nd generation DAQ…
  - On detector boards
  - Connection to DAQ : task force
  - EUDET repository for shared VHDL code
  - Worry of having ECAL Si wafer prototypes in time

- **EUDET modules in 2009 is challenging !**
  - Production of all ASICs mid 2008 !
  - Organization coming in place



JRA3 milestones

Milestone	date	Task	Mm/Yy
Mechanical concept available	12	A	Dec-06
Tech1 prototype available (skyrock)	12	E	Dec-06
DHcal ASIC prototype DHCAL1 available (Hardrock)	12	E	Dec-06
DAQ system prototype available	18	D	Jun-07
Design review	22	A,B,C,D,E	Oct-07
Ecal ASIC prototype TECH2 available	24	E	Dec-07
Ecal design and mould available	30	A	Jun-08
DAQ system prototype available	33	D	Sep-08
Production readiness review	34	A,B,C,D,E	Oct-08
Ecal ASIC production TECH3 finalised	36	E	Dec-08
ECAL PCB available	36	E	Dec-08
Silicon sensors available	42	A	Jun-09
DAQ system available	42	D	Jun-09
Ecal prototype available	42	A	Jun-09