Status Report on ADC developments @ LPC

ILC Group

IN2P3
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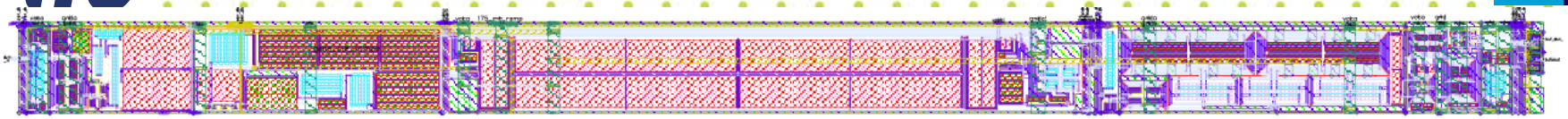
Ecal VFE ADC : requirements

- **Requirements for ADC**
  - Precision 10 – 12 bits
  - Ultra low power, 25µW per channel
  - Compactness, electronics embedded in detector

Ultra-low POWER is the KEY issue (C. de la Taille)

- **Three main developments @ LPC**
  - Wilkinson ADC 12 bits easy to implement in SKIROC but too slow for ILC
  - Pipeline ADC 10 bits tested and measured
  - New design : cyclic and pipelined ADC 12 bits
    - **Building blocks for 3V power supply**

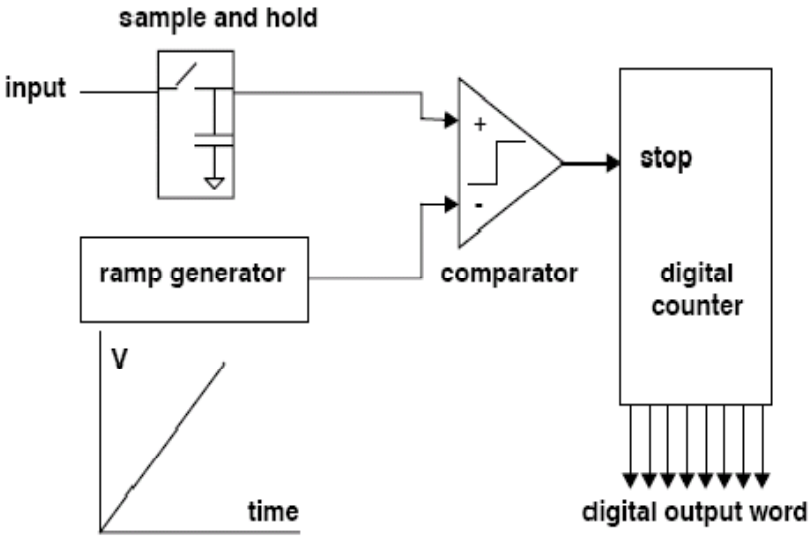
12 bits Wilkinson 3.5V ADC in SKIROC



- Characteristics:
  - Techno: **BiCMOS SiGe 0.35µm**
  - Power supply: **3.5V**
  - Conversion time : **80µs @50MHz**
  - Differential architecture
  - Open loop ramp generator
  - Gray counter
  - Die area: **0.12 mm²**

Designed by Gérard Bohner

Wilkinson ADC architecture



Consumption for 12 bits Wilkinson ADC

- **Dynamic consumption : 3 mW**
- **Conversion time: 80 us @ 50MHz**
- **Assuming:**
  - 128 channels per VFE chip
  - 1 ADC per channel so 128 ADC per chip
  - 5 events max per channel (memory depth)

➧ With power cycling, the integrated consumption per channel of the A/D conversion can be estimated by:

$$\frac{Pw \times Tconv \times Mem.}{Time\_cycle} = \frac{3mW \times 80\mu s \times 5}{200ms}$$ **= 6.2 µW/ch**

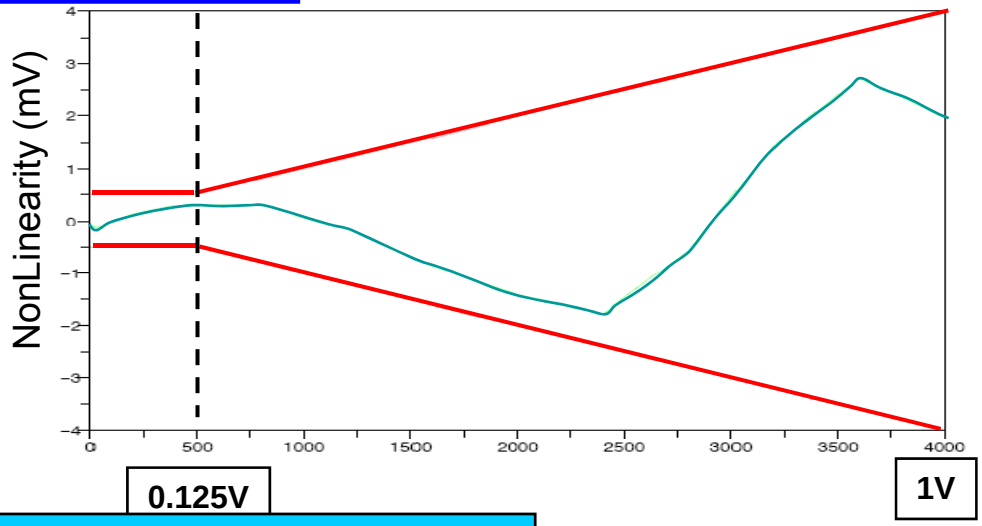
with *Pw*: power cons. of one channel
Tconv: time for one conversion
Mem: memory depth of one channel
Time_cycle: time between two trains

The ON-setting time effects can be neglected.

Performance from simulation of 12 bits Wilkinson ADC

- Resolution: 12 bits
- Consumption: 3 mW
- Conversion time: 80 µs (@ 50MHz)
- Current source (ramp generator):
  - **Input dynamic signal: 1V Common Mode**
  - **2V differential ramp generator**
  - **T° sensitivity : 40 ppm/°C max (20 to 50°C)**
  - **Power supply sensitivity: 5 ppm/V (±50 mV)**

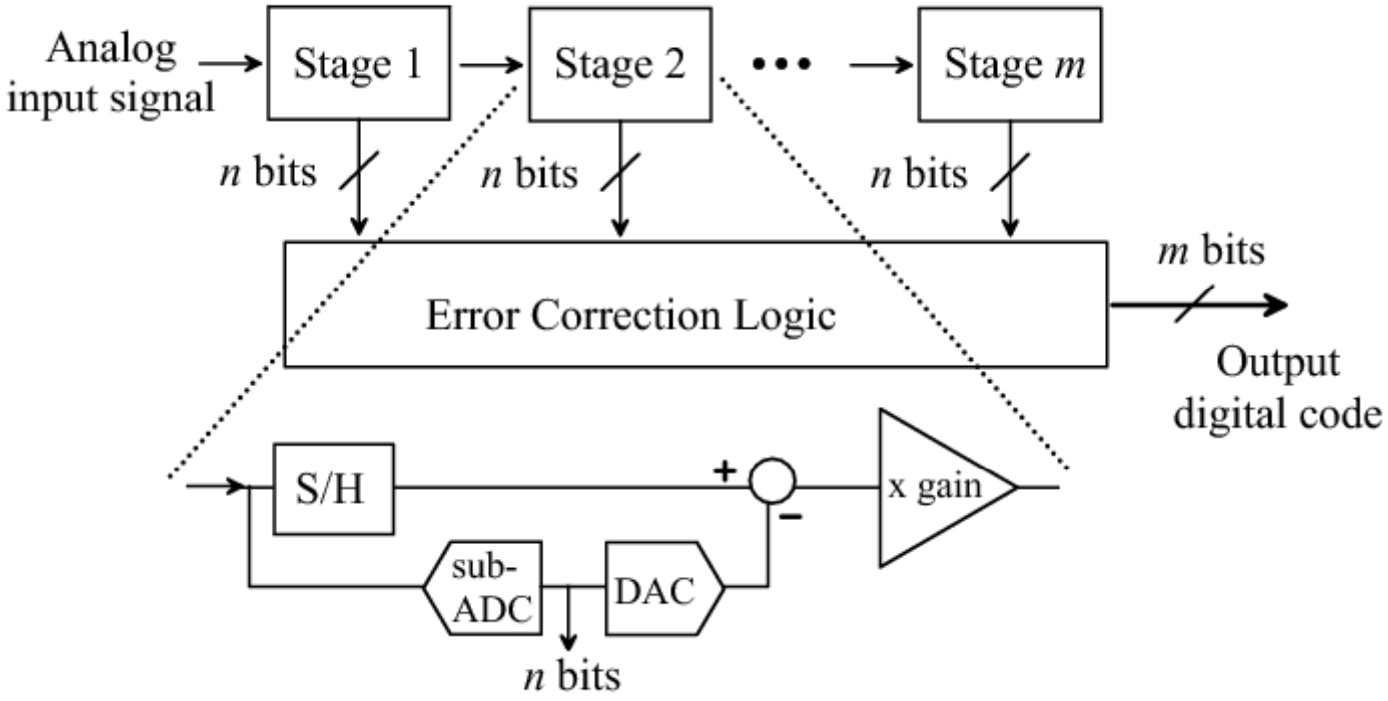
NonLinearity from simulation:
- < ± 500 µV up to 125mV
- < 0.1% from 125mV to 1V



Test in progress thank to the testbench designed by LAL

Pipeline ADC architecture

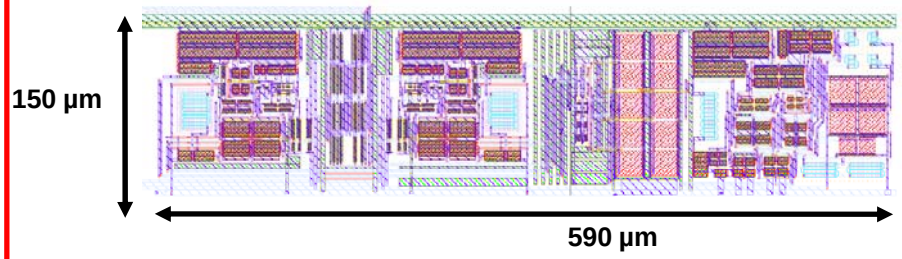
- Linearity mainly affected by the precision of the amplifier gain
- 1.5 bit per stage architecture
- Comparator offset tolerated ± 250mV for 2V range

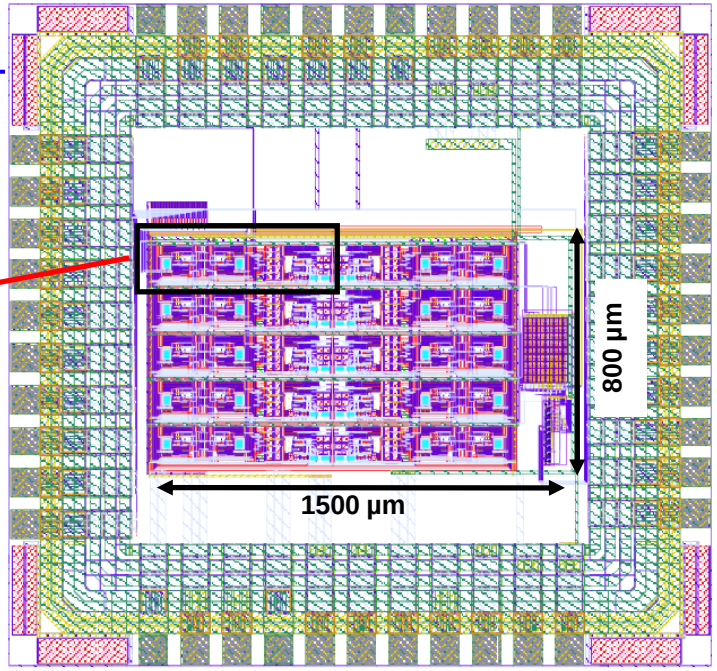


10-bits Pipeline 5V ADC

- **Characteristics:**
  - Technology: Austriamicrosystems CMOS 0.35µm
  - Power supply: 5V (digital: 2.5V)
  - Clock (sampling) frequency: 4 MHz (MS/s)
  - 10 bits ➔ 10 stages
  - 1.5bit/stage and differential architecture
  - Die area: 1.2 mm^2

Layout of 1 stage





Consumption for 10 bits pipeline ADC

- **Dynamic consumption : 35 mW**
- **Conversion time: 250ns @ 4MHz**
- **Assuming:**
  - 128 channels per VFE chip
  - 1 ADC per chip
  - 5 events max per channel (memory depth)

➡ With power cycling, the integrated consumption per channel of the A/D conversion can be estimated by:

$$\frac{Pw \times Tconv \times Mem.}{Time\_cycle} = \frac{35mW \times 250ns \times 5}{200ms}$$ **= 0.22 µW/ch**

with *Pw*: power cons. of one channel
Tconv: time for one conversion
Mem: memory depth of one channel
Time_cycle: time between two trains

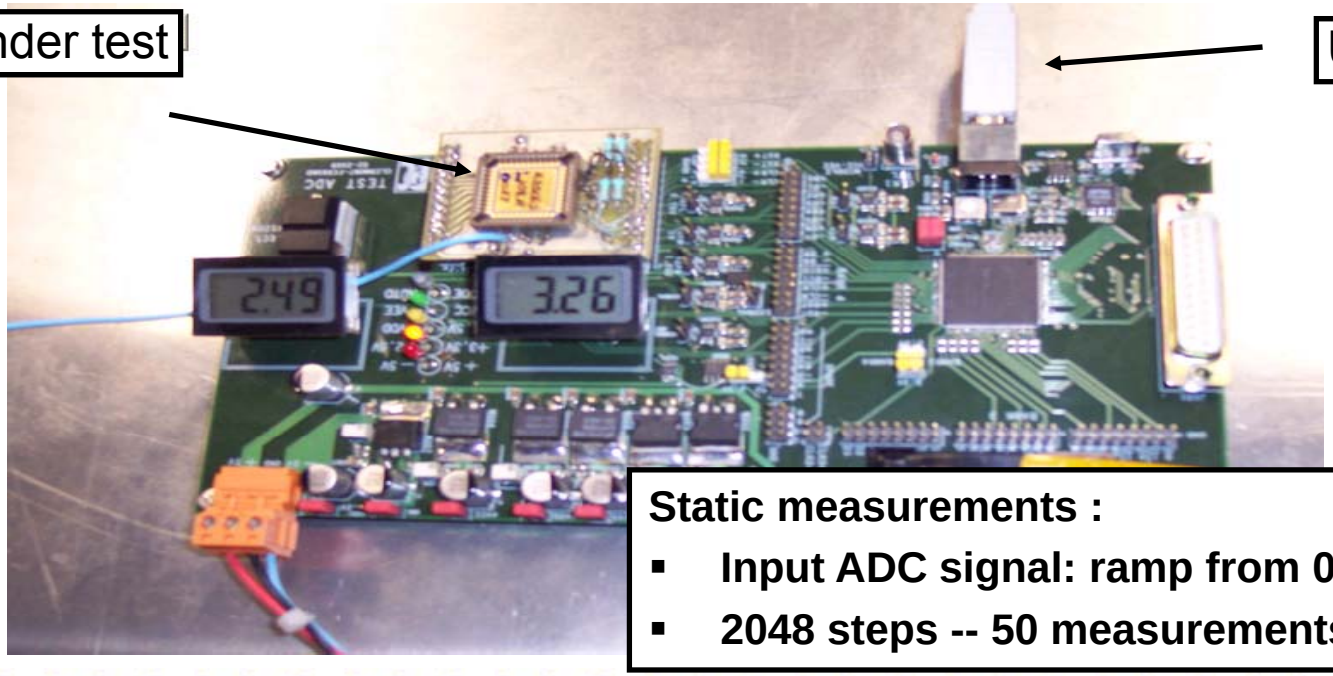
The ON-setting time and pipeline latency effects can be neglected.

Measurement setup for ADC

Test Bench:

Designed by Roméo Bonnefoy

- Generic board for ADC tests
- Analogue signal generator: DAC 16 bits (DAC8830)
- PC/LabView Slow Control through USB interface
- Data processing with Scilab package



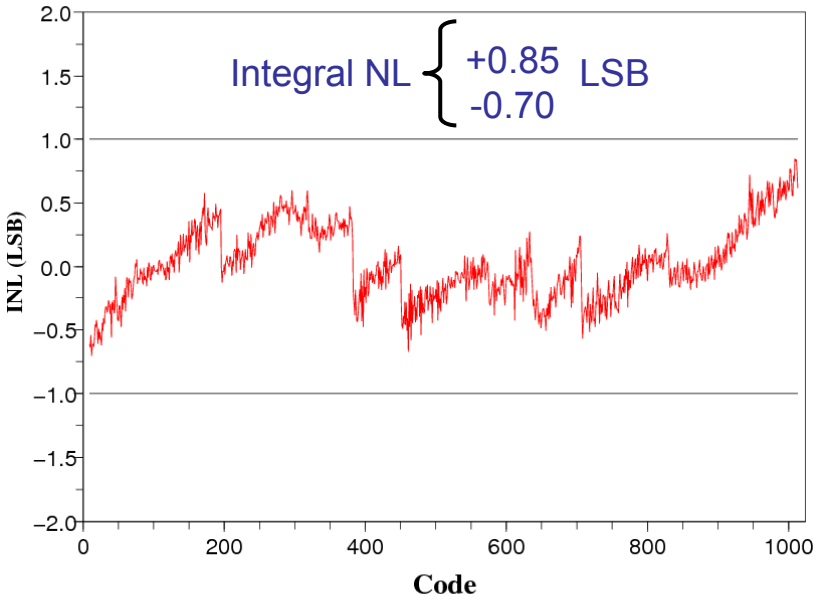
Static measurements :

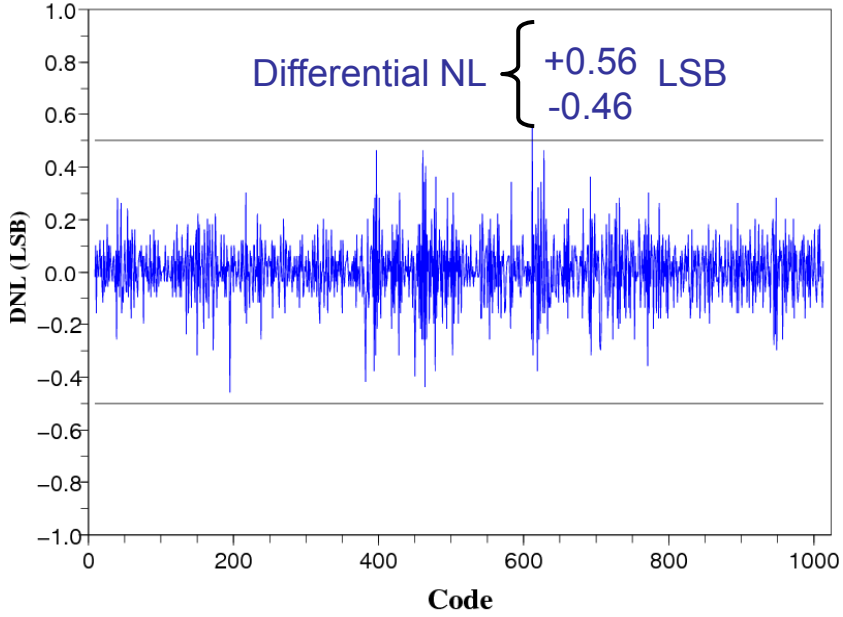
- **Input ADC signal: ramp from 0 to 2V**
- **2048 steps -- 50 measurements / step**

Performance measured for Pipeline ADC

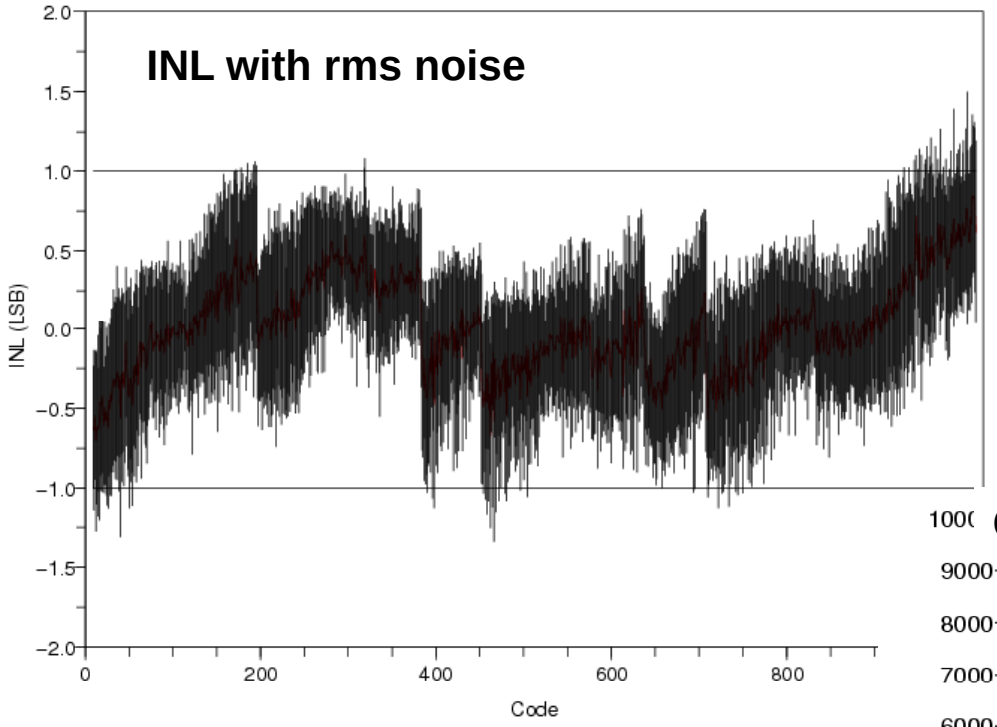
- Performance measured:
  - **Resolution: 10 bits**
  - **Consumption: 35 mW**
  - **Conversion time: 0.25 µs (@ 4MHz)**

NonLinearity (measured):

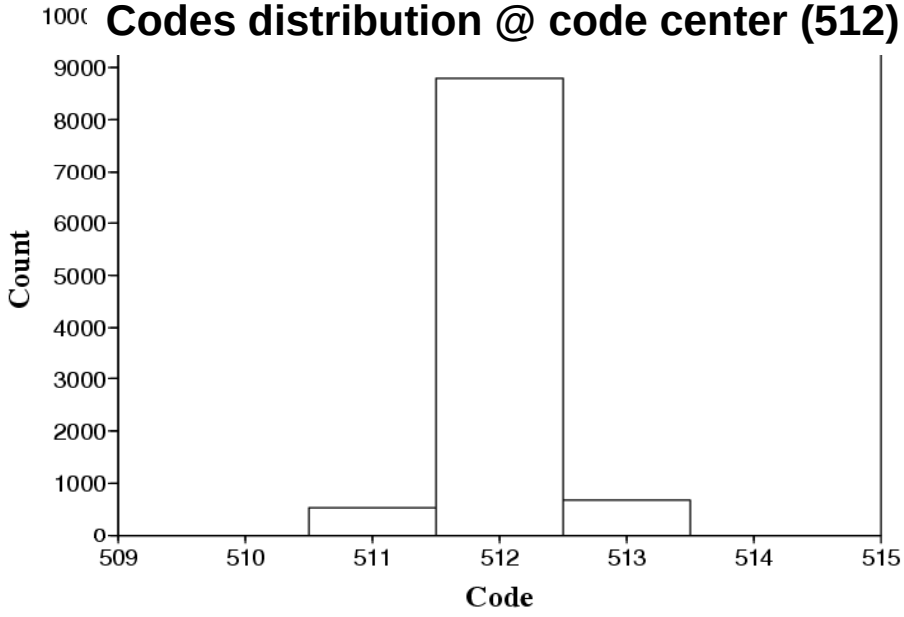




Noise performance for Pipeline ADC



Measured noise
(including the setup noise):
$\sigma < 0.5$ LSB



12 bits – 3V buildings blocks developments

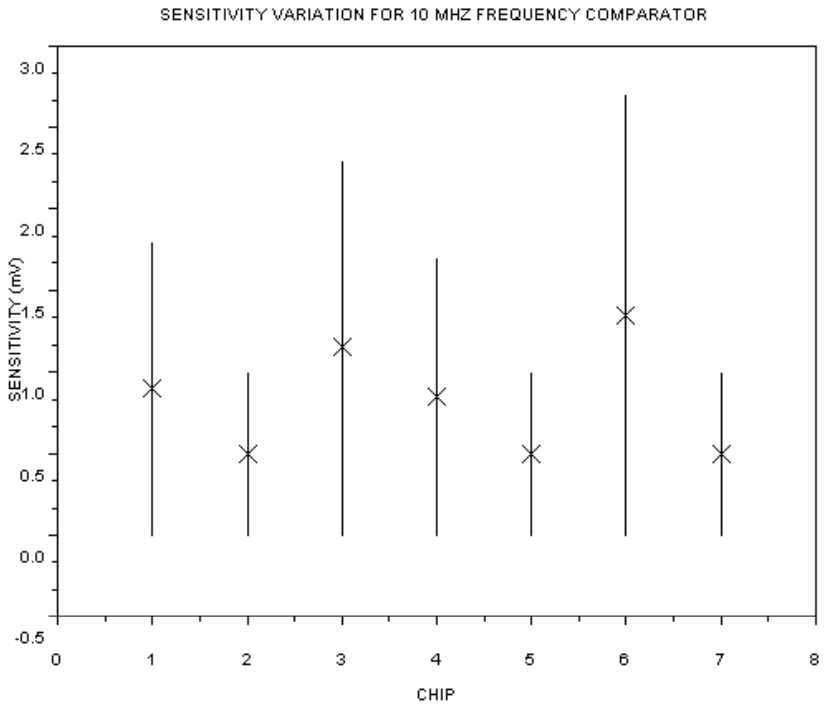
- **Objectives :**
  - Design a 12 bits pipeline or cyclic ADC
  - Gain 2 accuracy multiply by 4
    - 10 bits ADC accuracy is 1/1000
    - 12 bits ADC accuracy is 1/4000

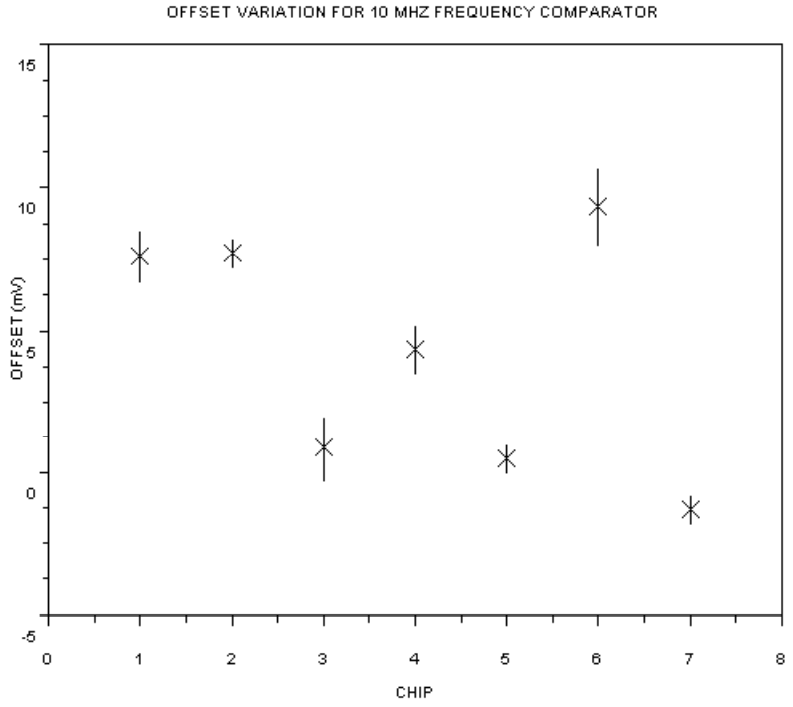
- **Two chips designed to characterize two main elements**
  - Comparator
  - Gain 2 amplifier

Comparator test results for 12 bits ADC

- **Characteristics:**
  - **Technology: CMOS 0.35µm**
  - **Power supply: 3V**
  - **Clock frequency: 10 MHz**
  - **Differential architecture**
  - **Consumption 68uA**
  - **7 chips tested**

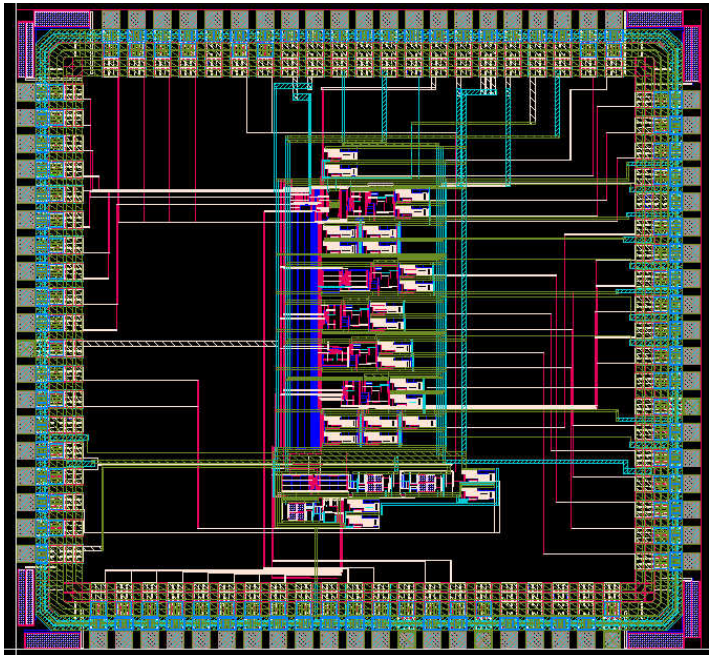
Average Sensitivity: 1.6 mV
Average Offset : 4.2 mV
Fullfit 12 bits precision requirements





Gain 2 amplifier for 12 bits ADC

- Characteristics:
  - **Technology: CMOS 0.35µm AMS**
  - **Power supply: 3V**
  - **Differential architecture**
  - **Die area 11mm2**
  - **84 pins**



- **Calice_07_07 in july 2007 july 2007**
  - **3V Gain 2 amplifiers with different layout structures capable to reach 12 bits**
  - **One ADC stage 12 bits 3V**
  - **Integrated shaper with analog memory**

Summary

- **12 bits Wilkinson ADC**
  - **Under test**
  - **Compactness, 128 wilkinson ADC per chip, die area of (128*0.12)mm2 for 128 ch.**
  - **Consumption, 6.2µW/ch , ≈ 30% total power of one channel**
- **10 bits pipeline ADC**
  - **Precision, INL: -0.70/+0.85 LSB , DNL: -0.46/+0.56 LSB, Noise: <0.5 LSB**
  - **Compactness, one pipeline ADC per chip, die area of 1.2mm^2 for 128 ch.**
  - **Consumption, 0.22µW/ch , ≈ 1% total power of one channel**
- **Under study (the best candidate): 12 bits cyclic ADC**
  - **Compactness, one ADC per chip around 0.2mm^2 for 128ch**
  - **Consumption, 0.22µW/ch , ≈ 1% total power of one channel**
  - **Possibility to have 1 ADC per channel**