

# Performance of the SiW ECAL prototype in the 2007 TB

Marcel Reinhard  
LLR – Ecole Polytechnique



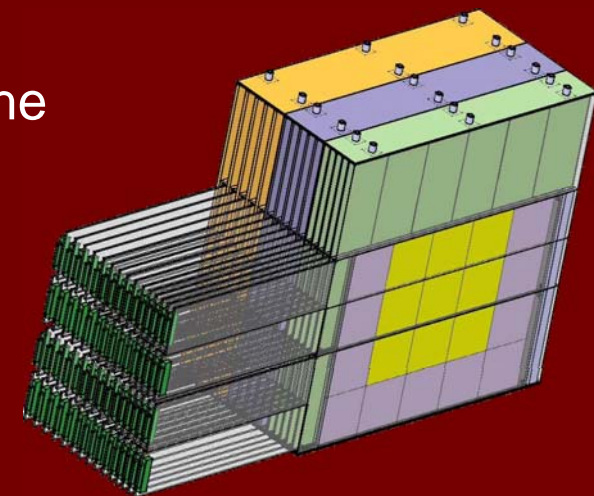
CALICE days 11-13/09/07, Prague

# Outline

- ECAL configuration & data taken
- ECAL response & stability
- Performance of new slabs
- Some problems
- Wishlist

# ECAL configuration in 2007 TB

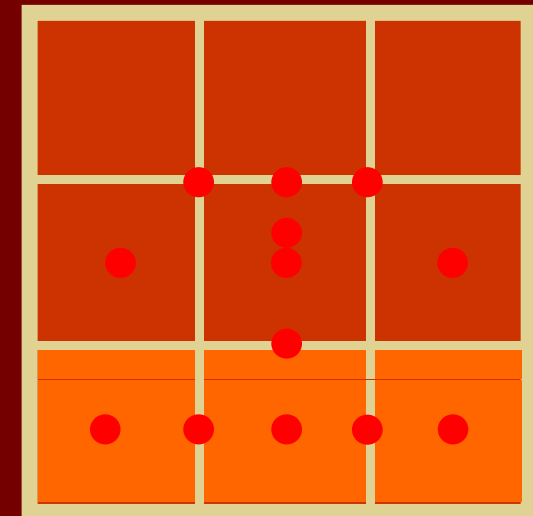
- Center part fully equipped (30 layers, 6480 channels)
- Bottom part (equipped subsequently from back to front):
  - June 23<sup>rd</sup>: 12 layers
  - July 4<sup>th</sup>: 6 more layers added
  - July 26<sup>th</sup>: 6 more layers added, tungsten dummies in empty slots-> 24 layers, 2592 channels
- 9072 channels in total
- 6 missing bottom PCBs already equipped with wafers, currently being tested
- ECAL will be fully equipped (9720 channels) by the end of this month !!!



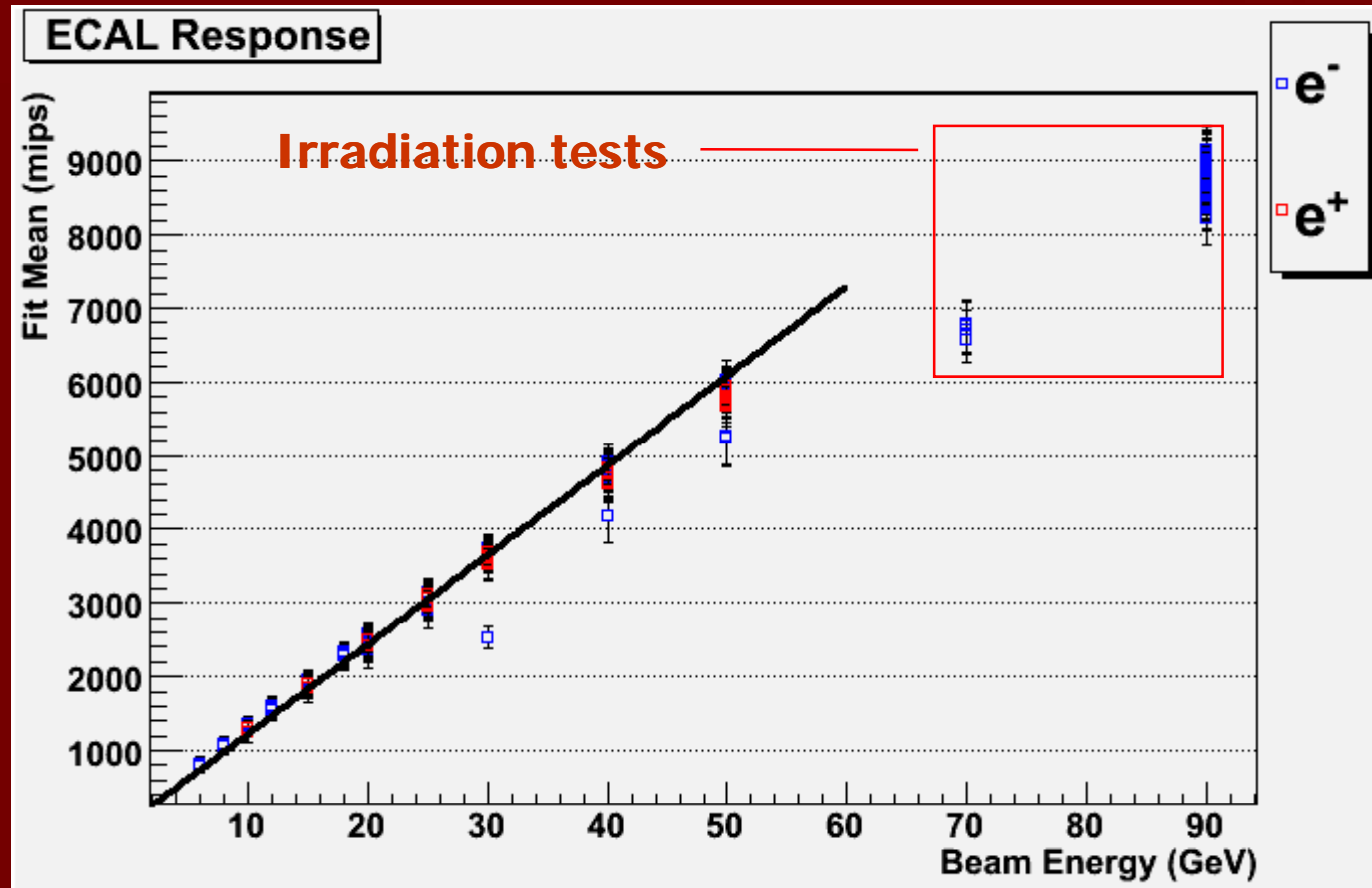
LLR

# Overview of data taken

- 1693 runs
- Many different impact points at various energies: >170 different combinations with 250k Events at least
- 4 different angles (0, 10, 20, 30 deg)
- Irradiation test (see Roman's talk)
- Everything worked very well over the whole TB period (no downtime due to detector malfunction !!!)



# ECAL response

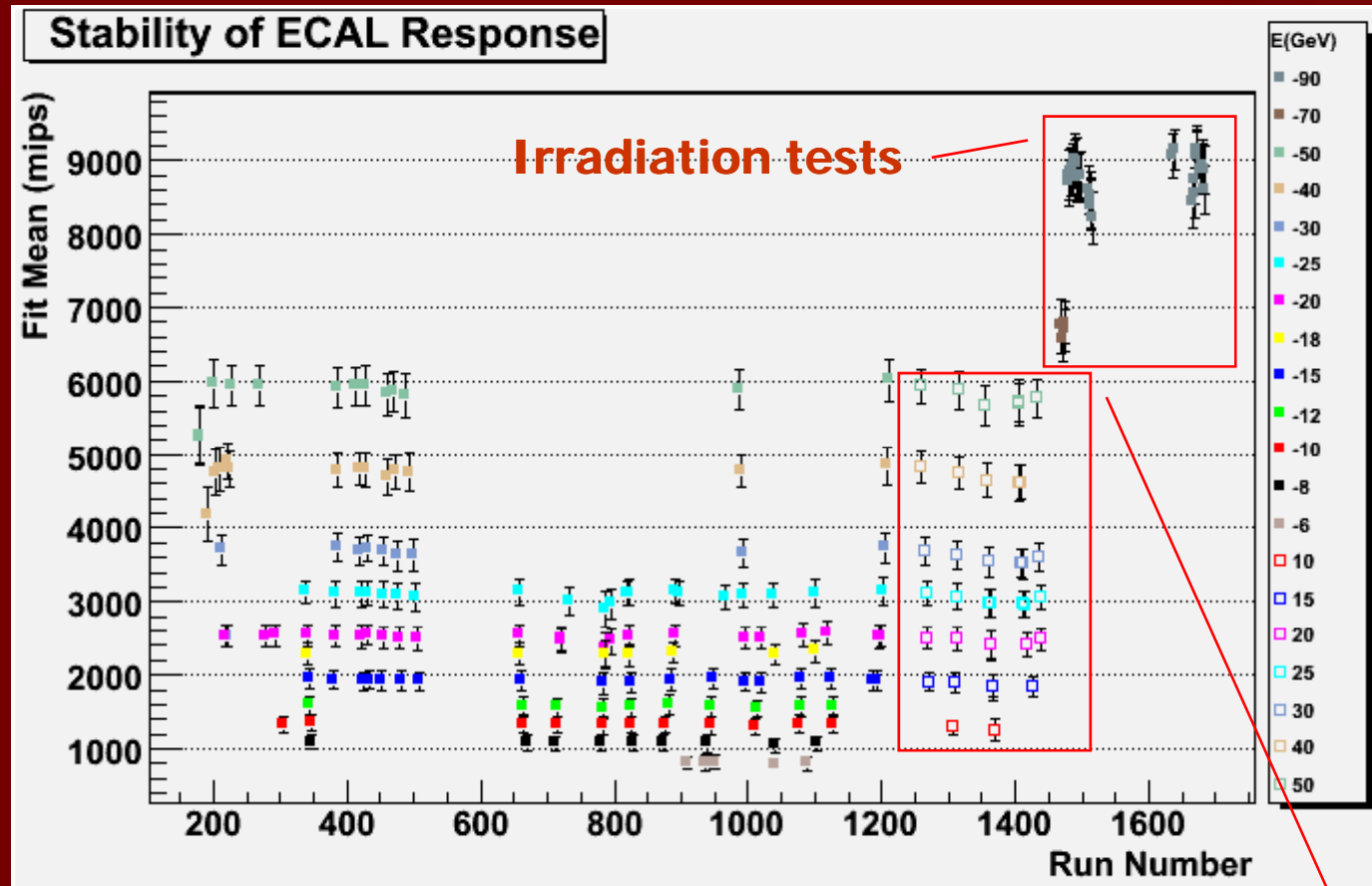


330179 - 331684

LLR

Marcel Reinhard  
LLR - Ecole Polytechnique

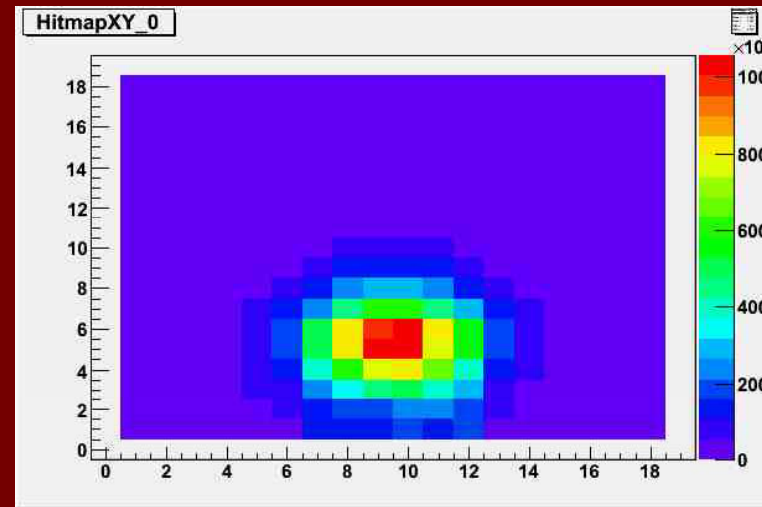
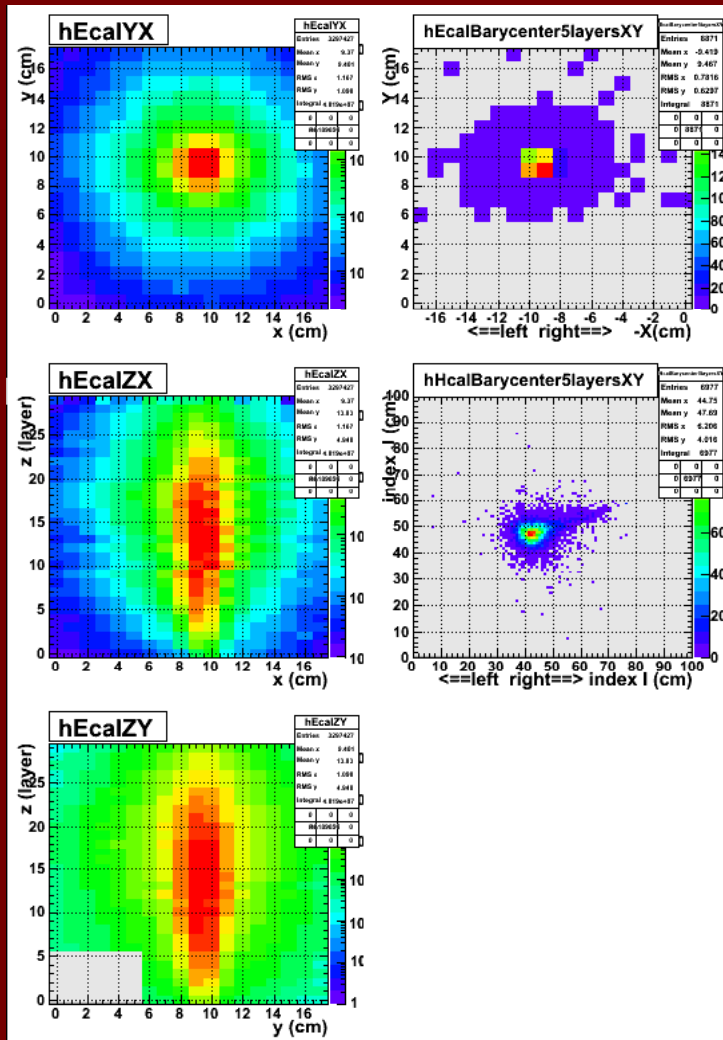
# Stability of response



Dependent on beam quality,... ?

LLR

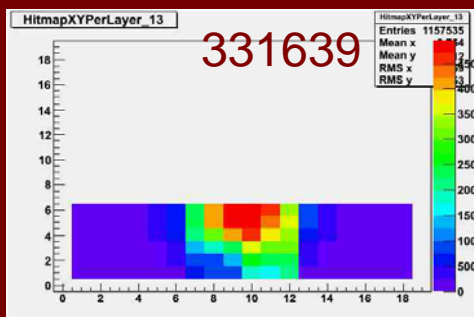
# Behavior of new slabs



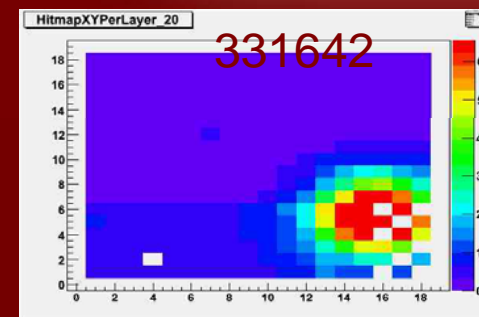
LLR

# Behavior of bottom slabs

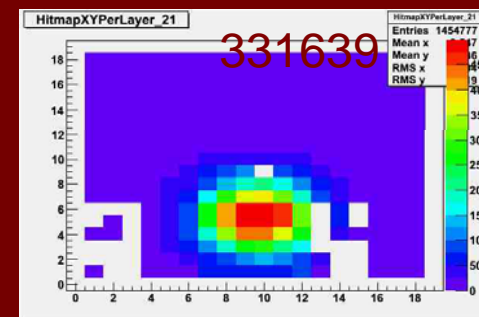
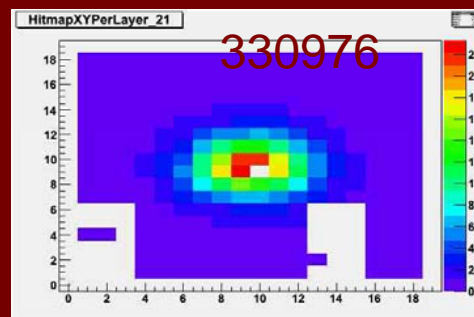
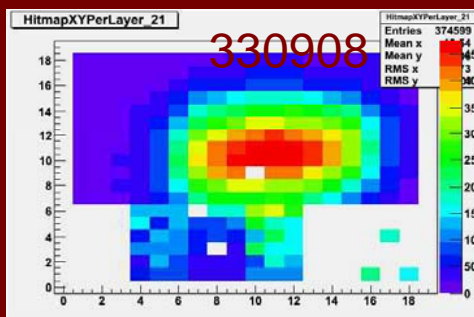
Layer 13



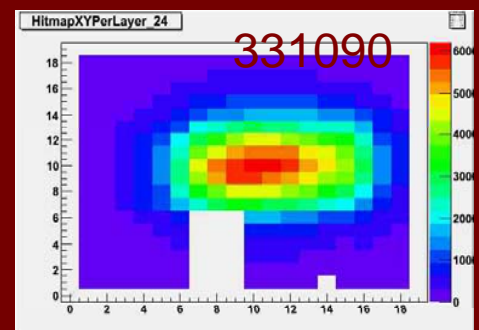
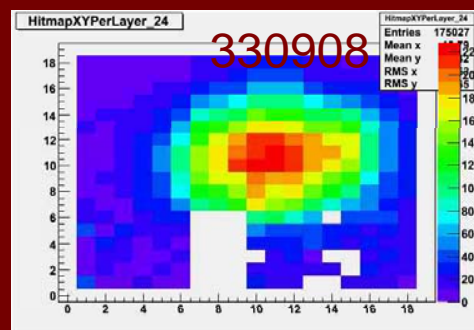
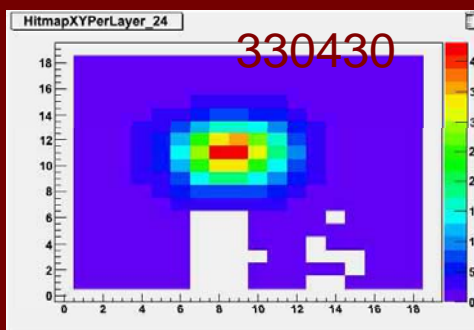
Layer 20



Layer 21



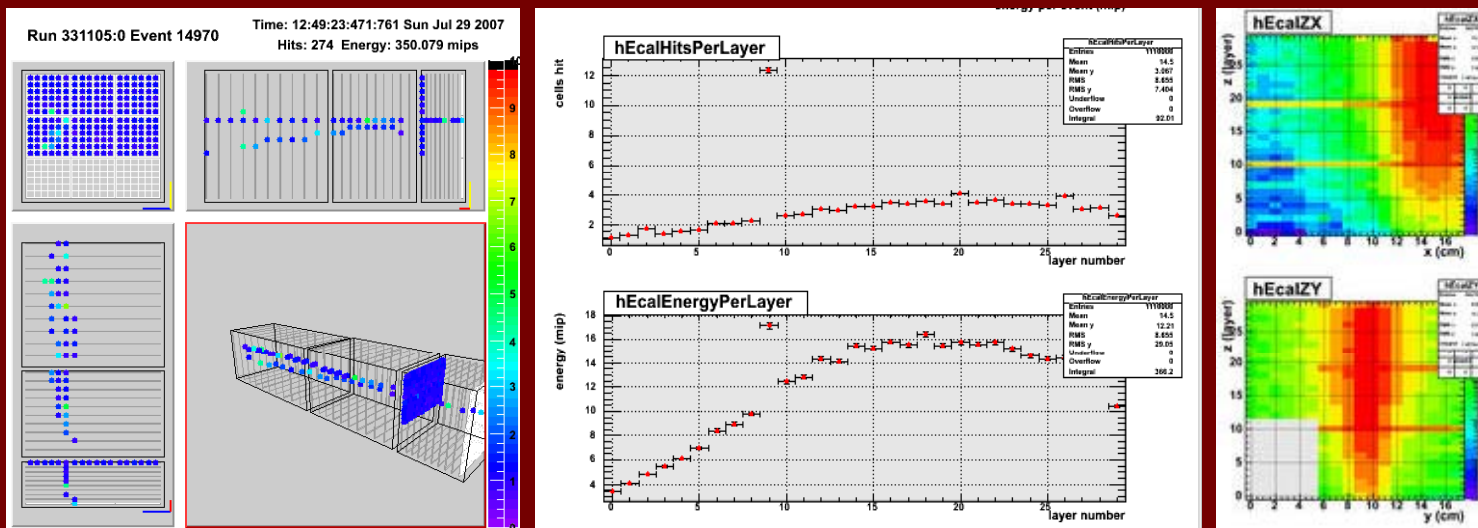
Layer 24





# Pedestal instabilities

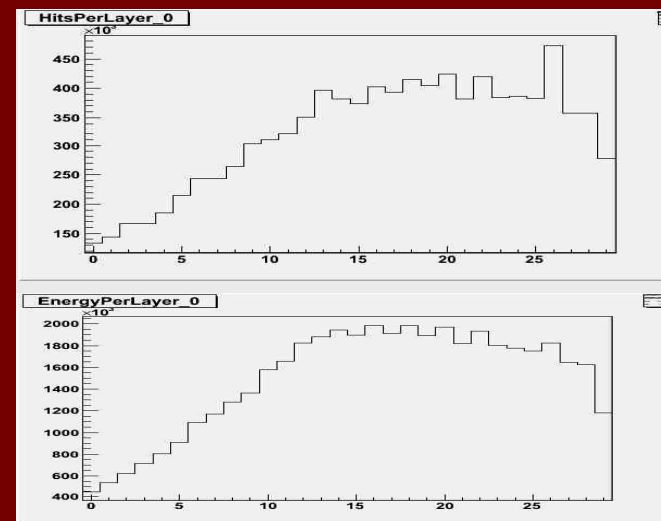
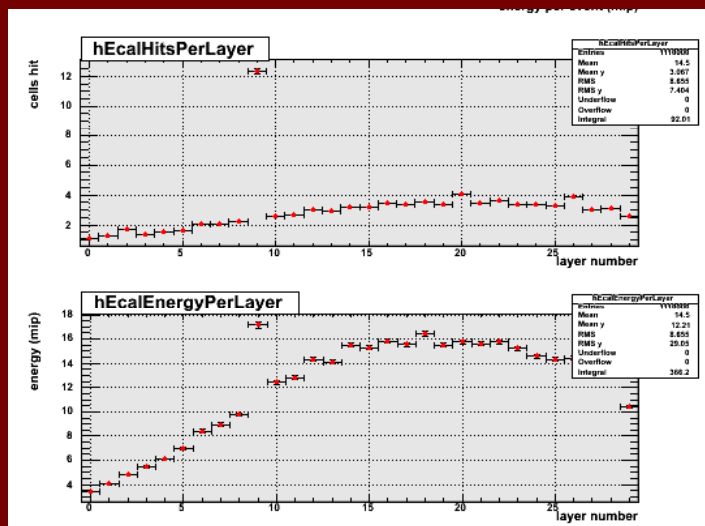
- Fake differential in chip PHY3 makes pedestals strongly depend on exterior effects
- Baseline of a whole PCB is changing dynamically
- Pedestal calculated in the pedestal events is no longer valid
- Calculation wrt to this pedestal may cause much too high values of energy deposit



LLR

# Pedestal instabilities

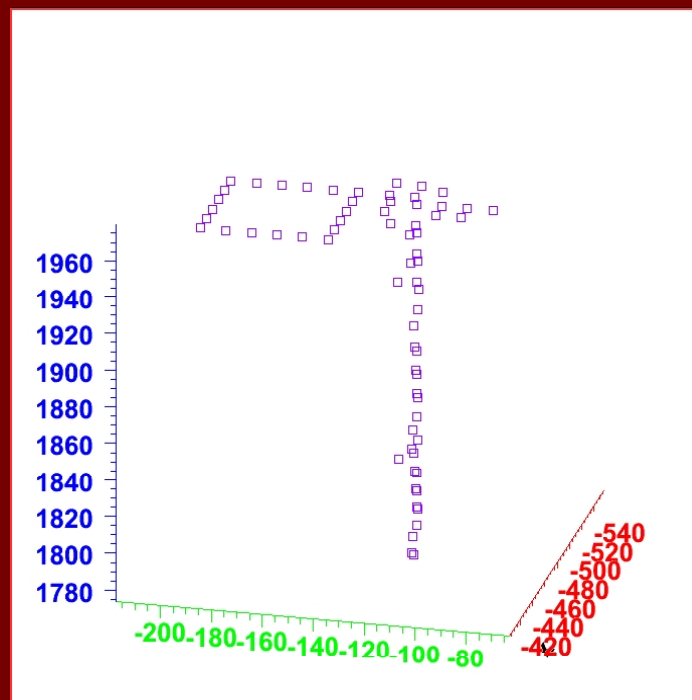
- Software solution: Correction in the reconstruction code calculating pedestal on event-by-event basis using non-hit wafers (becomes more difficult for high occupancies!, not complete correction in some cases)
- Hardware solution: Regulators; tests have been performed but without success (higher noise level)
- Seems to have distracted the shift crews a lot
- Include some correction in the Online Monitor ?



LLR

# Square events

- Invoked by the guard rings around the wafers
- Energy deposit in this guardring induces a signal in the outermost cells of a wafer
- ... can definitely not be changed for the proto
- Corrections under study

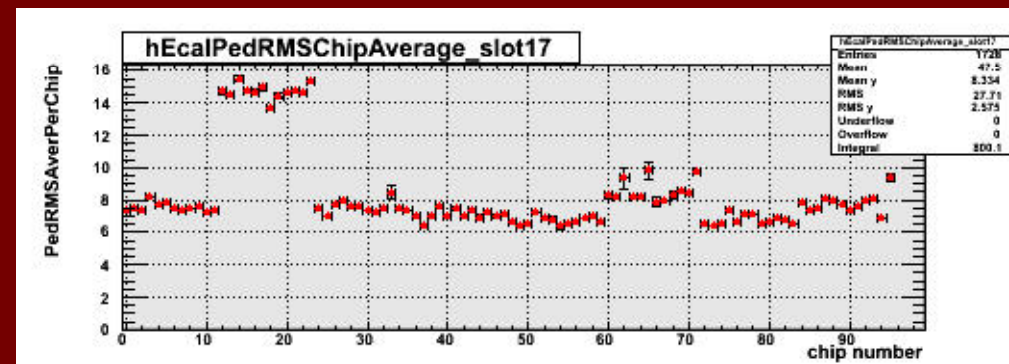


Marcel Reinhard  
LLR - Ecole Polytechnique

LLR

# Noise problems

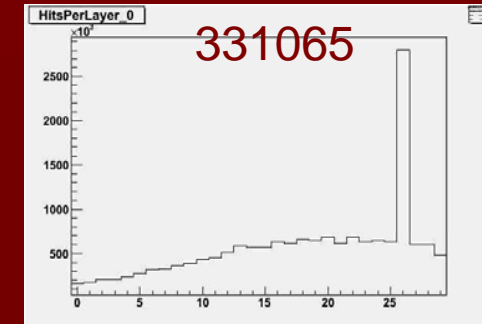
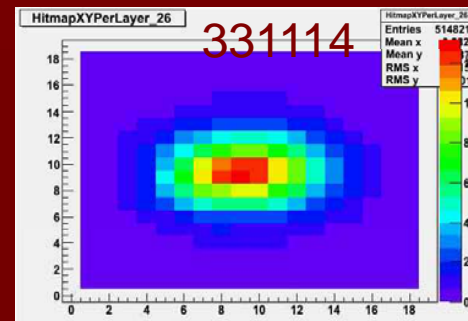
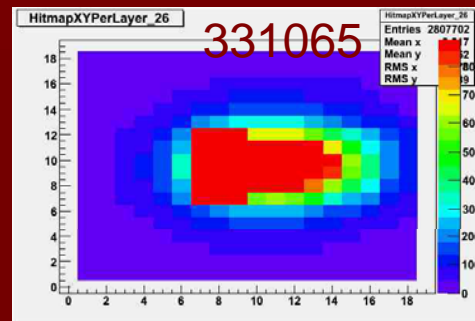
- All noise values for the cells on a PCB are too high
- Very sensitive to the delivered power, thus to the power supplies and/or the power cables
- Changing of power cable can solve the problem
- Several cables marked as „problematic“ – need replacements
- Access difficult in many cases (danger to do more harm than good)



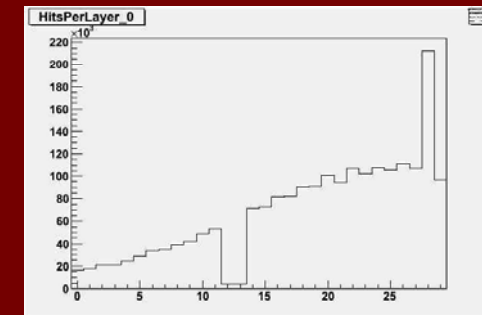
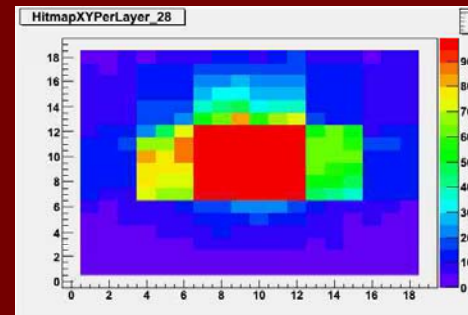
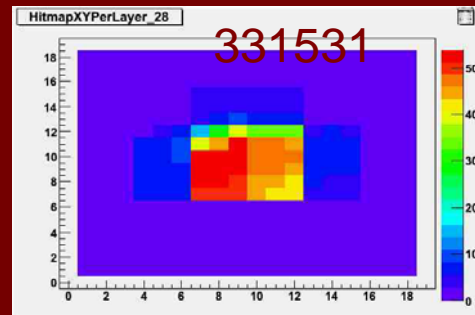

# Noisy chips

- Some chips can develop higher noise for a certain period in time

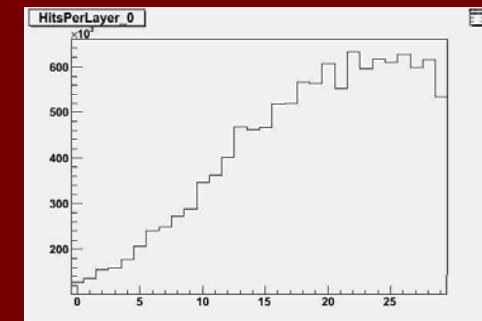
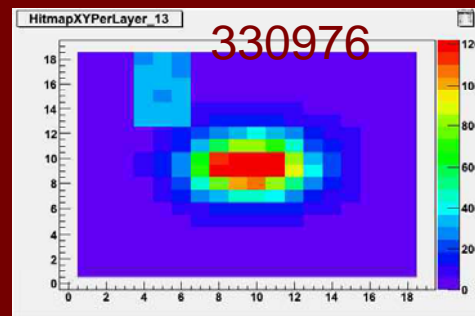
Layer 26



Layer 28

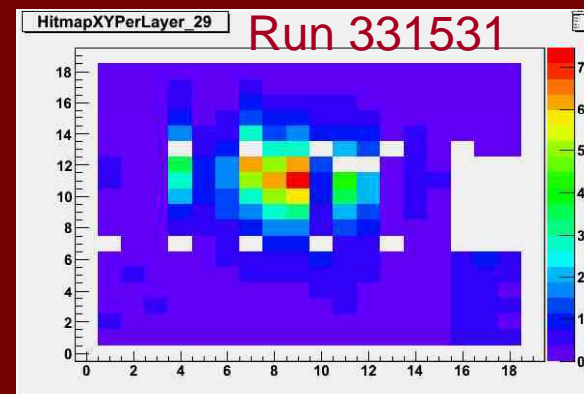
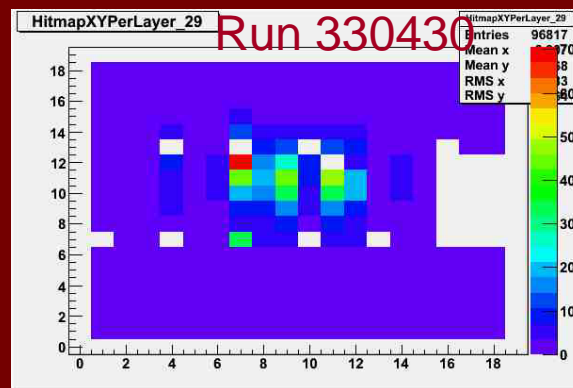


Layer 13




# Problems due to the connectors (?)

- Can cause noise in several cells
- Typical structure that one chip is not connected
- In some cases is the access impossible due to limited space
- No guarantee by de- and replugging
- Read-out problems (?)



LLR

# A wishlist ...for various timeframes

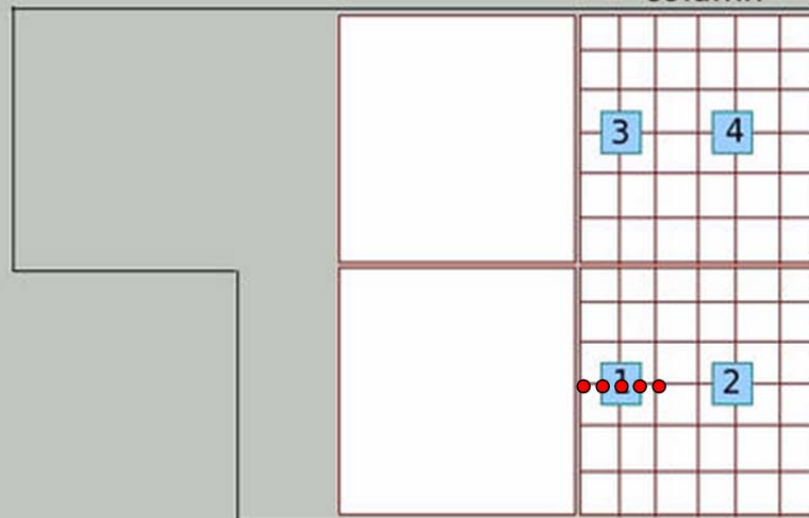
- Solution to instable pedestals (improved regulators?)
- Check of bottom slabs (transport next week?)
- Spare power cables and maybe a test of the existing cables + new ones will be needed when the detector is completed
- Data of ECAL slow control should be included in data stream (the most useful would be currents and tension at each wafer)
- Improved accessibility of ECAL cables
  - Power box for ECAL stage
  - Cables over ECAL  
(for now, removing the fans requires moving the ECAL out of its nominal center – time consuming)
- Revision of program for control of ECAL stage
- ECAL position on stage in database
- Online Monitor:
  - Possibility to limit visualisation to center/upper part
  - Correction for moving pedestals ?
- DESY test with all experts on site (with beam if possible!)



# Backup

Replacing Layer 12 (Slot 19, FE 2)

Left wafer  
column



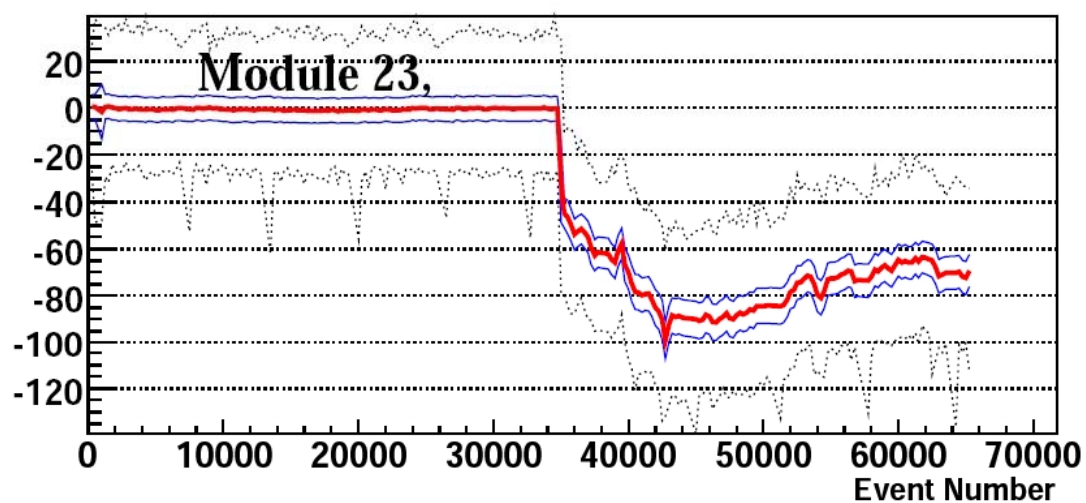
- 1: (-8.33,0)
  - 2: (-5.33,0)
  - 3: (-8.33,6.2)
  - 4: (-5.33,6.2)
- wrt ECAL (0,0)

LLR



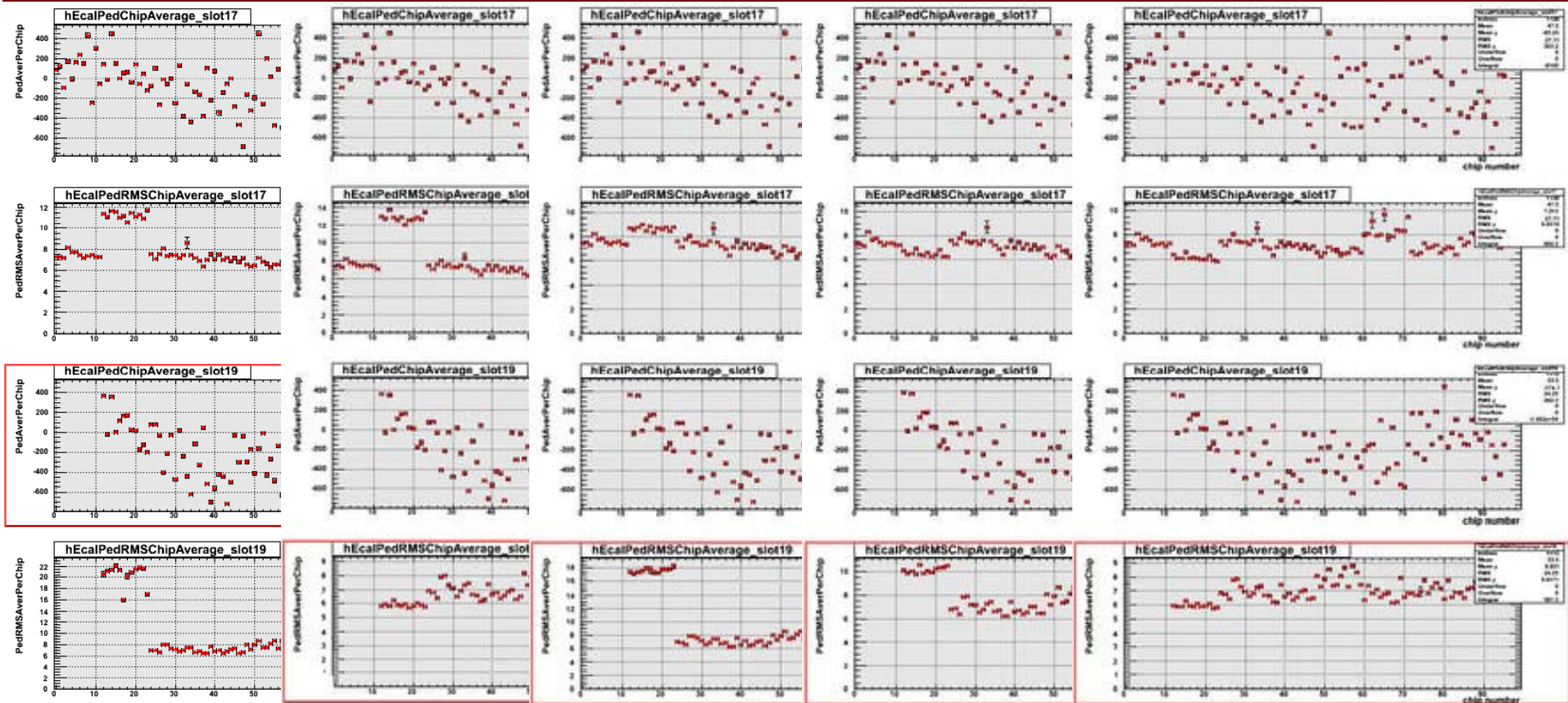
## Pedestal Instabilities

Pedestal as a function of the time :



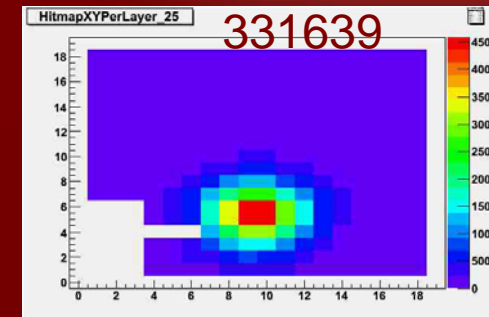
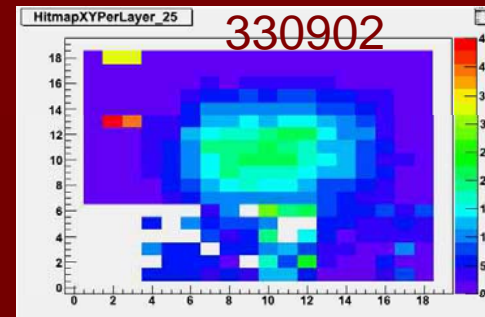
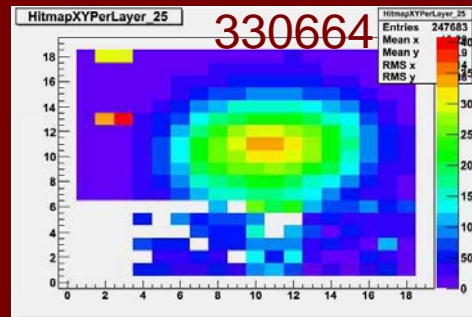
(A PCB with unstable pedestals)

# Pedestal shift in online monitor

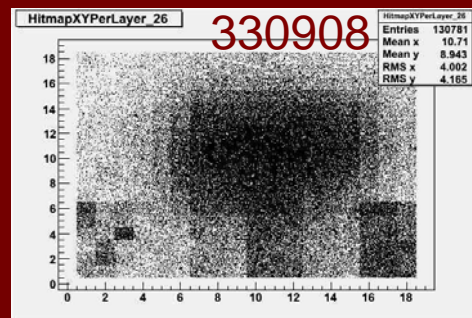


# More bottom slabs

Layer 25



Layer 26



Layer 28

