DIF for ECAL
some Technical aspects

DIF working group

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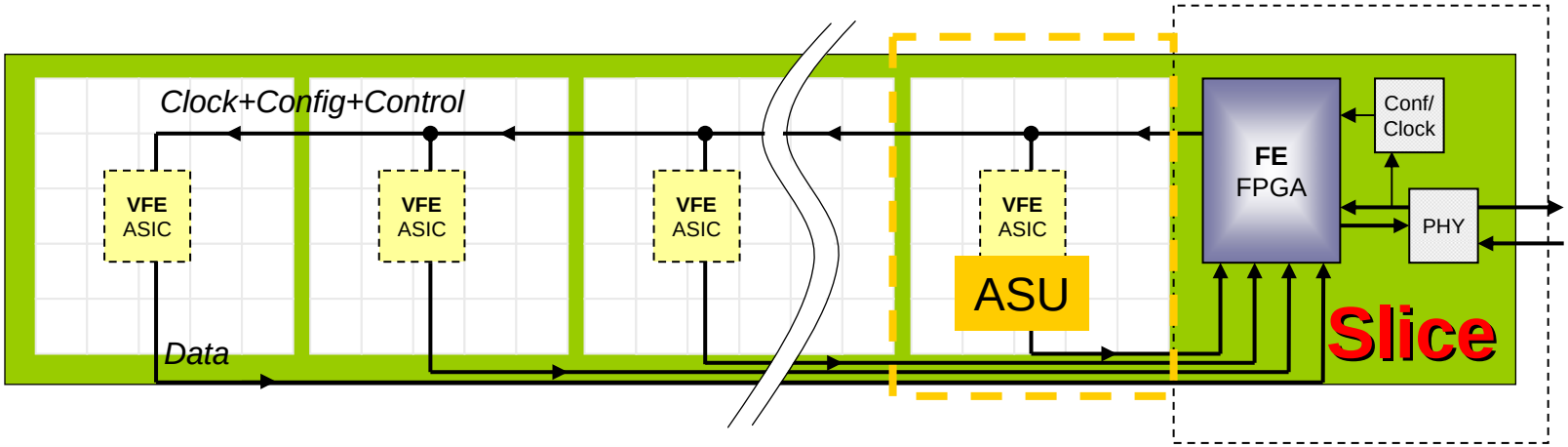
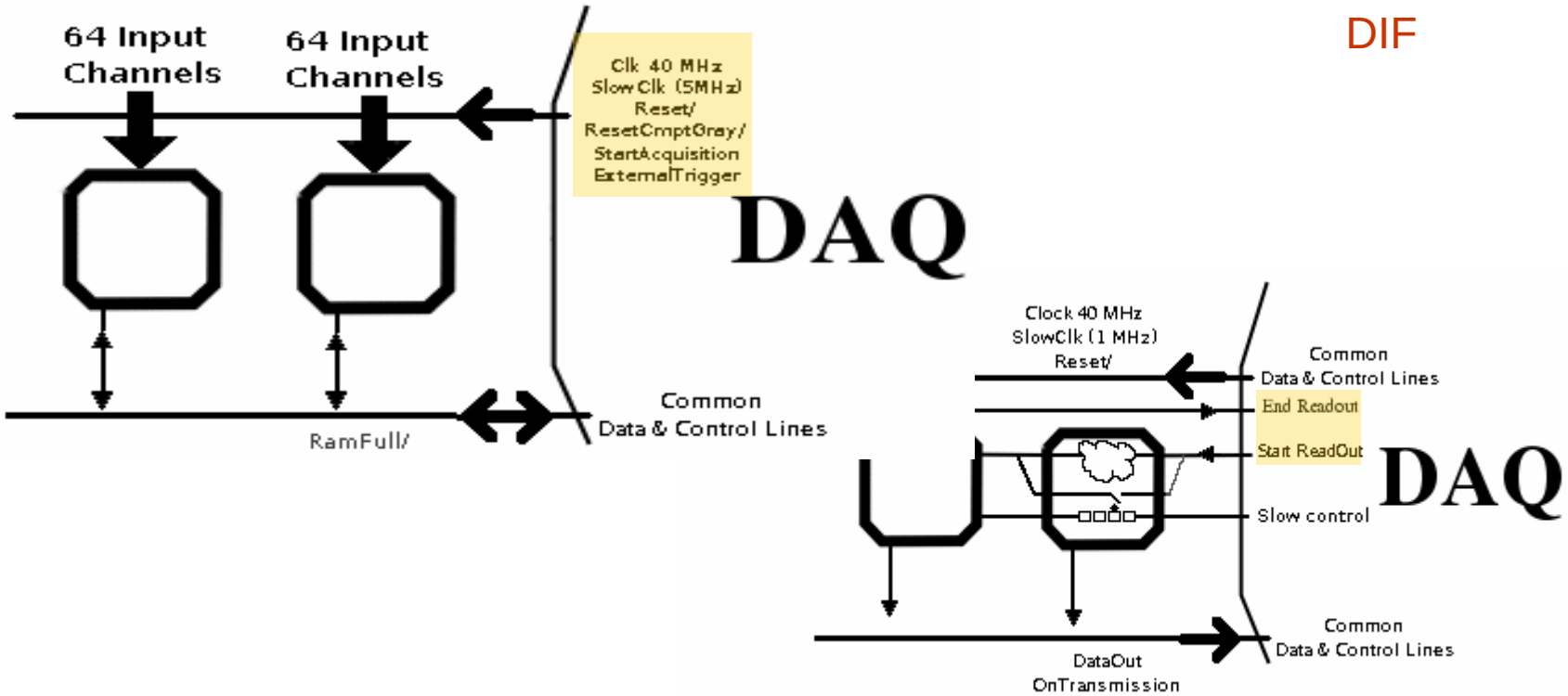
SKIROC read-out interface



DIF



ASU-DIF connector

- High Voltage
- Power
- Bias
- Clock, Control and Commands (CCC)
- Slow control
- Read-out
- Probe

System requirements

- Reliability
- Power dissipation
- Testability
- Signal integrity
- Timing
- Mechanical constraints
- Successive versions of ROC chips

As a first approach, linked to ASUDAQ developments : a try to list signals of ASU-DIF connector :

SKIROC Spring'07 compared to other chips

ASUDAQ et ISDDAQ implementees dans proto eDIF

LPC 22/06/07 11/09/2007 13:14

under work
need external hardware to run with every ROC versions
compatible with limitations (use of undevoted existing hardware)
fully compatible ROC/ASU/SLAB
extra features

I/O pour connecteur ASU/SLAB

		single signal					proto eDIF		
CATEGORIE	NOM	SKIROC Q3'07 doc LAL 06/06/07	SKIROC 08<	HaRDROC 07 doc LAL 06/06/07	SPIROC 07 doc LAL 06/06/07	ASU/SLAB	min. conf	add. Feature	dir from DIF
HV									
POWER	GND	33 different	1 single supply	many		1 single supply	1		
	3.3V	20 different	1 single supply	many		1 single supply	1		
BIAS		22 external	internal	?			0		
REFERENCE		13 external	internal	?			0		
CCC	clkp 40MHz	1 LVDS	1 LVDS	1 LVDS	1 LVTTL	1 LVDS	1 LVDS		O
	clkn 40MHz								
	Reset	1 OC	1 OC	1 LVTTL	1 LVTTL	1 OC	1 OC		OC
	test_in	Analogue		rtn			1		Aout
	resetb_pa	1 LVTTL						1 LVTTL	O
	resetb_discri	1 LVTTL		rst_counter				1 LVTTL	O
	adc_discrib	1 LVTTL						1 LVTTL	O
	adcchoice	1 LVTTL						1 LVTTL	O
	valid_discri	1 LVTTL						1 LVTTL	O
	startrampadc	1 LVTTL						1 LVTTL	O
	adc_pwr_puls	1 LVTTL		pwr_on_daq			1 LVTTL		O
	power_on_analog	1 LVTTL	?	4 LVTTL		1 LVTTL	4 LVTTL		O
	ramp	analogue			"+52 i" "+130 O"				AIn
SC	clk_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	rstb_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	sroutscbuf	1 LVTTL	1 LVTTL	1 LVTTL	?!	1 LVTTL	1 LVTTL		I
	srin_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	clkp_sc_lvds							1 LVDS	O
	clkn_sc_lvds								
SPY	clk_spy	1 LVTTL						1 LVTTL	O
	rstb_spy	1 LVTTL						1 LVTTL	O
	r (SCA)	5 LVTTL						5 LVTTL	O
	hb (SCA)	5 LVTTL						5 LVTTL	O
	out_analogue (SCA)	analogue							AIn
	srin_spy	1 LVTTL						1 LVTTL	O
	sroutspybuf	1 LVTTL						1 LVTTL	I
PROBE	ck_probe	1 LVTTL		ck_r				1 LVTTL	O
	rstb_probe	1 LVTTL		rst_r				1 LVTTL	O
	srin_probe	1 LVTTL		d_r				1 LVTTL	O
	analogue_probe	analogue	analogue			analogue	analogue		AIn
	digital_probe	1 LVTTL	1 LVTTL			1 LVTTL	1 LVTTL		I
	sroutprobebuf	1 LVTTL		q_r				1 LVTTL	I
READOUT	clk_5MHz / 1 MHz				1 LVTTL			1 LVTTL	O

Data from designer's doc

SKIROC Spring'07 compared to other chips

REFERENCE		13 external	Internal	?			0		
									O
									OC
									Aout
								LVTTL	O
	rebetb_discri	1 LVTTL		rst_counter				1 LVTTL	O
	adc_discrib	1 LVTTL						1 LVTTL	O
	adcchoice	1 LVTTL						1 LVTTL	O
	valid_discri	1 LVTTL						1 LVTTL	O
	startrampadc	1 LVTTL						1 LVTTL	O
	adc_pwr_puls	1 LVTTL		pwr_on_daq			1 LVTTL		O
	power_on_analog	1 LVTTL	?	4 LVTTL		1 LVTTL	4 LVTTL		O
	ramp	analogue							AIn
					"+52 I" "+130 O"				
SC	clk_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	rstb_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	sroutscbuf	1 LVTTL	1 LVTTL	1 LVTTL	?!	1 LVTTL	1 LVTTL		I
	srin_sc	1 LVTTL	1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		O
	clkp_sc_lvds							1 LVDS	O
	clkn_sc_lvds								
SPY	clk_spy	1 LVTTL						1 LVTTL	O
	rstb_spy	1 LVTTL						1 LVTTL	O
	r (SCA)	5 LVTTL						5 LVTTL	O
	hb (SCA)	5 LVTTL						5 LVTTL	O
	out_analogue (SCA)	analogue							AIn
	srin_spy	1 LVTTL						1 LVTTL	O
	sroutspybuf	1 LVTTL						1 LVTTL	I
PROBE	ck_probe	1 LVTTL		ck_r				1 LVTTL	O
	rstb_probe	1 LVTTL		rst_r				1 LVTTL	O
	srin_probe	1 LVTTL		d_r				1 LVTTL	O
	analogue_probe	analogue	analogue			analogue	analogue		AIn
	digital_probe	1 LVTTL	1 LVTTL			1 LVTTL	1 LVTTL		I
	sroutprobebuf	1 LVTTL		q_r				1 LVTTL	I
READOUT	clk_5MHz / 1 MHz				1 LVTTL			1 LVTTL	O
	clkp_5MHz / 1 MHz		1 LVDS	1 LVDS		1 LVDS	1 LVDS		O
	clkn_5MHz / 1 MHz								
	StartAcq		1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		O
	ValEvtp		1 LVDS	1 LVDS		1 LVDS	1 LVDS		O
	ValEvtn								
	RazChnp		1 LVDS	1 LVDS		1 LVDS	1 LVDS		O
	RazChnn								
	StartReadOut		1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		O
	EndReadOut		1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		I
	TransmitOn		1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		I
	Dout (out0)	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		I
	out	35 LVTTL	0	out_RS_trig<1..0>	0	0		35 LVTTL	I
	RamFull		1 OC	1 OC	1 LVTTL	1 OC	1 OC		OC
	TriggerExt		1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL	1 LVTTL		O
	TriggerOut		1 LVTTL	1 LVTTL		1 LVTTL	1 LVTTL		I
					"+2 O" "+1 I"				
?	CompOut		0	1 LVTTL				1 LVTTL	O
	LatchOut		0	1 LVTTL				1 LVTTL	O
	ValEvtOut		0	1 LVTTL				1 LVTTL	O
	RazChnOut		0	1 LVTTL				1 LVTTL	O
SPARE	spareI							2 LVTTL	I
	spareO							2 LVTTL	O
	spareLVDSO							2 LVDS	O (0 needed)
	spareLVDSI							2 LVDS	I (0 needed)
	spareOC							2 OC	(0 needed)

Data from designer's doc

ASU/SLAB connector I/O LPC 22/06/07

CAT	NAME			
HV				
POWER	GND	1		
	3.3V	1		
BIAS		0		
REFERENCE		0		
CCC	clkp 40MHz	1 LVDS	O	
	clkn 40MHz			
	Reset	1 OC	OC	
	power_on_xxxx	5 LVTTL	O	new 22/06
	testin	analogue	O	new 22/06
SC	clk_sc	1 LVTTL	O	
	rstb_sc	1 LVTTL	O	
	sroutscbuf	1 LVTTL	I	
	srin_sc	1 LVTTL	O	
PROBE	analogue_probe	analogue	Ain	
	digital_probe	1 LVTTL	I	
READOUT	clkp_5MHz / 1 MHz	1 LVDS	O	
	clkn_5MHz / 1 MHz			
	StartAcq	1 LVTTL	O	
	ValEvtp	1 LVDS	O	
	ValEvtn			
	RazChnp	1 LVDS	O	
	RazChnn			
	StartReadOut	1 LVTTL	O	
	EndReadOut	1 LVTTL	I	
	TransmitOn	1 LVTTL	I	
	Dout (out0)	1 LVTTL	I	
	RamFull	1 OC	OC	
	TriggerExt	1 LVTTL	O	
	TriggerOut	1 LVTTL	I	

ASU-DIF
ASU connector

Baseline for ASUDAQ test system

Many I/O more added to current board to follow SKiROC developments

To be discussed

Pending questions / Conclusion

- 5 power-on signals?
- 2 clocks ?
- signal integrity (termination, controlled impedance, …) ?
- **Missing signal ?**
- **Mechanics ?**

ASUconnector :

ASU-DIF

	O	I
LVDS	4	0
TTL	12	6
OC	2	
A	1	1
PWR	2	

Is something missing ?

ASUDAQ
First prototype

	O	I	spare O	spare I	total O	total I	SKIROC Q3'07 compat. needed O	SKIROC Q3'07 compat. needed I
LVDS	4	0	3	2	7	2	1	0
TTL	12	6	30	41	42	47	27	40
OC	2		2		4		1	
A	1	1	0	0	1	1	1	2