The DIF Task Force and a focus on the DHCAL DIF

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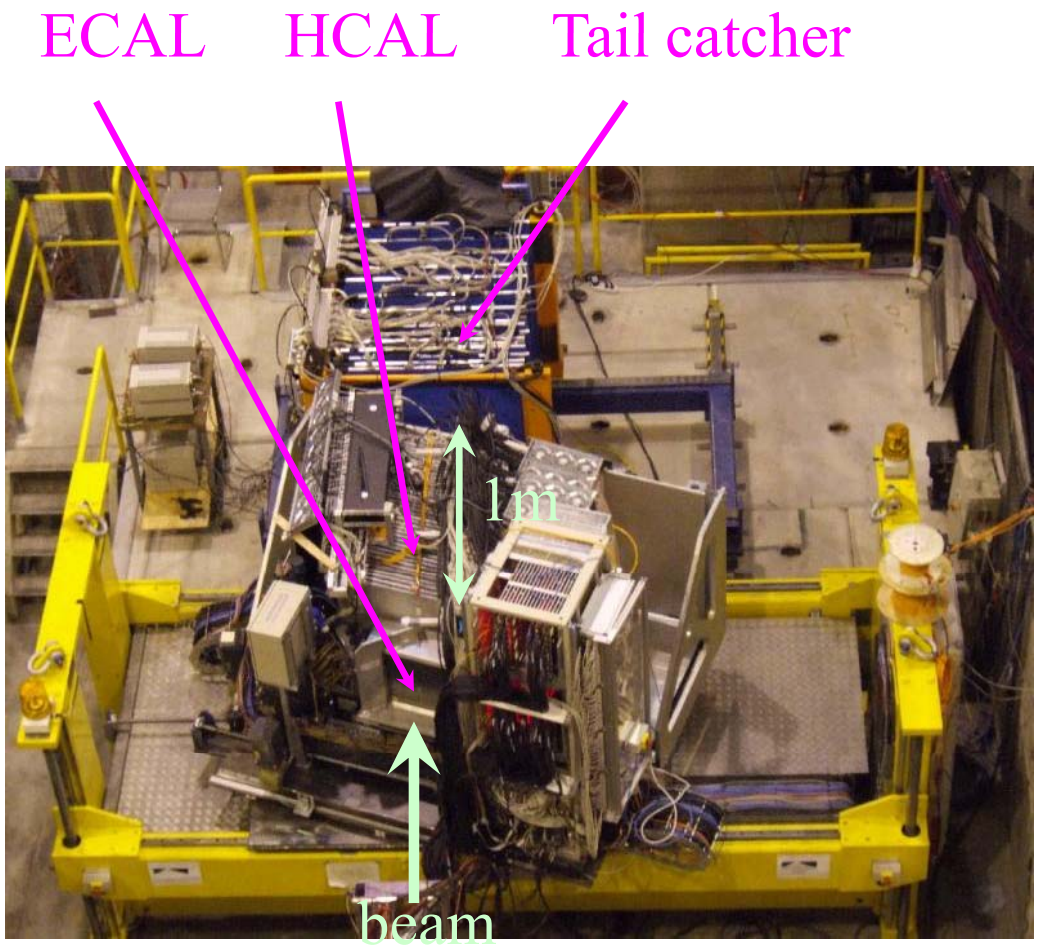
Prototype Running at Test Beam



• Prototype was in test beam at CERN for 2 months.

• Goal : Test physics prototype and prove algorithm.

• Already many channels :

ECAL	9072 channels
HCAL	7608 channels
tail catcher	320 channels

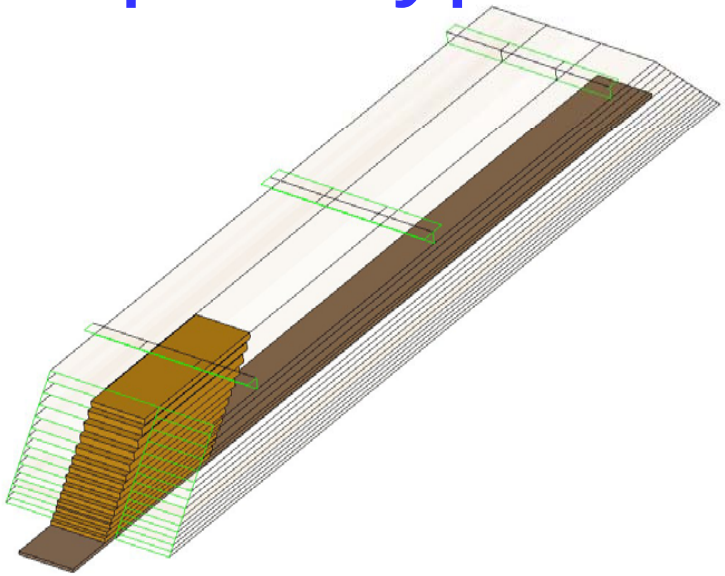
Total 17 k channels

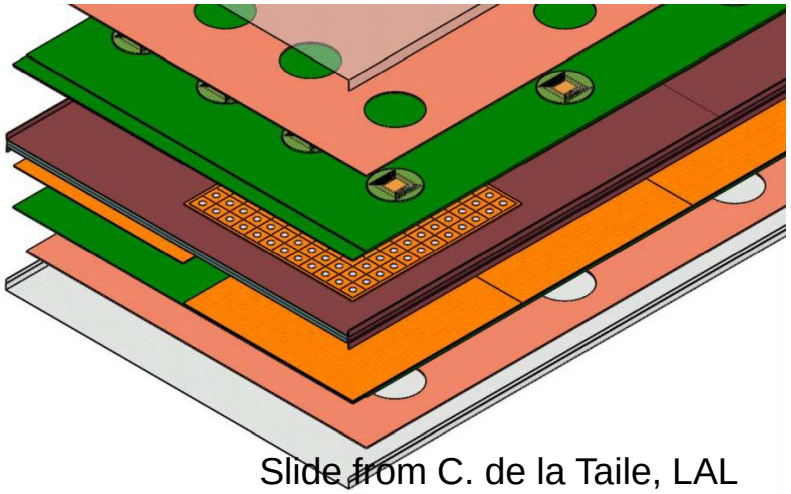
•Electronics sits at the side, but ILC needs: No dead volume
► concept for integrating the electronics

Slide from Peter Göttlicher, DESY

Moving to technological prototypes

- Now moving to large scale (1.5m) technological prototypes : « 2nd generation ASICs and DAQ»
  - SPIROC, SKIROC, HARDROC, …
- Front-end ASICs embedded in detector
  - High level of integration, low thickness
  - Ultra-low power with pulsed mode
  - Essential to demonstrate detector feasibility
- All communications via edge
  - 4,000 ch/slab, minimal room, access, power
  - small data volume (~ few 100 kbyte/s/slab)
- « Stitchable motherboards »
  - Minimal connections between boards





Low Cost and industrialization are the major goals

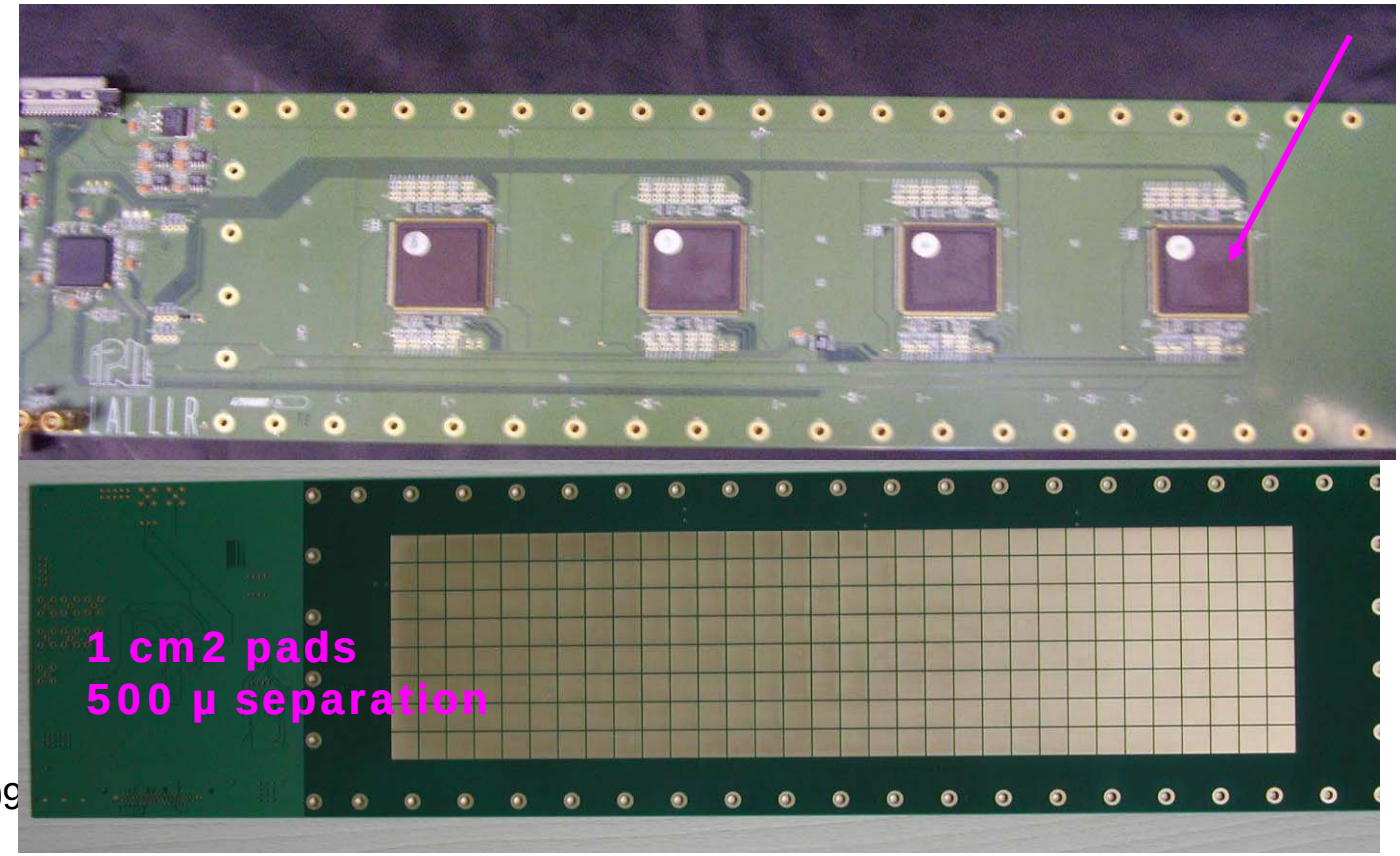
Slide from C. de la Taile, LAL

Focus on DHCAL

- First detector with 2nd generation ASICs and 2nd generation DAQ
  - 8X32 pads RPC detector, 8 layer PCB optimized to reduce crosstalk and compatible with MicroMEGA detector
- Board received in june 07, tests starting
  - Test beam and cosmics this fall

HaRDROC

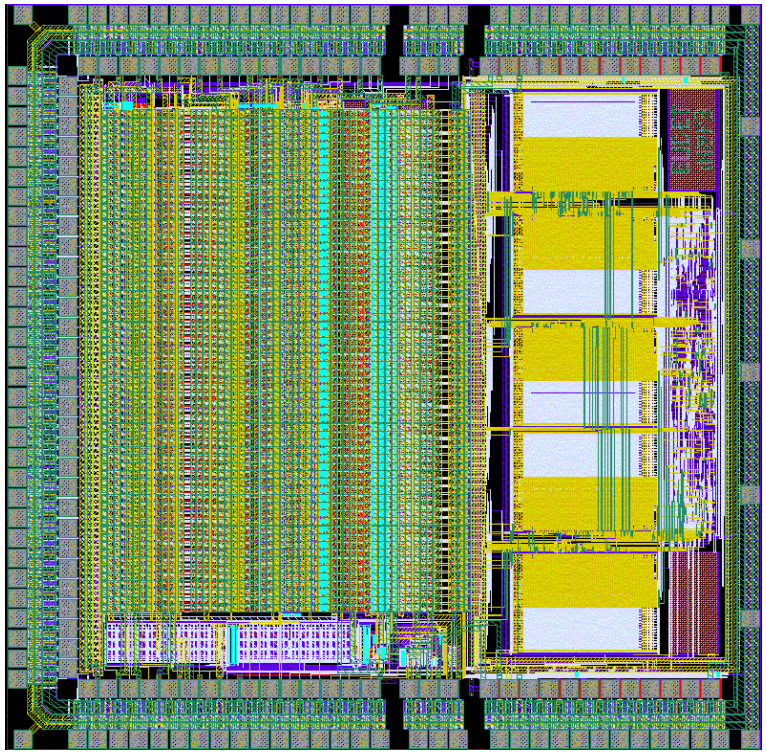
VFE ASIC



Slide from Imad Laktineh, IPNL

HaRDROC chip for DHCAL

Hadronic Rpc Detector Read Out Chip (AMS SiGe 0.35µm, Sept 06)
LAL IPNL



64 inputs, **1 serial output @ 1 or 5 MHz**

•Multiplexed **analog charge output** (debugging)

•**A 128 deep digital memory**: store all channels and BCID for every hit : 20k data transferred during interbunch.

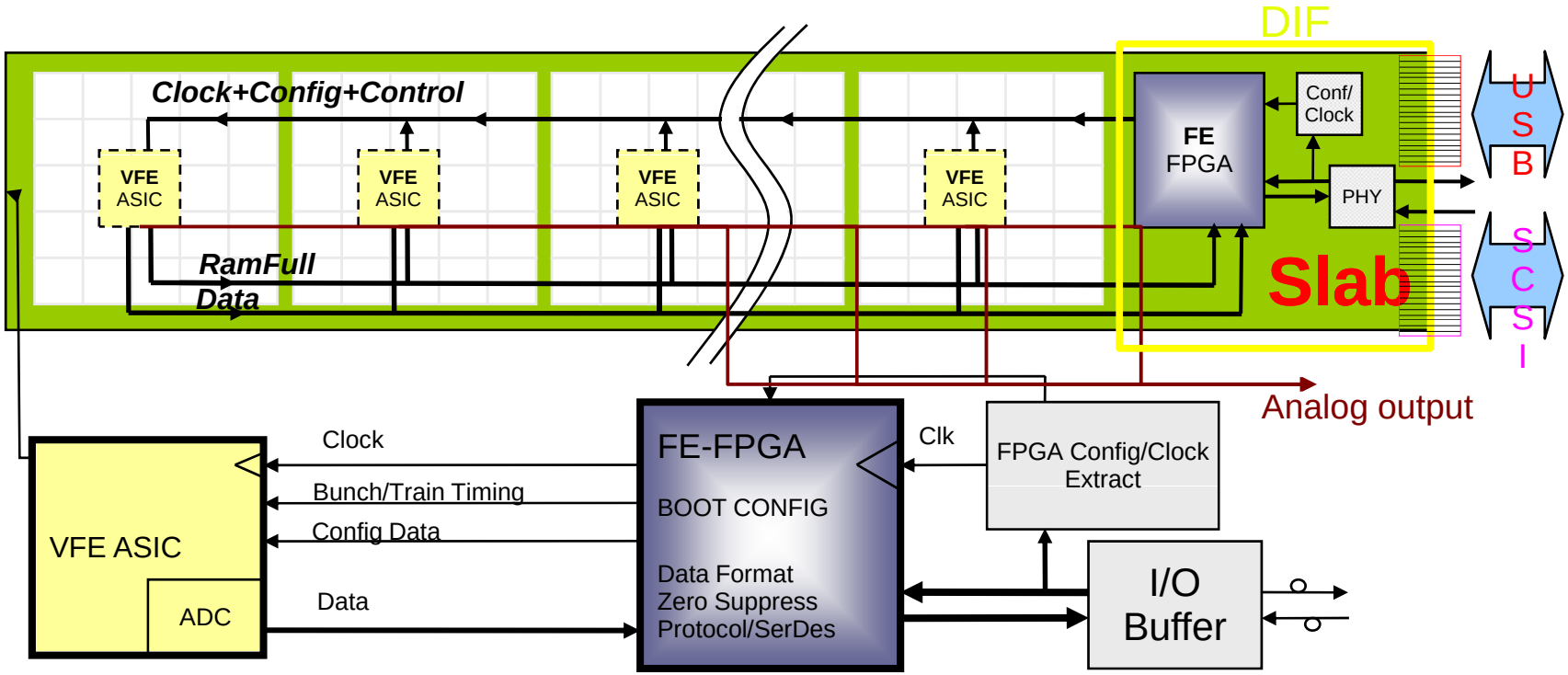
•**ASICs embedded** inside the detector for compactness and **daisy chained** to minimize output lines on the detector.

•**Full power pulsing**

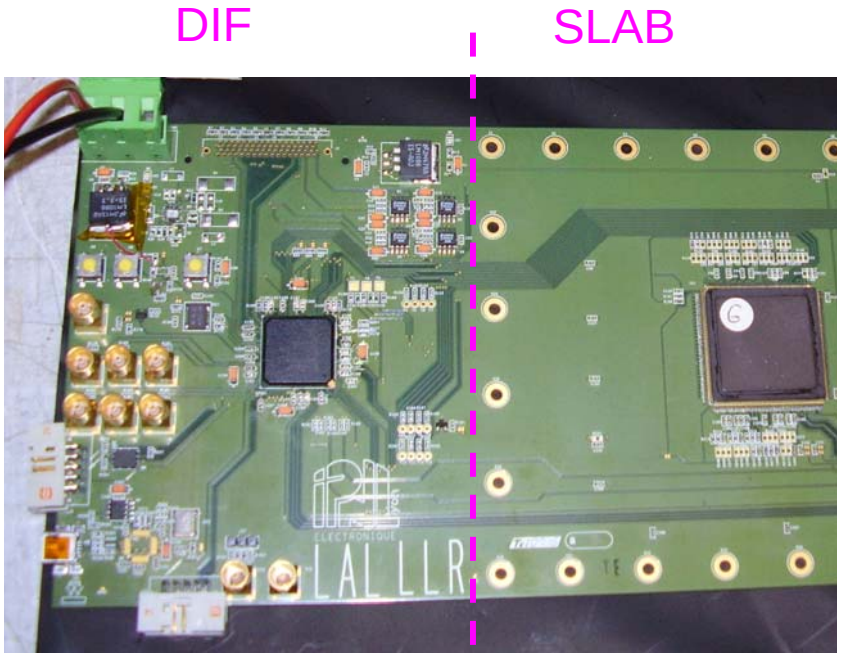
•**1700 chips** to be produced in 2007 for **1m^3 DHCAL prototype**.

HaRDROC digital part

- Chips to be embedded and daisy chained to minimize number of output lines inside the detector.
- FPGA based readout
- DAQ communication through USB



SLAB and DIF interface



- SLAB and DIF will be separated on the next DHCAL proto for more flexibility.
- SLAB/ DIF interface TBD
  - List of signals
  - Electrical levels
  - Connector choice (low height, reliability, …)
  - Pinout,
  - …

DHCAL SLAB/DIF current interface

Power supply and power cycling

Signal	Function	I/O for slab	Elec standard	Valid on	Pin count
DVDD	Digital power supply 3.5 V (-> 2.5V in future ?)	I	Power	-	?
AVDD	Analog Power supply (3.5 V)	I	Power	-	?
GND	Common ground	I	Power	-	?
Pwr_on_dac	Power cycling on dac part	I	LVTTL	high	1
Pwr_on_d	Power cycling on the digital part	I	LVTTL	high	1
Pwr_on_ss	Power cycling	I	LVTTL	high	1
Pwr_on_a	Power cycling on the analog part	I	LVTTL	high	1

Clocks and resets

Signal	Function	I/O for slab	Elec standard	Valid on	Pin count
Clk_40MHz	40 MHz clock for the internal state machines (SM)	I	LVDS	rising	2
CLK_5MHz	5 MHz clock for the BCID and the readout.	I	LVDS	rising	2
Reset*	Reset for internal SM.	I	LVTTL	low	1
RAZ_Chn	Reset for internal RS flip flops (discri outputs)	I	LVDS	high	2
RST_counter	Reset for the BCID counter Debug ?	I	LVTTL	high	1

DHCAL SLAB/DIF current interface (cont)

Fast and slow control

Signal	Function	I/O for slab	Elec standard	Valid on	Pin count
Val_evt	Validation window during which event is valid.	I	LVDS	high	2
StartAcq	Start acquisition mode (RAM @ = 0, …)	I	LVTTL	high	1
StartReadout	Start readout mode (empty RAM)	I	LVTTL	high	1
EndReadout	HardRoc chaining for readout (start-> end -> startReadout)	O	LVTTL	high	1
TransmitOn	Hardroc is transmitting data	O	Open collector	high	1
Dout	Serial output data for readout	O	Open collector	-	1
RAM full*	Internal RAM is full (sent by one of the asics) Cabled or	O	Open collector	low	1
RAMfullext	Stops current acquisition if an HC is ram full.	I	LVTTL	High	1
TriggerExt	External trigger input (mainly for test beam)	I	LVTTL	rising	1
TriggerOut	Or of the 64 discri (for debugging)	O	LVTTL	rising	1
RST_SC	Slow control : logic reset	I	LVTTL	low	1
Q_SC	Slow control : output data (output of the SR)	O	LVTTL	-	1
D_SC	Slow control : input data (Input of the SR)	I	LVTTL	-	1
CK_SC	Slow control : logic clock	I	LVTTL	Rising	1
Ctest	Allows to inject analog signal (for test or calibration)	I	analog		

DHCAL SLAB/DIF current interface (cont)

Debugging signals :

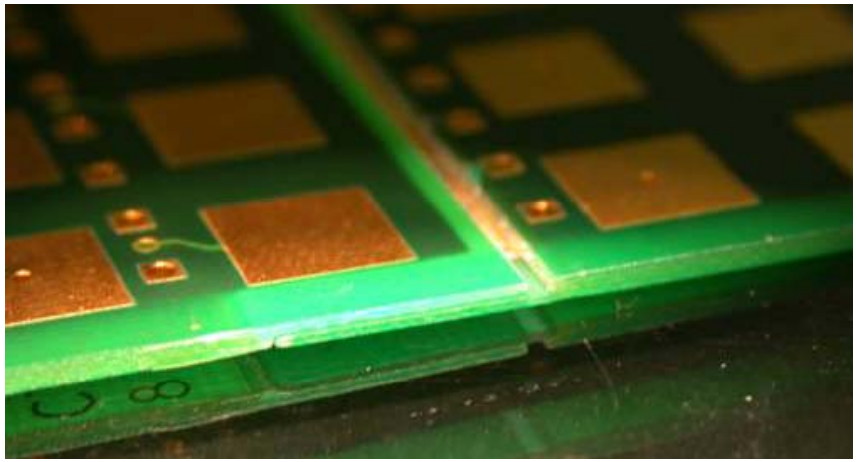
Signal	Function	I/O for slab	Elec standard	Valid on	Pin count
Q_R	Analog readout : Output of the SR	O	LVTTL	-	1
D_R	Analog readout : Input of the SR	I	LVTTL	-	1
CK_R	Analog readout : clk of the SR	I	LVTTL	rising	1
RST_R	Analog readout : reset of the SR	I	LVTTL	low	1
hold	Analog readout : hold	I	LVTTL	high	1
Out_q	Analog signal at the output of the mux.	O	analog	-	1
Ramfull_007	If ramfull OC signal is stucked to 0, allows debugging				4
Dout_007	If dout OC signal is stucked to 0, allows debugging				4
TransmitOn_007	If transmiton OC signal is stucked to 0, allows debugging				4
Out_fsb	For analog debug :	O			4
En_otaq	For debug :	O			4
Raz_chn_int	For debug :	O			4
Out_Trig_int	For debug :	O			4
RS_trig0	For debug : spy RS outputs	O	LVTTL	-	4
RS_trig1	For debug : spy RS outputs	O	LVTTL	-	4
Trig0	For debug : spy discri outputs	O		-	4
Trig1	For debug : spy discri outputs	O		-	4

DHCAL SLAB/DIF interface: Some questions …

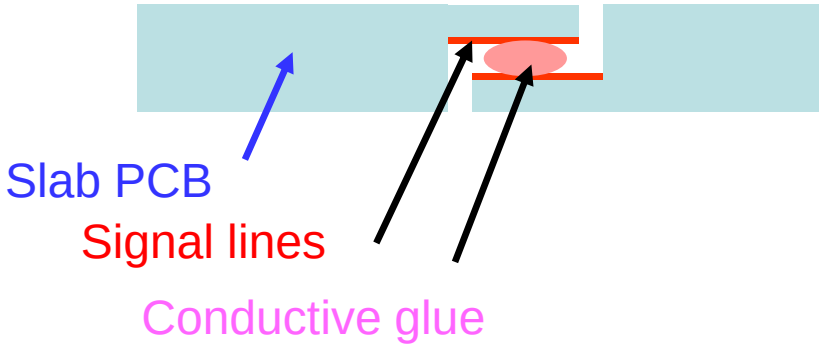
- **Electrical aspects :**
  - Is it really necessary to keep 4 signals for the power cycling?
  - Could we generate the 40MHz clock from the 5MHz clock with a PLL ?
  - Do we really need so many resets?
  - Do we really need such signals as:
  - TriggerOut ; Start_readout, end readout, .. ?
  - Add signals to strap one asic in the daisy chain ?
  - Foresee an other connector (or probes ?) for the debugging signals ?

- **Mechanical aspects :**
  - Number of connections
  - Density of the connector
  - Low height connector: a couple of mm
  - Reliability

SLAB Long Structure



ECAL PCB



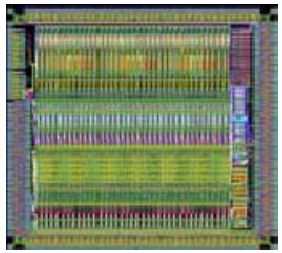
- Which technique to get the long structure (2 m) ?
- Gluing as for ECAL ?
- Other scenario ? See C. Combaret's talk
- Aim : manufacture standard sized PCBs : lower cost designs

- The SLAB/SLAB interface will be an essential parameter for the definition of the SLAB/DIF interface as it will impact the number of signals to consider.
  - Max 4 etches / cm ?

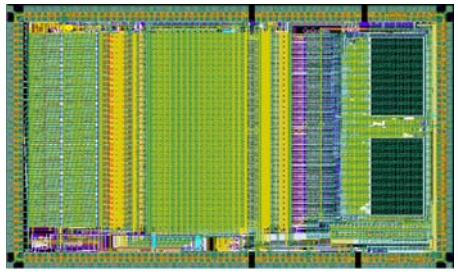
Pictures from Peter Göttlicher, DESY

Many similarities between the 3 subdetector ASICs and DIFs

- Details on DHCAL ASICs and PCB were given, but similar developments are being done on AHCAL and ECAL.
  - SPIROC ASIC for AHCAL and SKIROC ASIC for ECAL
- The 3 ASICs have been mostly developed by LAL and have a lot of common features, in particular the digital interface :
  - Serial link data output + daisy chained ASICs
  - Clock and timing control (BCID, …)
  - Fast control signals as start_acq, ram_full, …
  - Power pulsing



- DIFs have also some identical functions
  - ASIC Configuration
  - Synchronization and clock distribution
  - Readout
  - Interface with the DAQ
  - Based on FPGA



DIF Task Force

- To avoid duplication (triplication) of work, a small working group of 4 people has been created, with one people from each subdetector and one from the DAQ :
  - Remi Cornat (Clermont) : ECAL
  - Mathias Reinecke (DESY) : AHCAL
  - Julie Prast (Annecy) : DHCAL
  - Bart Hommels (Cambridge) : DAQ
- They will work in collaboration with all the people working on the different subdetectors, on the DIF or on the DAQ.

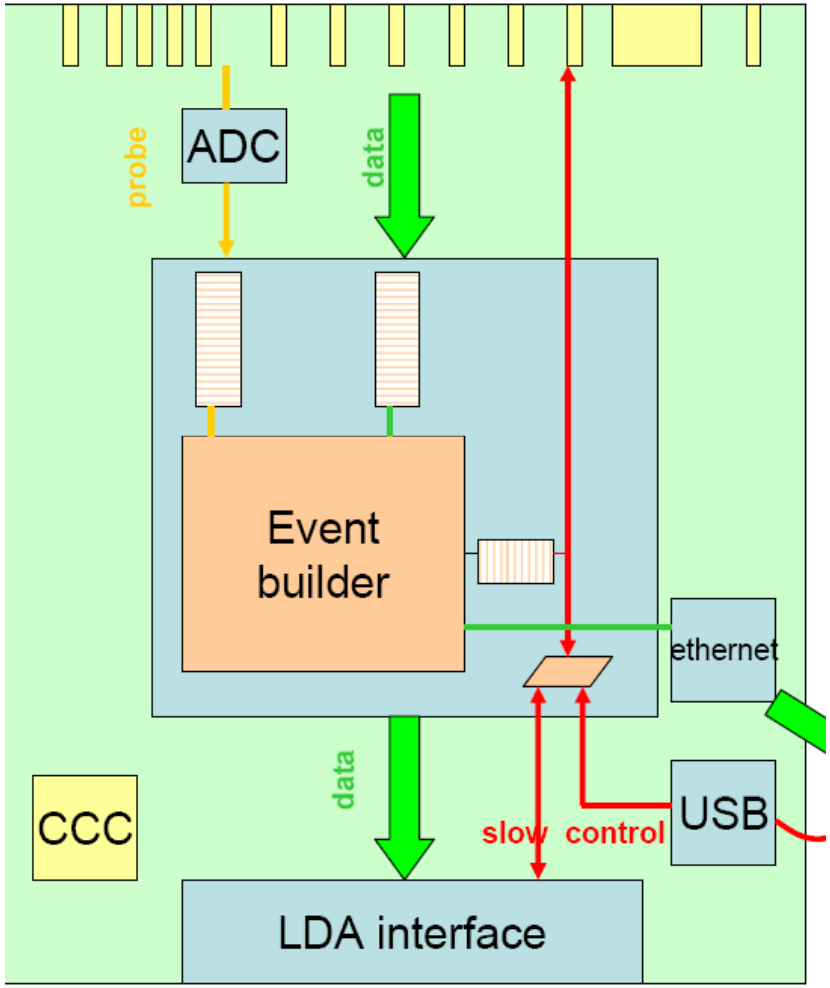
Aim of the task force

- Define the interface between SLABs and DIF
  - Connector pinout
  - Electrical signals and levels
  - Underlying what is common and detector specific
- Define the DIF architecture : common blocks and detector specific blocks, interface to DAQ and USB.
- Define common VHDL libraries.

- Summarize everything in a common document for the end of this year.

Others DIFs being developped : ECAL

- Test board for the SKIROC ASIC (on going)
- “ASUDAQ” : ECAL DIF for production test
  - Full Slow control
  - Readout of 4 SKIROCs through USB or Ethernet and PC.
  - Access to analog test points.
  - Design based on FPGA
  - LDA interface
  - The board is being design ; schematics done.



Others DIFs being developped : AHCAL

- Test board for the SPIROC
  - ASIC configuration and readout
  - Data acquisition
- Developments around the DIF architecture
  - HCAL and DAQ interfaces ; FPGA based
  - Calibration control, power supply and slow control
  - Felix at last electronics CERN meeting:

“DIF: need standards to parallelize developments”