AHCAL – DIF Interface

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At first a statement …

The concept presented in these slides is :

- neither fixed nor finished (=> preliminary state).

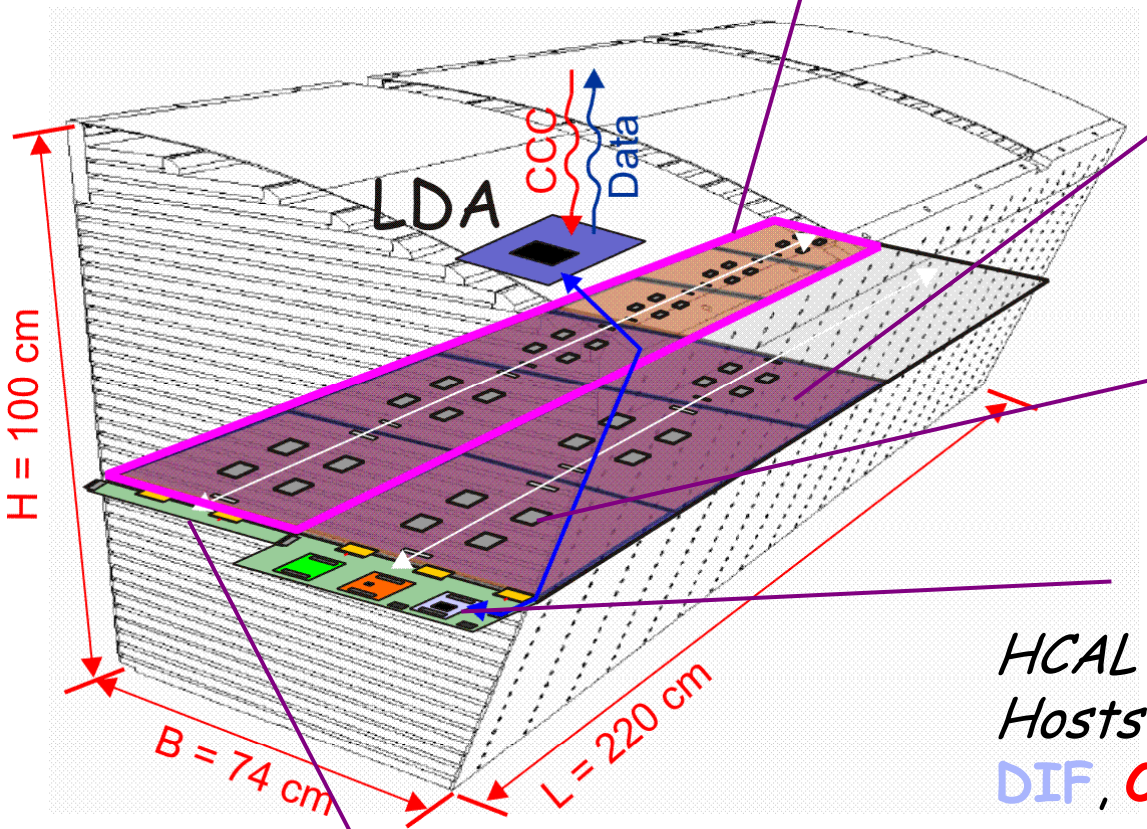
- not coordinated with the work from Julie, Remi or Bart.
  (‚there was simply not enough time before this meeting')

The actual mission of the DIF working group of coordination starts ‚now'.

AHCAL Half Sector - Integration

AHCAL Slab

6 HBUs in a row



HBU

HCAL Base Unit

typ. 12 x 12 tiles

SPIROC

typ. 4 on a HBU

HEB

HCAL Endcap Board

Hosts mezzanine modules:

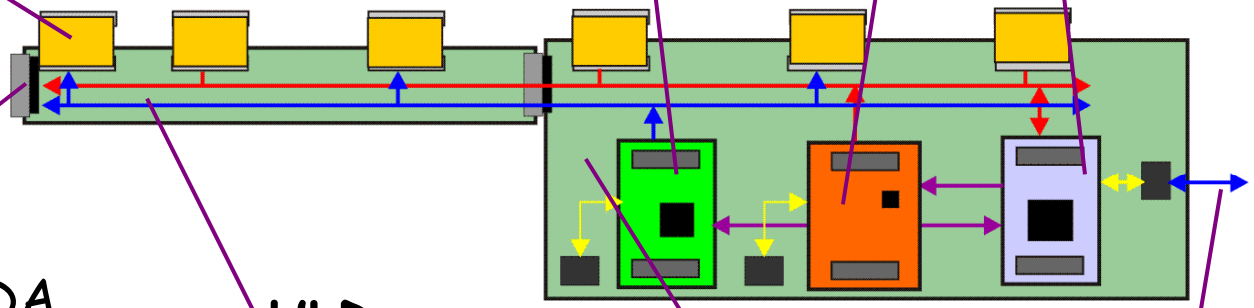
DIF, **CALIB** and **POWER**

HLD

HCAL Layer Distributor

HEB Interconnection Concept

Flexlead and 80-pin connector
Interconnection to AHCAL-Layer (HBU)



DIF-DIF conn.
Redundancy against failures of DIF or LDA

HLD
Changes Size from Layer to layer

HEB
Same Size for all 38 AHCAL layers

To LDA

DIF - *Detector Interface (Configuration and Operation)*
CALIB - *Light and/or Charge calibration and monitoring*
POWER - *Layer power and temperature monitors*

Mezzanine setup allows independent development of different groups.

Slabs of an AHCAL layer

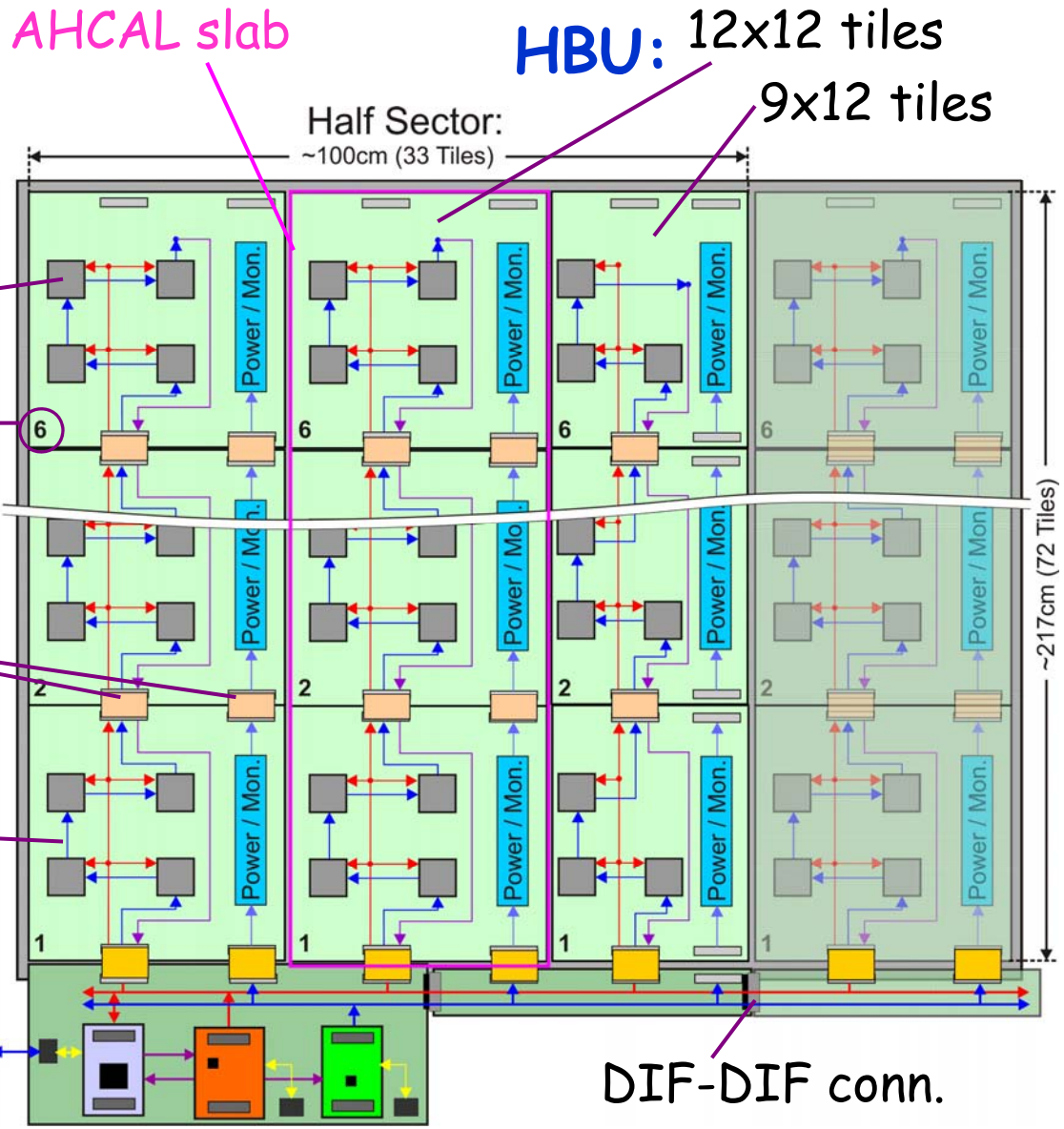
Number of channels per layer not constant!

24 SPIROCs in chain

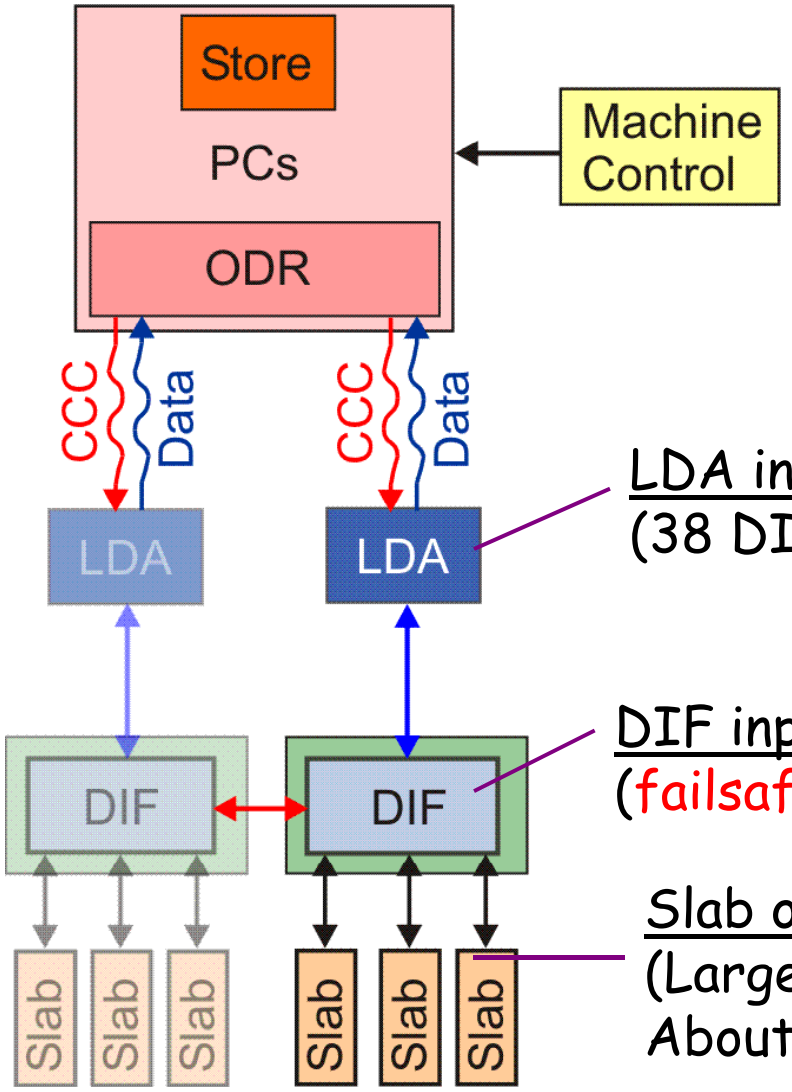
6 HBUs in a row

Two flexleads for interconnection

Slow-Control and Readout token



DAQ and AHCAL Data Rate



ODR: Off-Detector Receiver
LDA: Link/Data Aggregator
DIF: Detector (specific) Interface
CCC: Clock/Control/Config

LDA input data rate: max. 105MBit/bunch train
(38 DIFs connected)

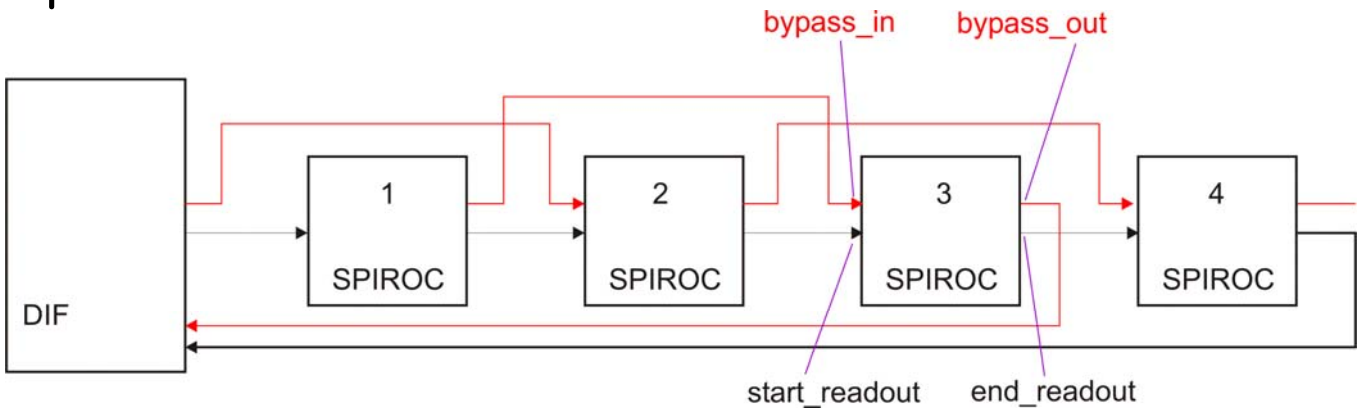
DIF input data rate: max 2.8MBit/bunch train.
(failsafe setup: up to 6 slabs per DIF)

Slab output data rate: max. 460kBit.
(Largest slab: 24 SPIROCs in a readout chain,
About 19kbit data per SPIROC)

Failsafe Setup

Up to 24 SPIROCs (864 detector channels) in slow-control and readout chain (AHCAL).

A broken chip would disable the complete chain.
Proposal:



„If e.g. chip 2 fails, chip 1 uses bypass_out, chip 3 uses bypass_in".

If agreed, needs implementation in next ASIC versions!

SPIROC – DIF Signalling

First ideas about signals between DIF and AHCAL slabs.

SPIROC operation more complex than HARDROC.
- present prototype has many debug signals.
- some of the complexity remains due to analogue operation - as for ECAL chip

How many of the debug, power-cycling and reset signals are needed for production version?

Failsafe setup needed for Slow-Control and Readout?

We propose an enable signal to the power block in order to switch off a complete layer/slab.

Should we foresee a readback possibility of slow-control data?

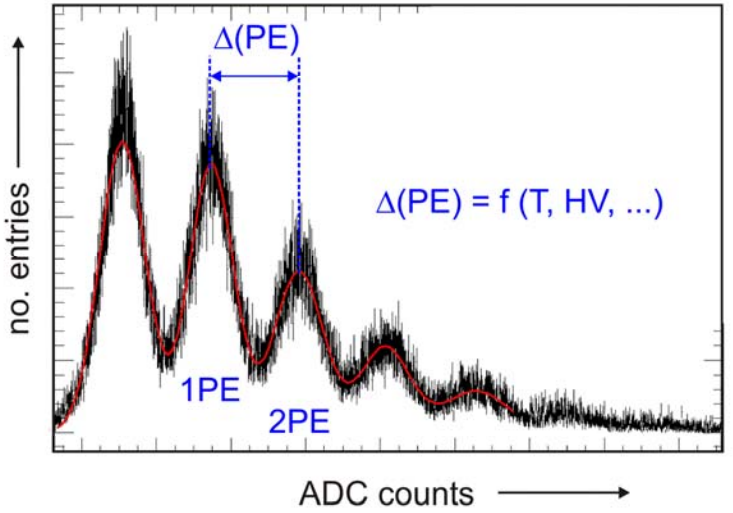
AHCAL Light Calibration System

SiPM response strongly depends on temperature and bias voltage.

LCS (based on UV LEDs) needed for:

-Calibration (ADC counts per PE)

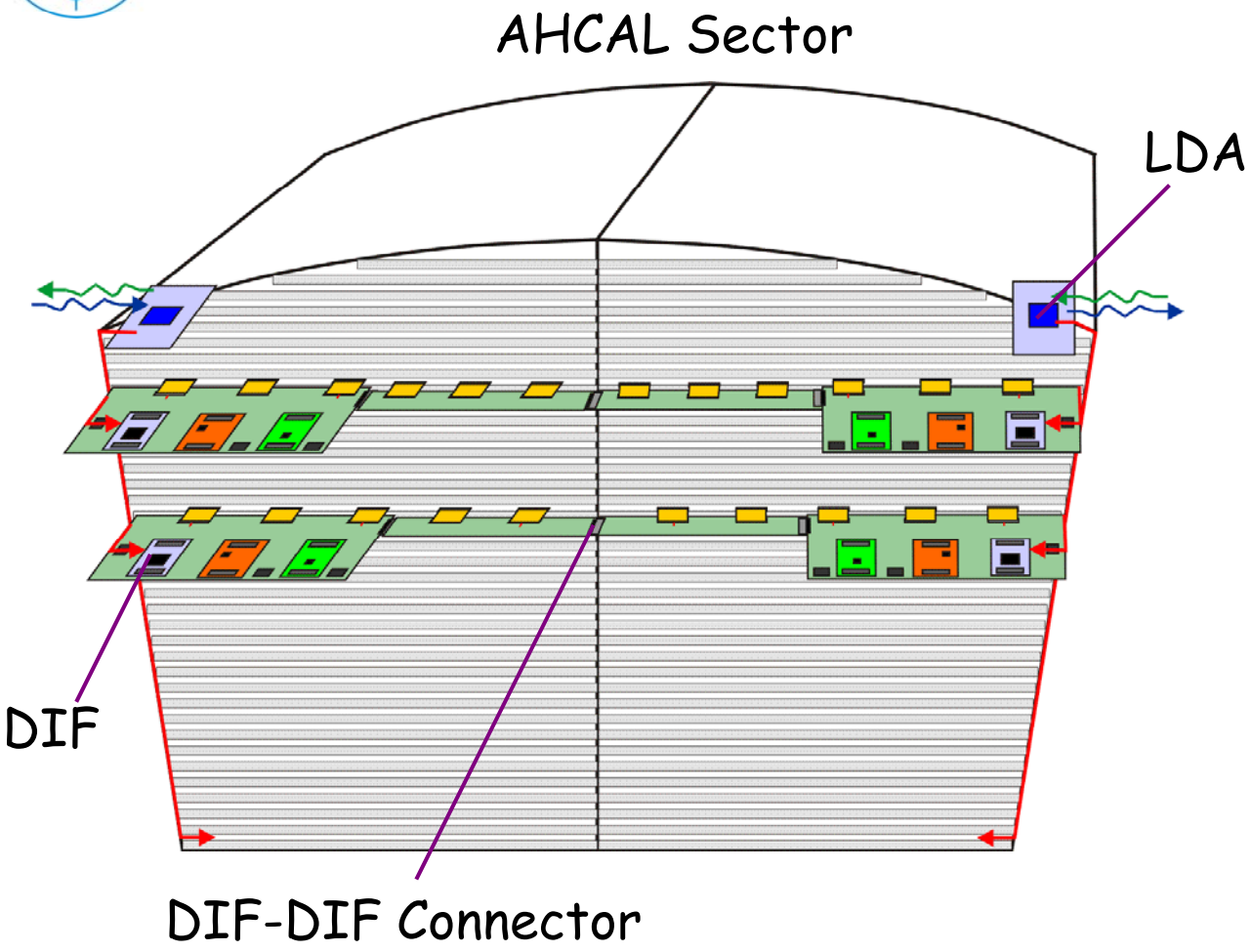
-Gain Monitoring



Two different concepts under investigation (same DIF setup):

- Quasi-Resonant LED driver setup on DIF, fibers into AHCAL gaps
  (see: our Prague colleagues, I. Polak et al.)
- One LED per tile, direct coupling without fibers
  (currently tested at DESY)

Redundancy



Each AHCAL slab is connected to two DIFs and two LDAs

Redundancy proposal by M. Goodrick, Bart Hommels et al.

Conclusion

- First ideas about AHCAL-DIF setup have been collected.
  Now: discussions and coordination in DIF working group.

- The working group needs input and a final ‚ok' from ASIC designers and „ILC users" about a proposed concept.