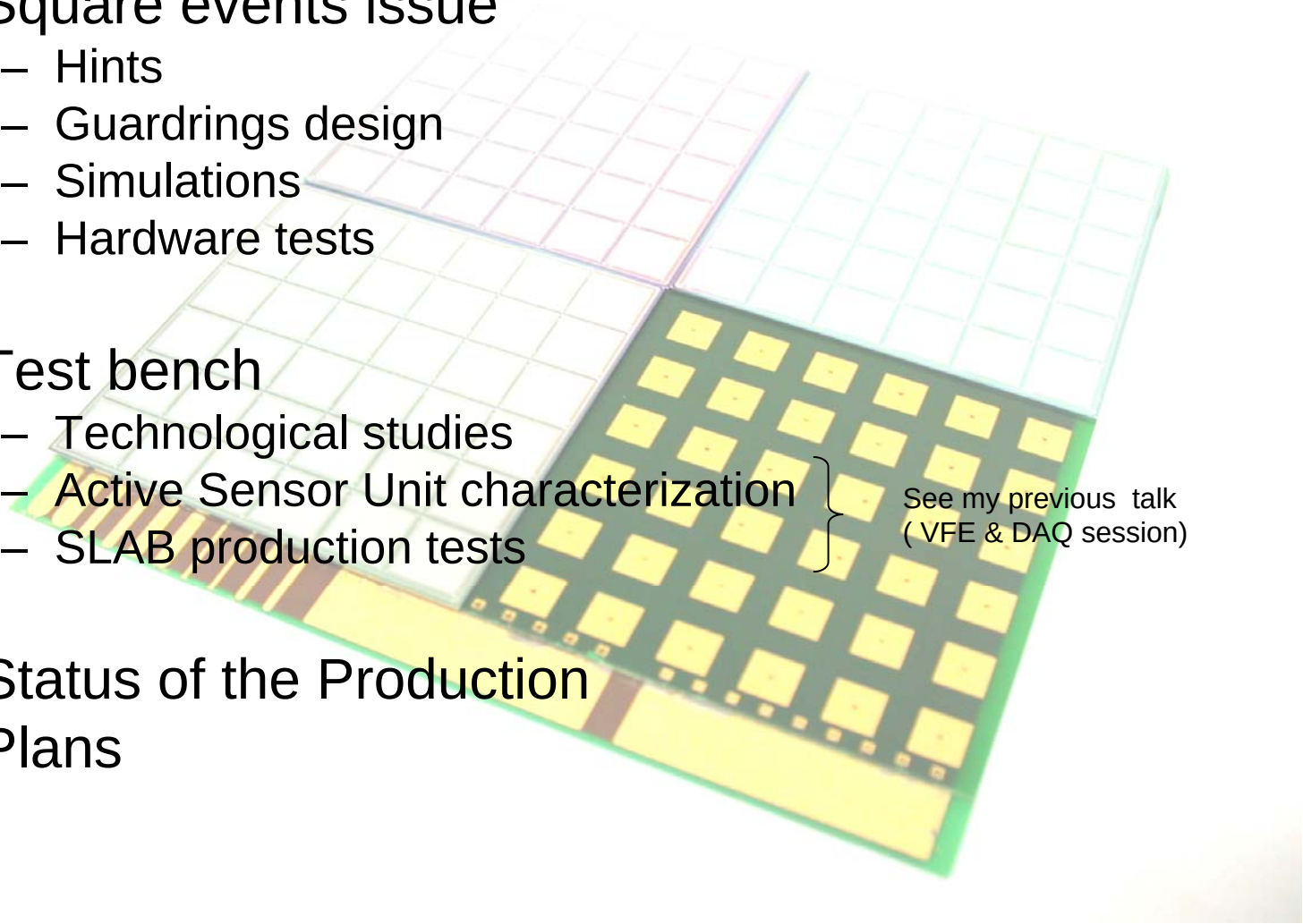
Silicon Wafers for EUDET module design and test bench

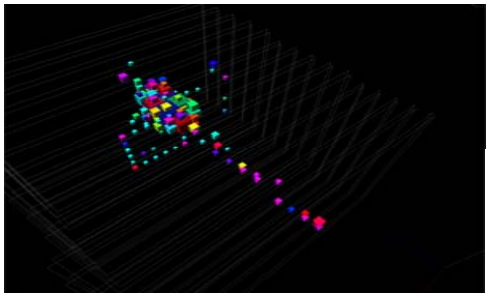
Akli Karar (LLR)
Jean Charles Vanel (LLR)
Rémi Cornat (LPC)
Mustapha Benyamna (LPC)

Overview

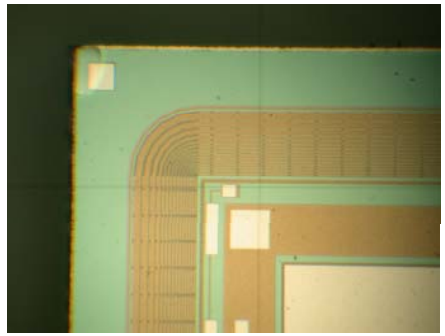
- Square events issue
  - Hints
  - Guardrings design
  - Simulations
  - Hardware tests
- Test bench
  - Technological studies
  - Active Sensor Unit characterization
  - SLAB production tests
- Status of the Production
- Plans



See my previous talk
(VFE & DAQ session)



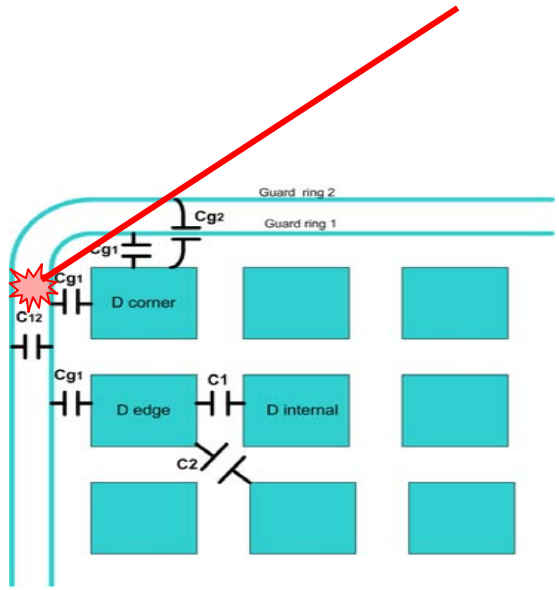
Understand the origin of Square events



Guard-rings are needed to avoid high leakage current at the wafer border…

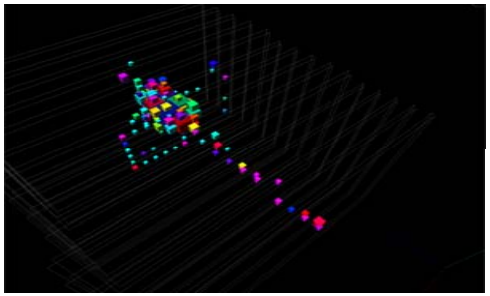
The square shape corresponds to guard-rings location

Effects of a particle hit on guard-rings could be propagated to every bordering pixels



= cross-talk effect

Other source effects ?
Need to check and crosscheck…



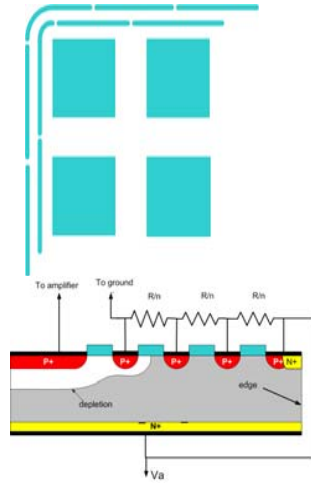
Find a turnaround

Square event issue must be solved

Many possibilities to explore
- Guardring implementation
- Guardring technology
- Others ?

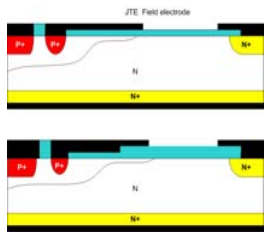
Guardring implementation
- continuous (baseline)
- segmented
- polarized

With various spacing and V

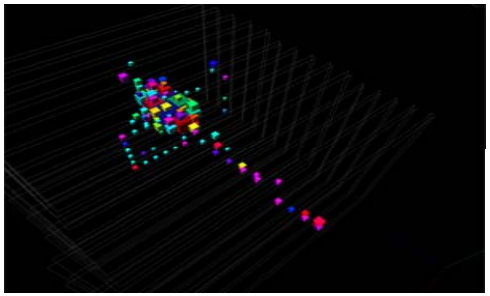


See Akli's talk @ Seoul

Guardring technology
- P+ implant (standard)
- progressive doping
- MOS
- brutal etching
- new ?



Others ?
- Priority given to crosstalk as it is most probable and "easy" to test segmented topology



Crosstalk hypothesis verification

Method

Square event

Understand

Simulation

SILVACO

Guardring design

Splited
Polarized
Progressive

Charge injection

Photon
Electron

Effects on
Leakage
Capacitance

Current flow

SPICE

Pure crosstalk

Electrical level

Try to reproduce the phemenon

Physical Model

Splited guardring impact on pure crosstalk

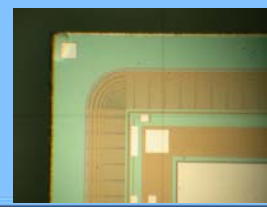
Characterize

Measurment Bench

Samples

Find out best candidate

Test new designs
- layout
- technologic improvements

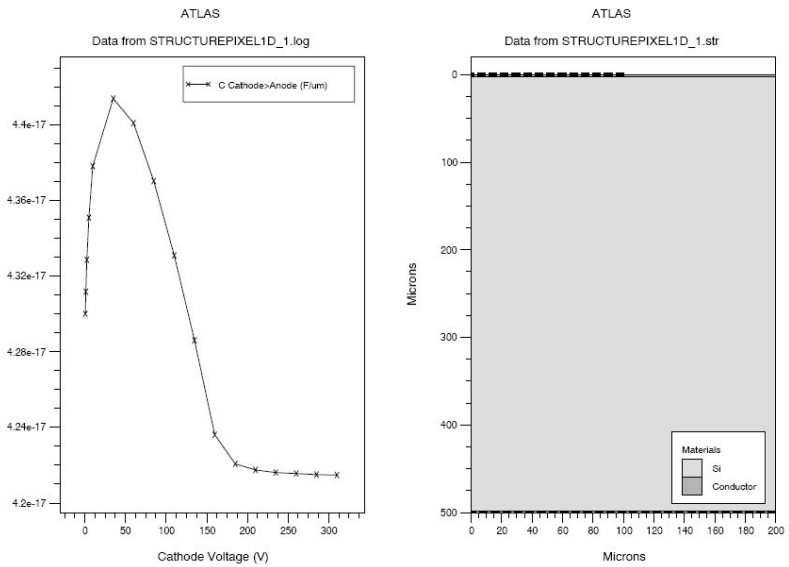


Simulation bench

Cu-Epo "wafer"

Various 3x3 test wafer to be produced by OnSemi
As result, select the best design technique…

Simulations with SILVACO



C(V) between pixel and common bias and C(V,a,b,c,d…)

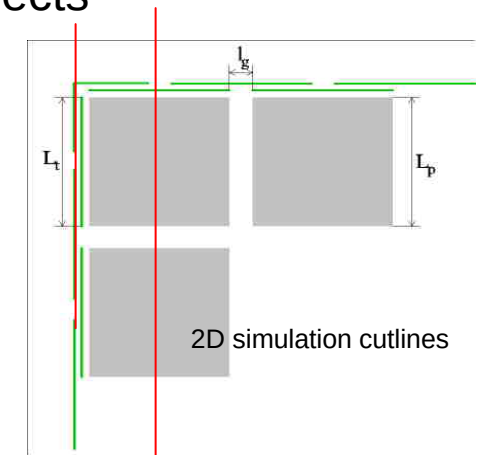
First step to verify capacitance values between pixels, guardrings, substrate

Then back annotate to SPICE simulation

Simulated Cap. Values are within a 20% range from expected values calculated with first order formula

See Akli's talk @ Seoul

3D simulation are ongoing to take into account border effects



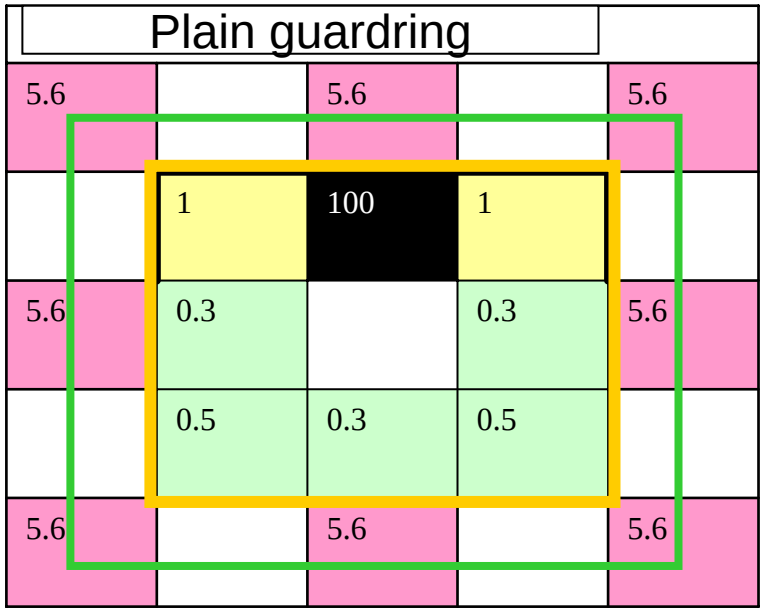
Second step to simulate ionization effects (electron or photon) or SEE/SEU events

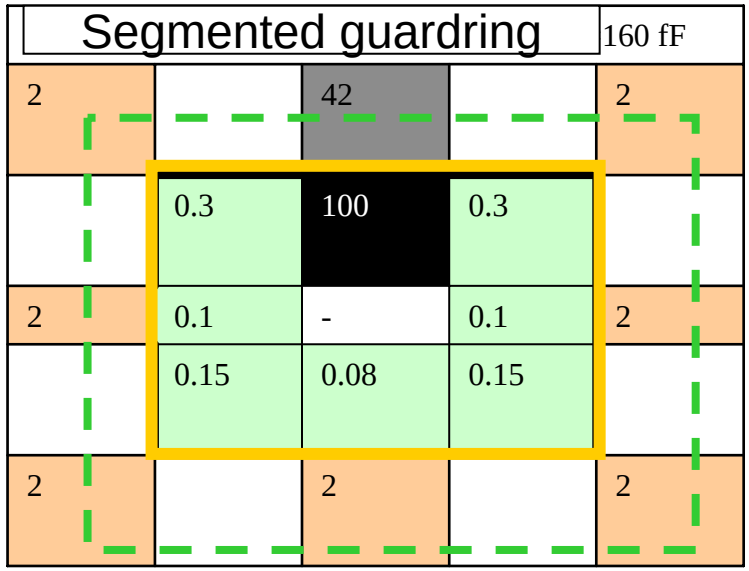
Third step (following months) to evaluate design parameters impact on C and explore new designs of guardrings from crosstalk point of view

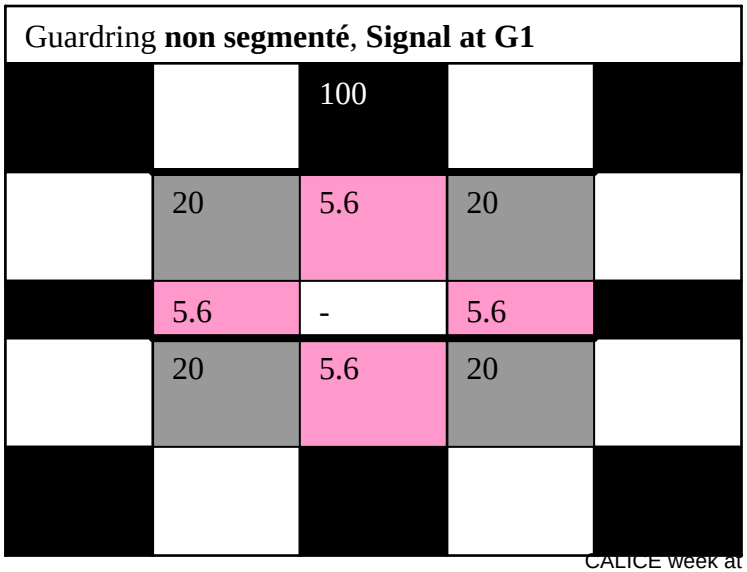
Segmented guard-rings technique may prevent Xtalk by a factor 3

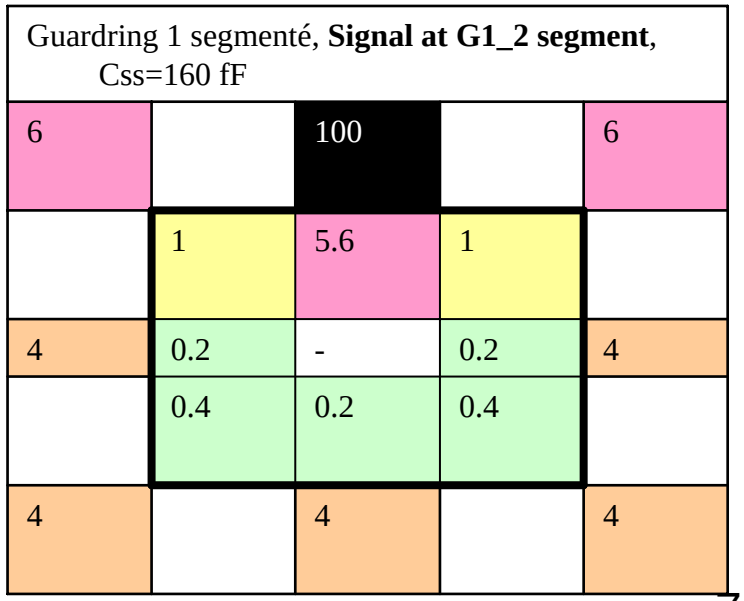
diaphonie pixel – 3x3 matrix
Cgb = 4 pF Cgg=24pF Cpg = 1 pF

Simulations with SPICE

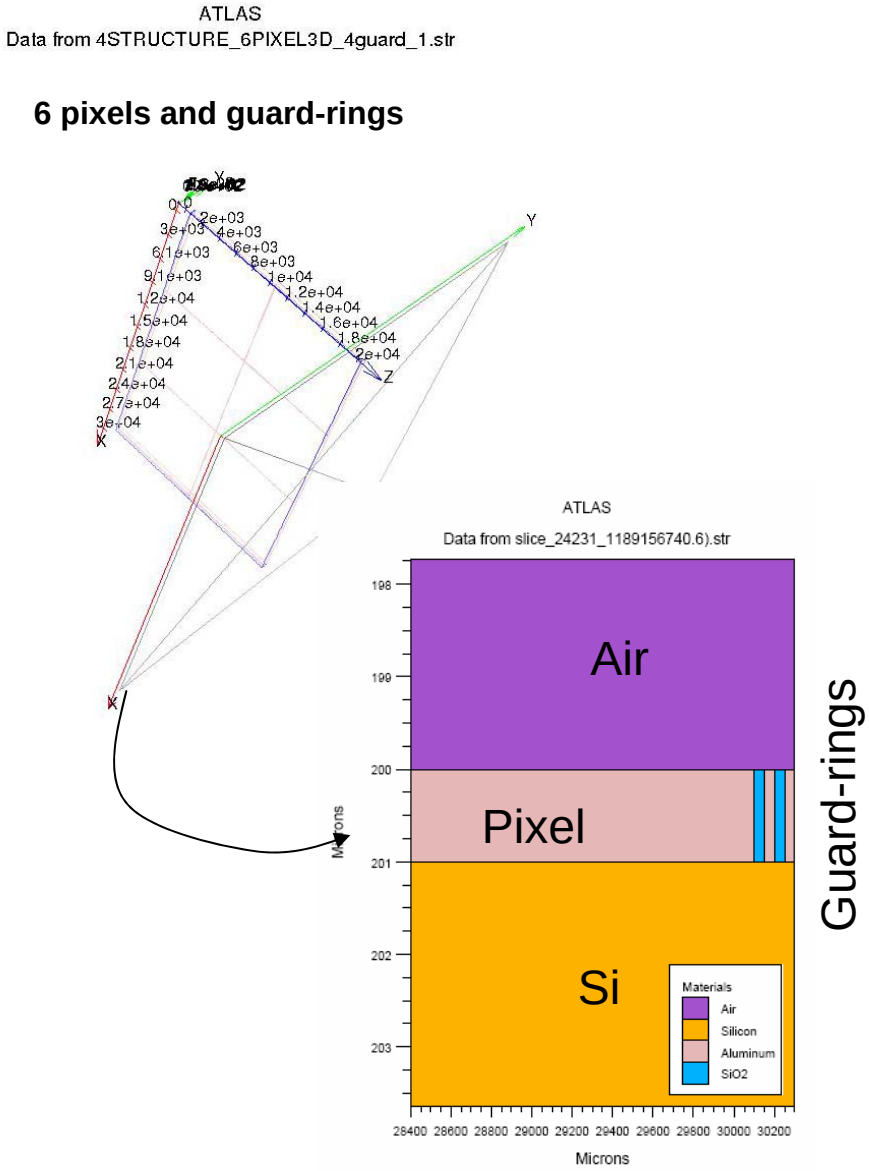








Simulations with SILVACO 3D



3D simulations enabled

3D simulation are ongoing to take into account border effects

3D caps extracted : same range as for 2D

Next steps :

- SPICE simulations with extracted parameters
- radiation induced effect (photon and ionizing particles)

Angle etched wafers
And other techniques

Informations from :

A vertical high voltage termination structure for high-resistivity silicon detectors

Segal, J.D.; Kenney, C.J.; Aw, C.H.; Parker, S.I.; Vilkelis, G.; Iwanczyk, J.S.; Patt, B.E.; Plummer, J.
Nuclear Science Symposium, 1997. IEEE
Volume , Issue , 9-15 Nov 1997 Page(s):299 - 303 vol.1

http://ieeexplore.ieee.org/iel4/5472/14772/00672589.pdf?arnumber=672589

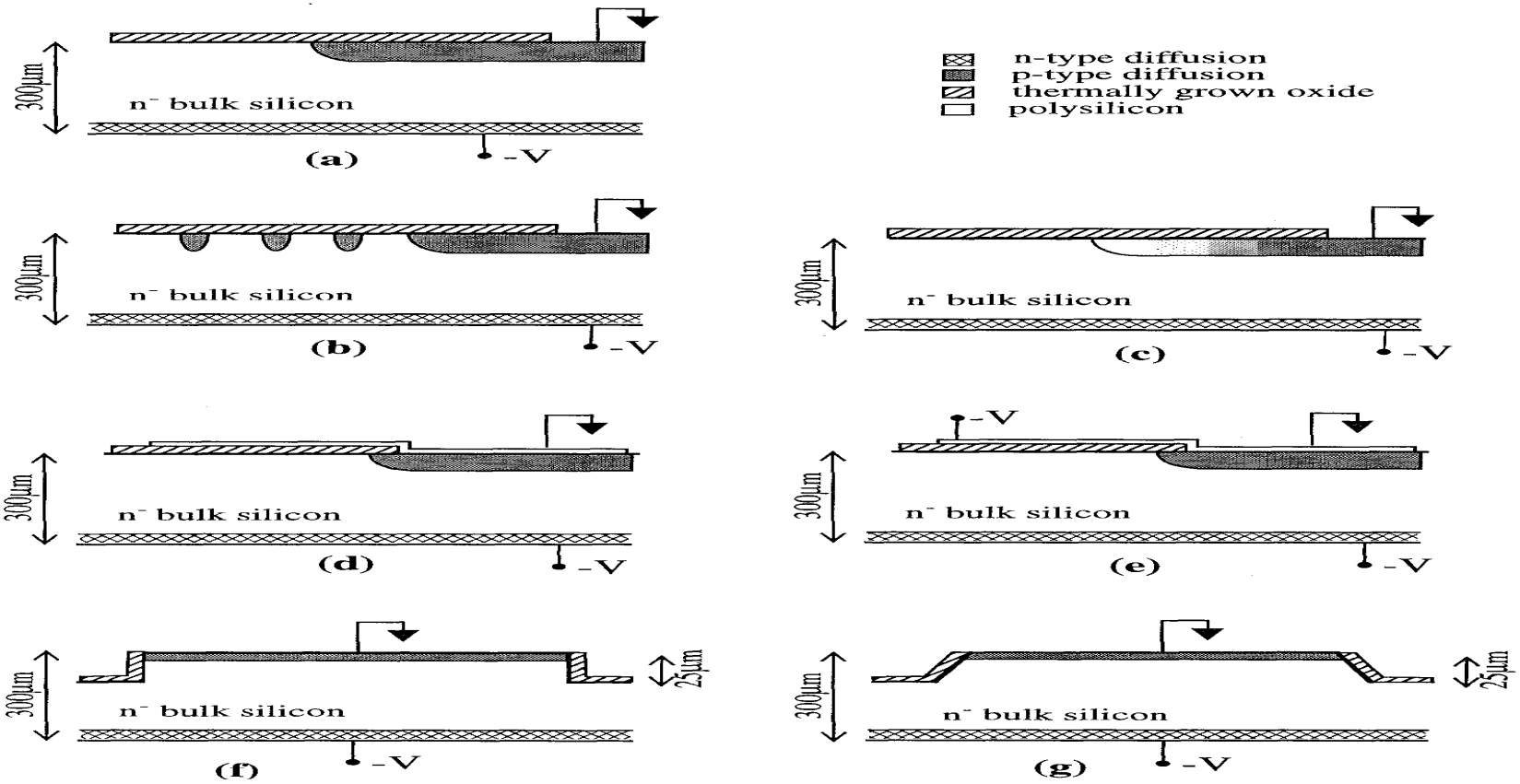


Figure 1 : Simulated diode termination structures in n-type bulk: a) unimproved diffused junction, b) three floating rings c) linearly graded junction in lateral dimension, d) field plate termination, e) field plate with linear potential, f) new one-mask termination with vertical etch g) new one-mask termination with angled etch.

A vertical high voltage termination structure for high-resistivity silicon detectors

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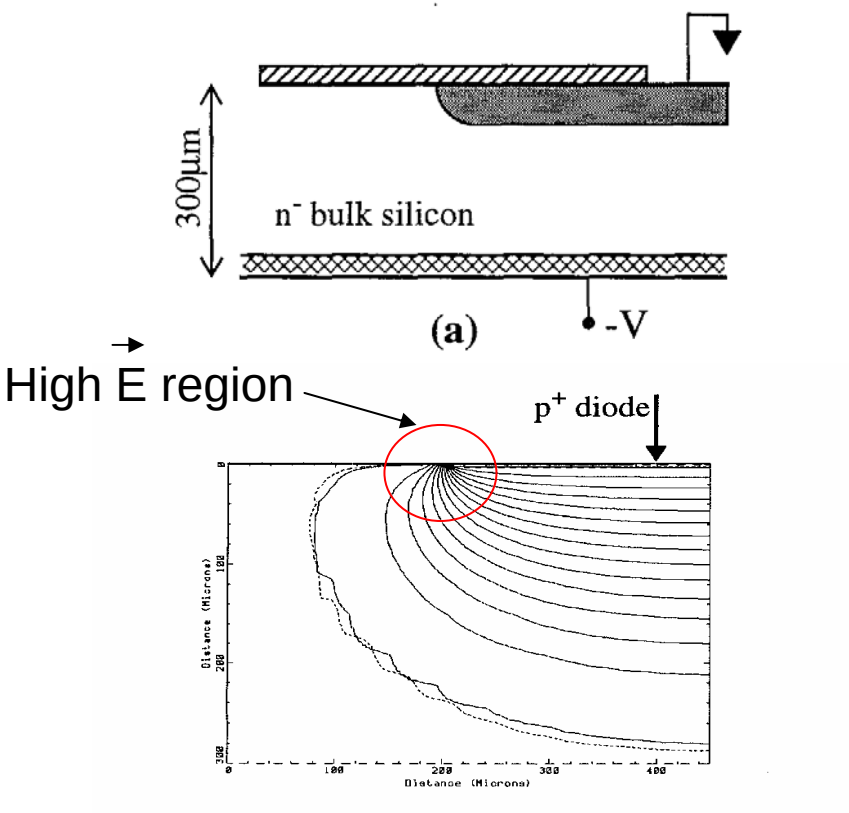
Volume , Issue , 9-15 Nov 1997 Page(s):299 - 303 vol.1

Un-improved junction



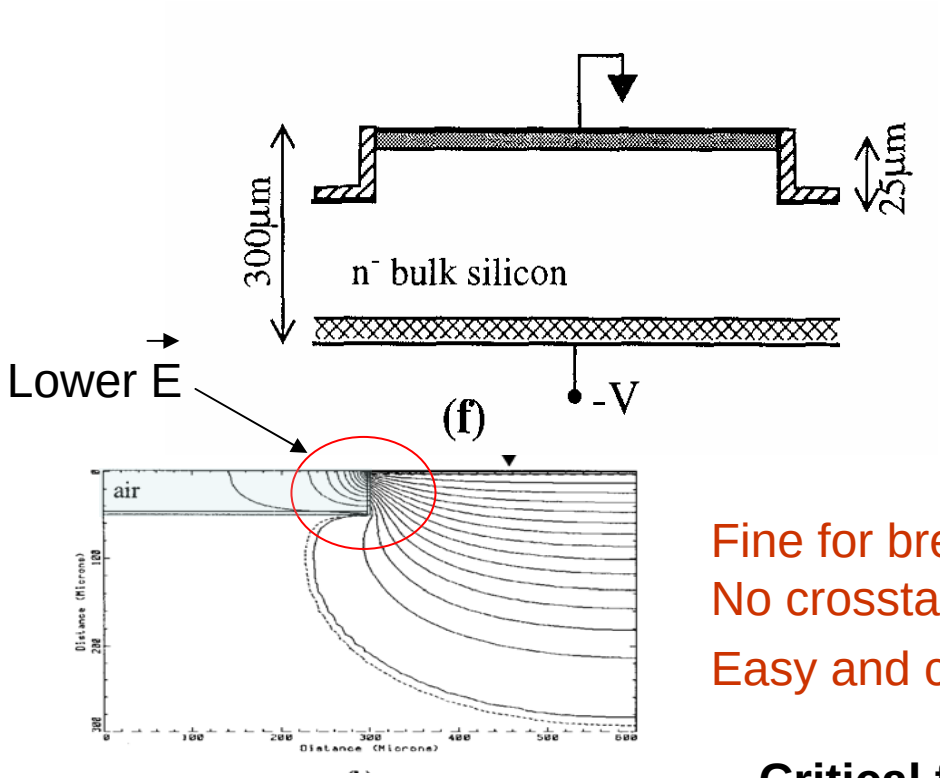
n-type diffusion
p-type diffusion
thermally grown oxide
polysilicon

Critical field at breakdown 2E5 V/cm
(Ref: Semiconductor Devices S.M.SZE)

Table 1: Comparison of high voltage termination structure simulation results for 300µm thick 1e12/cm^3 n-type bulk requiring 70V to deplete, with 2µm deep p-type junction,

junction termination structure	peak electric field for Q_f=0	peak electric field for Q_f=1e11/cm^2
un-improved diode	3.9E4 V/cm	8.0E4 V/cm

Vertical etch termination



Fine for breakdown = guard-ring replacement
No crosstalk due to guard-ring – pixel cap.
Easy and cost effective

Critical field at breakdown 2E5 V/cm
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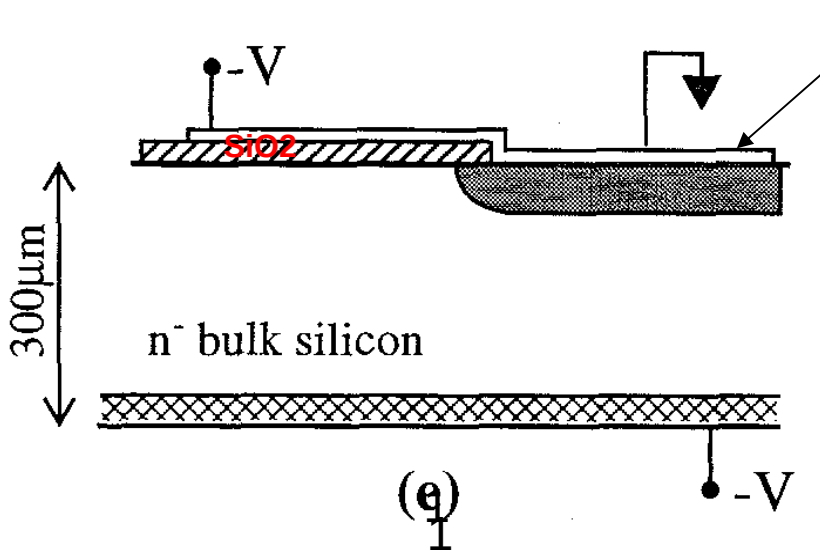
junction termination structure	peak electric field for Q_f=0	peak electric field for Q_f=1e11/cm^2
vertical etch junction termination	2.0E4 V/cm	4.7E4 V/cm



Very good but needs bias voltage

Critical field at breakdown 2E5 V/cm

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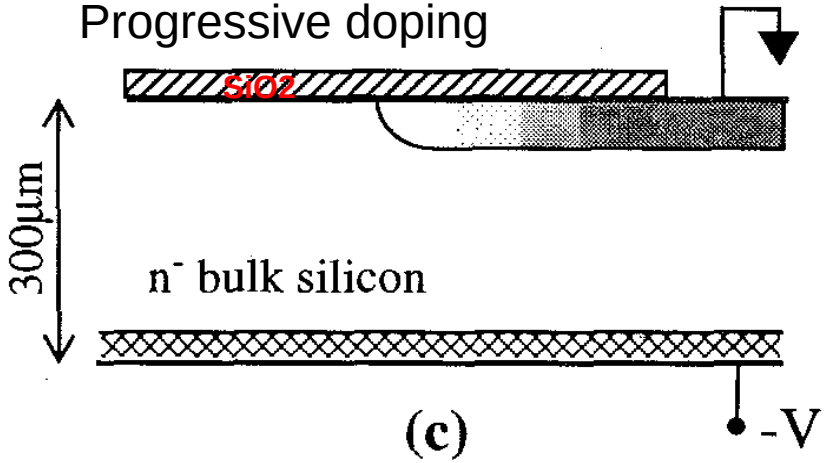

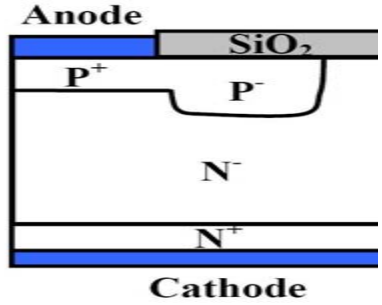

junction termination structure		peak electric field for Q_f=0	peak electric field for Q_f=1e11/cm^2
poly field plate extension (with linear voltage gradient)	(e)	0.8E4 V/cm	1.0E4 V/cm
linear implant gradient	(c)	1.5E4 V/cm	2.3E4 V/cm

Courtesy of Akli Karar (LLR)

Table 1: Comparison of high voltage termination structure simulation results for 300µm thick 1e12/cm^3 n-type bulk requiring 70V to deplete, with 2µm deep p-type junction,

junction termination structure	peak electric field for Q_f=0	peak electric field for Q_f=1e11/cm^2
un-improved diode	3.9E4 V/cm	8.0E4 V/cm
three floating rings (optimized) But square events	1.3E4 V/cm	3.1E4 V/cm
poly field plate extension (at uniform bias)	2.8E4 V/cm	5.8E4 V/vm
poly field plate extension (with linear voltage gradient)	0.8E4 V/cm	1.0E4 V/cm
linear implant gradient	1.5E4 V/cm	2.3E4 V/cm
vertical etch junction termination	2.0E4 V/cm	4.7E4 V/cm
angled etch junction termination	2.5E4 V/cm	6.0E4 V/cm

Critical field at breakdown 2E5 V/cm *(Ref: Semiconductor Devices S.M.SZE)*

A vertical high voltage termination structure for high-resistivity silicon detectors

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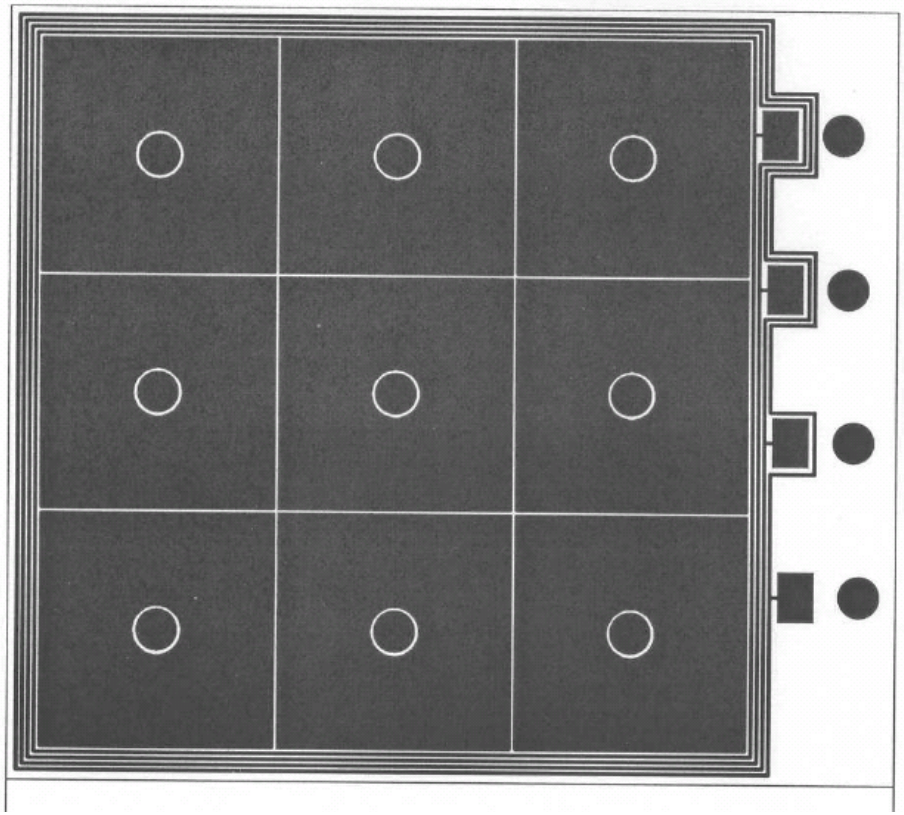
Nuclear Science Symposium, 1997. IEEE
Volume , Issue , 9-15 Nov 1997 Page(s):299 - 303 vol.1

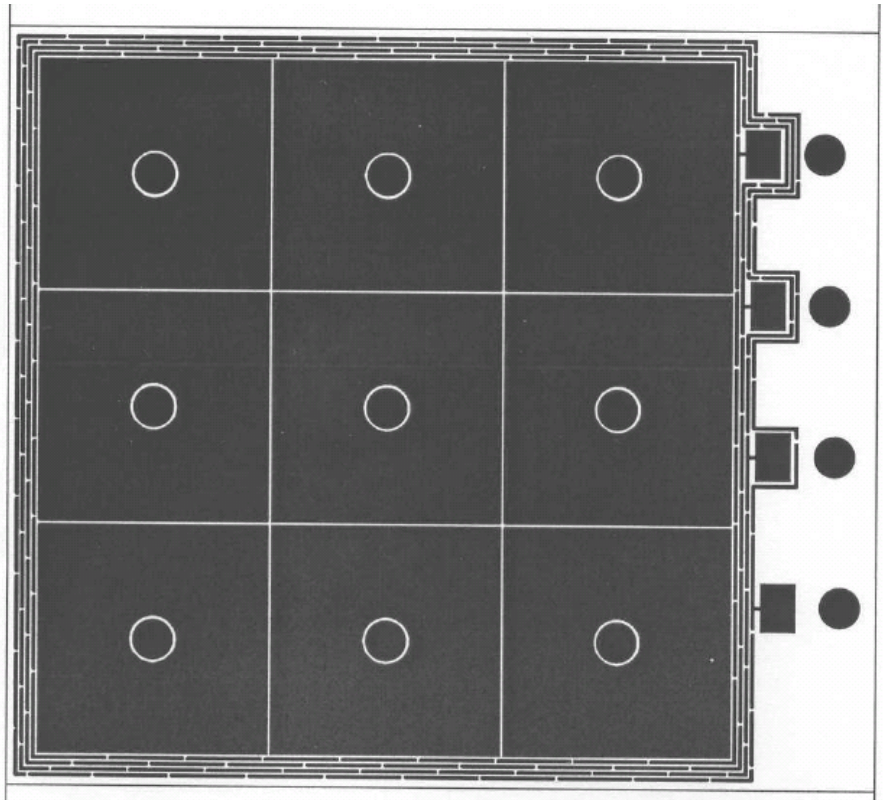
All these techniques can be simulated in accordance with ECAL wafer characteristics

Physical Model : Cu-Epoxy

- Study pure crosstalk effects (various configurations)
- Measurement method validation
- Test bench calibration



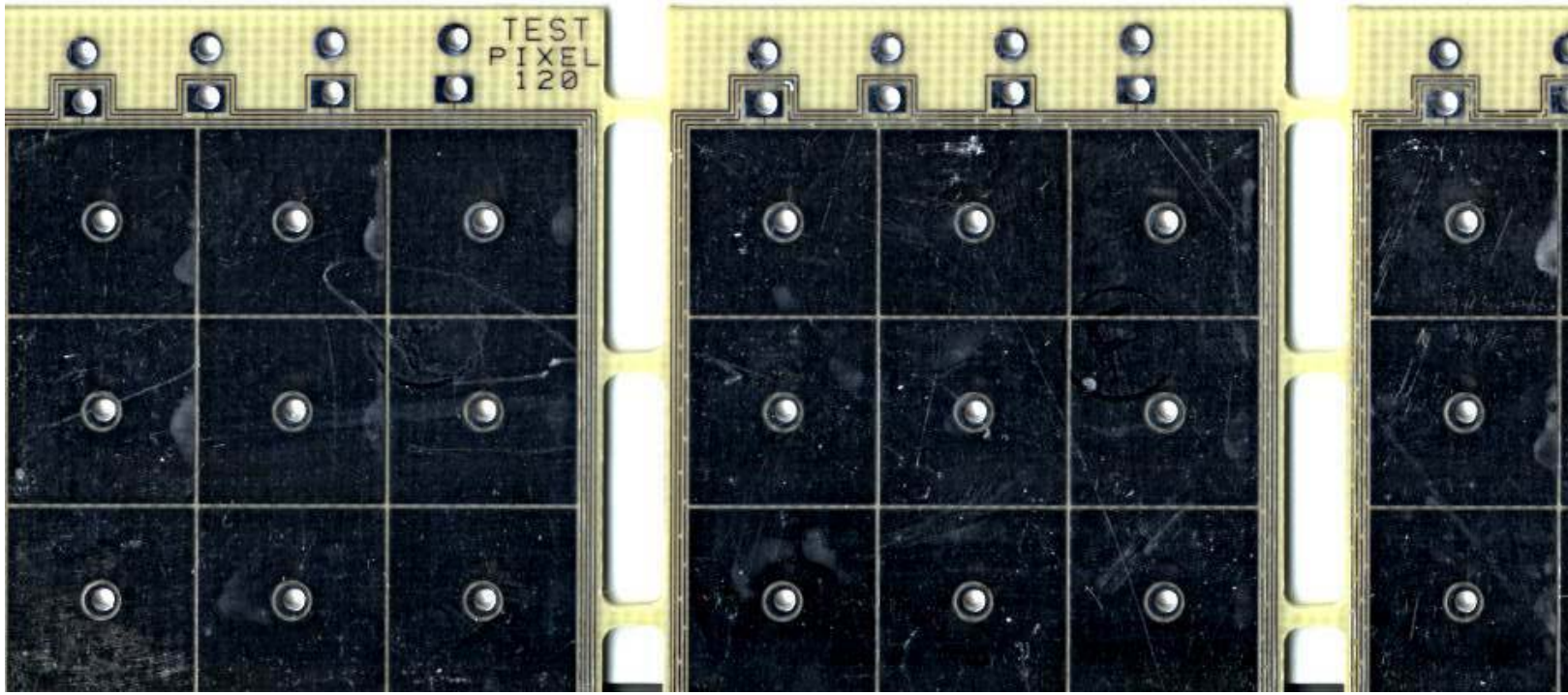
Continuous guardring

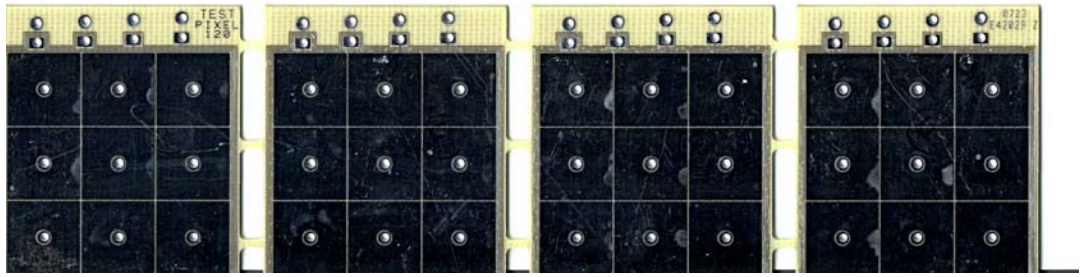


Splited guardring

- 4 @ 1 cm
- 4 @ 3 mm
- 2 @ 1 cm + 2 unsplited

Physical Model : Cu-Epoxy

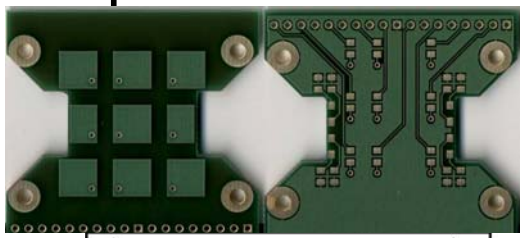


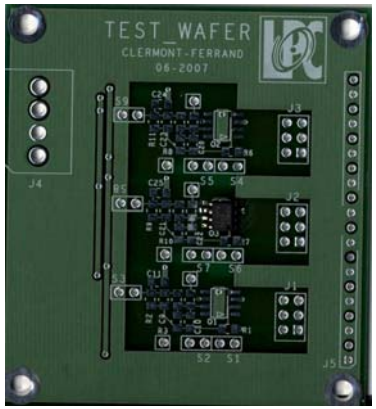


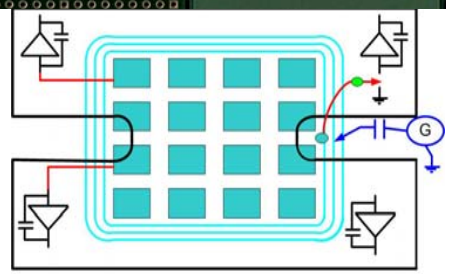
Hardware Test bench

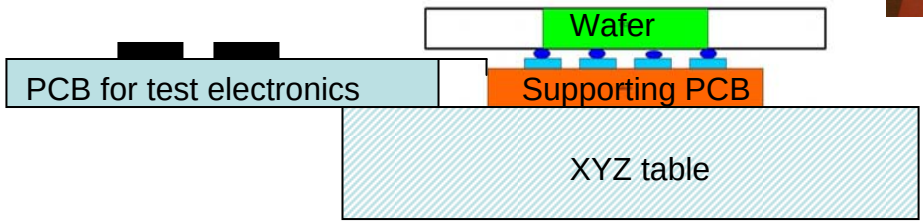
Setup and tools

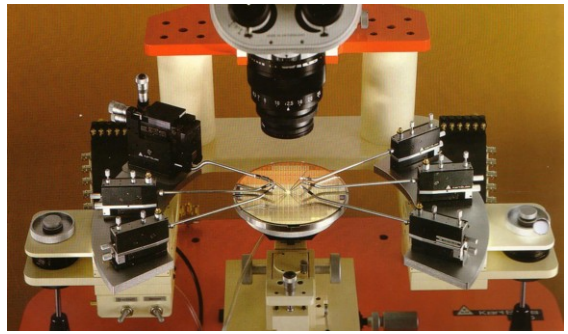
- pulse generator
- micropositioner & probes
- shaper + scope











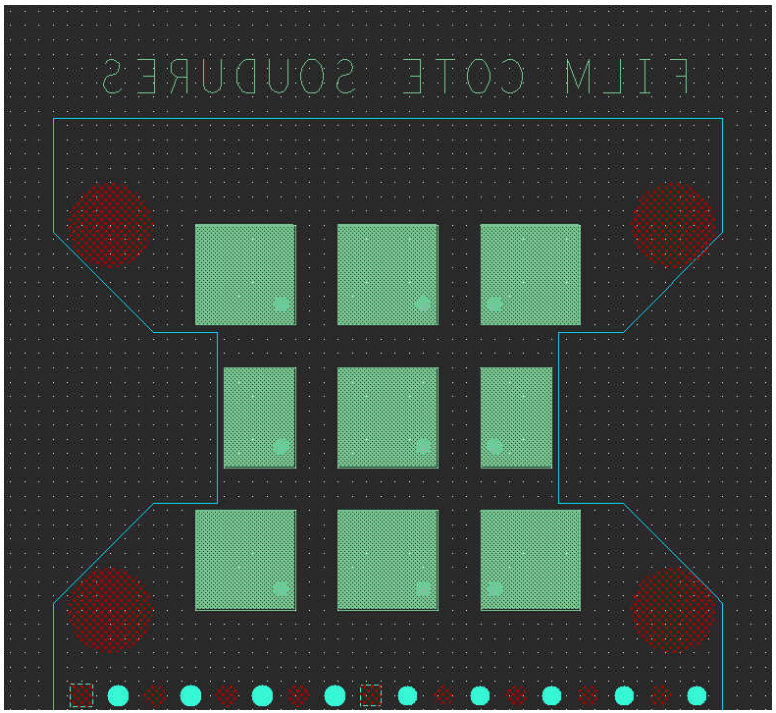
Characterization
- Charge injection
- pixel signal analysis

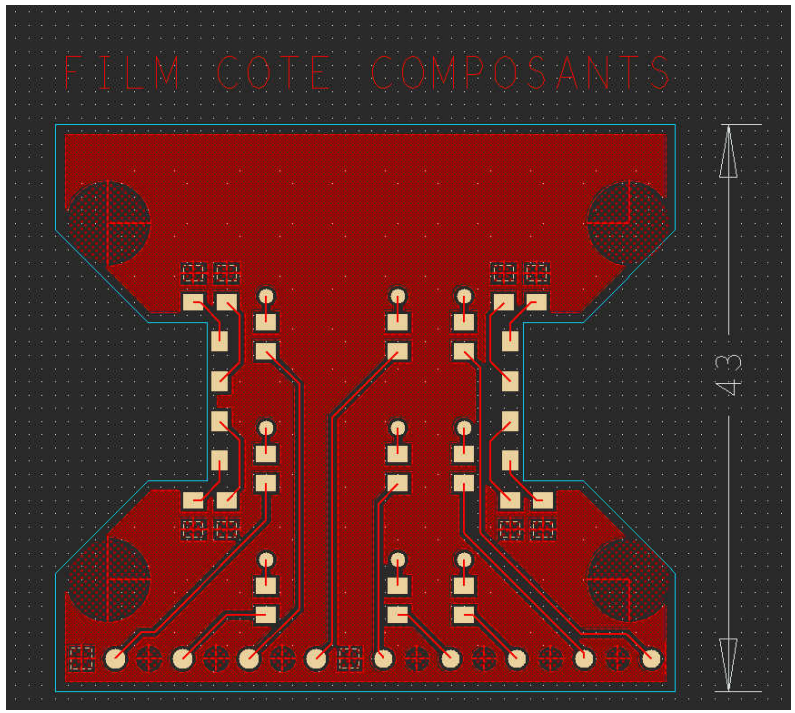
Includes 3 OPA (OPA380 or OPA657) for signal shaping and transimpedance adaptation to a scope

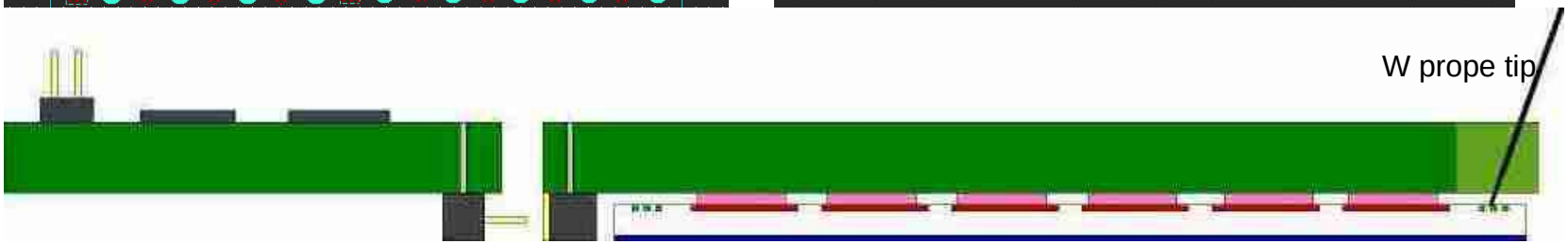
Nd:YAG laser could be used to inject signal (or by simulations)

PCB to glue 3x3 test wafers

Allows bounding of guard-rings
Access to each pixel







Pedestal drift

In case of a huge signal occurs, the pedestals of every pixels of the same wafer drift

Hint : common impedance on high voltage bias
- Glue
- Contact
- Resistivity N+ doped region

Additional issue to study…

Wafer Production Status

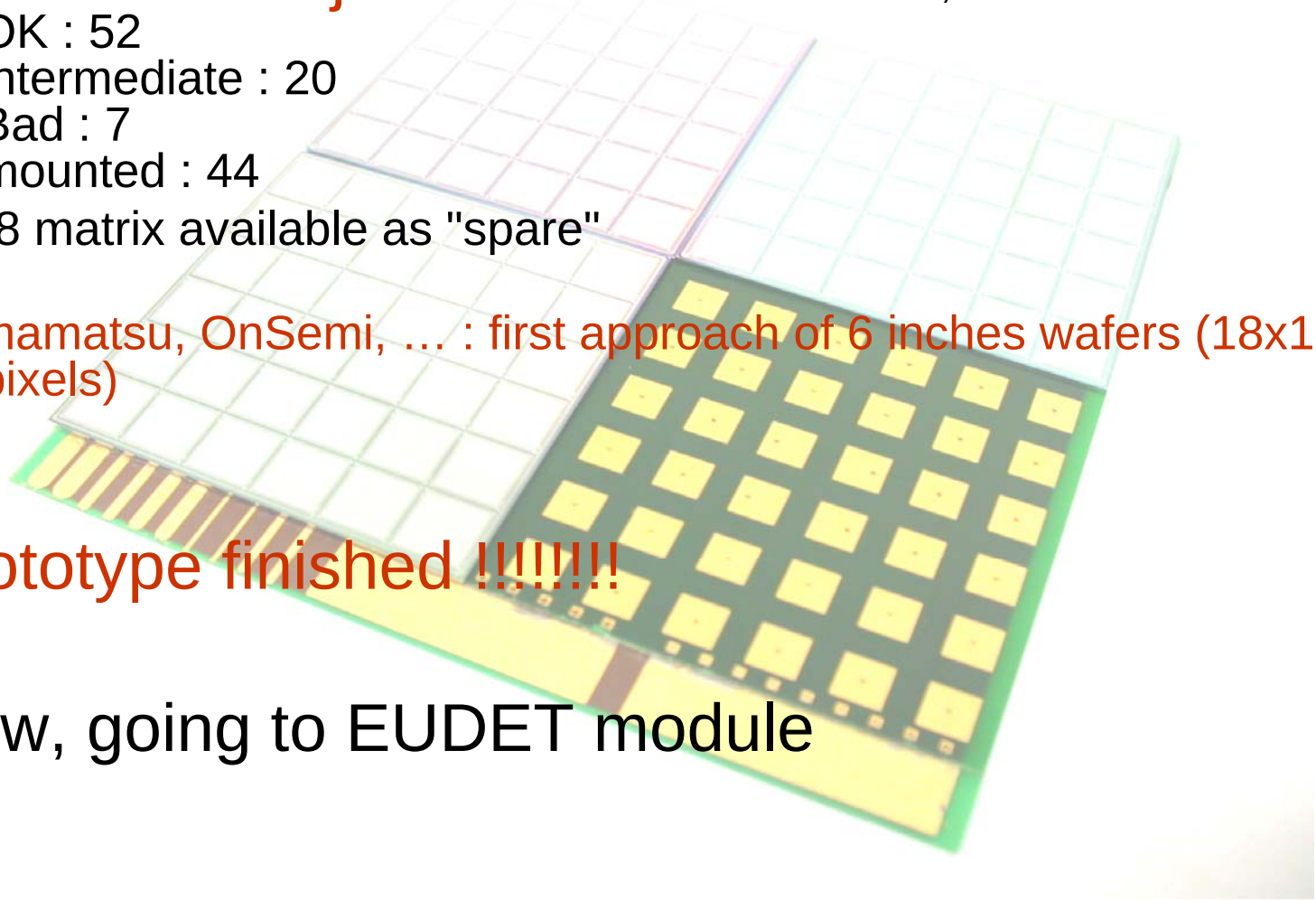
Jean-Charles Vanel (LLR)

Production of june'07 : Total of 79 matrix, tested at LLR

OK : 52
intermediate : 20
Bad : 7
mounted : 44

28 matrix available as "spare"

Hamamatsu, OnSemi, … : first approach of 6 inches wafers (18x18 pixels)



Prototype finished !!!!!!!

Now, going to EUDET module

Plans & Conclusion

Visit to OnSemi (Roznov) this Friday

- 3x3 wafers specs and manufacturing

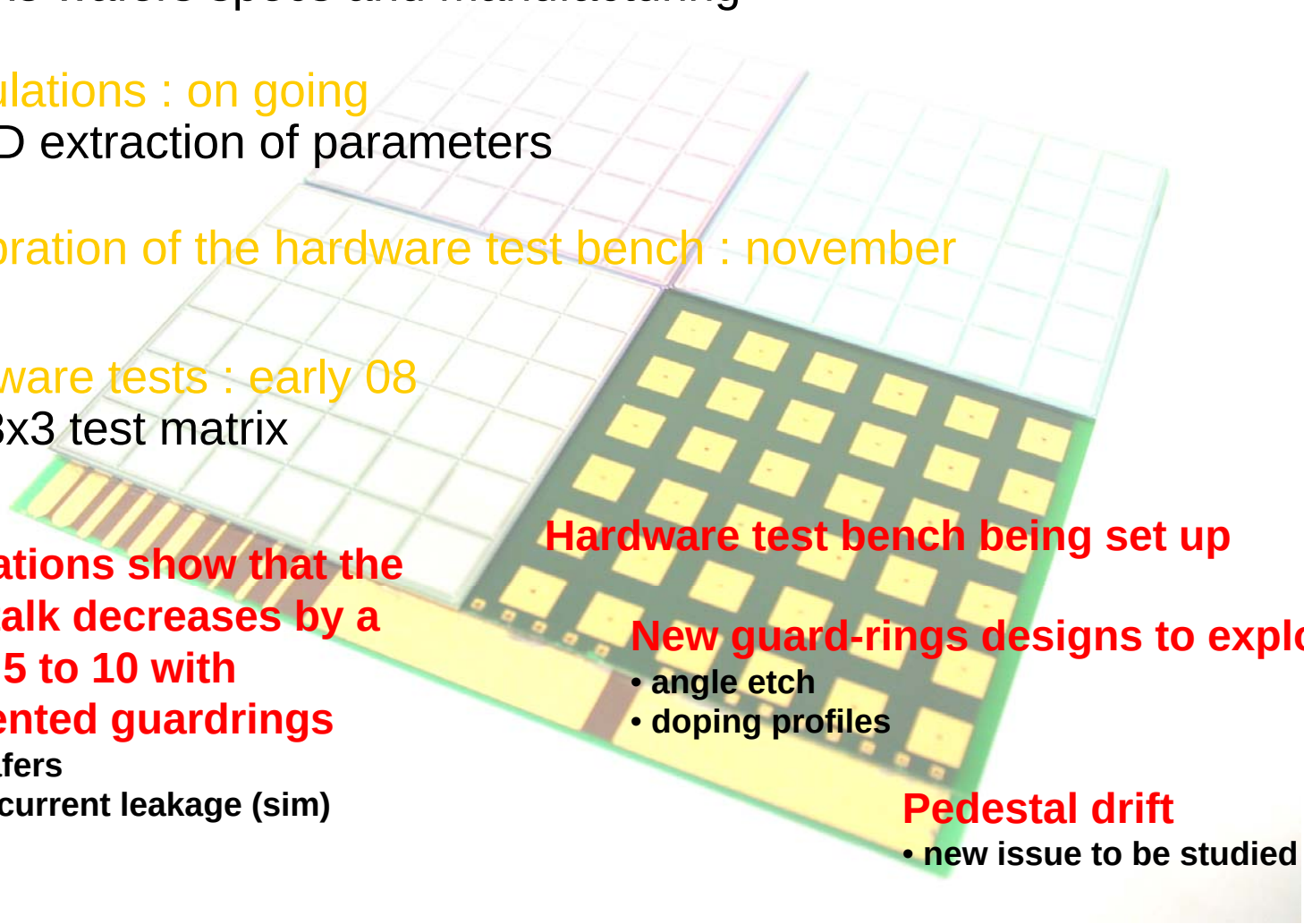
Simulations : on going

- 3D extraction of parameters

Calibration of the hardware test bench : november

Harware tests : early 08

- 3x3 test matrix



Simulations show that the crosstalk decreases by a factor 5 to 10 with segmented guardrings

- **3x3 wafers**
- **check current leakage (sim)**

Hardware test bench being set up

New guard-rings designs to explore

- **angle etch**
- **doping profiles**

Pedestal drift

- **new issue to be studied**