Digital HCAL Electronics Current Status & Plans

Gary Drake

Argonne National Laboratory

CALICE Collaboration Meeting

Prague, Czech Republic

Sept. 12, 2007

Representing the Work of Our DHCAL Group:

John Butler, BU
Tim Cundiff, ANL
Vic Guarino, ANL
Bill Haberichter, ANL
Eric Hazen, BU
Jim Hoff, FNAL
Scott Holm, FNAL
Jia Li, UTA
Andrew Kreps, ANL

Ed May, ANL
G. Mavromanolakis, FNAL
Ed Norbeck, Iowa
José Repond, ANL
Shouxiang Wu, BU
Lei Xia, ANL
Dave Underwood, ANL
Andy White, UTA
Ken Wood, FNAL
Jae Yu, UTA

BOLD = Electronics Design Contributions
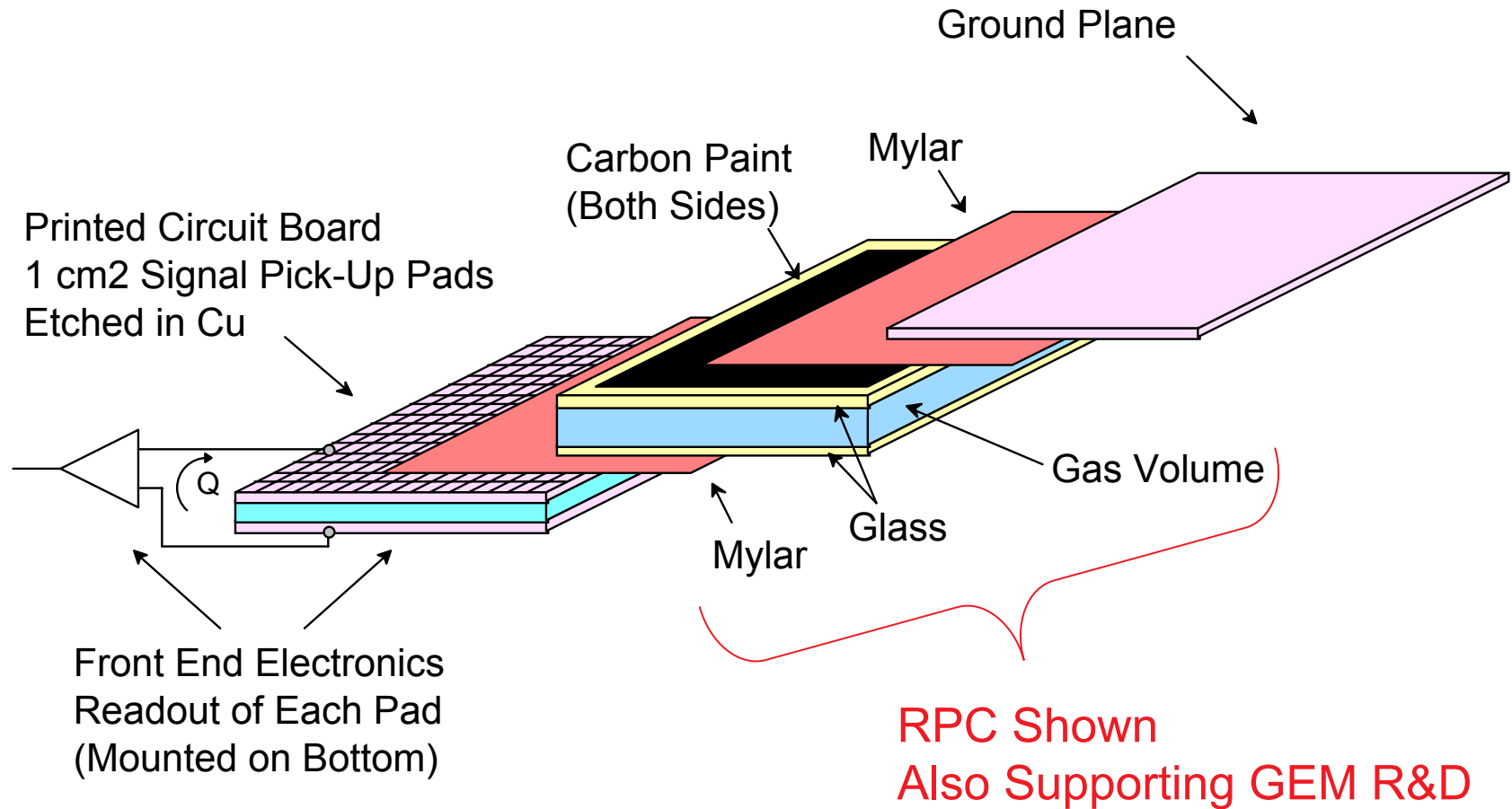
The Goals of our R&D Program:

- **To measure hadronic showers using a "fine-grain" detector having 1-bit resolution → *"Digital Calorimetry"***

- **To use these measurements in the development of Particle-Flow Algorithms**
  - **How well do current simulations work?**
  - **Provide a physical measurement basis for current and future simulations**
  - **Caveat: Can't do full PFAs without Tracking, But can get single particle profiles**

- **To develop detector technologies suitable for PFAs and the ILC → RPCs & GEMs**

- **To begin to develop instrumentation techniques suitable for this approach**

We are NOT developing instrumentation for a real ILC detector

We are NOT trying to solve all of the problems & issues associated with instrumenting and building a real ILC detector
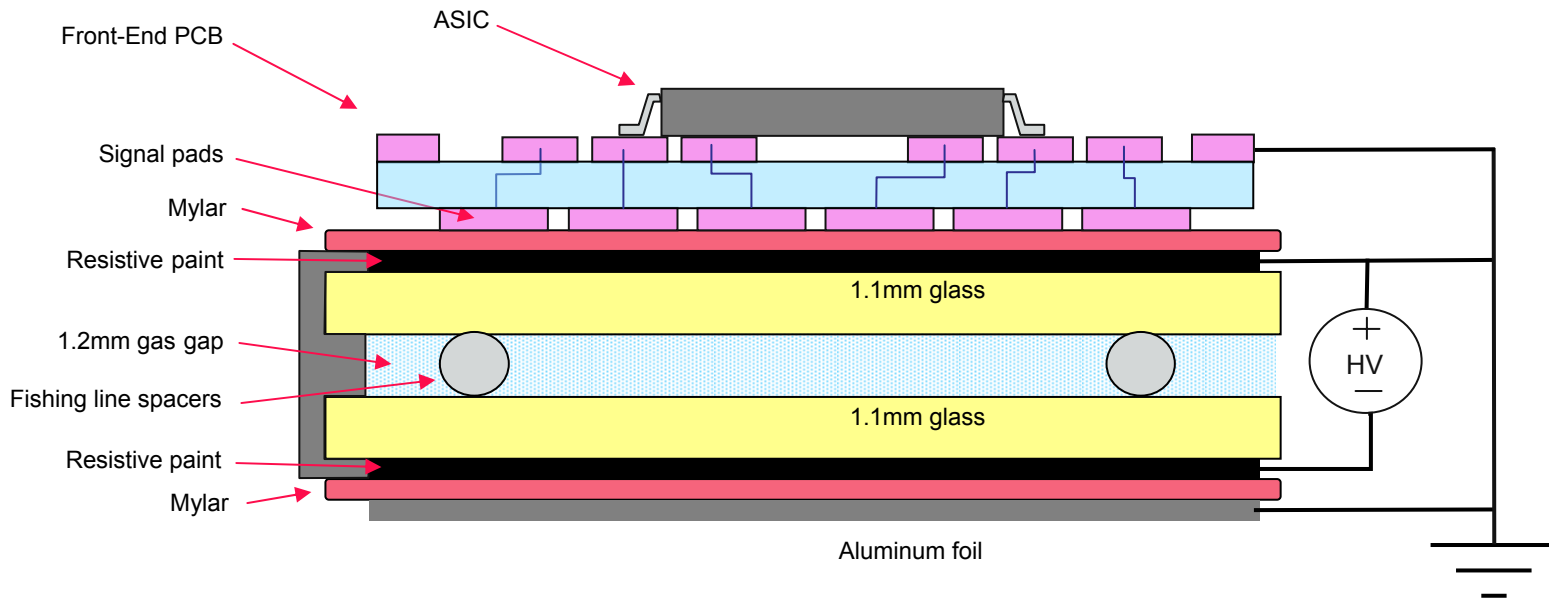
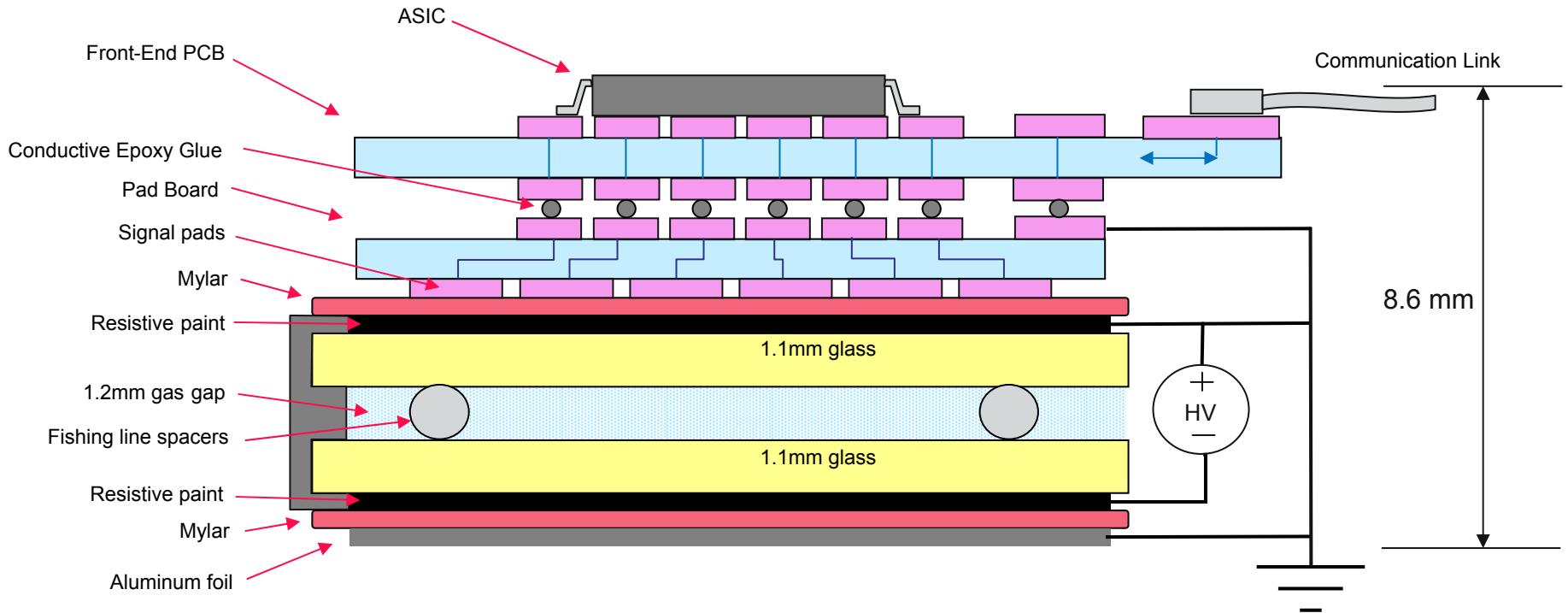*We ARE forming a basis for future developments in Digital Hadron Calorimetry*

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Detector Configuration

Ground Plane

Carbon Paint
(Both Sides)

Mylar

Printed Circuit Board
1 cm2 Signal Pick-Up Pads
Etched in Cu

Q

Gas Volume

Glass

Mylar

Front End Electronics
Readout of Each Pad
(Mounted on Bottom)

RPC Shown
Also Supporting GEM R&D

Detector Configuration

Original Conception (RPC Shown):

Front-End PCB

ASIC

Signal pads

Mylar

Resistive paint

1.1mm glass

1.2mm gas gap

Fishing line spacers

1.1mm glass

Resistive paint

Mylar

Aluminum foil

HV

Detector Configuration

Current Construction:

Labels (left side):
- ASIC
- Front-End PCB
- Conductive Epoxy Glue
- Pad Board
- Signal pads
- Mylar
- Resistive paint
- 1.2mm gas gap
- Fishing line spacers
- Resistive paint
- Mylar
- Aluminum foil

Labels (in diagram):
- Communication Link
- 8.6 mm
- 1.1mm glass
- 1.1mm glass
- HV

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General System Specifications & Design Decisions

- Front-end instrumentation to use 64-channel custom ASIC
  - 1 cm^2 pads, 1 meter^2 planes, 40 planes, → ***400,000 channels***
- Front-end channel consists of amplifier/shaper/discriminator
- ***Single programmable threshold*** → 1 bit dynamic range
  - DAC has 8-bit range
  - Common threshold per ASIC
- ***2 gain ranges***
  - High gain for GEMs (20 fC - ~200 fC signals)
  - Low gain for RPCs (100 fC - ~10 pC signals)
- 100 nSec time resolution
- ***Timestamp each hit***
  - 1 second dynamic range → 24 bits @ 100 nSec
  - Synchronize timestamps over system
- ***Data from FE consists of hit pattern in ASIC + timestamp***
  - 24 bit timestamp + 64 hit bits = 88 bits (+ address, error bits, etc.)

General System Specifications & Design Decisions (Continued)

- Capability for *Self Triggering* → Noise, Cosmic rays
- Capability for External Triggering → Primary method for beam events
  - 20-stage pipeline → 2 μSec latency @ 100 nSec
- Capability of FE to source prompt Trigger Bit (simple OR of all disc.)
- Capability to store up to 8 triggers in ASIC output buffer (FIFO)
- Design for 100 Hz (Ext. Trig) nominal rate
- ***Deadtimeless Readout***
- Zero-suppression implemented in front-end
- Time-sorting of data implemented in VME readout
- On-board charge injection with programmable DAC
- Design for 10% occupancy
- Concatenate data in front-ends
- Use serial communication protocols
- Slow controls separate from data output stream
- Compatibility with CALICE DAQ

System Block Diagram
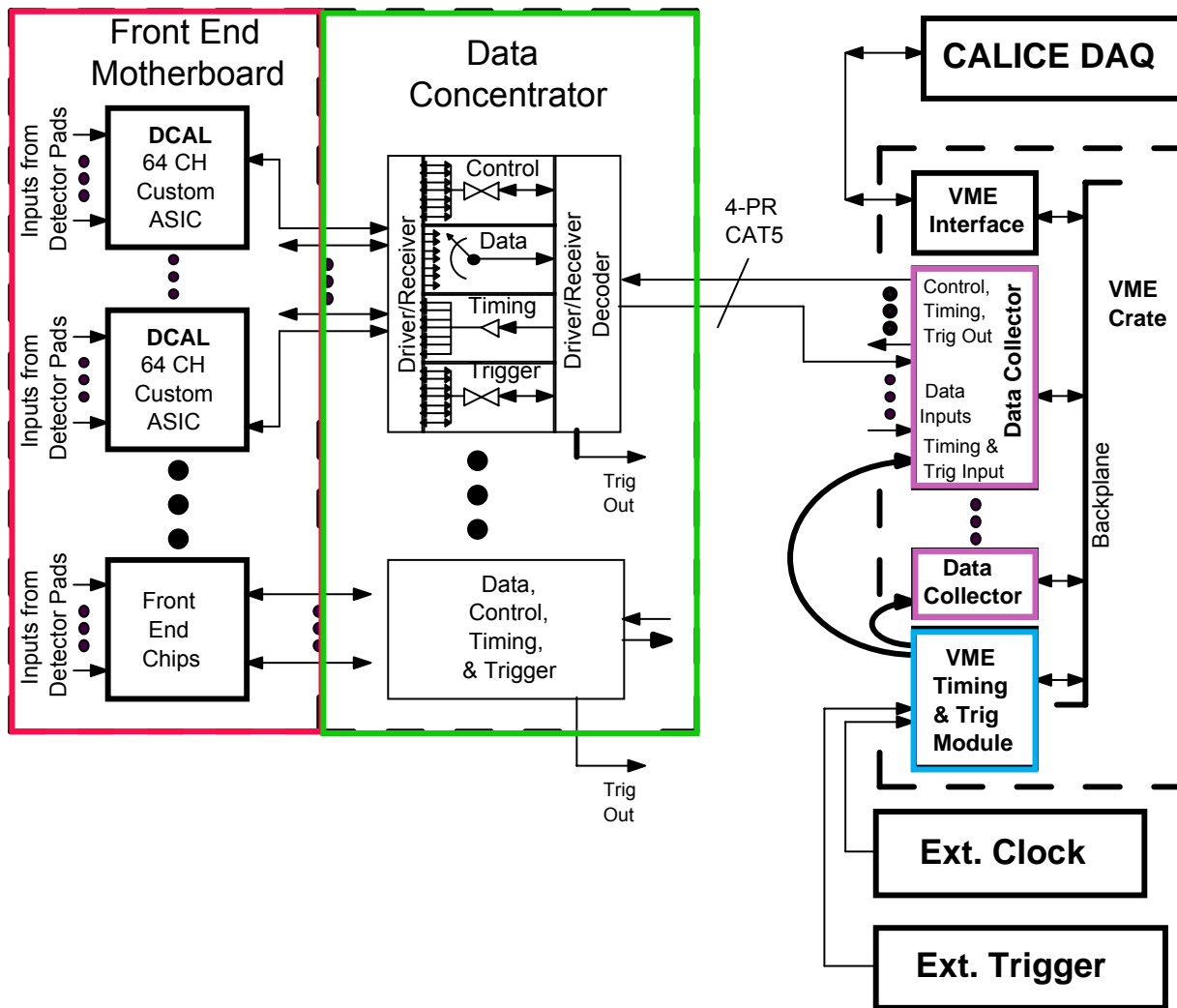
System Physical Implementation

Communication Link

Data Concentrators

VME Interface

Data Collectors

GPS IN

Ext. Trig In

To PC

6U VME Crate

Timing Module

Chambers – 3 per plane

Front End Board with DCAL Chips

Data Concentrators

Square Meter Plane
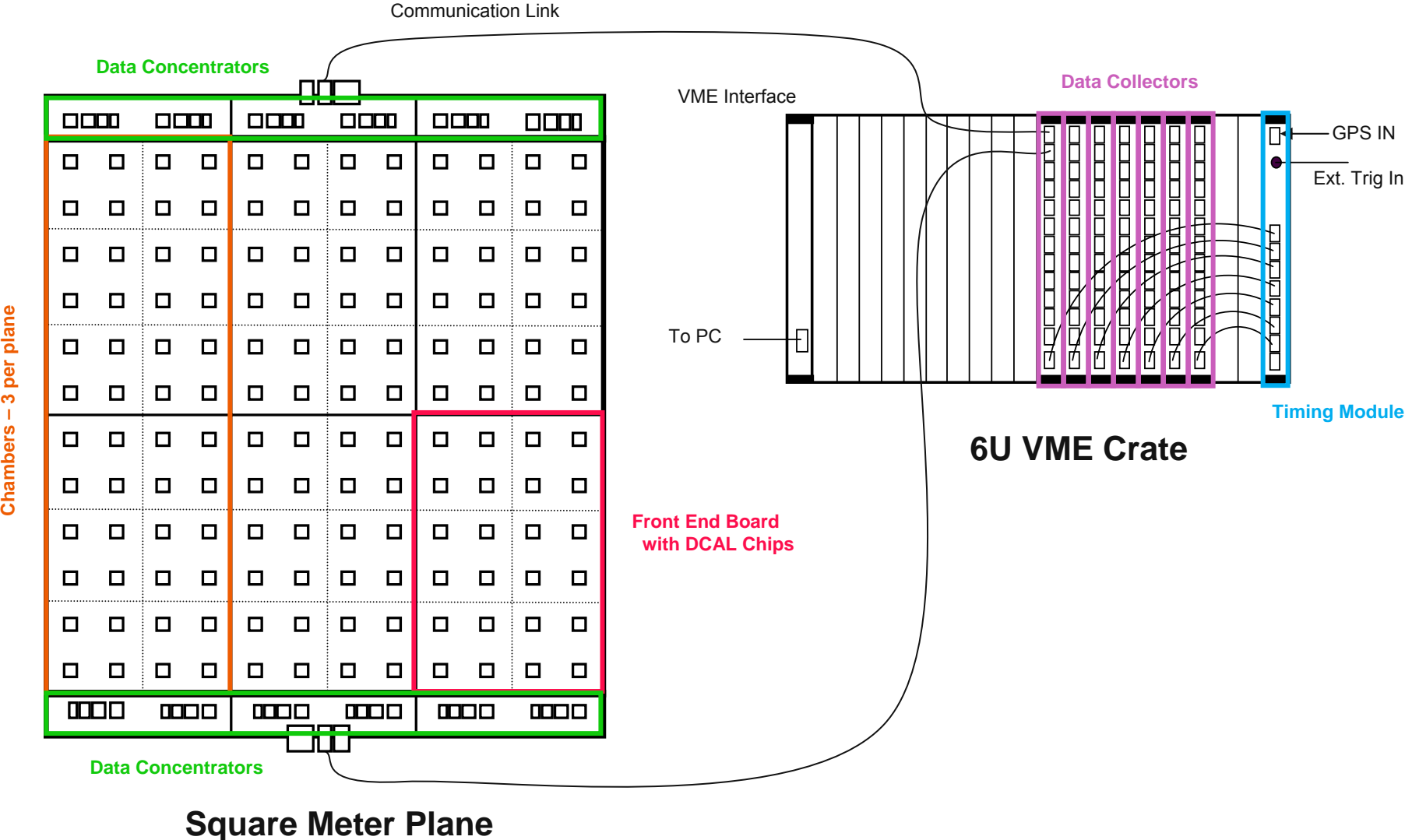
Block Diagram of the DCAL ASIC
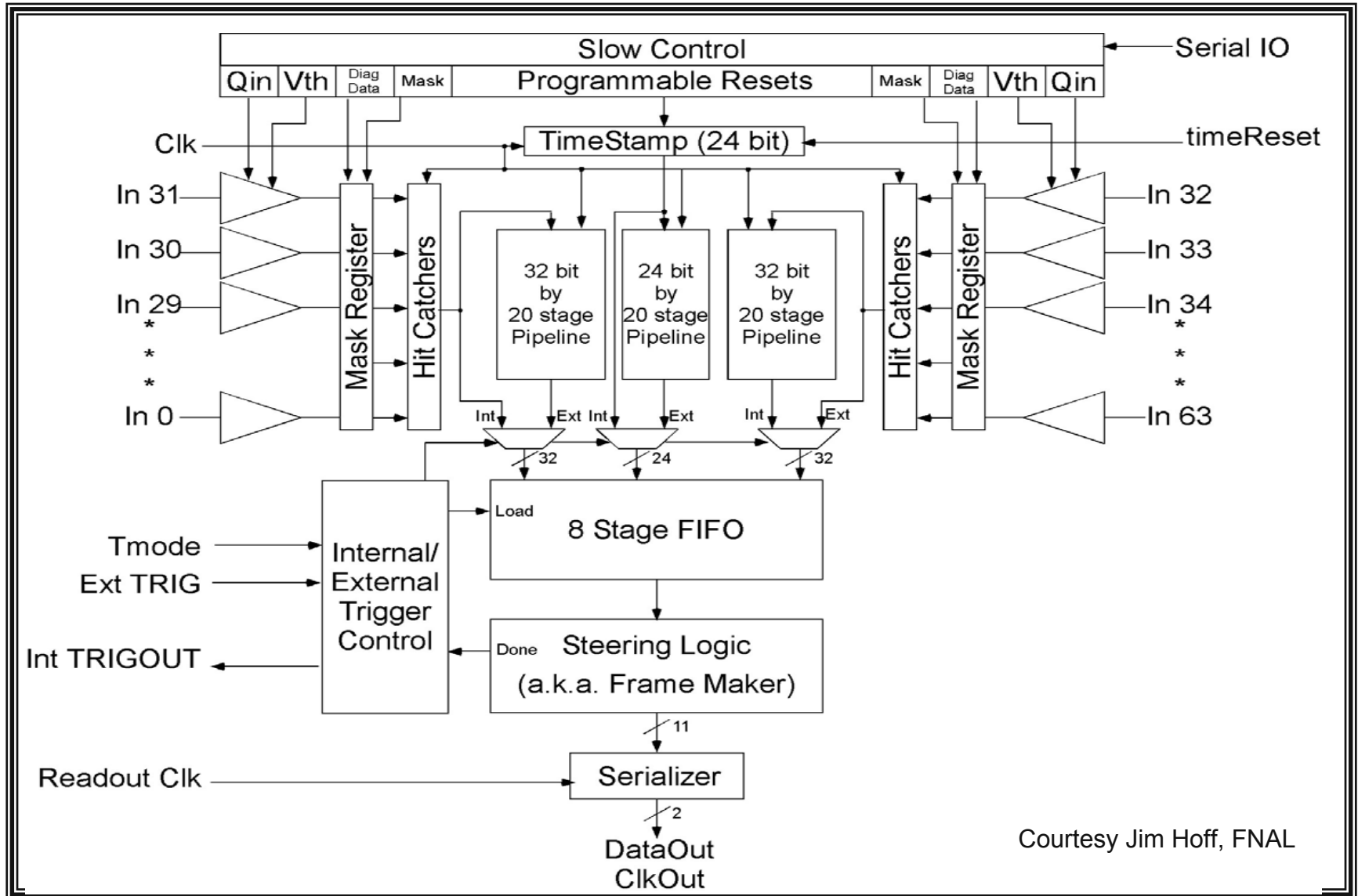
Courtesy Jim Hoff, FNAL

Features of the DCAL ASIC
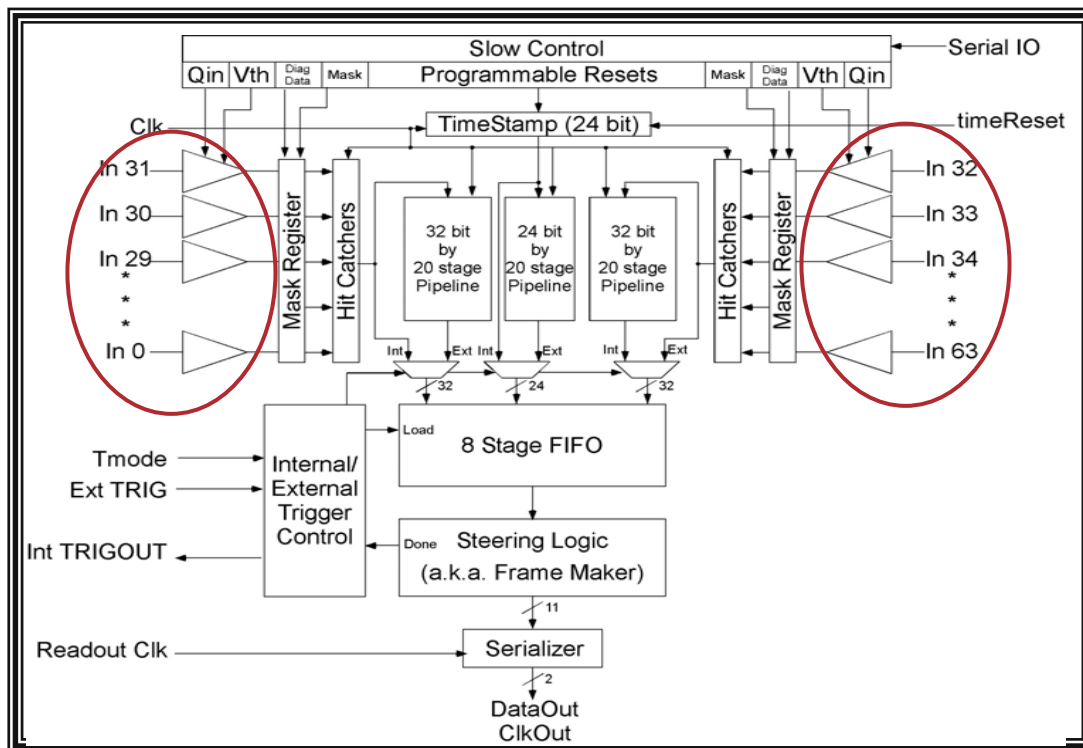
- Front-End consists of amplifier / shaper / baseline restorer
  - Charge preamp has selectable gain (1.5pF for GEMs, 9.9pF for RPCs)
  - CR-RC Shaper has selectable peaking times
    (65 nS, 85 nS, 100 nS, 125 nS)
  - BLR selectable (on or off)
  - 64 channels per chip

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Features of the DCAL ASIC
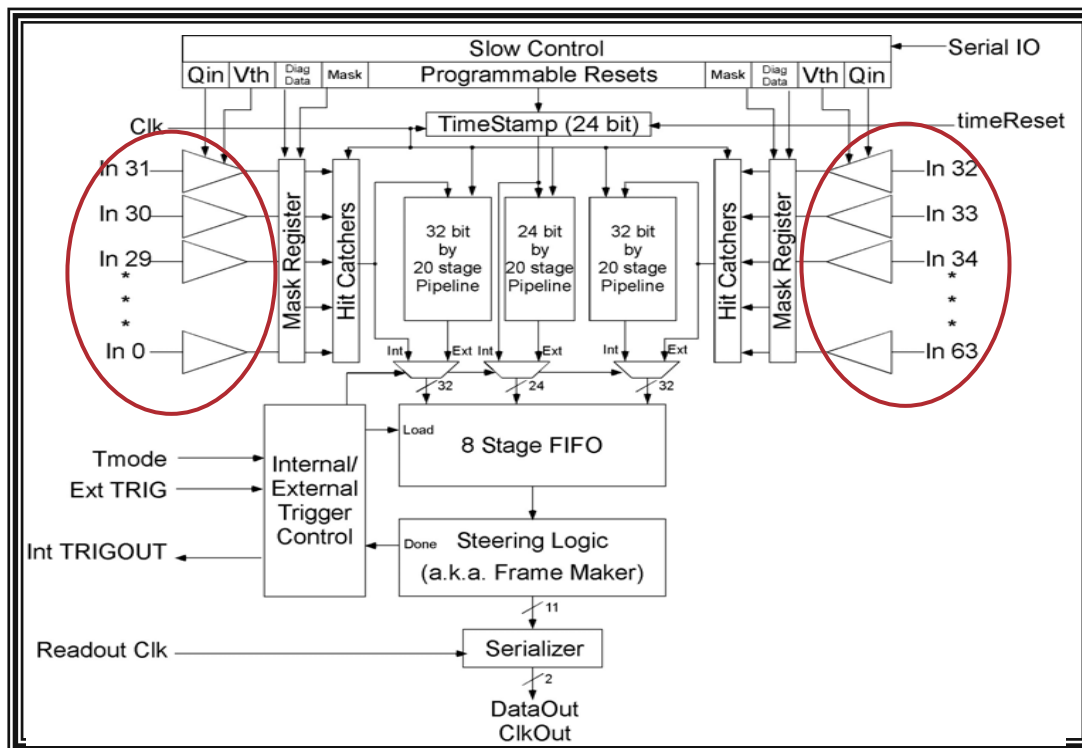
- **Front-End Discriminator**
  - Single threshold level
  - Common threshold for all channels on a chip
  - 8-bit DAC range

Features of the DCAL ASIC
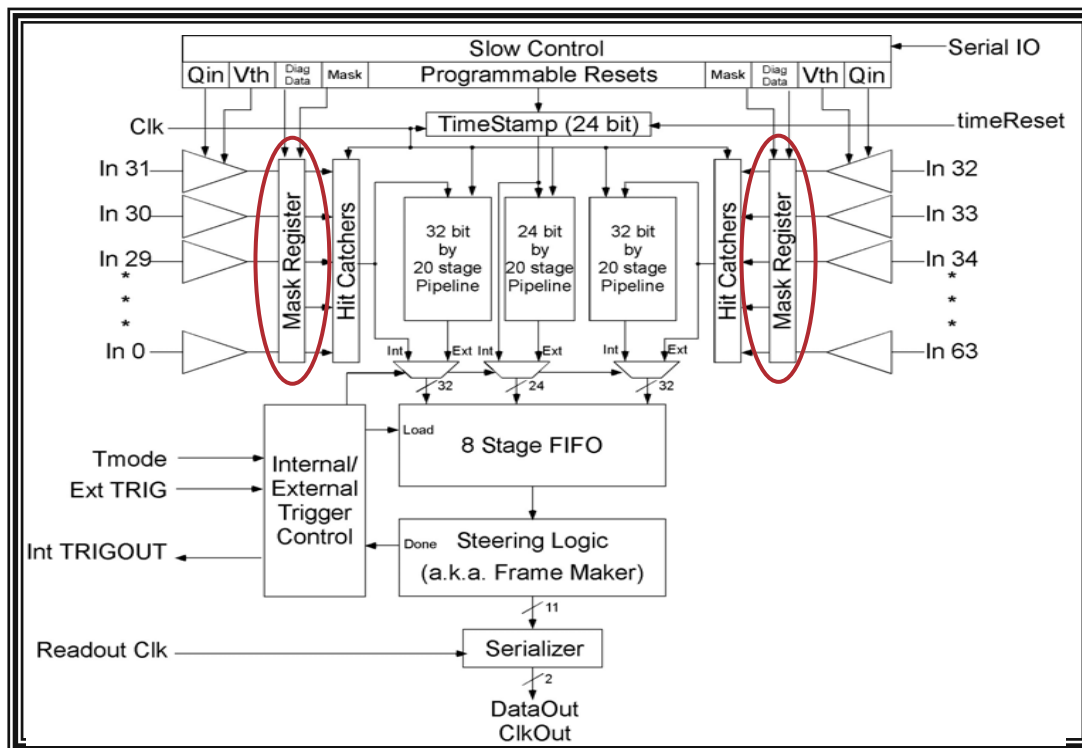
- **Chip Mask**
  - 64-bit mask register – turn off bad or noisy channels
  - Chip-wide enable bit – turn off bad chips

Features of the DCAL ASIC
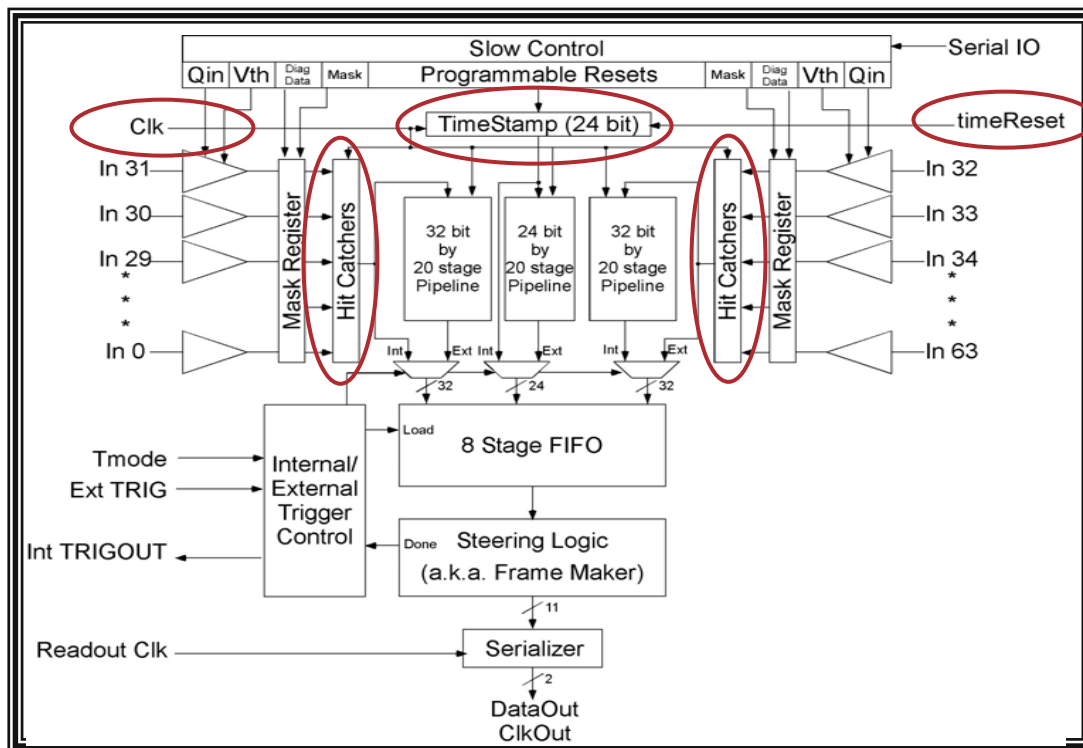
- **Timestamp**
  - Implemented as a counter, using 10 MHz system clock
  - Any Hit channel captures value of 24-bit timestamp counter (plus all 64 discriminator states)
  - Dedicated counter reset for synchronizing all counters across the system

Features of the DCAL ASIC
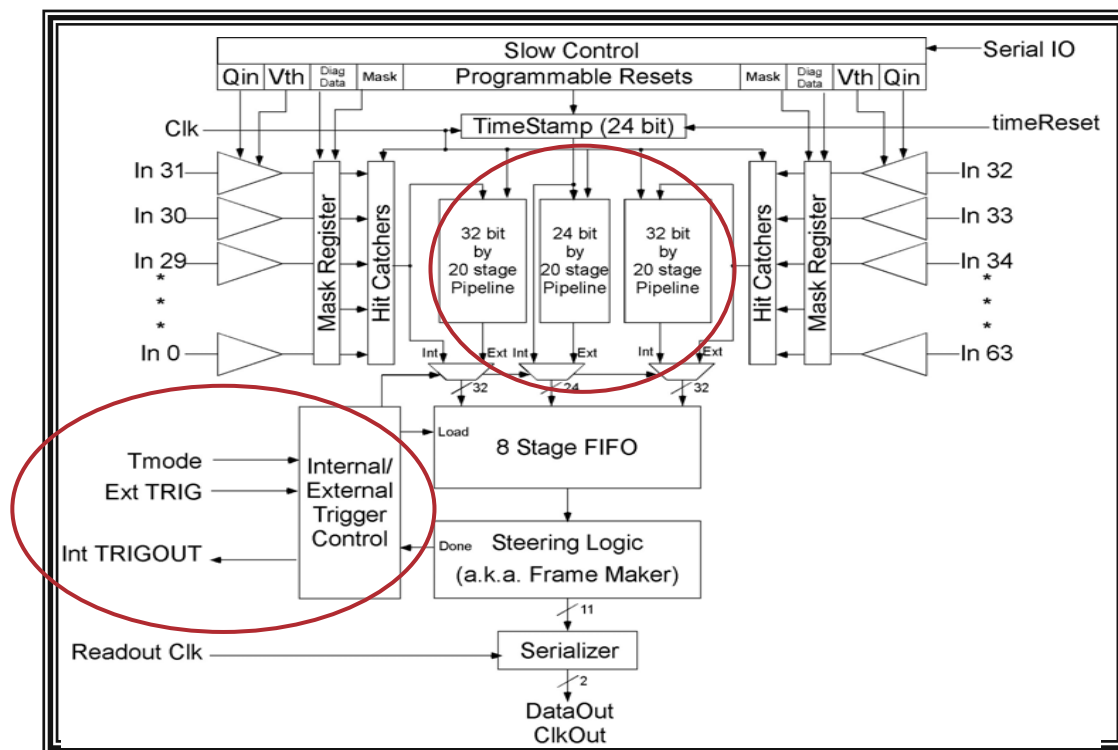
- **Triggering**
  - 20-stage pipeline for external trigger latency – use or bypass
  - Self-trigger – simple OR of all discriminators
  - External trigger input capability
  - Each trigger (internal or external) captures 1 clock cycle of data
  - Prompt generation of output trigger bit

Features of the DCAL ASIC
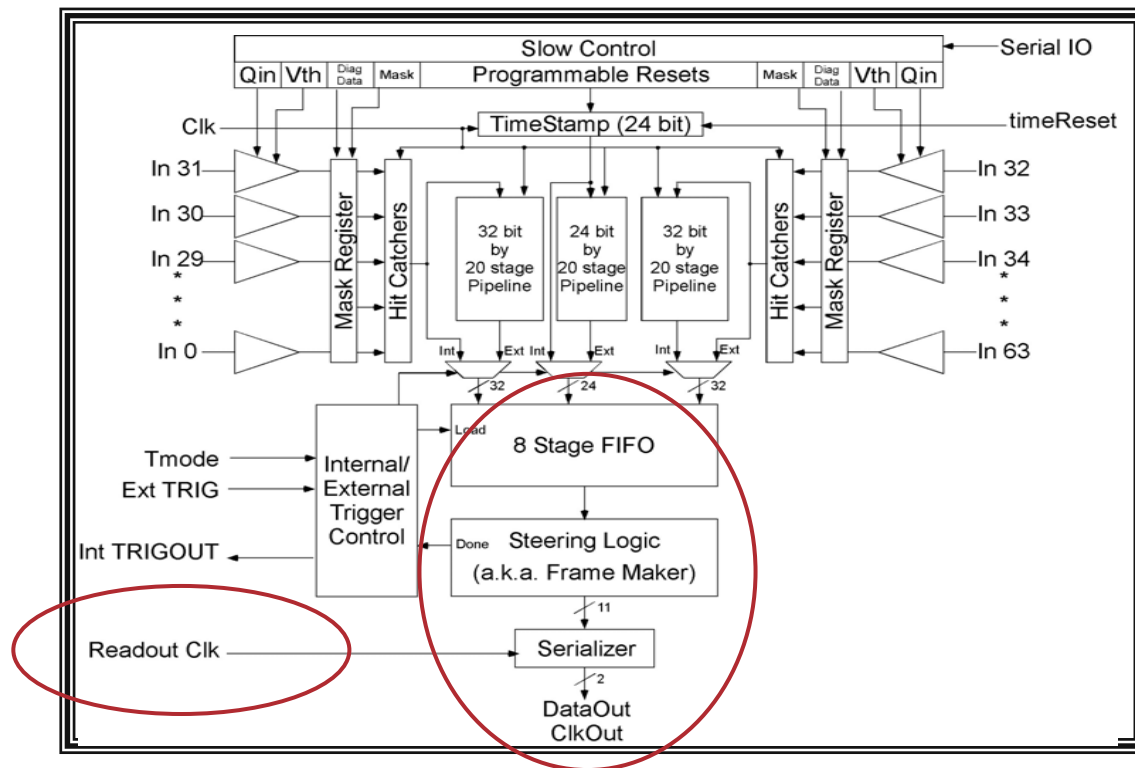
- **Output**
  - 8-stage output FIFO – can store 8 events, sequential or not
  - Data consists of 24 bits of timestamp + 64 discriminator states → 11 bytes
  - Each byte is parsed into 8-bit frames → 121 bits
  - Data transmitted LVDS, serially using 10 MHz system clock – 10 Mbps → 12.1 μSec to read 1 event (~80 KHz)
  - Point-to-point connection – No daisy-chaining or token-ring topologies

Features of the DCAL ASIC
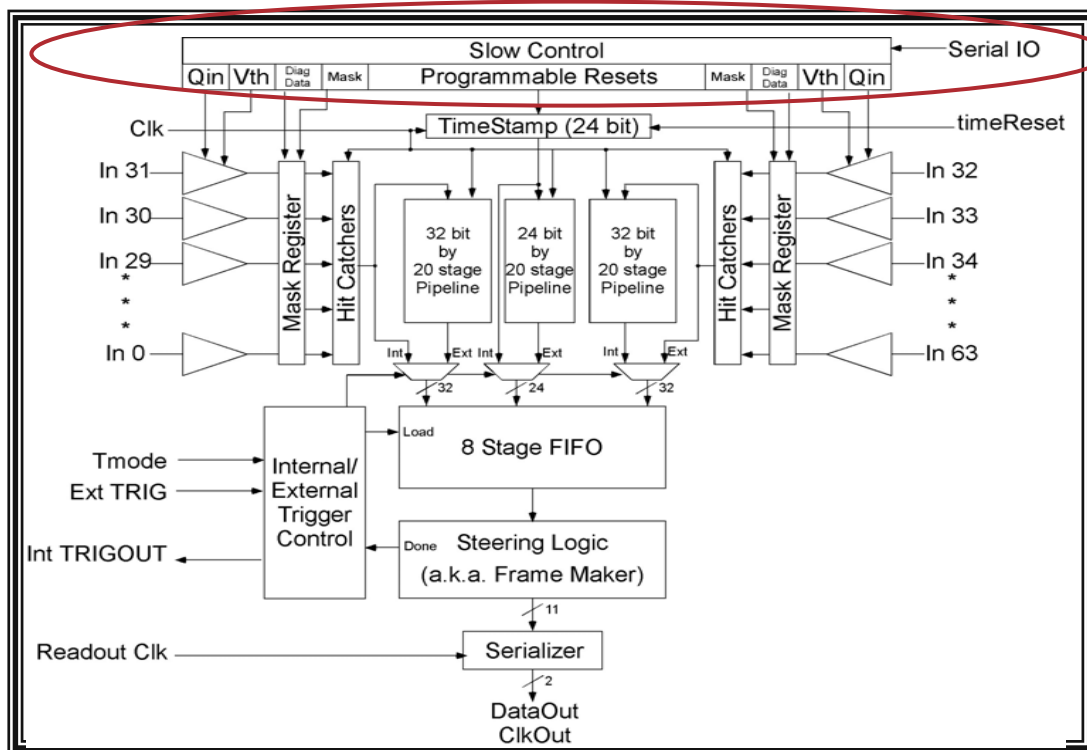
- **Slow Controls**
  - Set up FE conditions, trigger mode, mask register, pipeline enable, etc.
  - Set up charge injection (8-bit DAC, uses dedicated ext. sig. TCAL)
  - Chip has 5-bit addressing for communication in bussed operation
  - Most registers R/W, can do global (broadcast) set/reset/write
  - Data transmitted R/W, LVDS, serially using 10 MHz system clock

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DCAL Serial Data Output Format

Serial lines need synchronization → "Heartbeat"

No Data to Output   Data to Output

Status Word (1 Sample Clock)

Sync Word (1 Sample Clock)

Snapshot Frame (11 Sample Clock)

Sync Bit
Data
Data Type

$1 \; D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0 \; T_1 T_0$

00=SYNC
01=DATA
10=TIME
11=STATUS
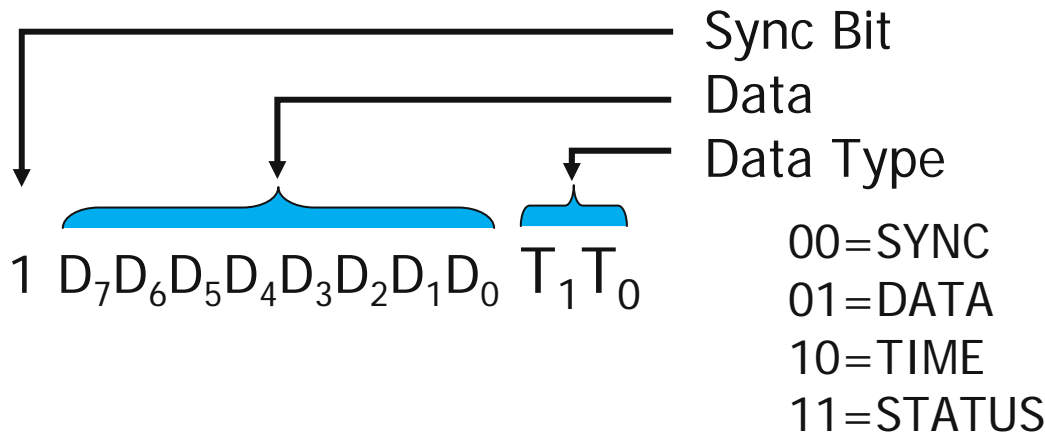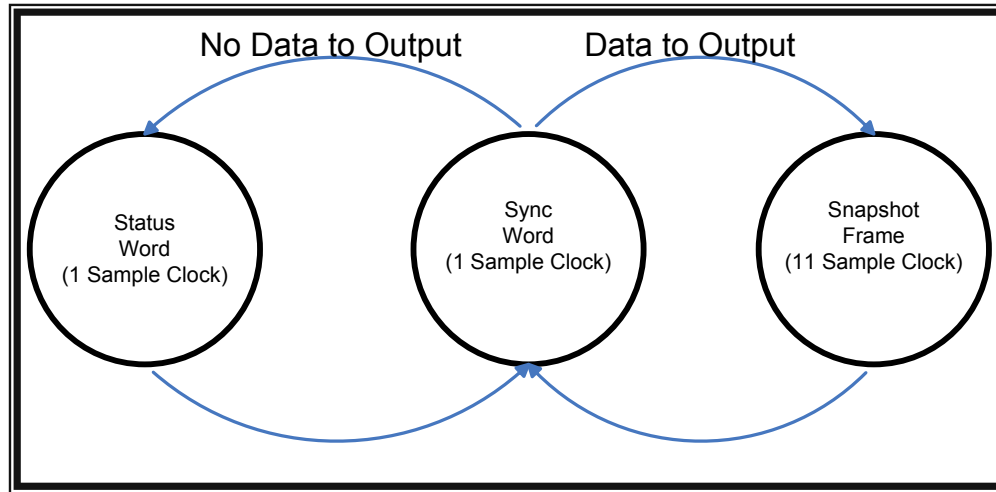
```
00
10000000000  SYNC
11000000111  STATUS
10000000000  SYNC
11000001111  STATUS
10000000000  SYNC
11000010111  STATUS
10000000000  SYNC
10000000010  TIME
10000000010  TIME
10000010010  TIME
10001000001  Hit Bits
11000000001  Hit Bits
10000001001  Hit Bits
10001000001  Hit Bits
10100000001  Hit Bits
10000000101  Hit Bits
10000100001  Hit Bits
10000001001  Hit Bits
10000000000  SYNC
11000001111  STATUS
10000000000  SYNC
11000010111  STATUS
100000
```

DCAL ASIC Layout – Version 2

Fabricated in TSMC 0.25 μm CMOS
Die ~4 mm x 6 mm, 160-pin TQFP package
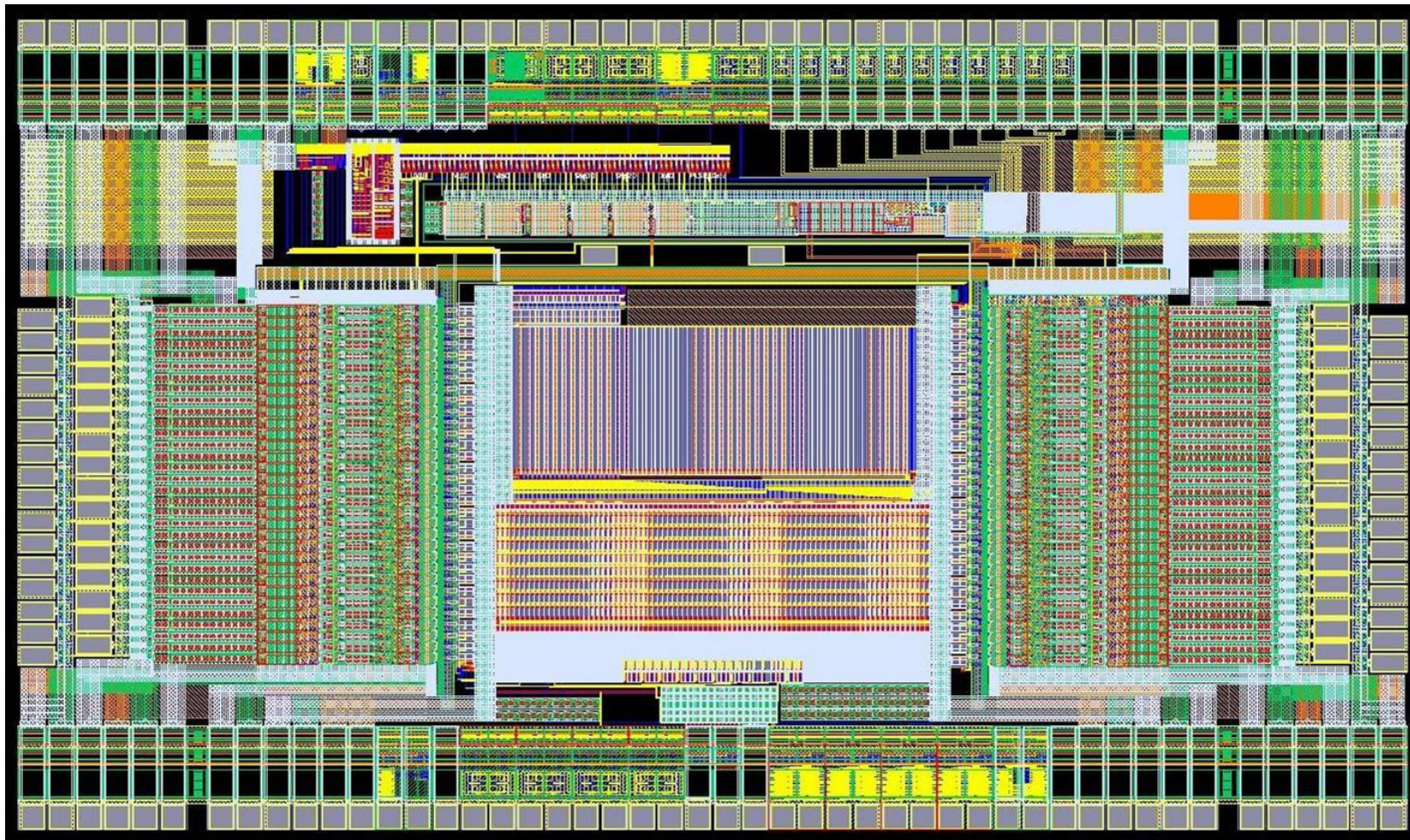
Fermilab

DCAL Chip Testing

- Design
  - Specified by Argonne
  - Designed by Fermilab
- 1st Version
  - Fabricated 40 chips, bare die
  - Extensively tested
- 2nd Version
  - Fabricated 104 chips, packaged
  - Main changes:
    - *Decrease gain for hi & lo ranges*
    - *Decouple output serial clock*
    - *Allow 10 MHz output serial clock operation*
  - Extensively tested at bench
  - Used in Vertical Slice
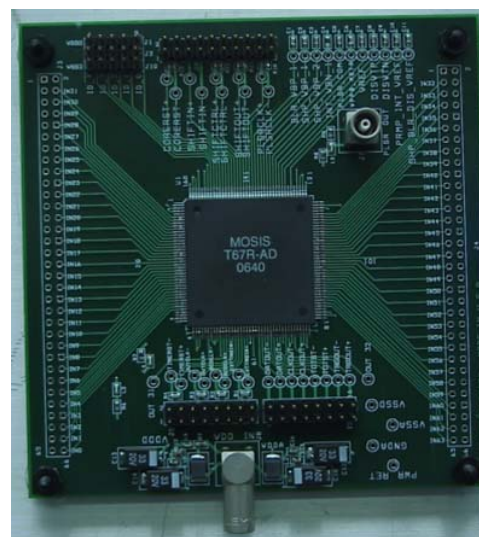
DCAL2 Testing – Charge Response

DCAL 2.1 - DAC = 128

Channel 00

DCAL 2.1

For GEMs

High gain

Error bars rms
of distributions

For RPCs

Low gain

Charge injector [DAC counts]
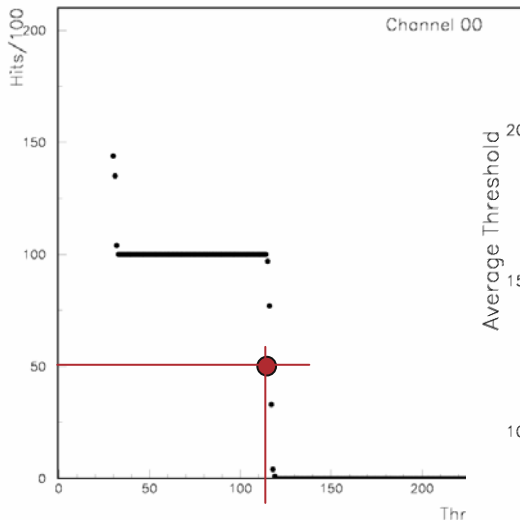
Threshold Scans
Internal or External QInj
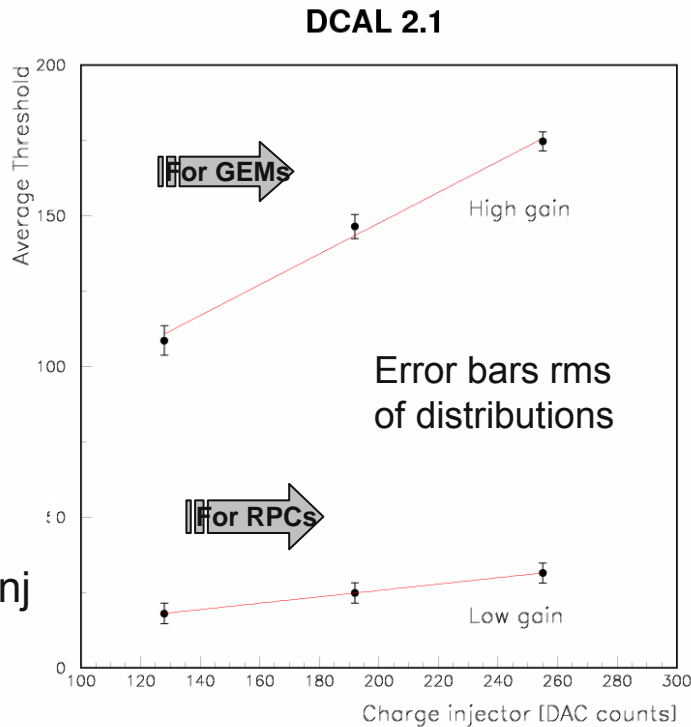
Internal Charge Injection
Ratio of high to low gain
R = 6.4 ± 0.2
(exactly as expected)
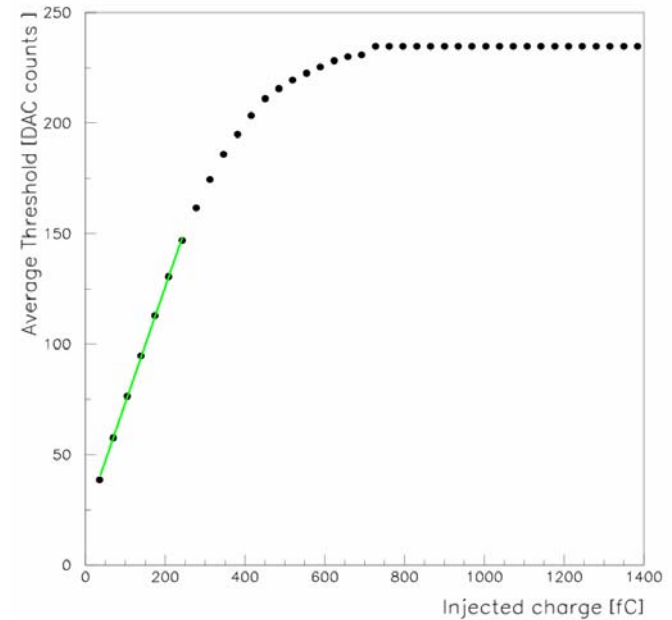
External Charge Injection
100 pF C_S
Low Gain:
Q(fC) = 1.91·THR DAC - 39.9

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DCAL2 Testing – Intrinsic Crosstalk within Chip

DCAL2.1 - Qinj = 5.0 pC

DCAL2.1 - Qinj = 10.0 pC

Crosstalk

Crosstalk

Nominal Operating Point
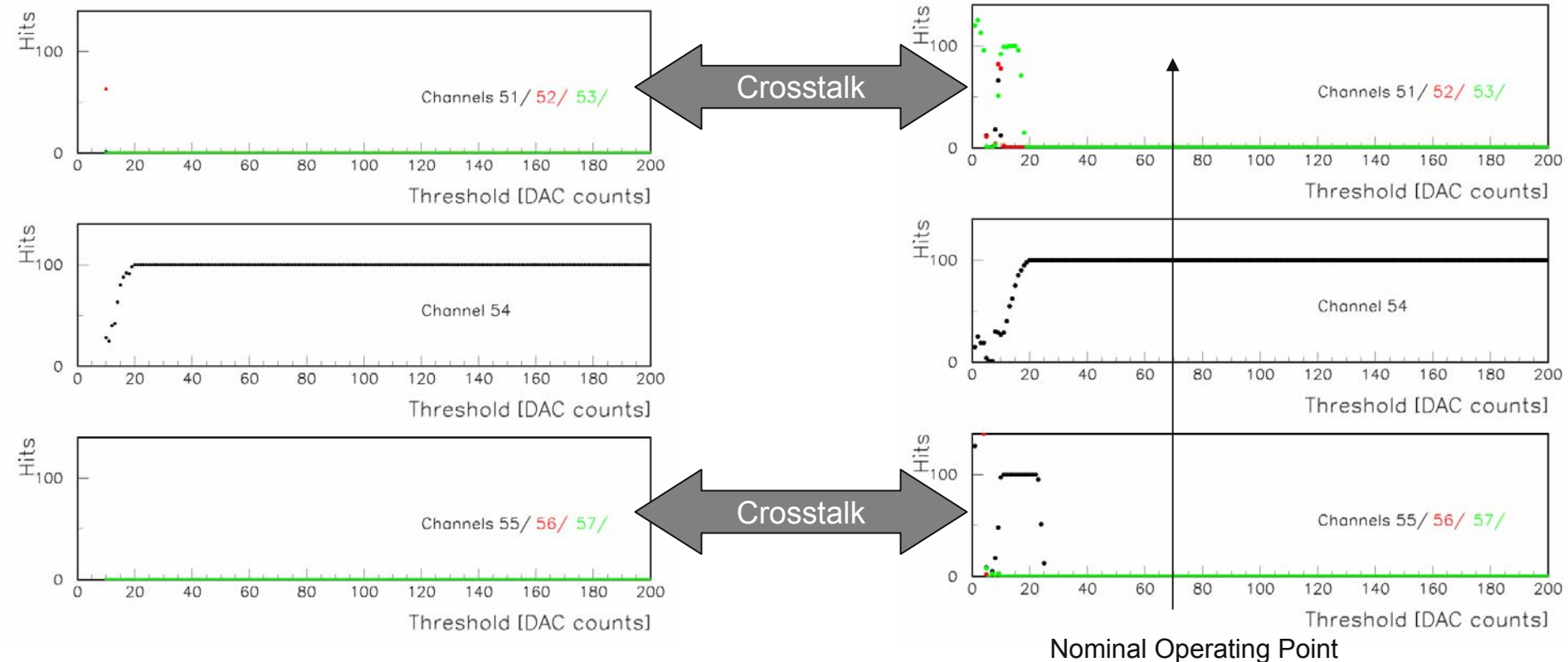
No Evidence of Crosstalk @ 5 pC

Neighbors See Crosstalk @ 10 pC

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Pad Board & Front End Board Design

4-layer Pad-board (3 shown)
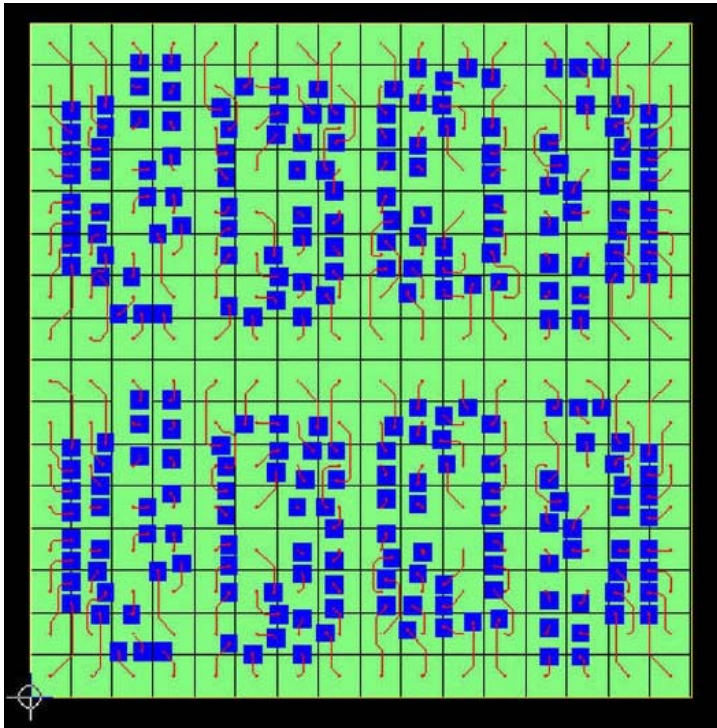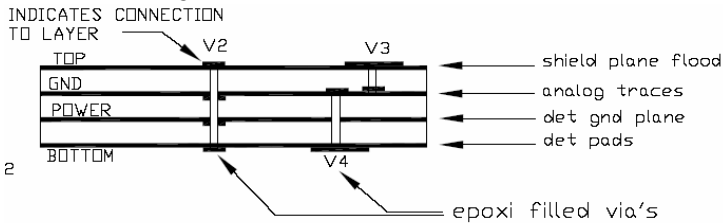
Blind vias to route sensitive signals to glue pads – needed to minimize contact with digital lines in FEB

8-layer FE-board (3 layers shown)
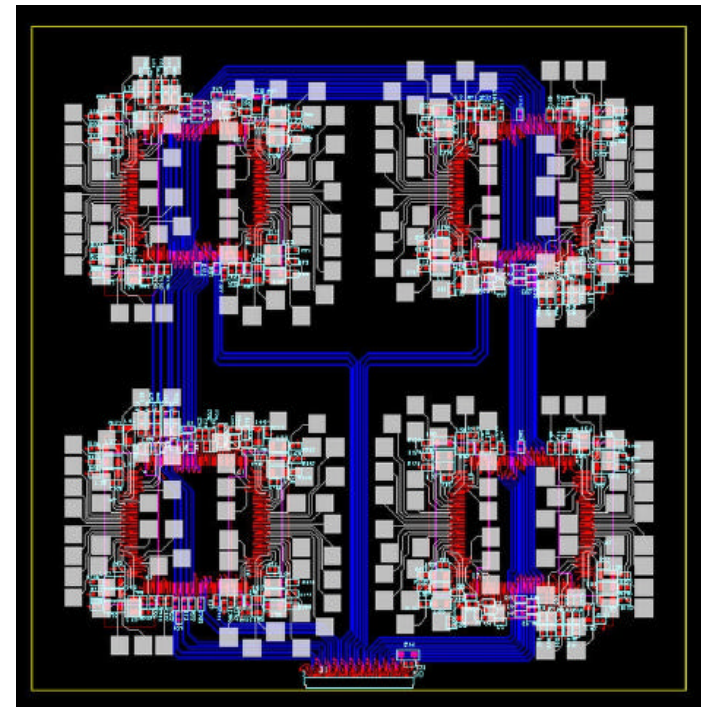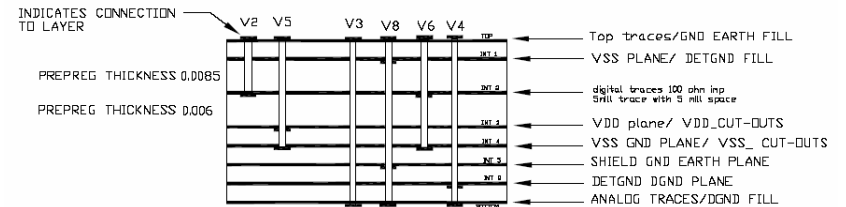
Also has blind vias
→ Very complex board design to minimize crosstalk & digital noise pickup

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Front End Board Construction & Testing
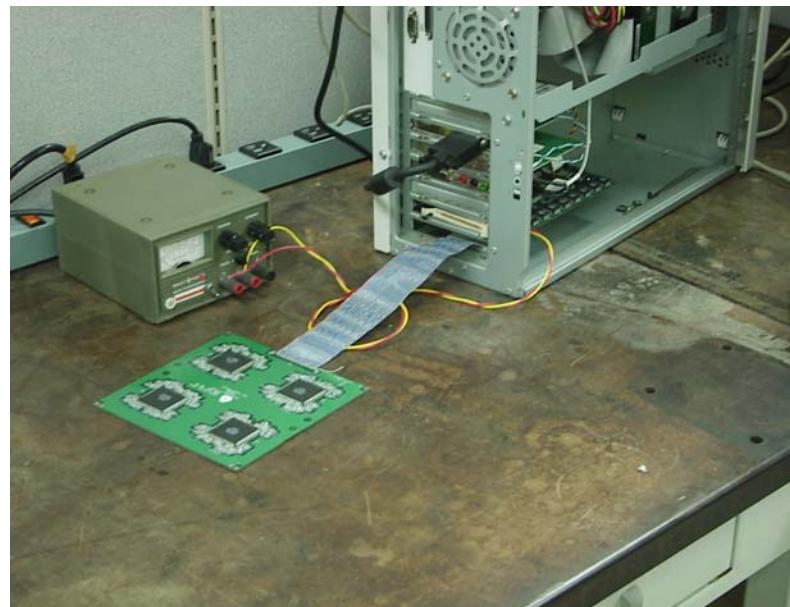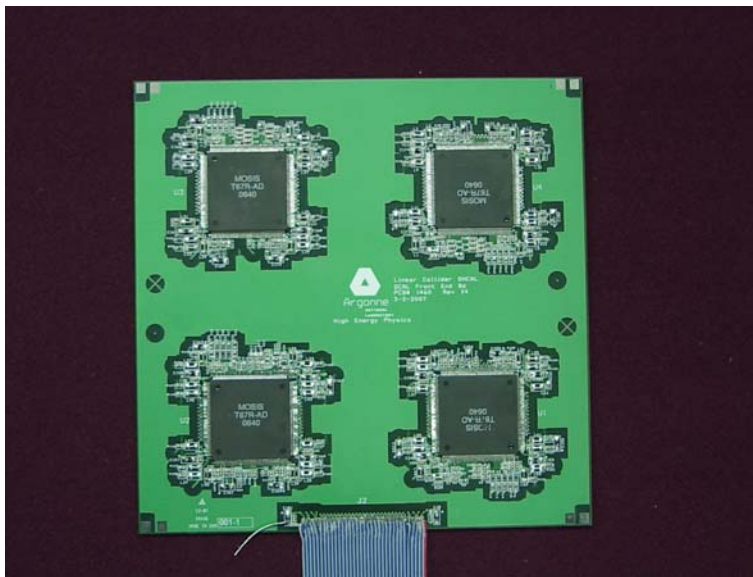
- Have built & checked out 14 boards.
- Chips not tested in advance of assembly.
- Yield ~85%.

Measurement of FEB Noise Floor
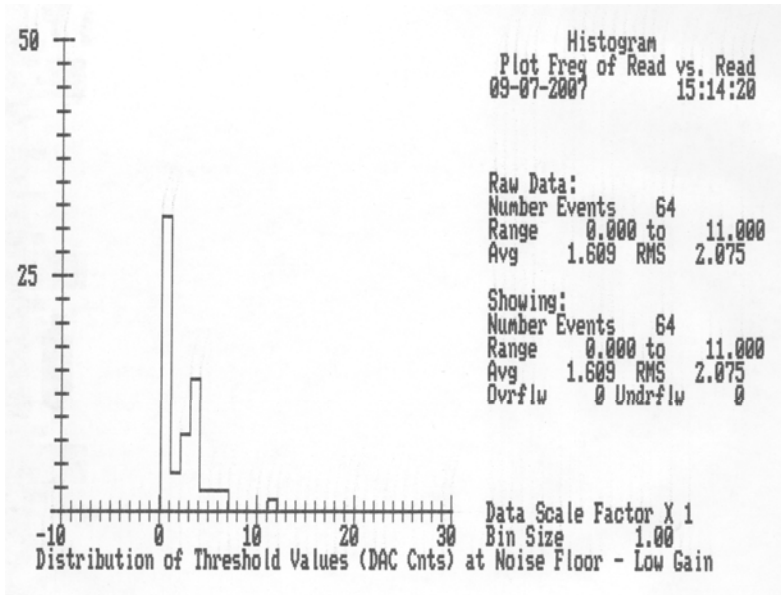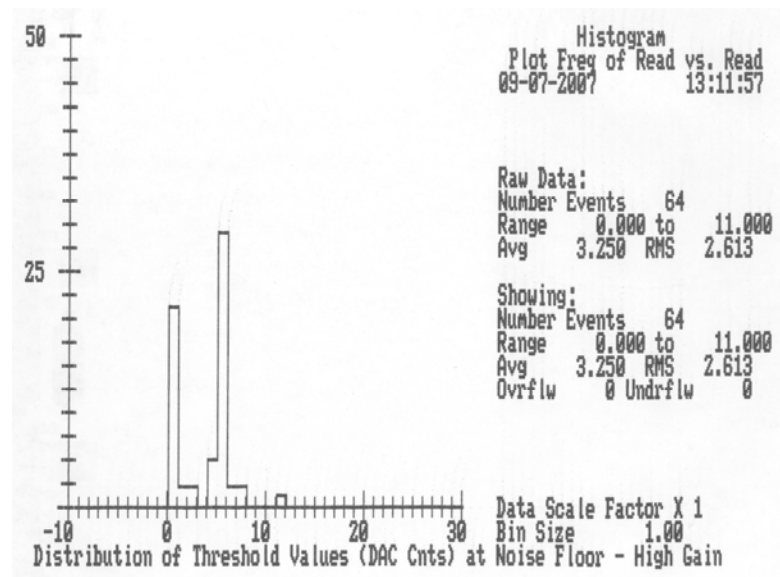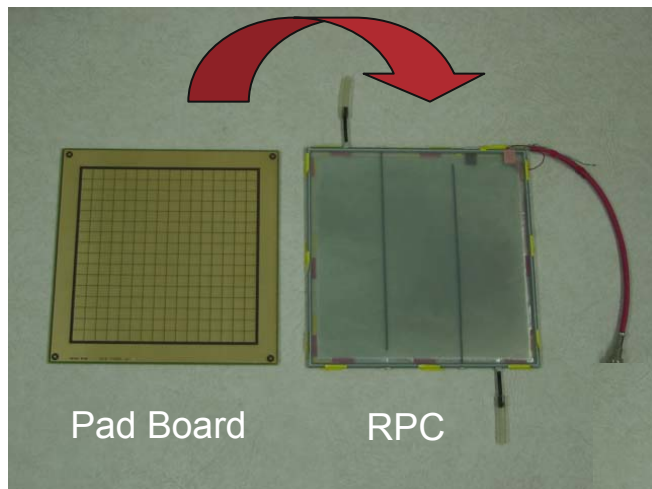

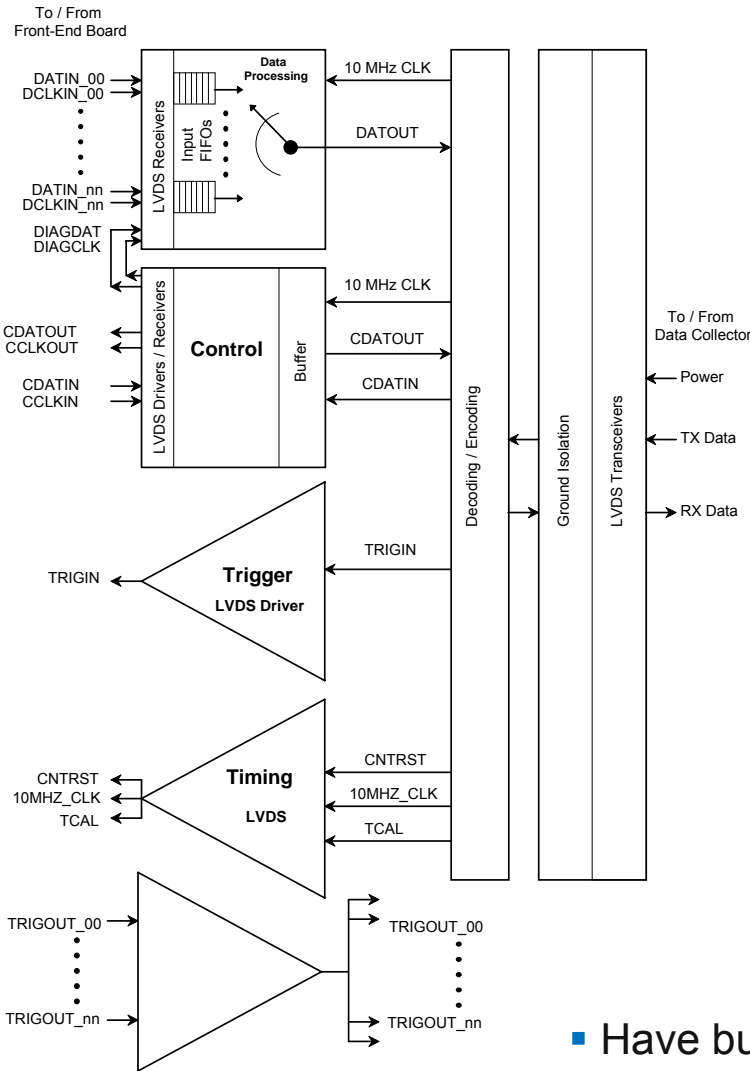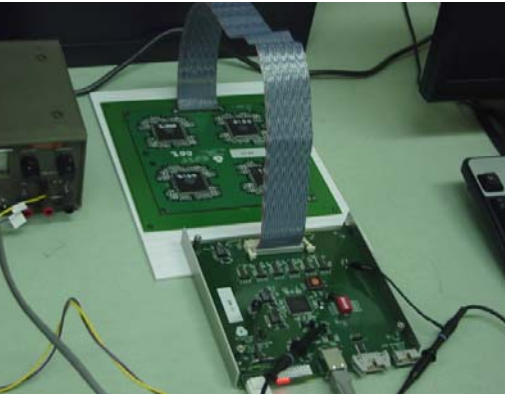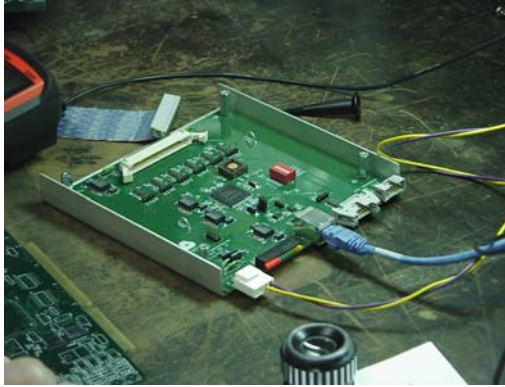Low Gain   High Gain

Distribution of Threshold DAC Values to give 10% Hits
Tests on Bare Front End Board
No C_S
No Charge Injection

⇨ *Excellent Noise Performance!*

Vertical Slice Electronics Construction

Pad Board   RPC

FEB Board   RPC & Pad Bd

Assembled & Tested Beforehand

Side View

Completed Assembly
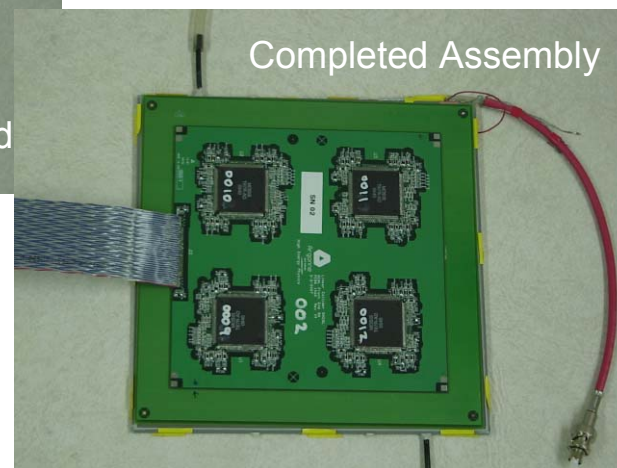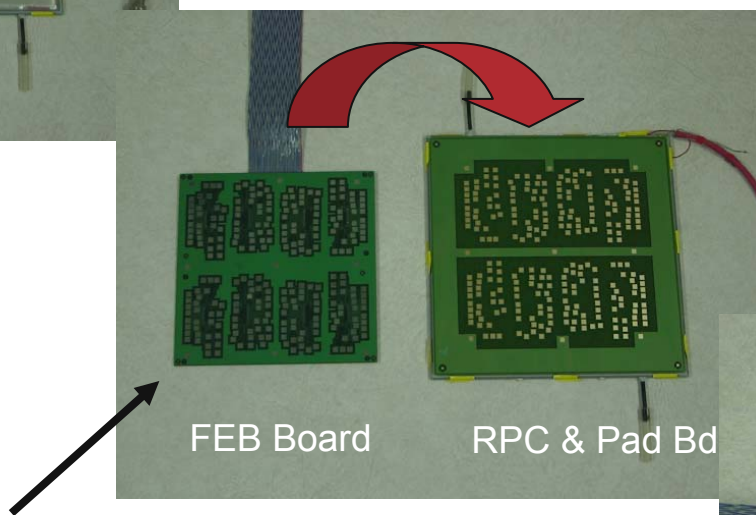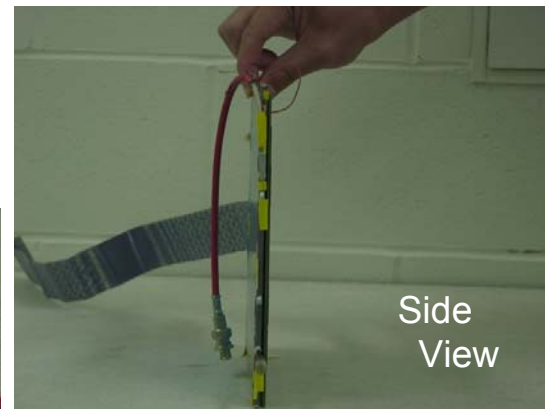
Prototype Data Concentrator

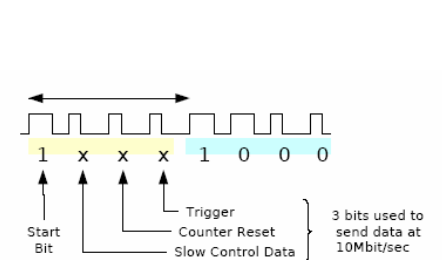| Pin	Signal	Pin	Signal
1	Tx data +	5	Test -
2	Tx data -	6	GND
3	+3.3V	7	Rx data +
4	Test +	8	Rx data -

Table 1: Front-End Link Connector Pinout

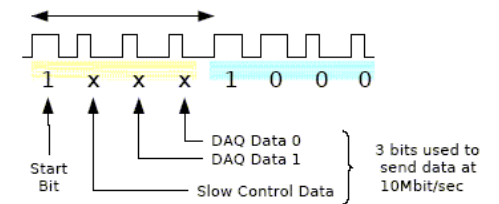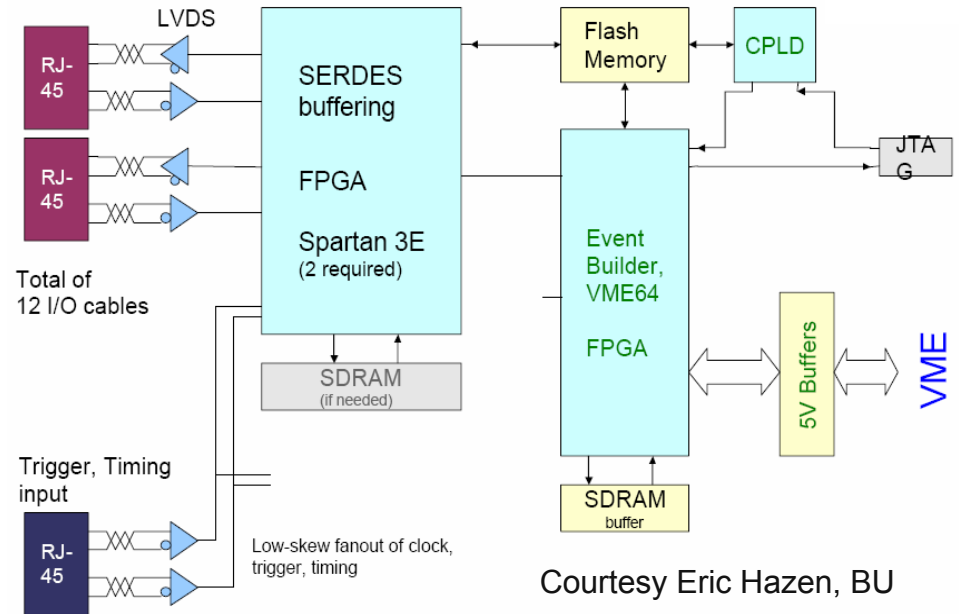Illustration 2: Front-End Link Low-Level Protocol: from DCOL to front-ends

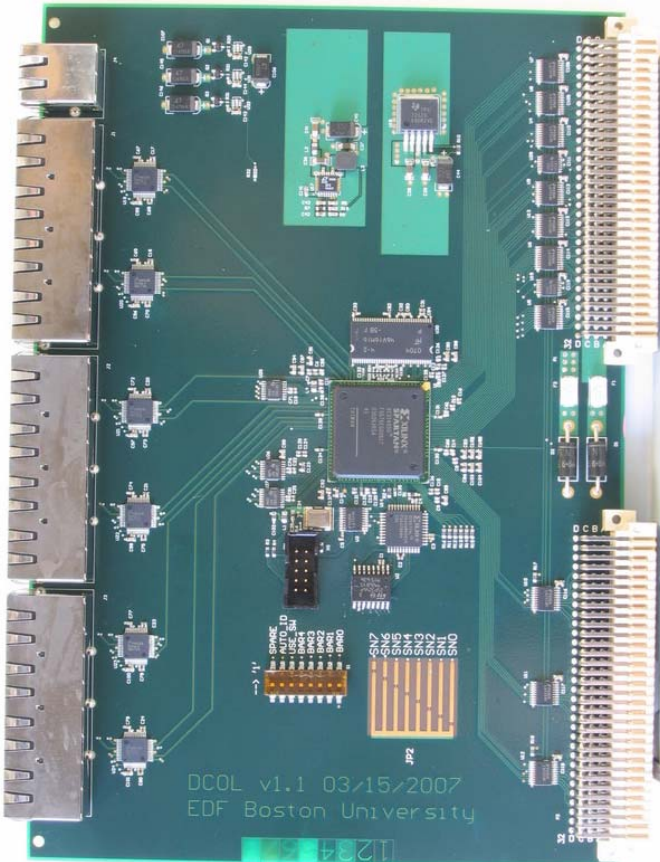Illustration 3: Front-End Link Low-Level Protocol: from front-ends to DCOL

- Have built & checked out 14 boards.

Data Collector

Courtesy Eric Hazen, BU

▪**Functionality:**

— Receives data as packets
Timestamp (24 bits) +
Address (16 bits) +
Hit pattern (64 bits)

— Groups packets in buffers
(by matching timestamps)
— Makes buffers available for VME transfer
— Monitor registers (scalars)
— Provides slow control of front-end
Allows read/write to DCAL chips or
data concentrator boards

▪ Have built & checked out 3 boards.

Timing & Trigger Module (TTM)

GPS Receiver Input

Trigger Inputs
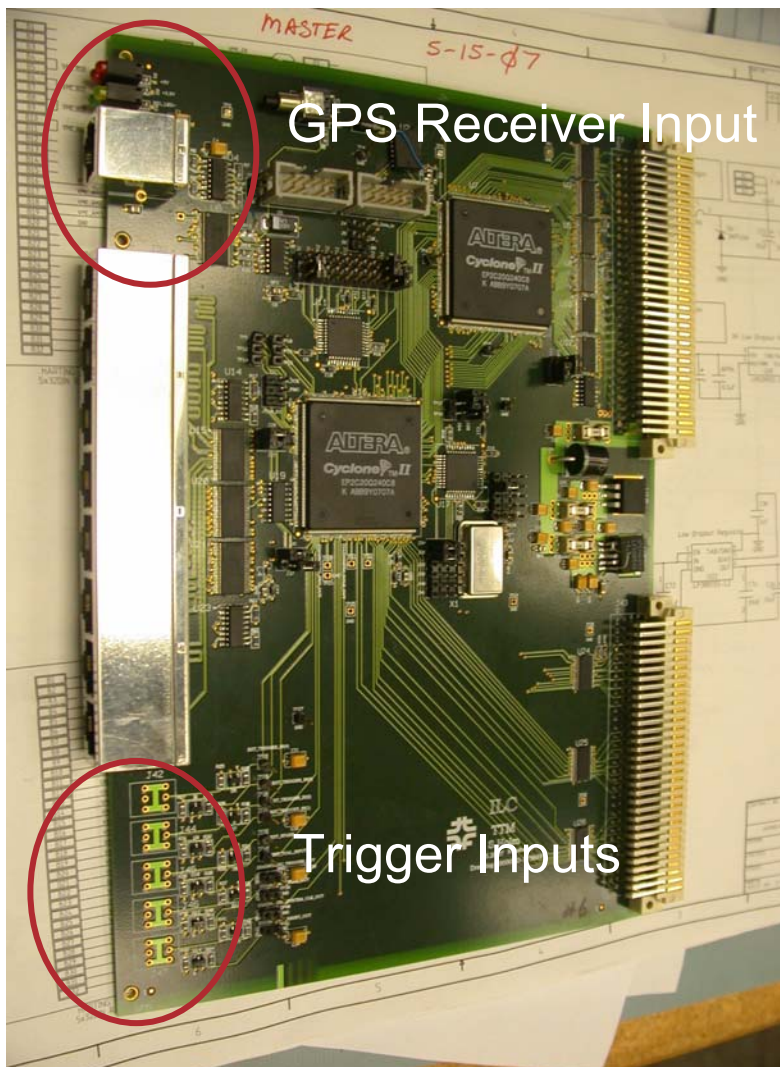
- **Functionality:**
  - Provides synchronized clock & trigger signals to Data Concentrators, which in turn fan out to front ends
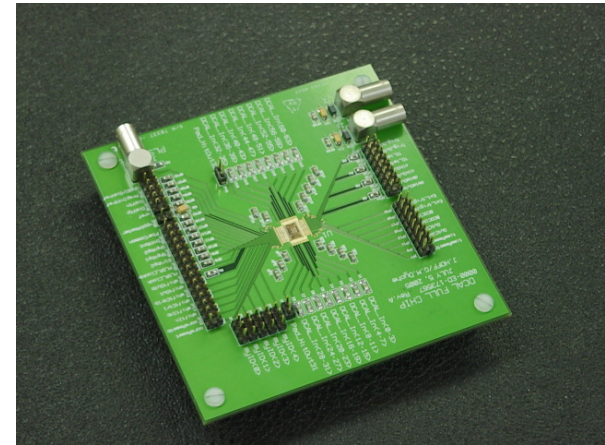 - Contains registers for timestamping triggers, histogramming, etc.

- Have built & checked out 3 boards.

Fermilab

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Implementation Plan: Staged Approach

1. Develop & Test ASIC
   - Version 1 ➜ **Completed**
   - Version 2 ➜ **Completed**

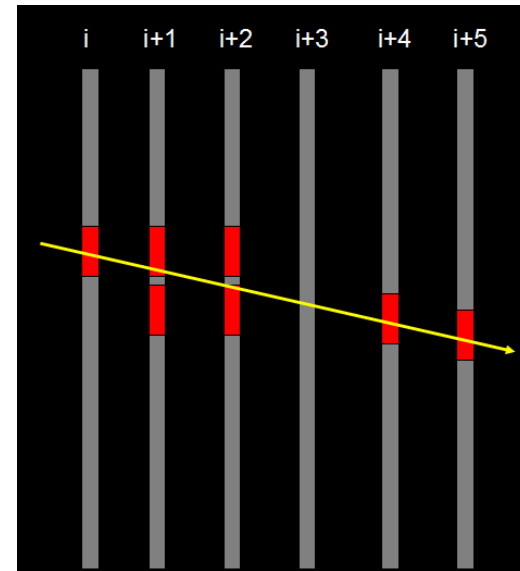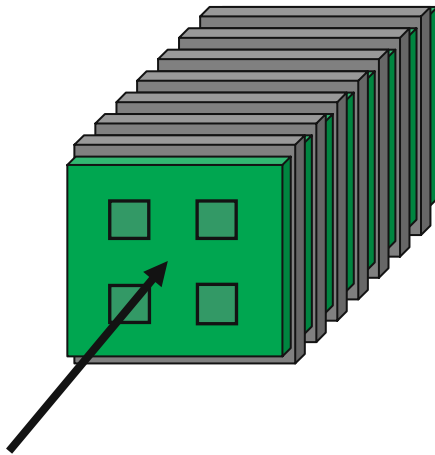⇨ *Extensively tested at the bench*
⇨ *Will need 1 more tweak to design, but ready for production*

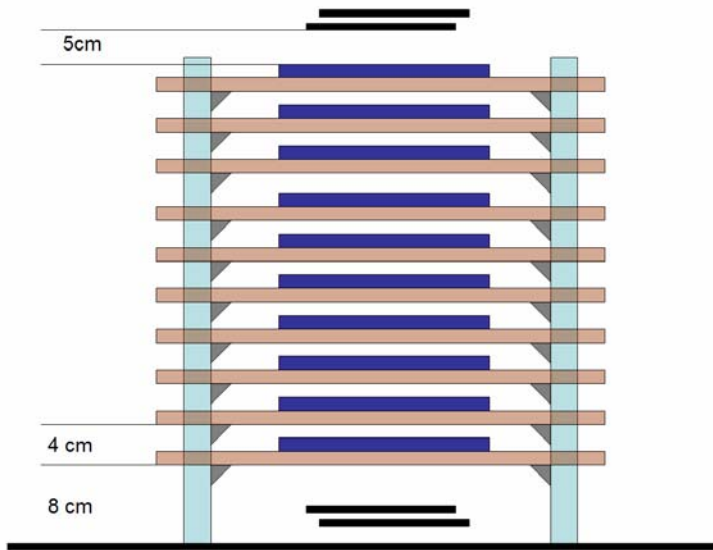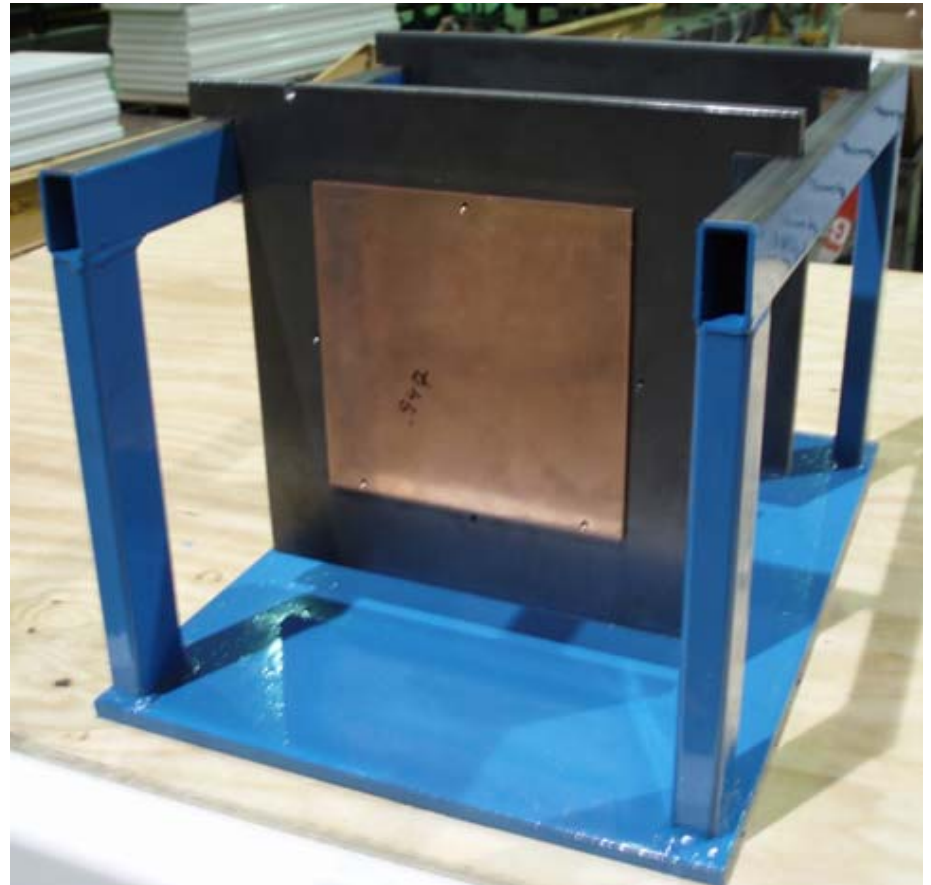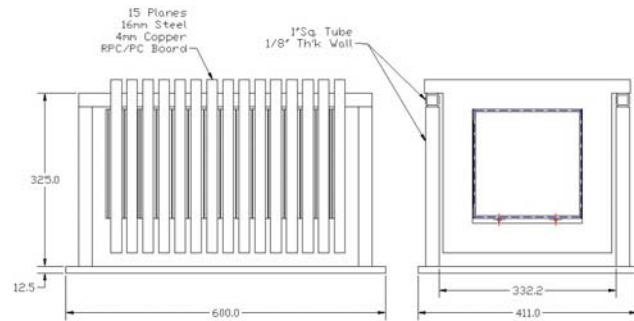# Implementation Plan: Staged Approach (Cont.)

2. Build "Vertical Slice"
    - (10) 256-channel planes – 2500 channels total
    - 4 ASICs per plane
    - Test with cosmic rays & testbeam
    - Goals: Develop prototypes, perform small system tests,
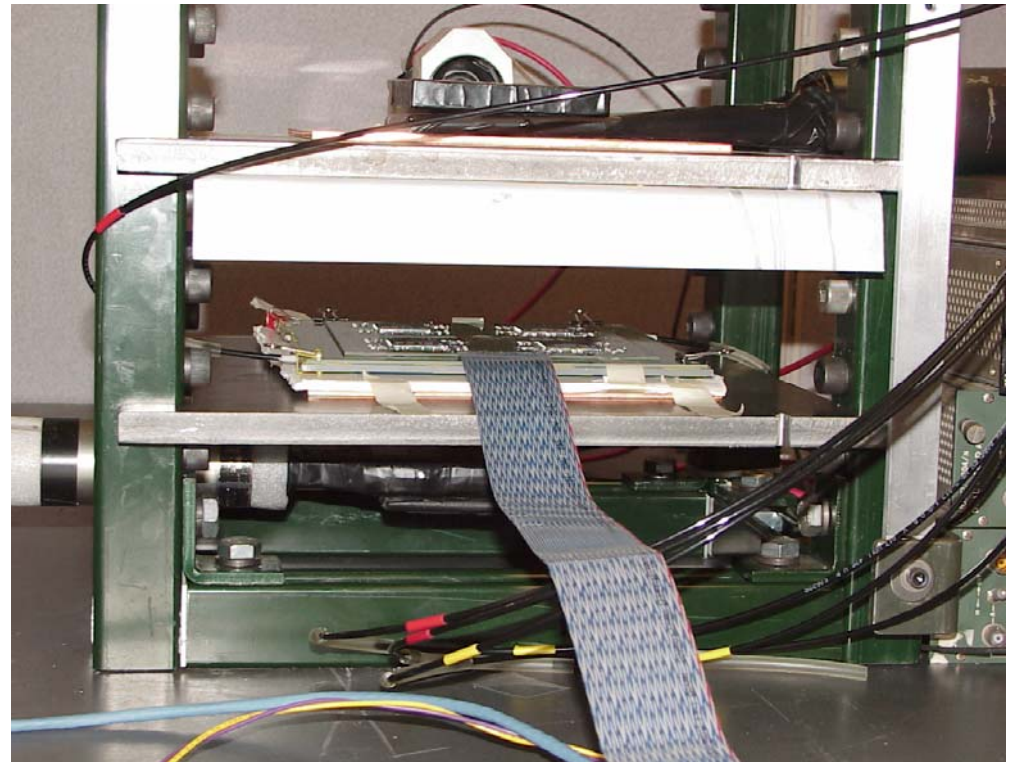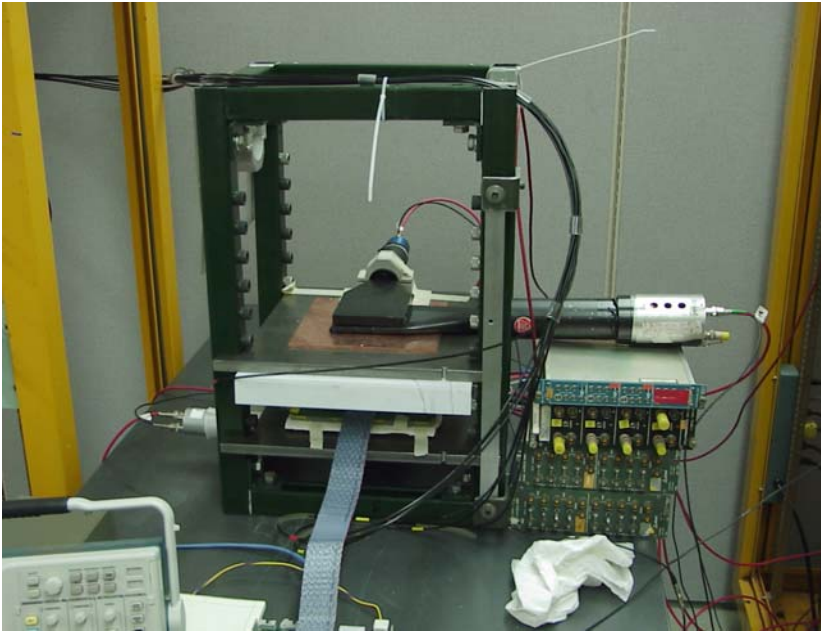   Debug design before production of cubic meter
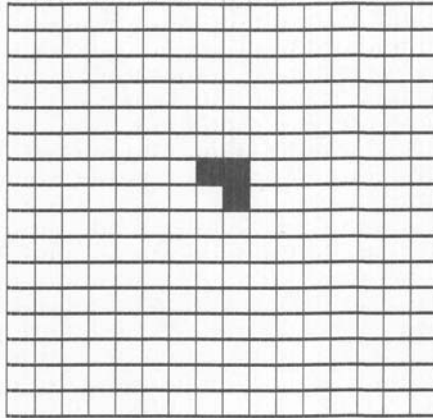   → **Completed**

Vertical Slice Construction
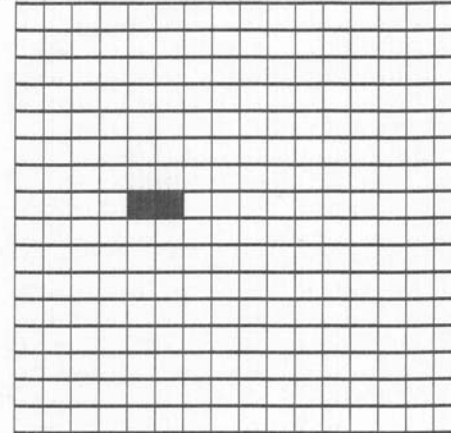
Tests with Cosmic Ray Hodoscope

First Cosmic Ray Events – 1 Plane, Triggered

Event 1 Timestamp 1212504 Hits 3 Running Efficiency 1.0000

Hit Any Key to Continue, or B to Go Back to Main Menu...

Event 24 Timestamp 588154 Hits 2 Running Efficiency 0.8750

Hit Any Key to Continue, or B to Go Back to Main Menu...

Event 21 Timestamp 13311779 Hits 11 Running Efficiency 0.8571

Hit Any Key to Continue, or B to Go Back to Main Menu...

- ■ 3 chambers on – Droege
- ▲ 1 chamber on – Droege
- ● 1 chamber on – Bertan
- ▼ All HV off

36.5 fC   100 fC
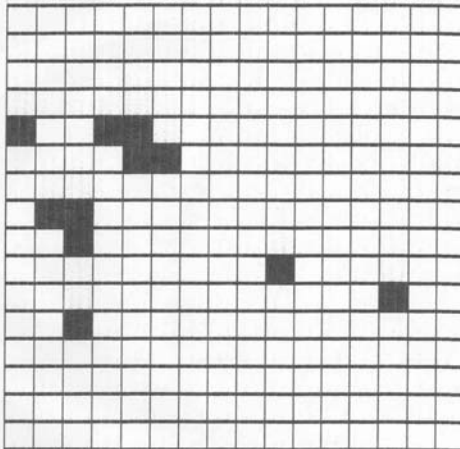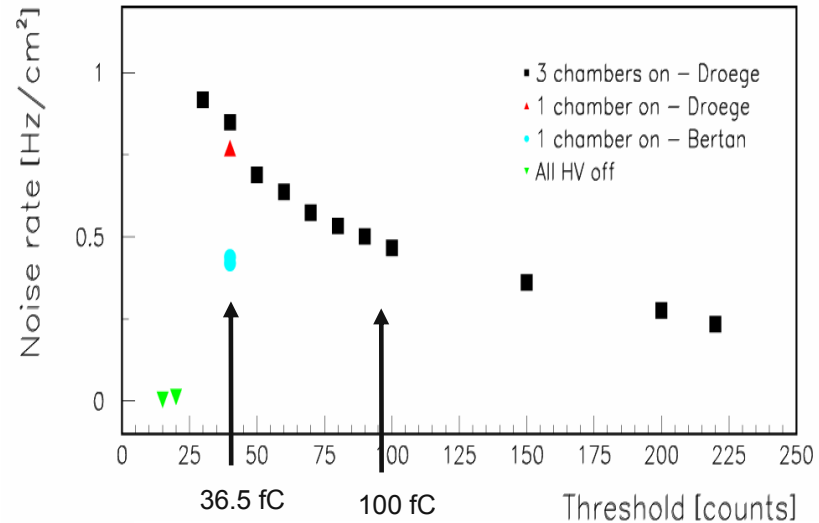
Noise rate of electronics ~ 0
Noise rate of chamber < 1 Hz/cm^2

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Vertical Slice at the Fermilab Testbeam
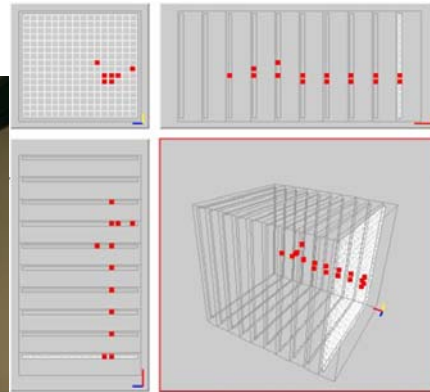
See José Repond's Talk

Implementation Plan: Staged Approach (Cont.)

3. Build the Prototype Section
   - (40) 10,000 channel planes
     → 400,000 channels total
   - 144 ASICs per plane
     → 5760 ASICs total
       (Fab ~9000)
   - Test with cosmic rays & testbeam
   → **Development In Progress…**

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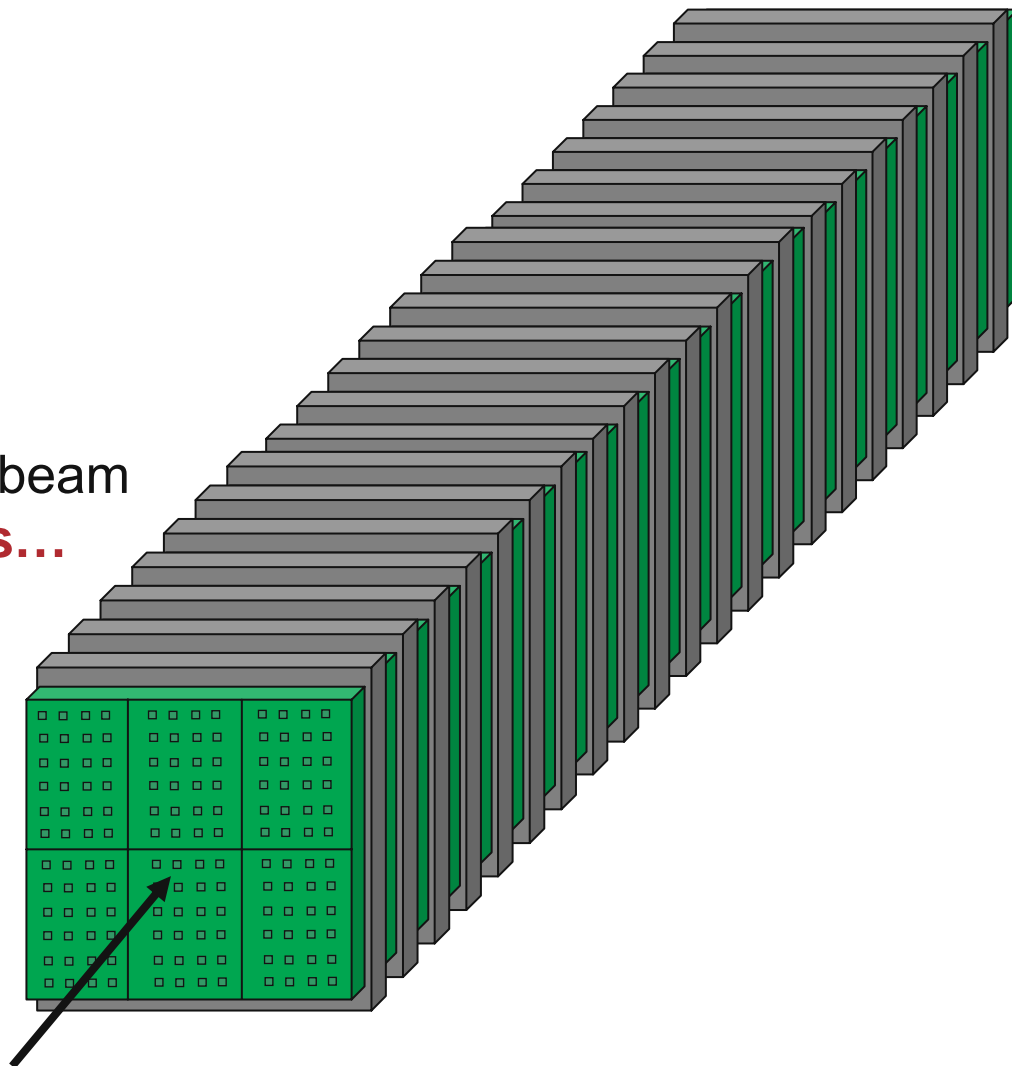
Next Step: Build the Prototype Section

Actual Size RPC & Pad Board

Status of System Components

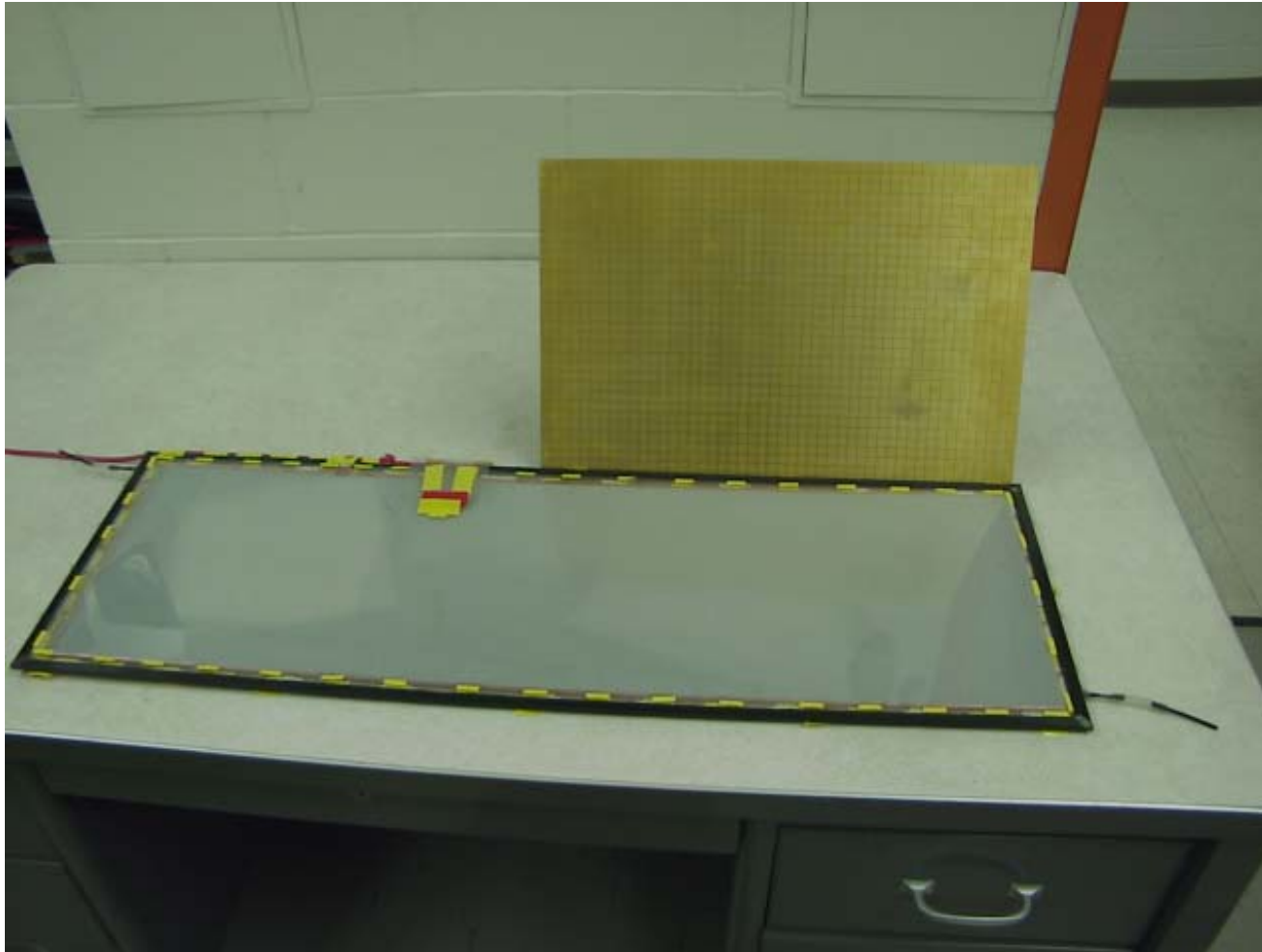| Subcomponent	Vertical Slice Test		Design Status	Prototype Section	
	Inputs → Outputs	Units Needed		Inputs → Outputs	Units Needed
Pad boards	256 → 256 (Analog)	10	Increase size Have 1st prototype Working on reducing cost	1584 → 1584 (Analog)	240
FE-boards	25... (...log...)	10	Increase size Working on reducing cost & manufacturability	256 → 4 (1584 → 72 ?)	1440 (240 ?)
DCAL ASICs		40	Need final design tweak Ready for production	64 → 1	5760 (9000)
Data Concentrators		10	Redesign in progress 4:1 → 72:1	72 → 1	80
Data Collectors		1	Need minor firmware changes Ready for production	12 → 1	7
Timing module		1	Implement ISR for DAQ Ready for production		1

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Summary

- **Well advanced in electronics design**
  - 2 versions of ASIC, thoroughly tested at bench
  - No show-stoppers in system performance
  - Robust architecture ideal for detector development
  - All system components prototyped & work well
  - Mature checkout test stands & software

- **Vertical Slice**
  - Successful cosmic ray run with hodoscope
  - Successful beam test at Fermilab
    (See Repond talk yesterday & one that follows)
  - We learned much – DAQ bugs, noise, timing problems, communication problems, etc.
  - Have proven electronics readout concept is Robust and Viable
  - Have demonstrated to our funding agency that this project is worth supporting

- **Next Step: Prototype Section**
  - Completing final design preparations now
  - Begin production of components by end of 2007

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