DHCAL
PCB STUDY
for
RPC and MicroMegas

(Electronics recent developments for the European DHCAL)

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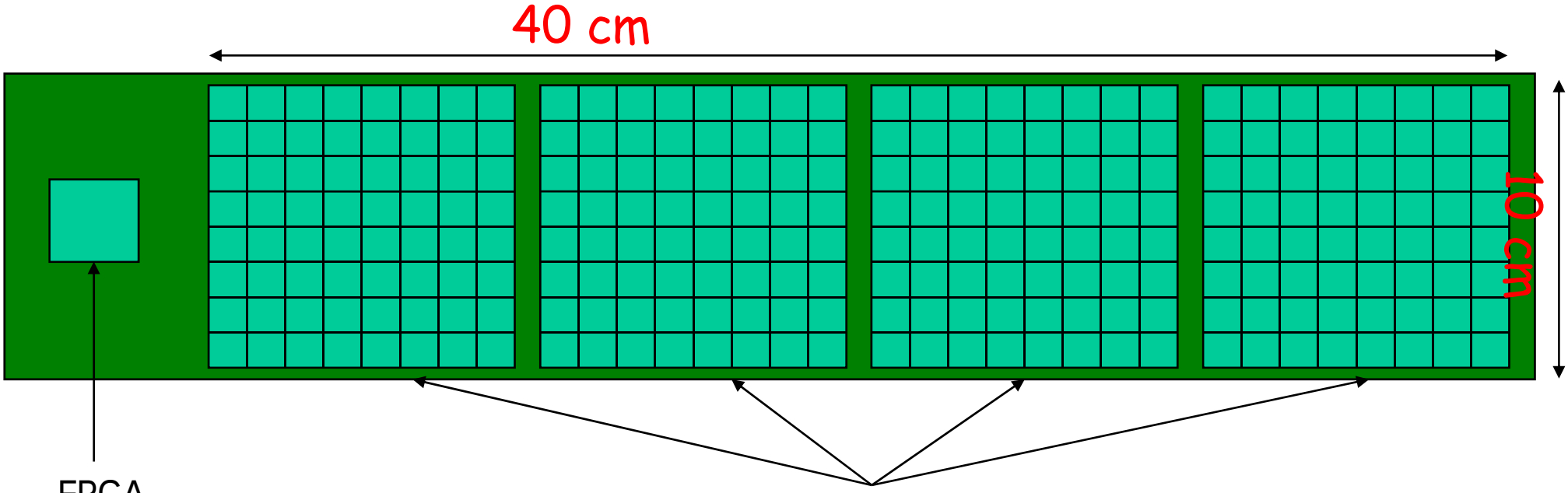
Collaboration with LLR and LAL

LAYOUT DESIGN

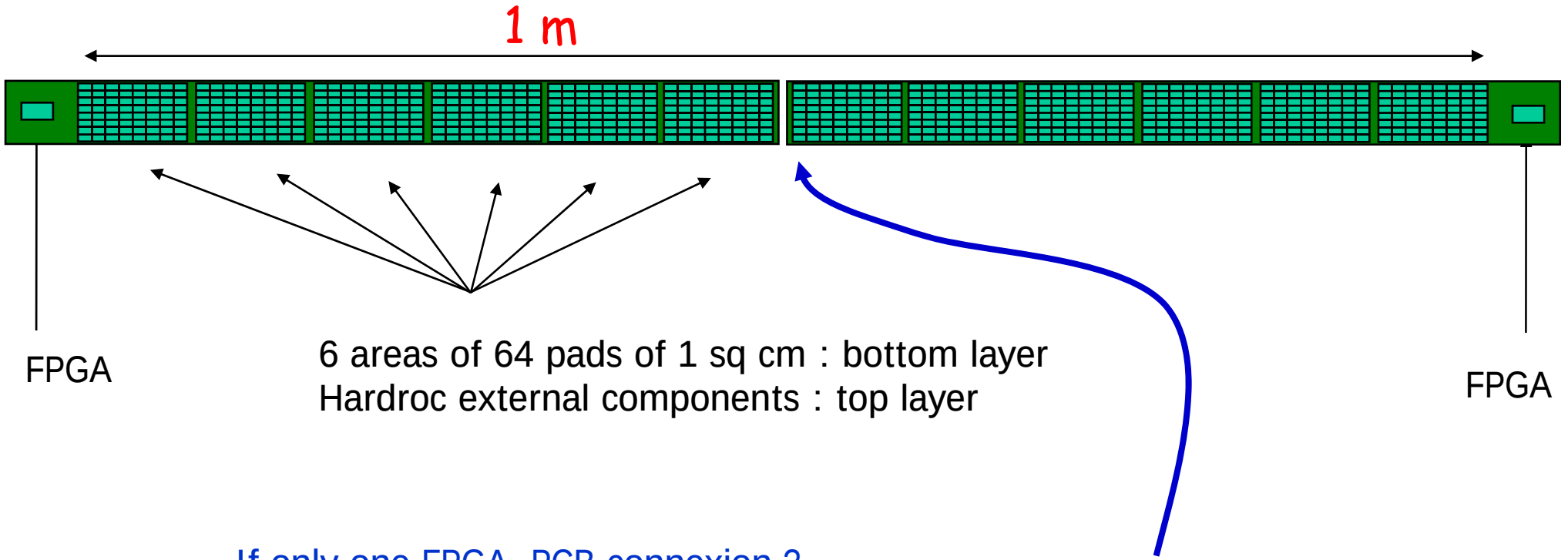
Design RPC PCB front end board prototype

- 4x64 1 sq cm pads
- 4 Hardroc Asics chained
- 1 FPGA to concentrate and send data using USB



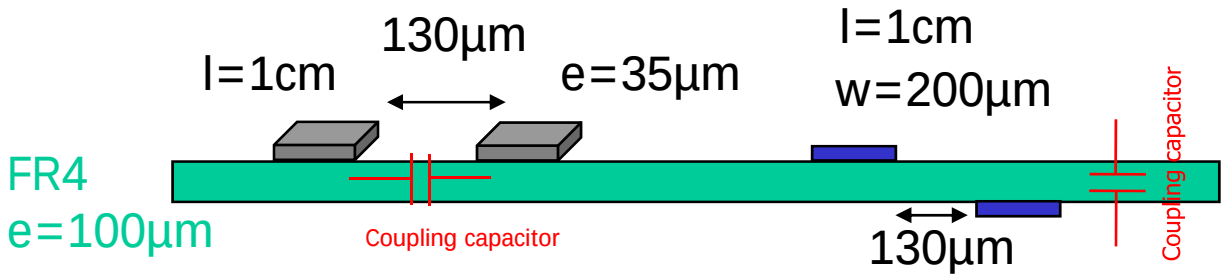
4 areas of 64 pads of 1 sq cm : bottom layer
Hardroc external components : top layer

LAYOUT DESIGN



If only one FPGA, PCB connexion ?
Others solutions can evaluated : 1 pcb for 1 Asic (see Christophe's talk)

Cross-talk in PCB



C=Er*E0*S/e

Cross-talk depends on coupling capacitor values

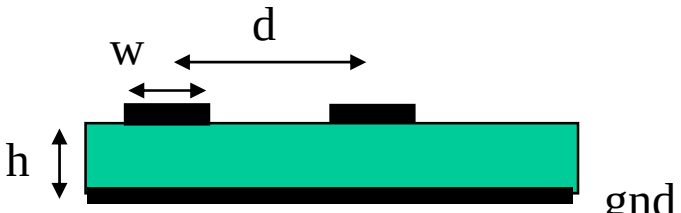
Er (FR4)=4.5 C=800fF/cm abacus gives 1 pF/cm for 2 path face to face

C is less than 1pF/cm in all other cases

Er (glue between 2 level of PCB)=4.5 C=100fF/cm first approximation

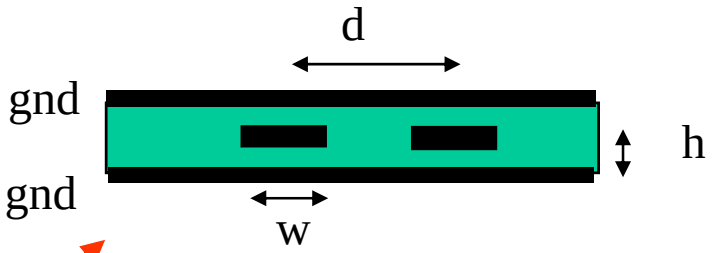
But the real calculation is more complicated (with abacus C = 500fF/cm)

Cross-talk increase as C increase and depends on PCB achitecture



h=100µm,w=200µm,d=330µm

C = 150 fF/cm



h=50µm,w=200µm,d=330µm

C = 50 fF/cm

Best way to reduce Xtalk

LAYOUT DESIGN

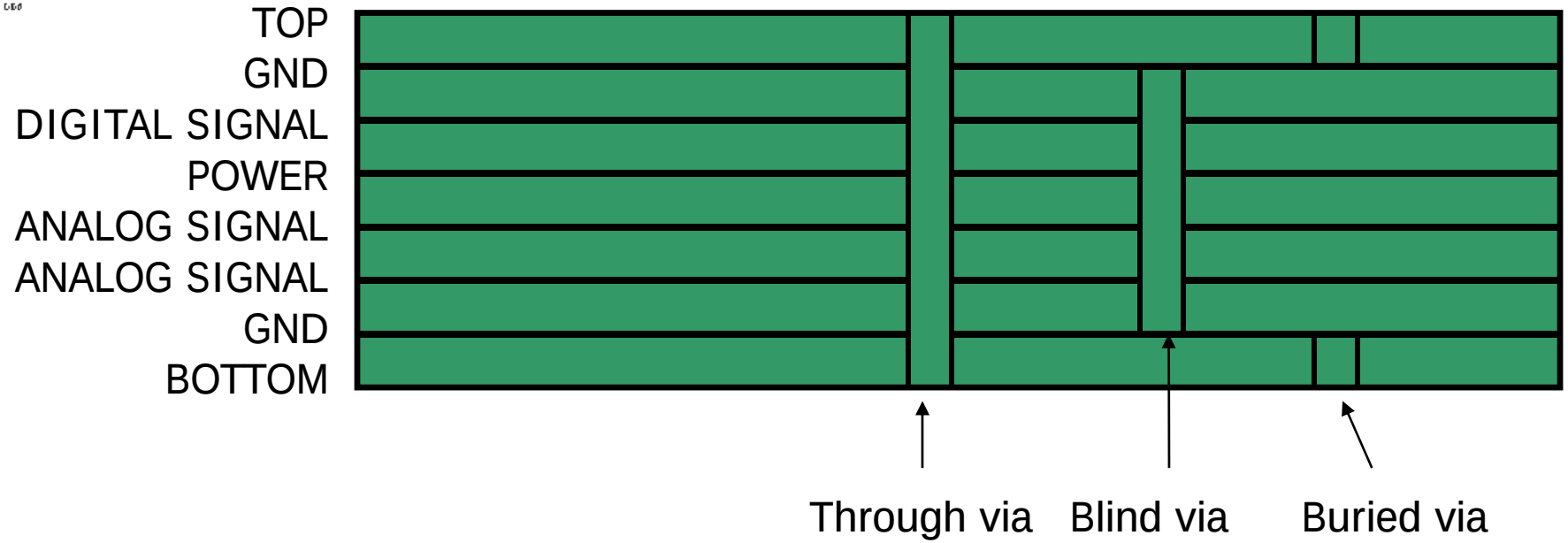
Prototype Design :

- PCB 8 layers for 2 blocks of 64 pads
- PCB 7 layers for 2 blocks of 64 pads (if we reduce Asics external components we can probably use 6 layers)
- PCB 8 layers with 2 GND layers added : not possible for this design

Prototype Design :

- PCB extra thin (0.8 mm in 8 layers and 0.6 mm in 6 layers)
- Special PCB with blind and buried vias
  - Bottom layer is free to accept RPC pads without constraints and vias
- Passive Component extra flat (0.3mm max except Hardroc in cqfp package)
- Total thickness 1.1mm

Layout in 8 layers (solution1)



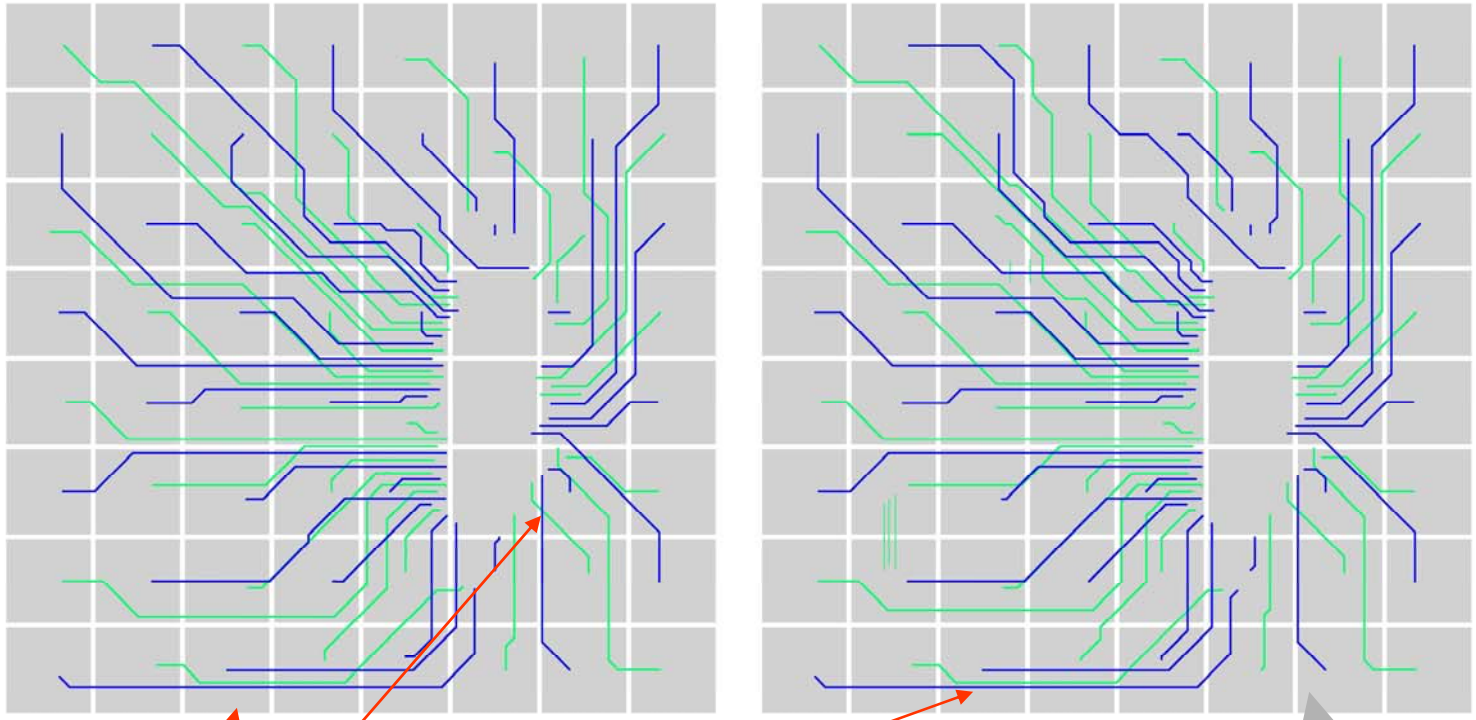
Layer definition (except FPGA area)

TOP LAYER	: Component layer
GND	: Ground layer and access to internal layers
DIGITAL SIGNAL	: Layer to interconnect hardroc and FPGA
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

Analog input and Pads (8 layers)

Track between pads and hardroc Input

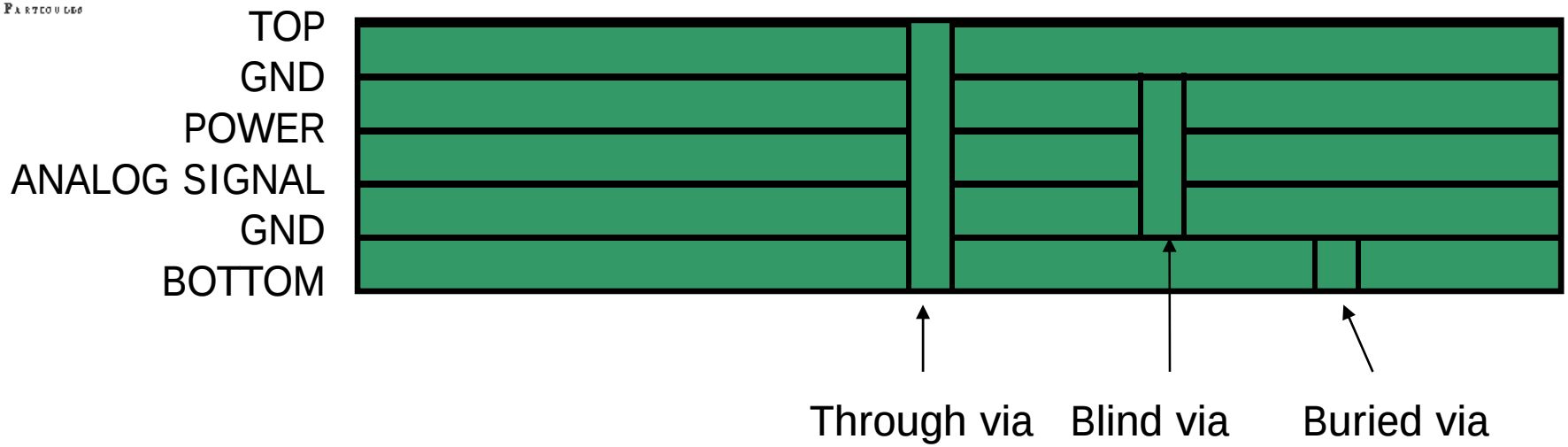
Track between pads and hardroc Input



Pads

We have to paid attention to this routing points

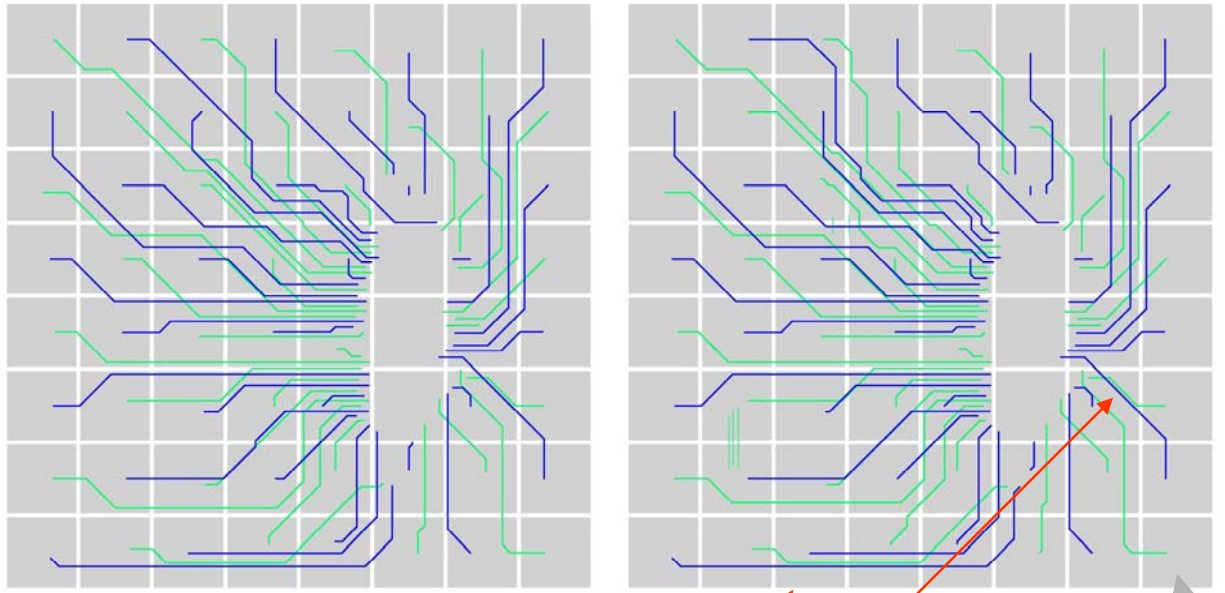
Layout in 6 layers (solution2)



Layer definition (except FPGA area)

TOP LAYER	: Component layer+interconnect between hardroc and FPGA
GND	: Ground layer and access to internal layers
POWER	: Power to hardroc
ANALOG SIGNAL	: Layer to interconnect pad signals
BOTTOM	: RPC pads layer

Analog input and Pads (7 layers)

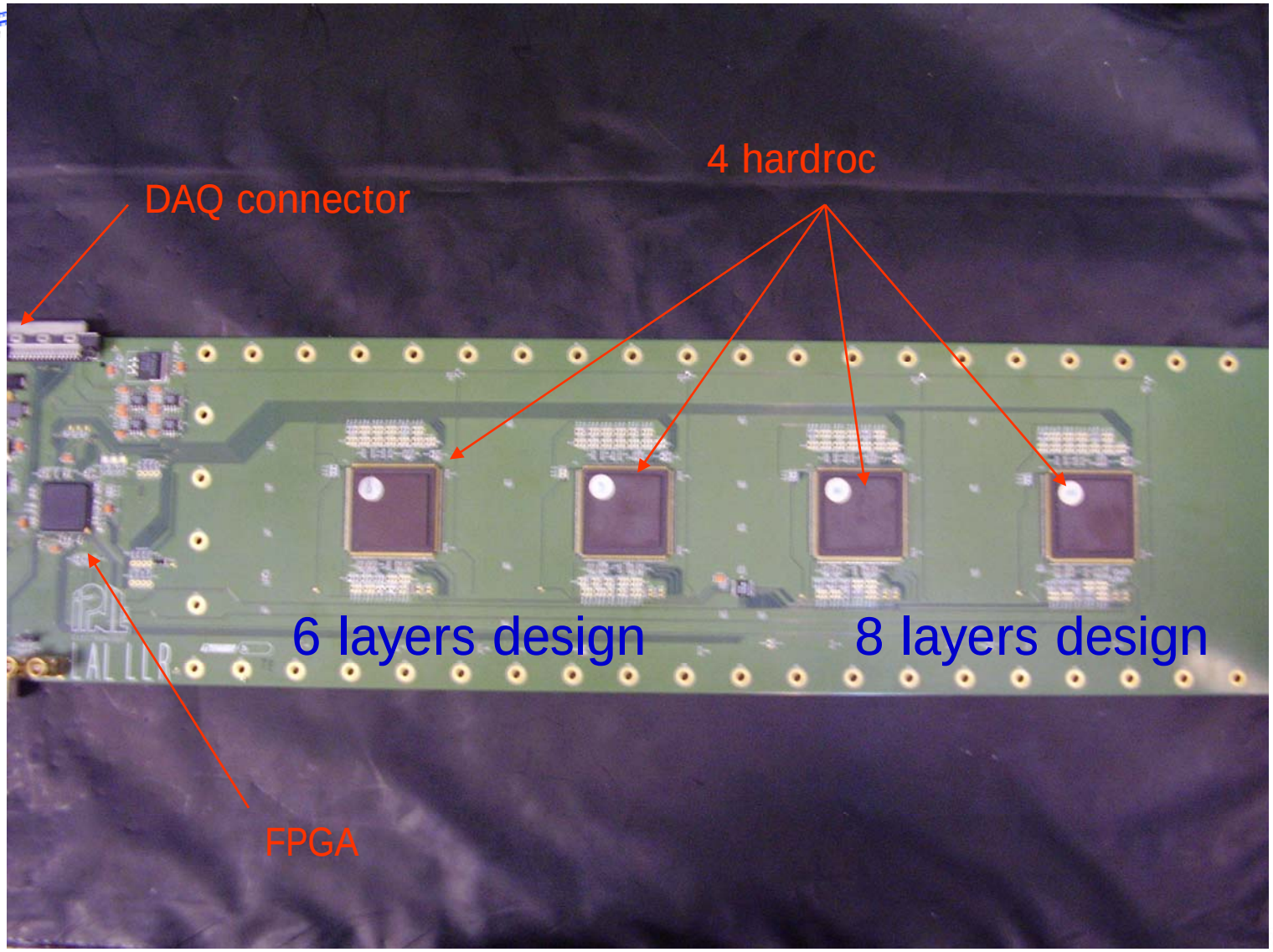


(Same picture as before, just to illustrate)
All tracks are on the same layer

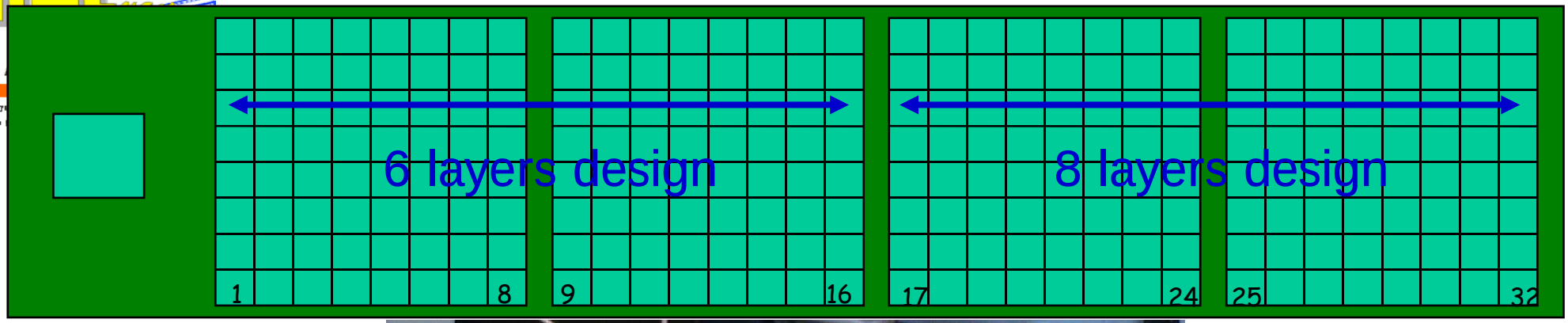
Pads

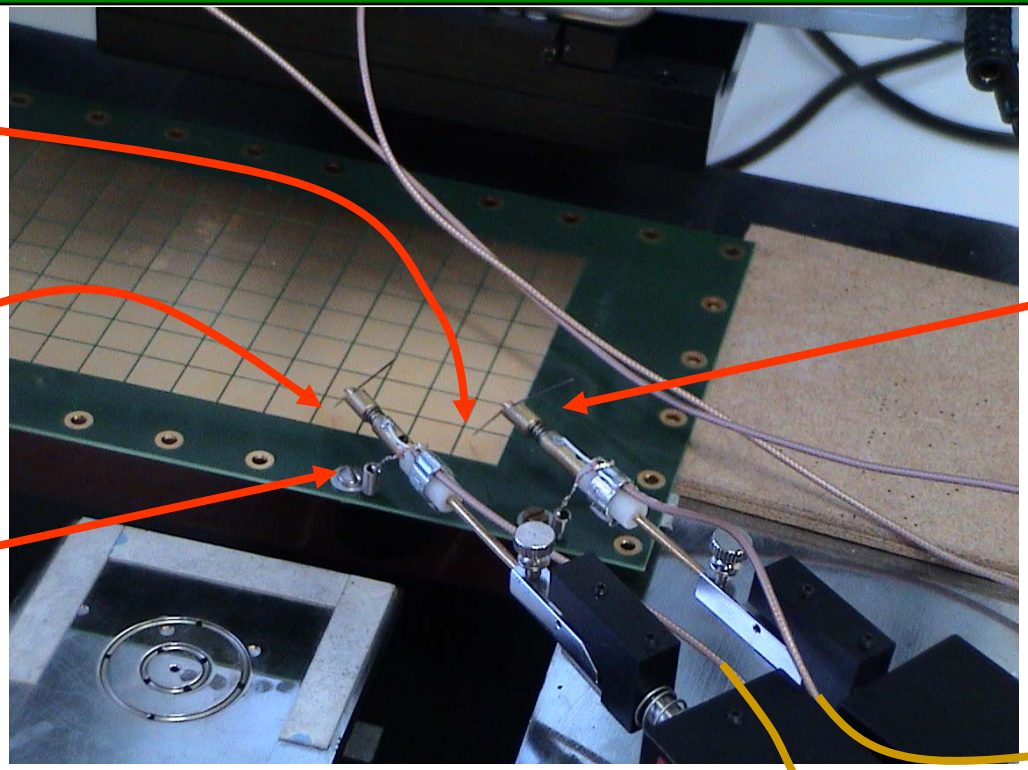
We have to paid attention to this routing points

Board with components



Setup Xtalk measurement





Injection Pad

Measurement Pad

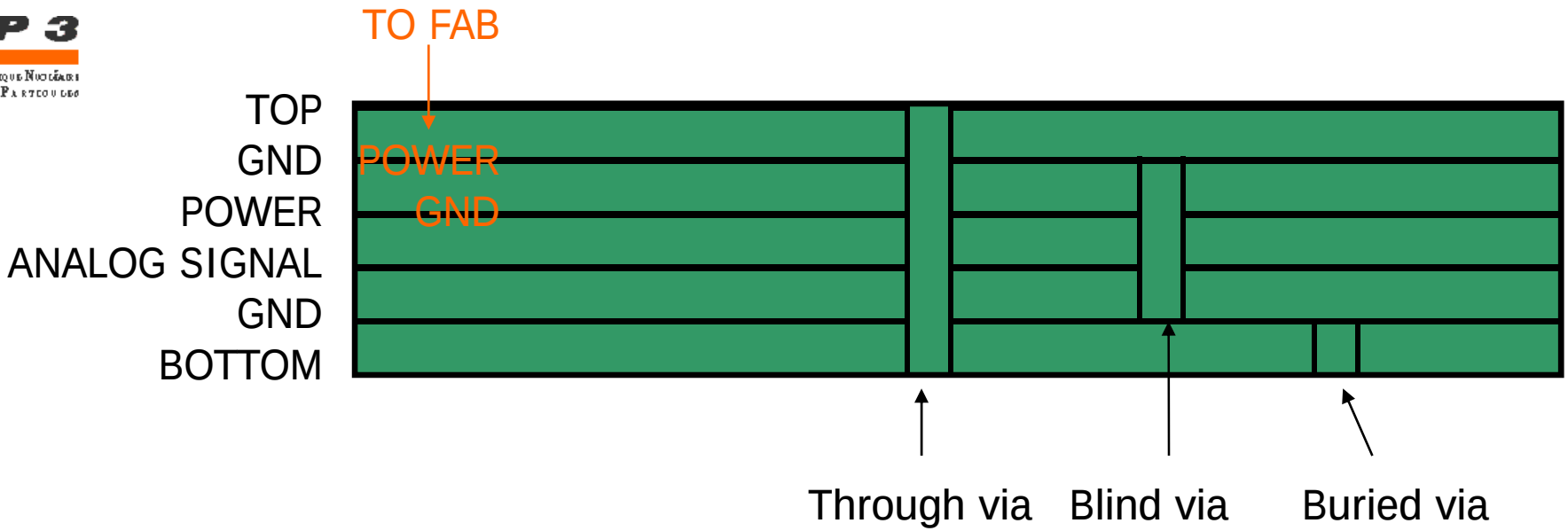
Shield connection

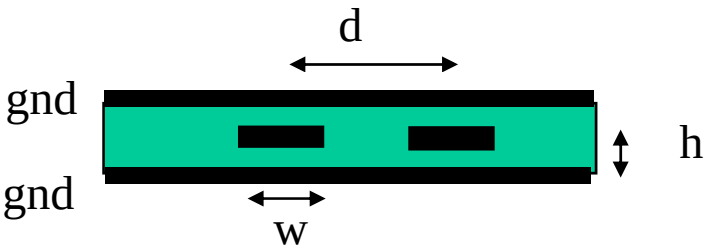
10 µm probe

From Square wave Generator

To scope

Layout in 6 layers (2 parallels paths on 1 layer)

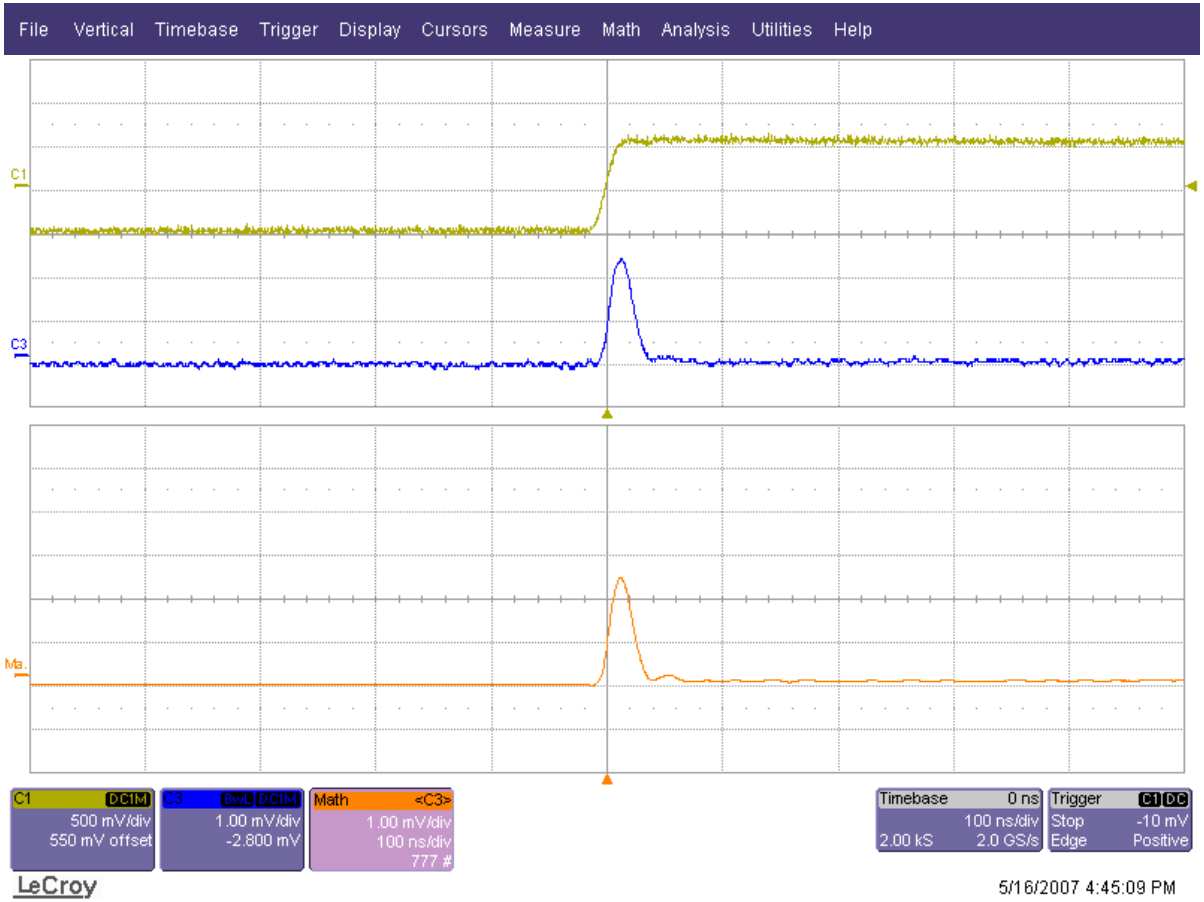




h=50µm,w=200µm,d=330µm

C = 50 fF/cm

Layout in 6 layers (2 parallels paths on 1 layer)



Input

Measure

Average of Measure

PCB 6 Layers : 2 parallels paths

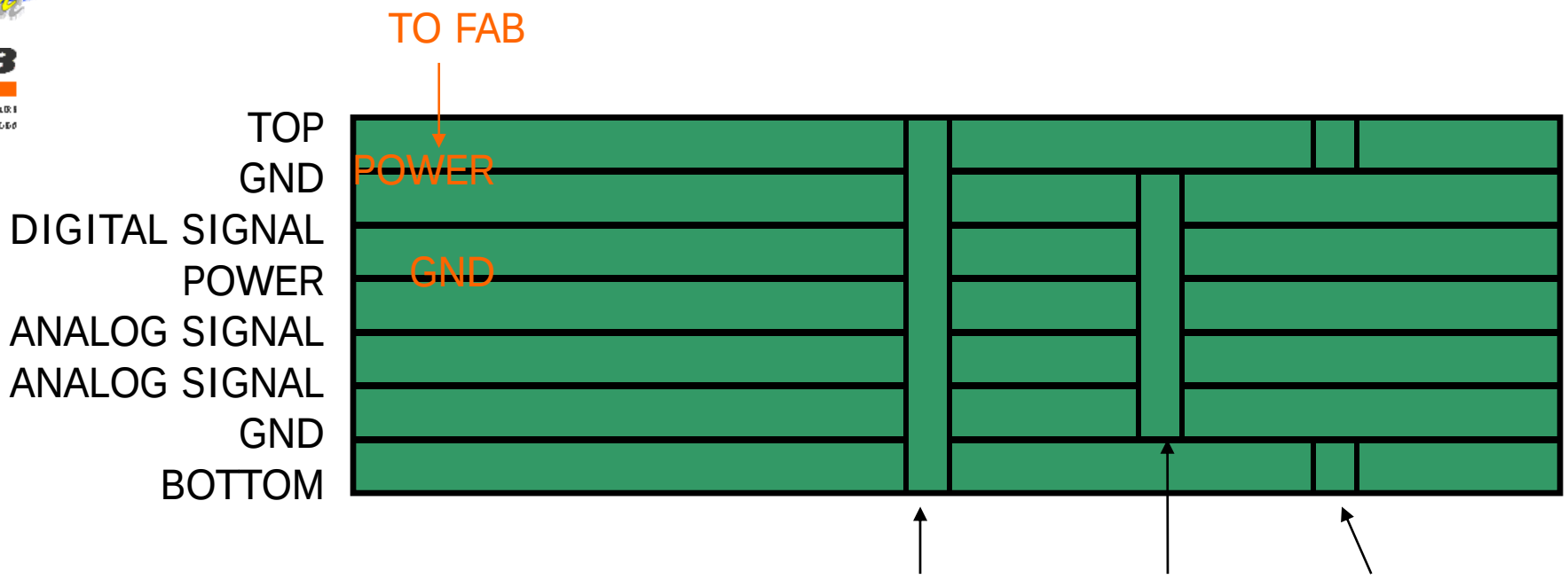
Hardroc Pin 2-3 (50 Ohms to GND) Pad 6-8

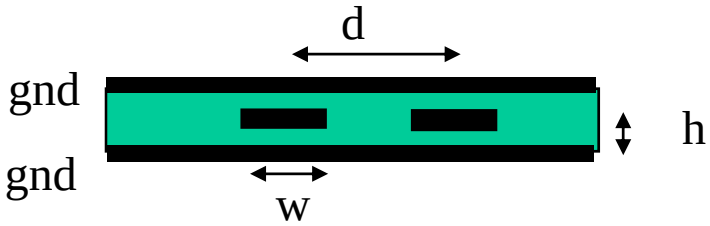
Input on Rpc Pad = 1V

Measure = 3.5 mV

Xtalk = 0.35%

Layout in 8 layers (2 parallels paths on the same layer)

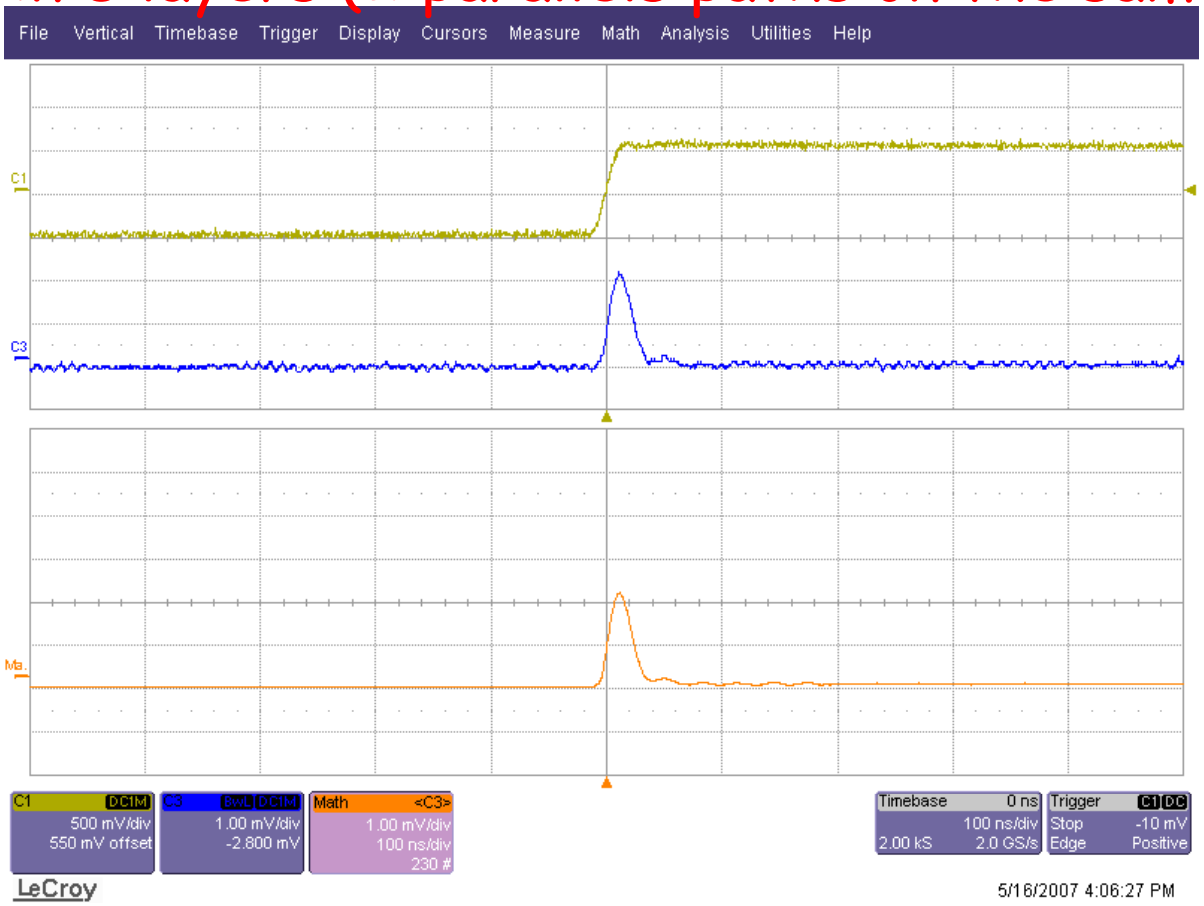




h=200µm ,w=200µm,d=330µm

C = 120fF/cm

Layout in 8 layers (2 parallels paths on the same layer)



Input

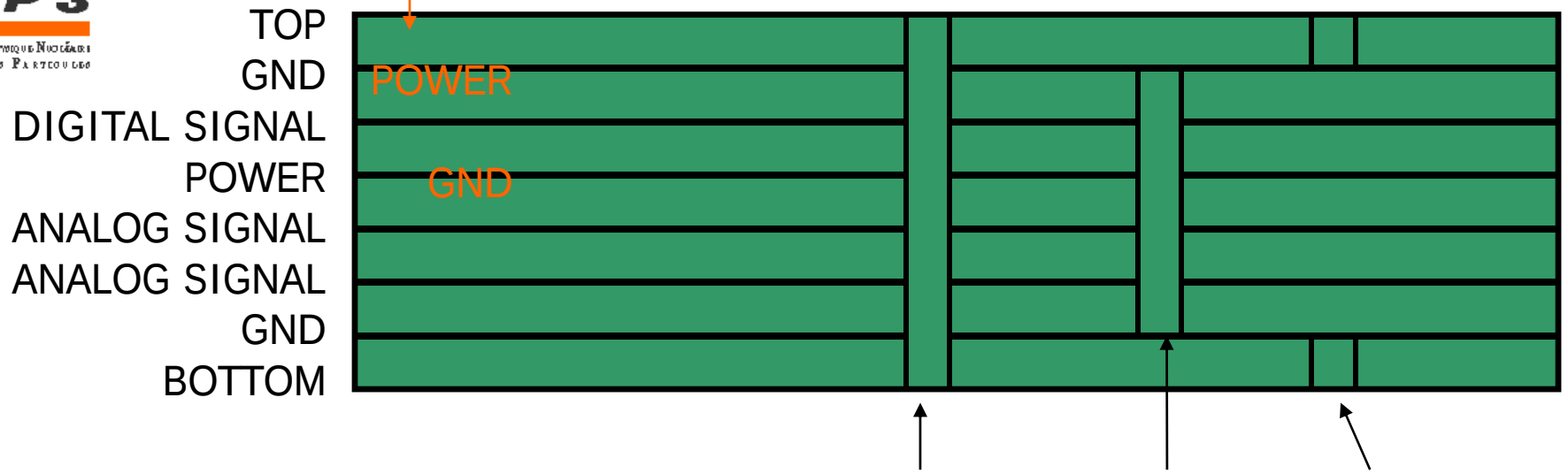
Measure

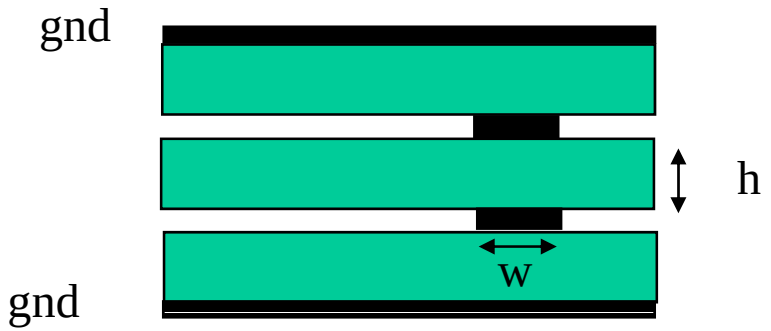
Average of Measure

PCB 8 Layers : 2 parallels paths on the same layer
Hardroc Pin 2-3 (50 Ohms to GND) Pad 22-24
Input on Rpc Pad = 1V
Measure = 4 mV

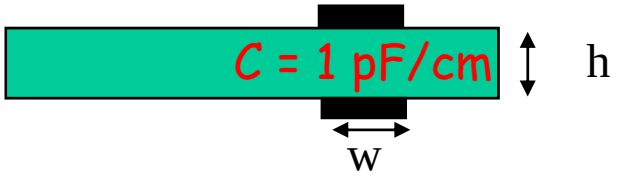
Xtalk = 0.4%

Layout in 8 layers (2 face to face paths on 2 layers)
(Not on the total lenght)





h=100µm,w=200µm

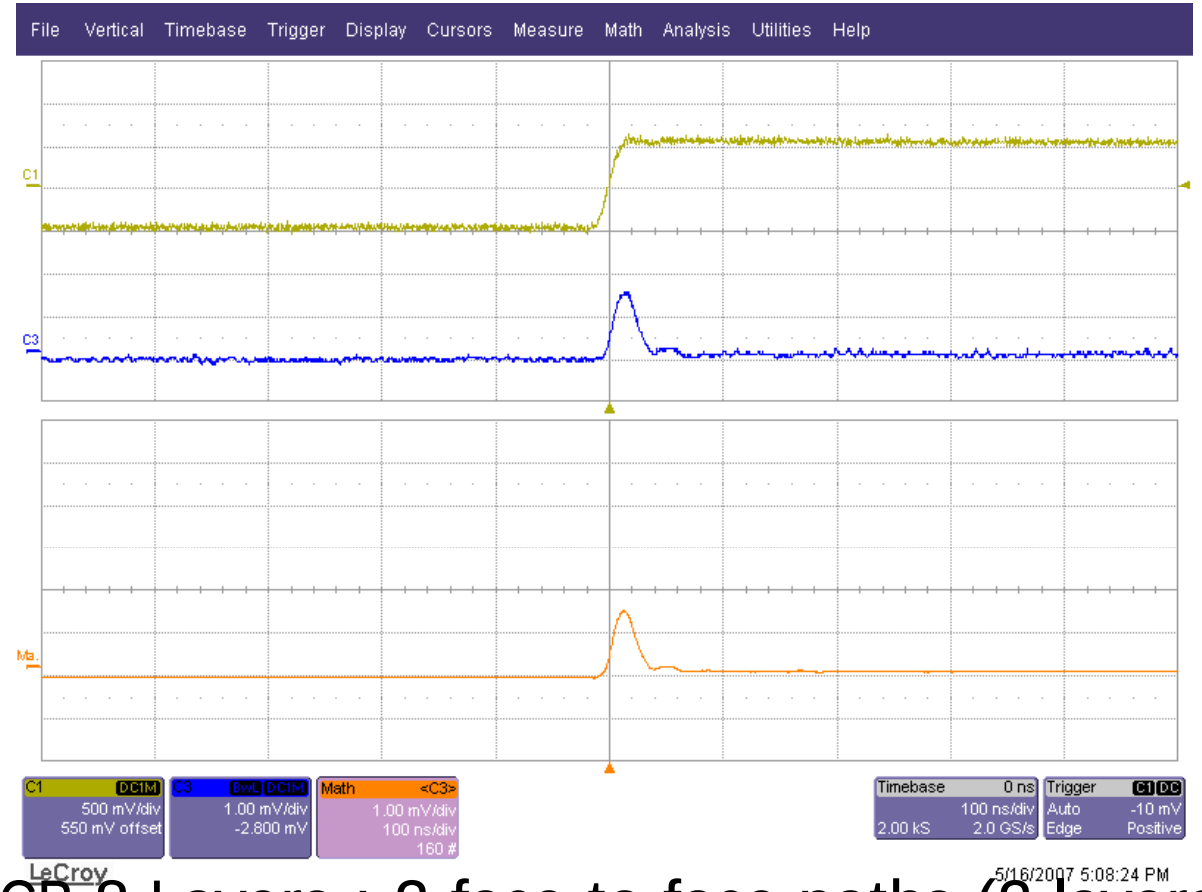


Convoluted With

Tracks between
2 gnd Layer

120fF/cm < C < 1 pF/cm

Layout in 8 layers (2 face to face paths on 2 layers) (Not on the total lenght)



Input

Measure

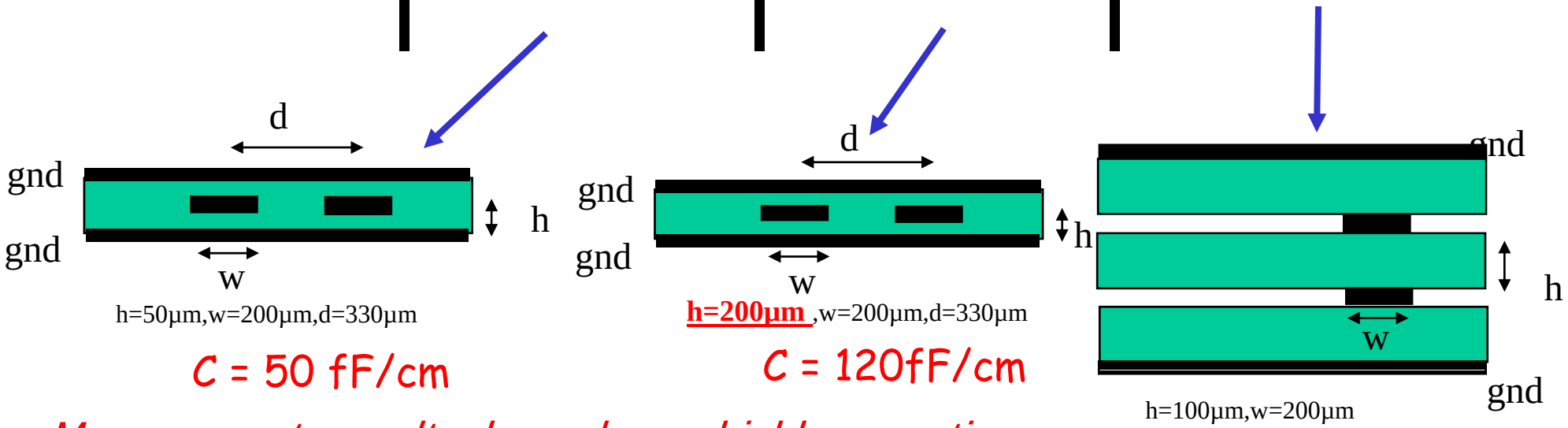
Average of Measure

PCB 8 Layers : 2 face to face paths (2 layers)
Hardroc Pin 2-7 (50 Ohms to GND) 29-32
Input on Rpc Pad = 1V
Measure = 1.5 mV

Xtalk = 0.15%

Xtalk summary

	6 layers	8 layers same layer	8 layers 2 diff layers
Coupling Cap	50 fF/cm	120 fF/cm	120fF/cm to 1pF/cm
Xtalk	0.3 %	0.4%	0.3%



Measurements results depends on shield connection
Difficult to conclude what configuration is the best
Xtalk < 0.5%

Conclusion

Xtalk measurement

- PCB Xtalk difficult to mesaure but less than 0.5%
- Major part of Xtalk will be in the ASIC Chip
- We can probalably use a 6 layers design

PCB status

- 6 boards manufactured
- 3 boards with there components
- 1 of this 3 boards is use to debug hardware and firmware
- 3 boards without components