Design of a 16 bit ΣΔ DAC for ECAL calibration Status report

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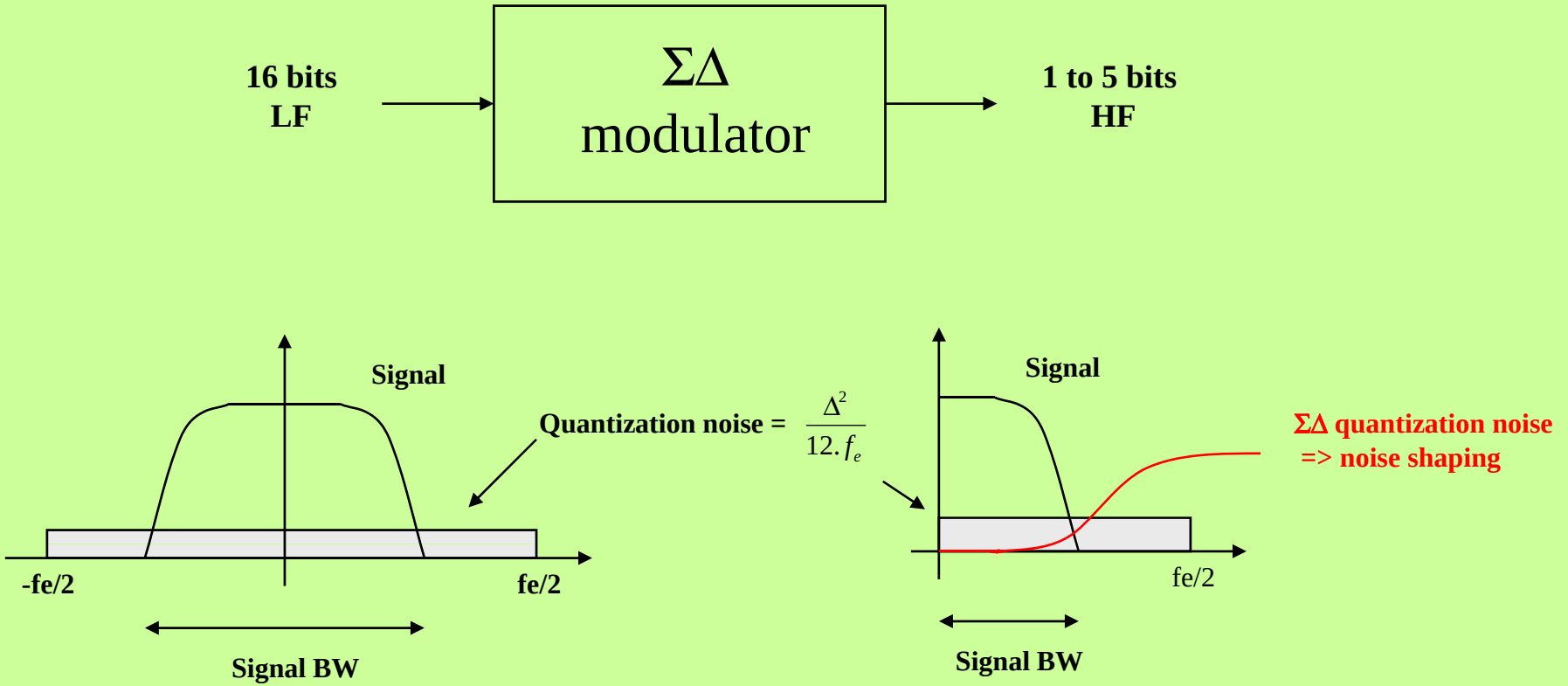
- **Theory**
  - ΣΔ modulators
  - 1st order modulator implementation
- **Design**
  - Modulator
  - Dynamic Element Matching
  - SC DAC
  - SC Filter
- **Conclusion – Remaining tasks**

ΣΔ converter theory oversampling and noise shaping



Signal to Noise Ratio of ideal converters

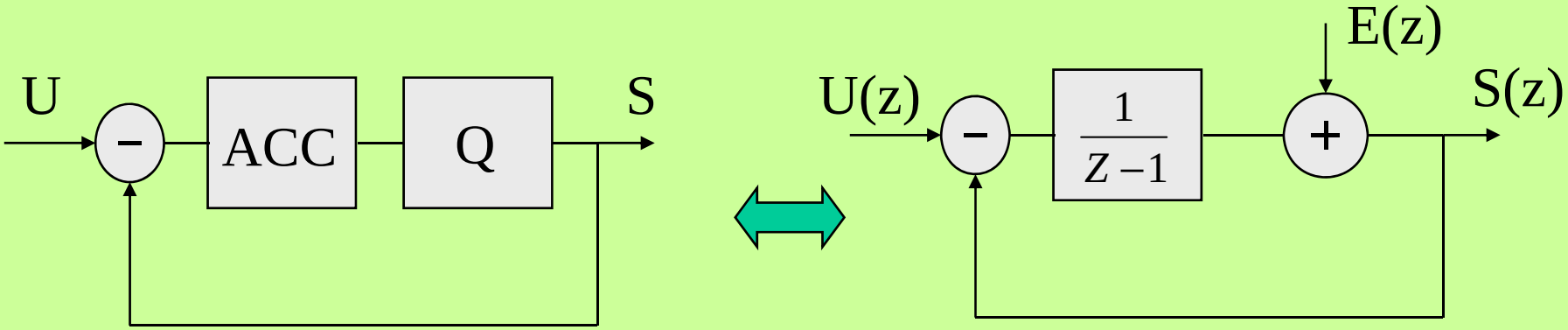
Nyquist rate converters : $SNR_{db} = 6.02 \times N + 1.76$

Oversampled converters : $SNR_{db} = 6.02 \times N + 1.76 + 10\log(OSR)$

ΣΔ converters : $SNR_{db} = 10\log(3\frac{2k+1}{\pi^{2k}} \times 2^{2N-1} \times OSR^{2k+1})$

with
- N : number of bit
- OSR : oversampling ratio
- k : modulator order

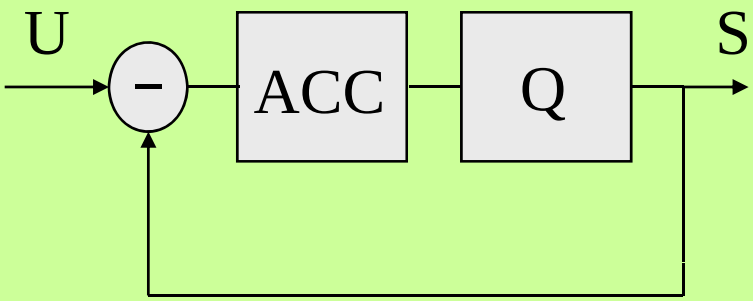
First order ΣΔ modulator
DAC implementation (1)

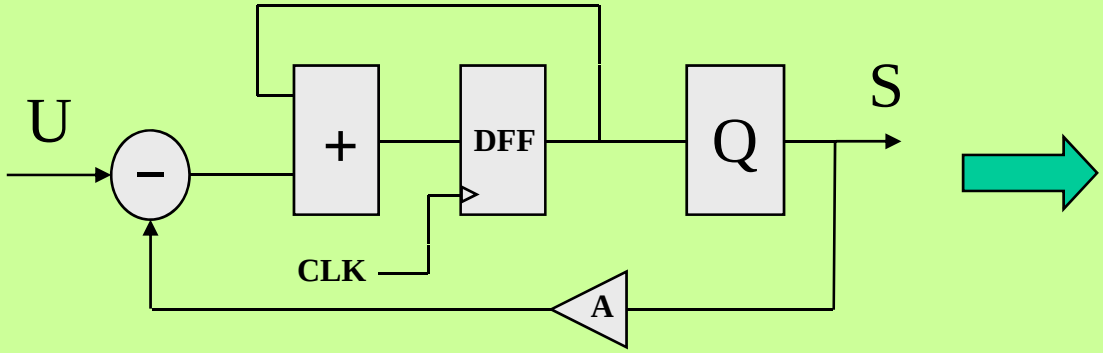


E(z) : quantization noise

$$\begin{cases} S(z) = z^{-1}U(z) + (1 - z^{-1})E(z) \\ STF = Z^{-1} \\ NTF = 1 - Z^{-1} \text{ (high pass filter)} \end{cases}$$

First order ΣΔ modulator DAC implementation (2)

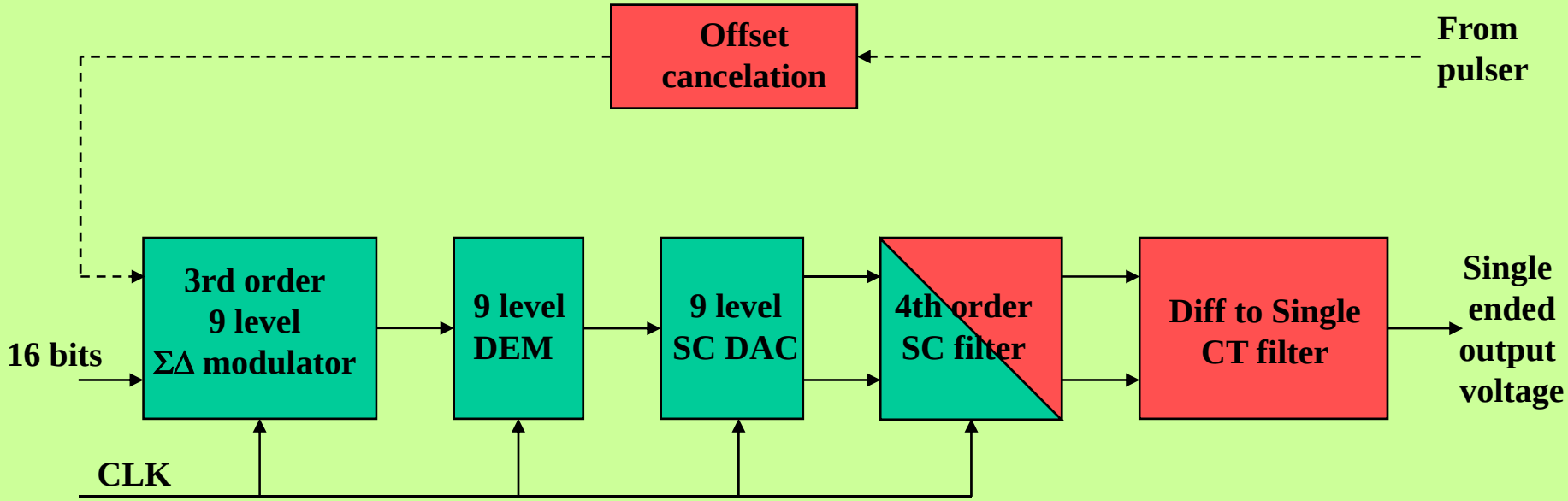




Standard CMOS techno.
VHDL implementation

The output S can be single or multi-bit.

A 16 bit ΣΔ DAC block diagram



A 16 bit ΣΔ DAC
3rd order, 9 level modulator (1)

A 96 dB SNR is necessary to achieve a 16 bit resolution.

A 3rd order, 9 level (3.2 bit) modulator leads to a SNR :

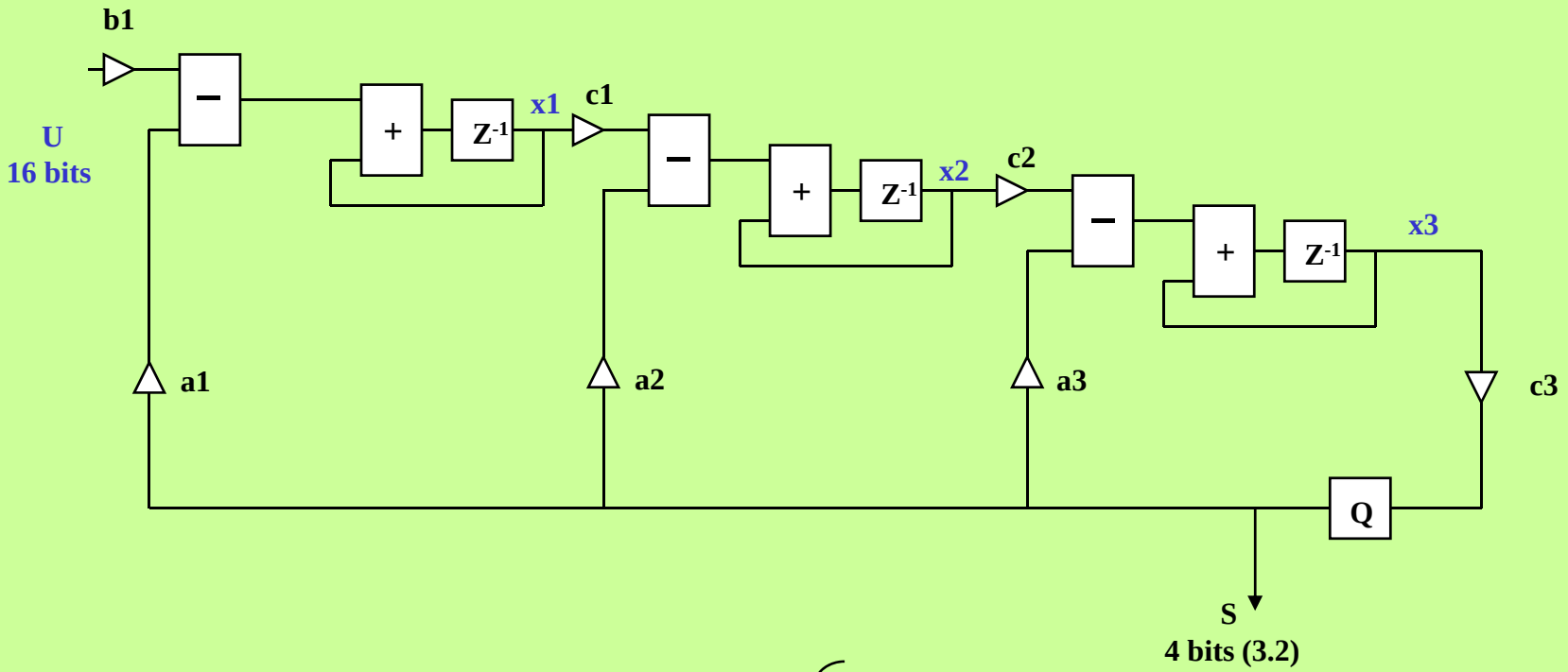
168dB for OSR=256
147dB for OSR=128
126dB for OSR=64

} => related to the SC filter design (settling time).

Multi-bit : SC filtering and OPA constraints are relaxed
quantization noise is reduced,
a DEM is necessary to reduce the DNL effect of the 9 level DAC.

The modulator was designed using the Matlab toolbox written by R. Schreier

A 16 bit ΣΔ DAC
3rd order, 9 level modulator (2)



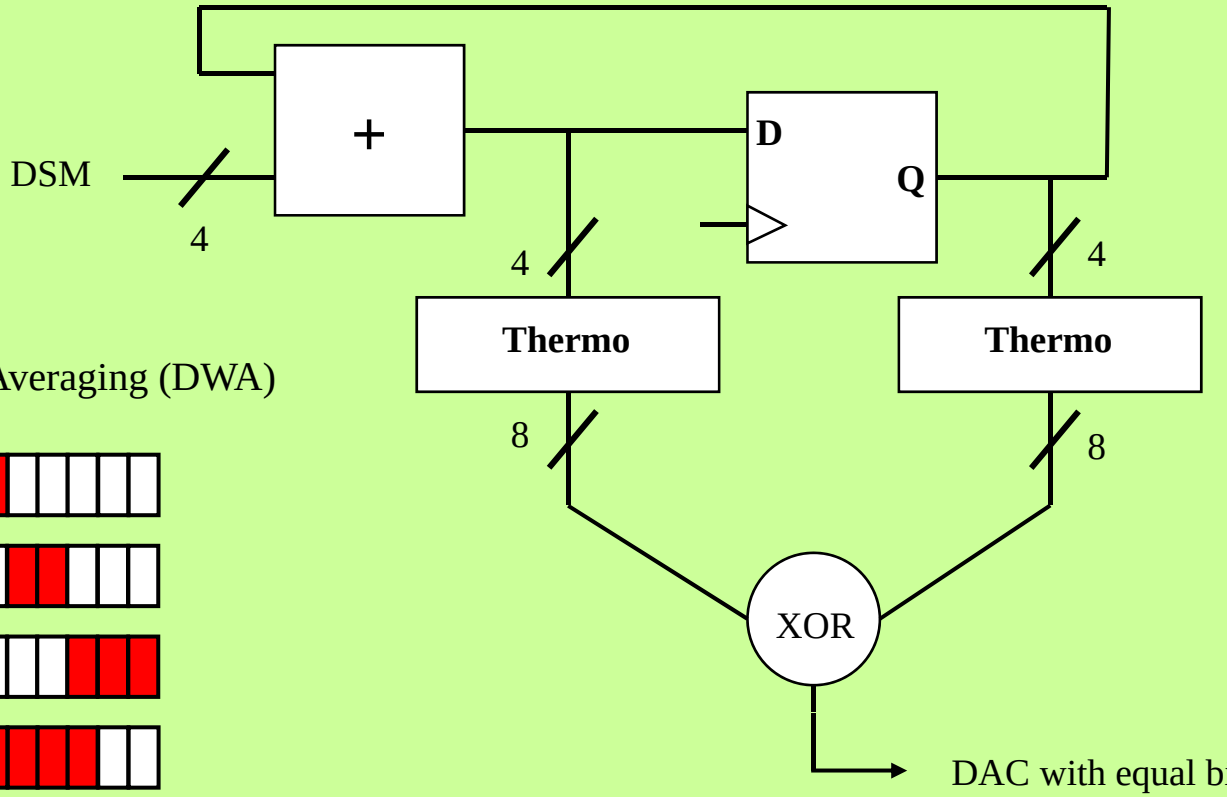
VHDL implementation

Can also be simulated using C language

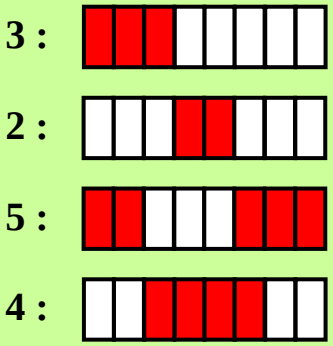
```
S=c3*x3;
if (S>4) S=4;
if (S<-4) S=-4;
x3=x3 + c2*x2 - a3*S;
x2=x2 + c1*x1 - a2*S;
x1=x1 + U - a1*S;
```

Adders overflow is not simulated with this code.

A 16 bit ΣΔ DAC
Dynamic Element Matching (1)



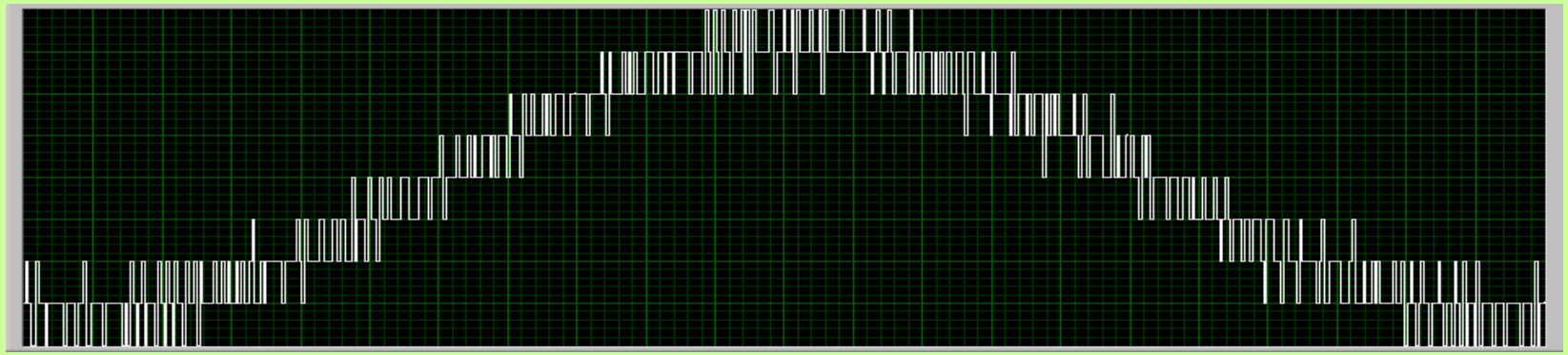
Data Weighted Averaging (DWA)

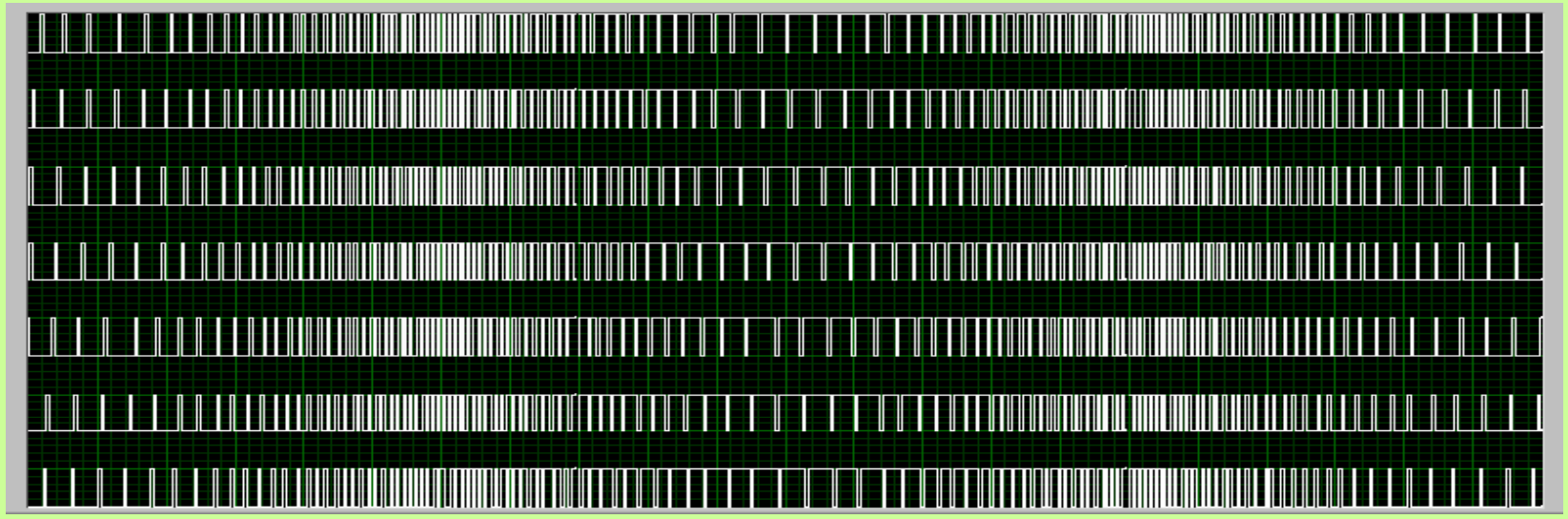


Random re-mapping turns elements mismatch into white noise.

DWA re-mapping shapes DAC errors noise.

A 16 bit ΣΔ DAC
Dynamic Element Matching (2)





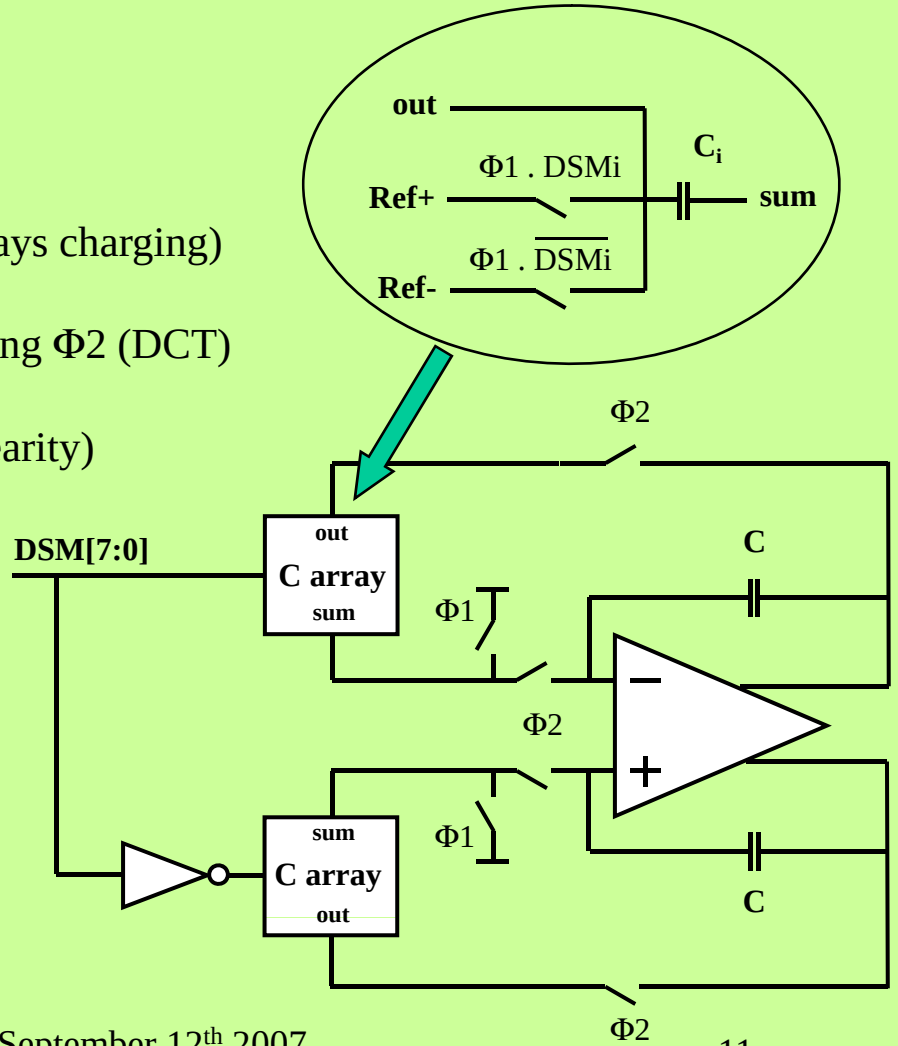
A 16 bit ΣΔ DAC
SC DAC

Based on Direct Charge Transfer (DCT) :

- DAC operation is performed during Φ1 (capacitor arrays charging)

- Charges are shared with the feedback capacitor C during Φ2 (DCT)

- Ref voltage is limited by the OPA dynamic range (linearity)



Low pass DCT :

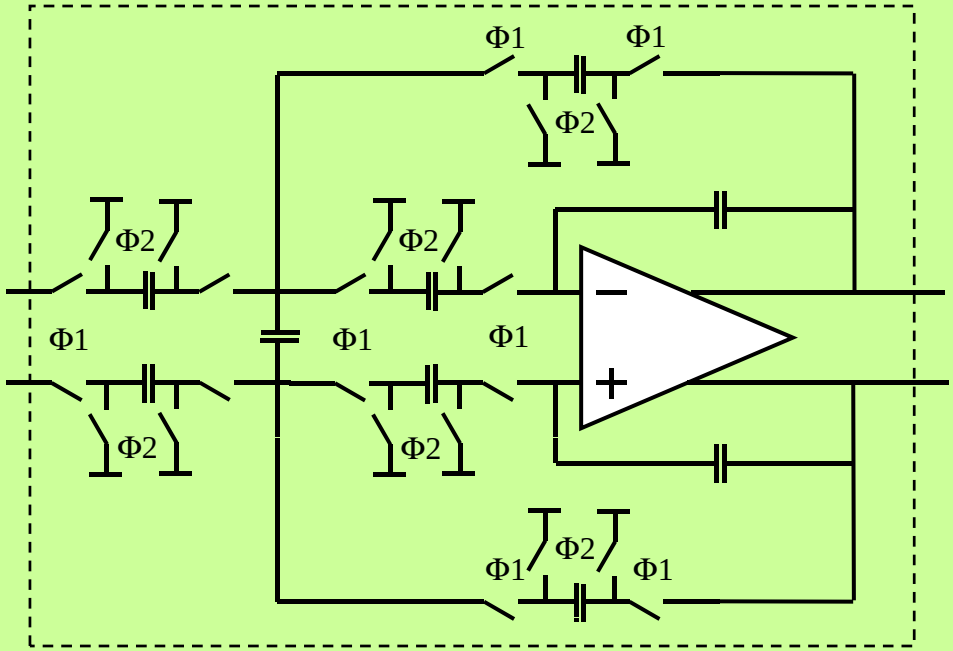
$$H(z) = \frac{1}{1 + a - a \cdot z^{-1}}$$

$$a = \frac{C}{\Sigma c_i}$$

A 16 bit ΣΔ DAC
SC Filter

4th order, SC direct implementation of a MFB Butterworth Filter (Fc = 2kHz)

- Two 2nd order filter cascaded
- Two differential OPA



A 16 bit ΣΔ DAC
Differential OPA (1)

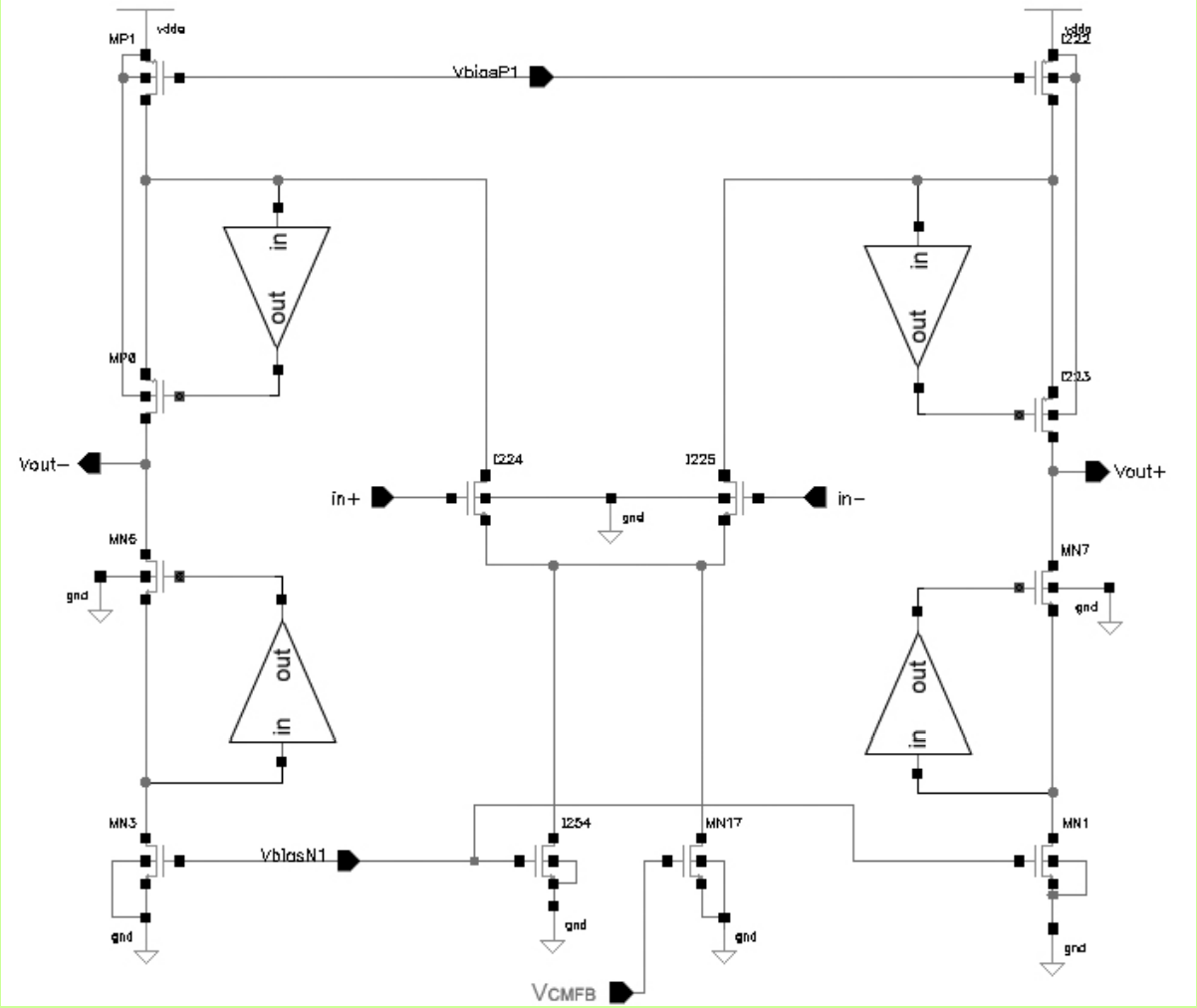
The OPA used in the SC DAC and in the SC Filter was designed (D. Dzahini) to be implemented in 12 bit , 25MHz ADCs.

The main features of this OPA are :

- Open loop gain : 100dB
- Gain-band product : 130MHz
- Dynamic range : 1.6V
- Power consumption : 6mW (3 instances required => 18mW)

Simulations have to be carried out to reduce the power consumption.

A 16 bit ΣΔ DAC
Differential OPA (2)



A 16 bit ΣΔ DAC
Remaining tasks

- Simulations have to be carried out to complete the SC filter design :
  - filter topology & response
  - OPA power consumption

- The output stage has to be designed :
  - differential to single ended converter (if implemented in the 1st proto)
  - CT filter (if implemented in the 1st proto)
  - output buffer (s)

- Pulser & Offset cancellation : ?
  - Pulser specification and design (who ?)
  - The modulator has an offset cancellation capability, its control depends on the pulser design.

A first prototype will be submitted to the January 2008 run