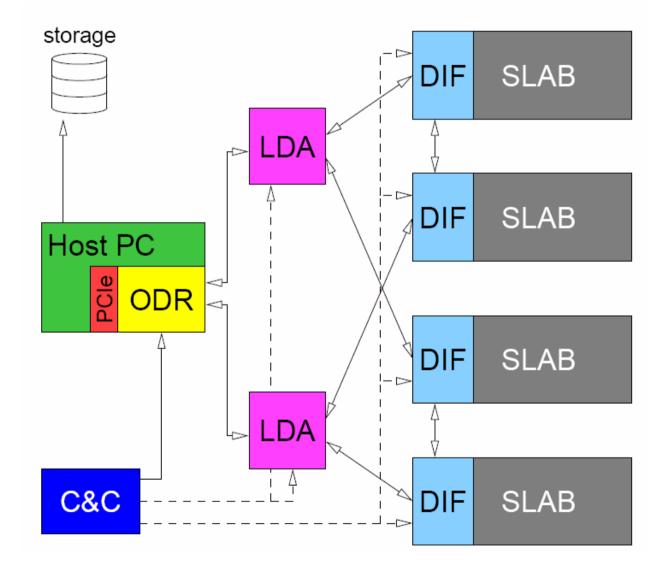
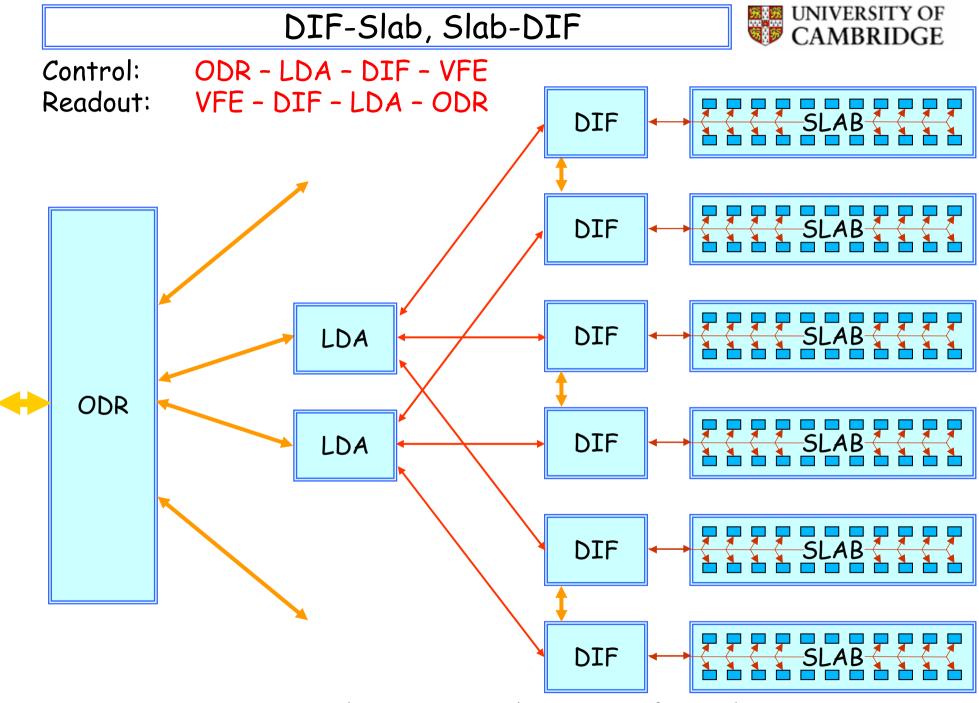
ECAL DIF: Issues & Solutions

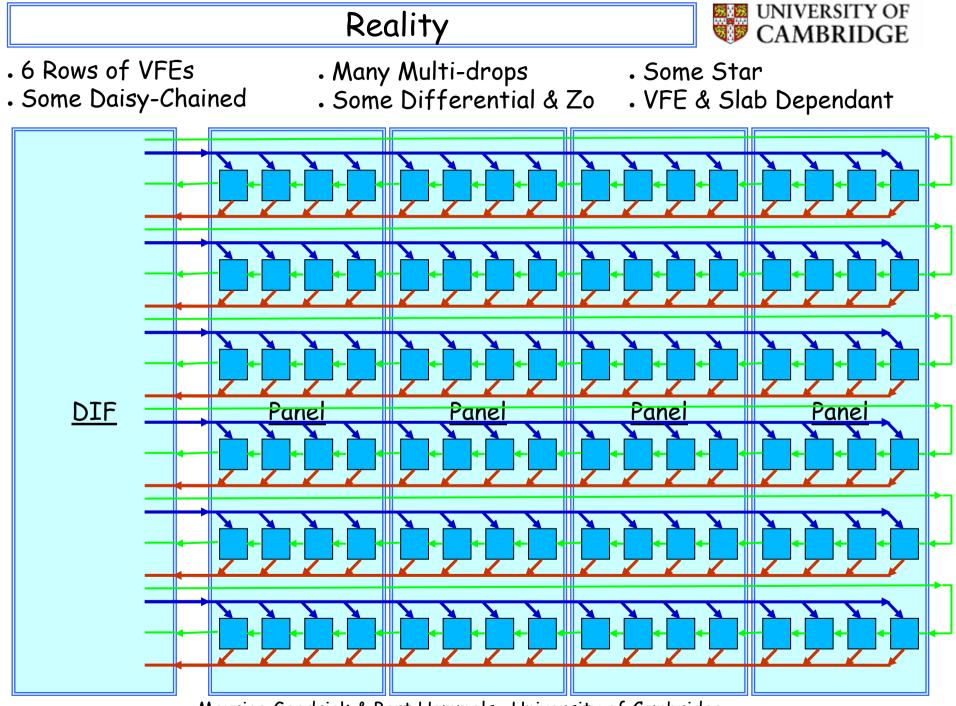


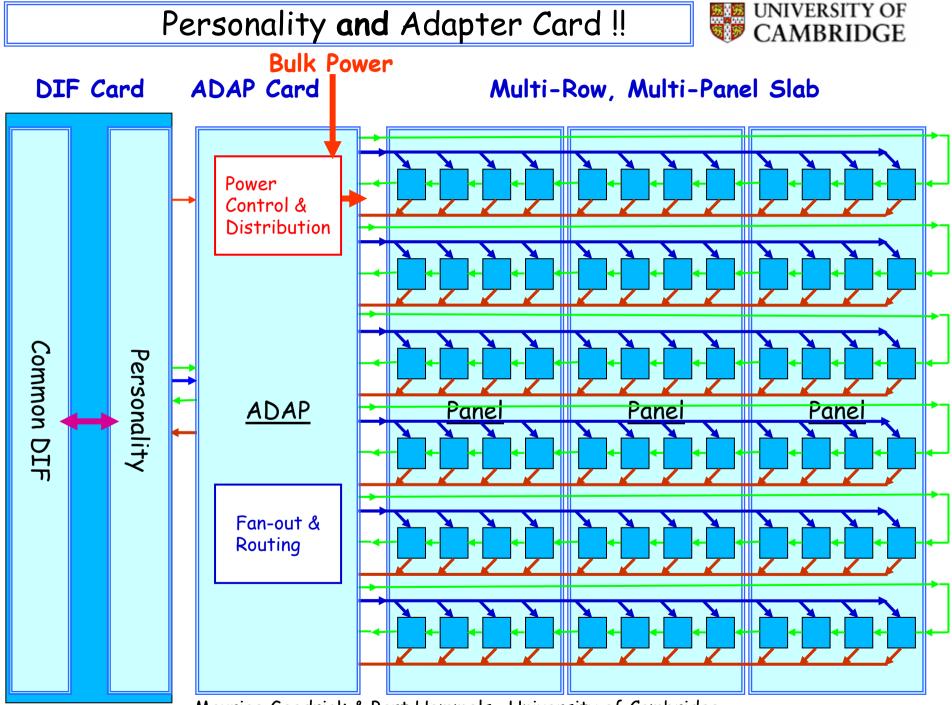
Readout Architecture





Maurice Goodrick & Bart Hommels , University of Cambridge





= A Multi Purpose DIF for ECAL



Should Support:

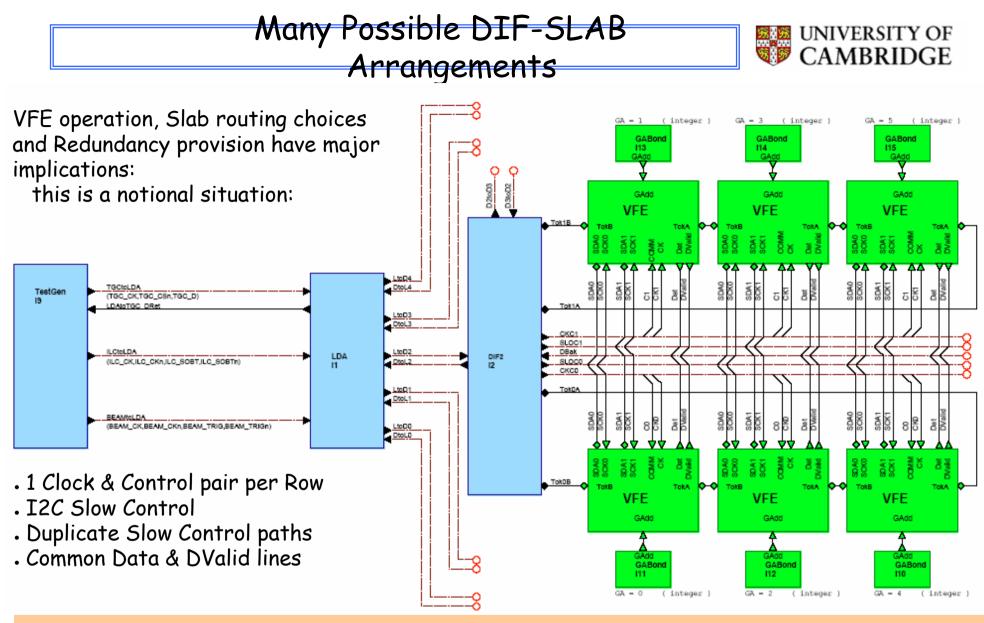
.Test Slab in the Lab - WP2.2 core work

.EUDET prototype in the lab

.EUDET prototype in Test Beam

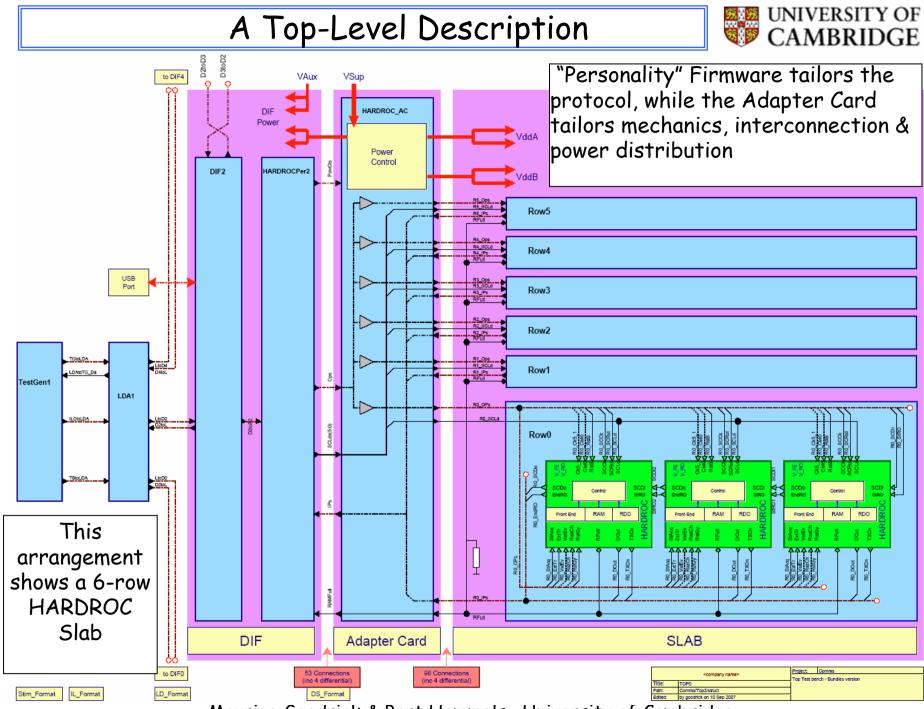
.Next ASICs

.Test bed for ILC environment



We will encounter a large number of different arrangements thanks to permutations of:

- . VFE variants: HARDROC, SKIROC, ,, with their iterations
- . Evolving Slab designs

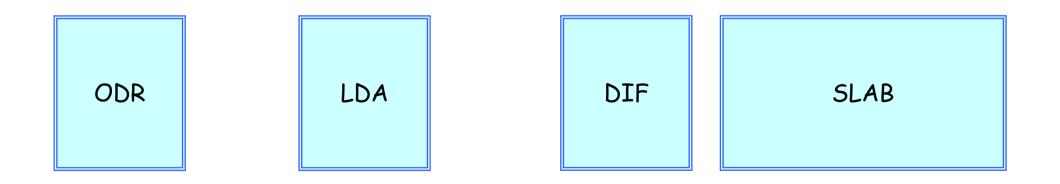


VHDL



It is very worthwhile adopting a VHDL description at this stage:

- behavioural description provides key framework:
 - . will prove the viability of the scheme
 - will allow fine tuning
 - allows rapid description and testing of different flavours for different tasks (Test Panel, EUDET Prototype, ...)
- specific VFE VHDL code can be included (as has been done for HARDROC)

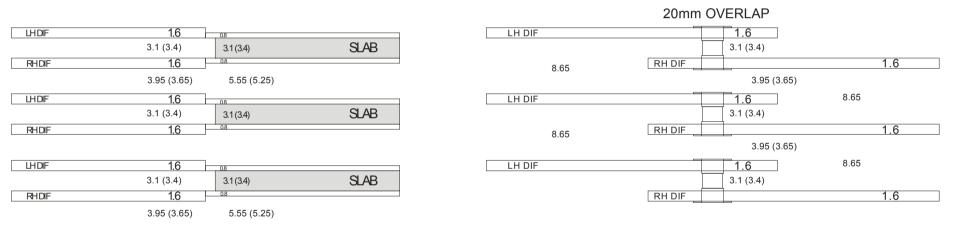






Card Spacing: based on Marc Anduze's ECAL Module design

NOMINAL SPACINGS (ADAPTER CARDS IGNORED)

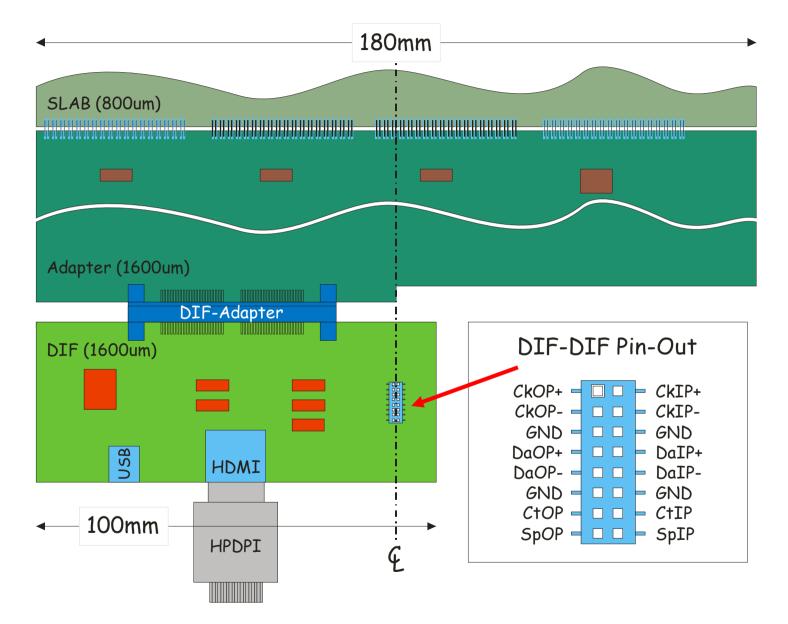


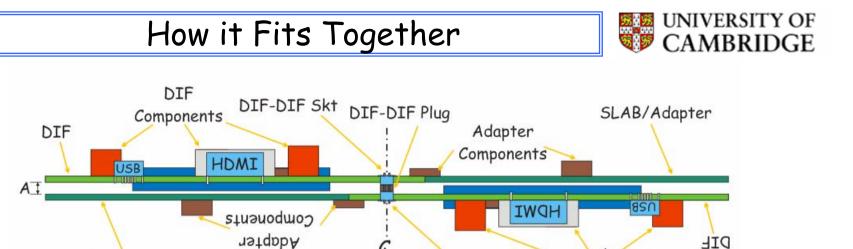
Side View

Rear View

A Layout







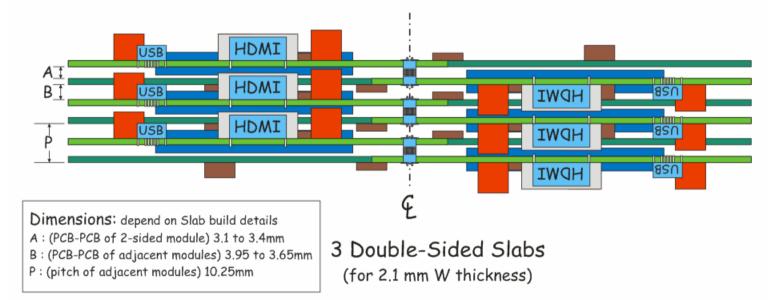
DIF-DIF Skt

stagnoquos

The rotation routes DIF-DIF Outputs to Inputs and, combined with the lateral asymmetry, gives head room for components

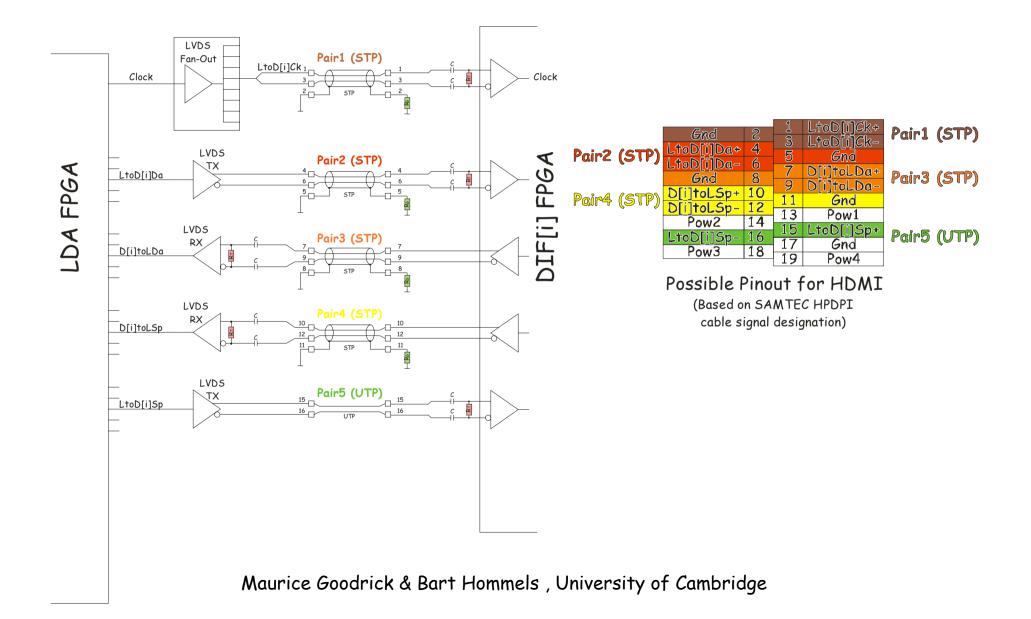
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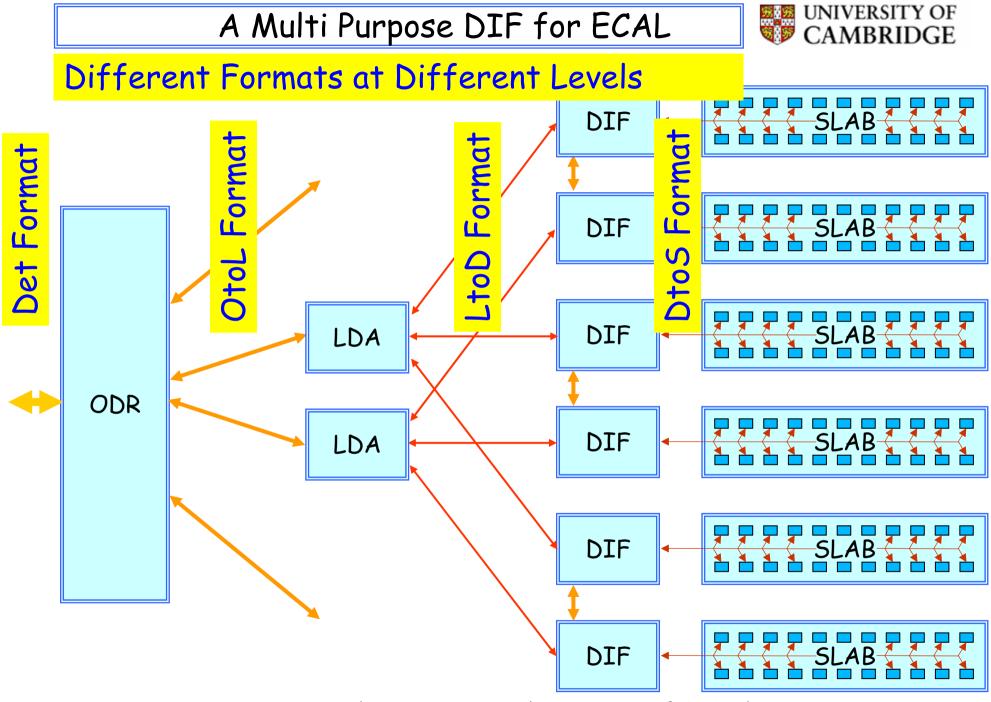


LDA-DIF Cable and Connector





- We are producing a Multi-purpose DIF for ECAL
- We are working on the Adapter Card and Personality to allow it to be used for further Slab signal path studies using the existing Test Panel
- It will support laboratory work with prototype Slabs with different
 VFE chips and their different iterations
- . It will be usable with single and multiple EUDET ECAL modules
- The VHDL model should be an invaluable testbed for modelling different VFEs and Slabs
- . It should also allow command and data structures to be tested
- . We welcome discussion with other interested groups



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