ASU and standalone test setup for ECAL

MAIA BEE project

Overview
DAQ dedicated Sensor test
In situ debug and maintenance DAQ on beam

LPC LAL LLR

MAIA BEE
(Y)

M aintenance
A pparatus
I ncluding (data)
A cquisition (on)

B eam (for)
E UDET
E CAL

{ASUDAQ, ISDDAQ} = MAIA BEE

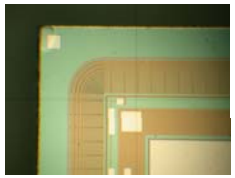
ASUDAQ = ASU DAQ

ISDDAQ = In Situ Debug DAQ (of one SLAB)

Ongoing work at LPC
from Wafer to data acquisition for ECAL

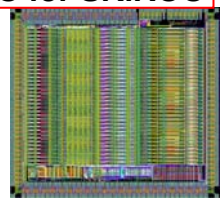
Detector

Wafer

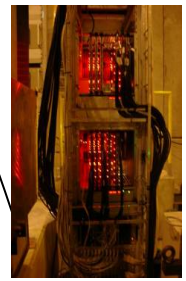


Front-end

ADC for SKiROC

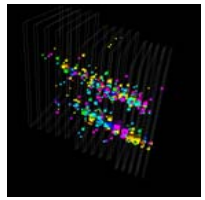


Read-out DAQ



Test bench

Analysis Software



ASU = Active Sensor Unit

Wafer
Crosstalk studies
Design validation

ASUDAQ
Sensor validation
Cosmic tests

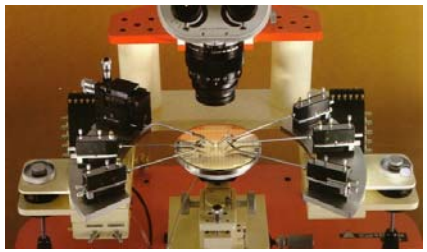
ISDDAQ
Debug, Monitoring
Maintainance

SW reconstruction

ASUDAQ prototype
- Wafer+SKiROC production tests

Wafer test bench
- Square event studies

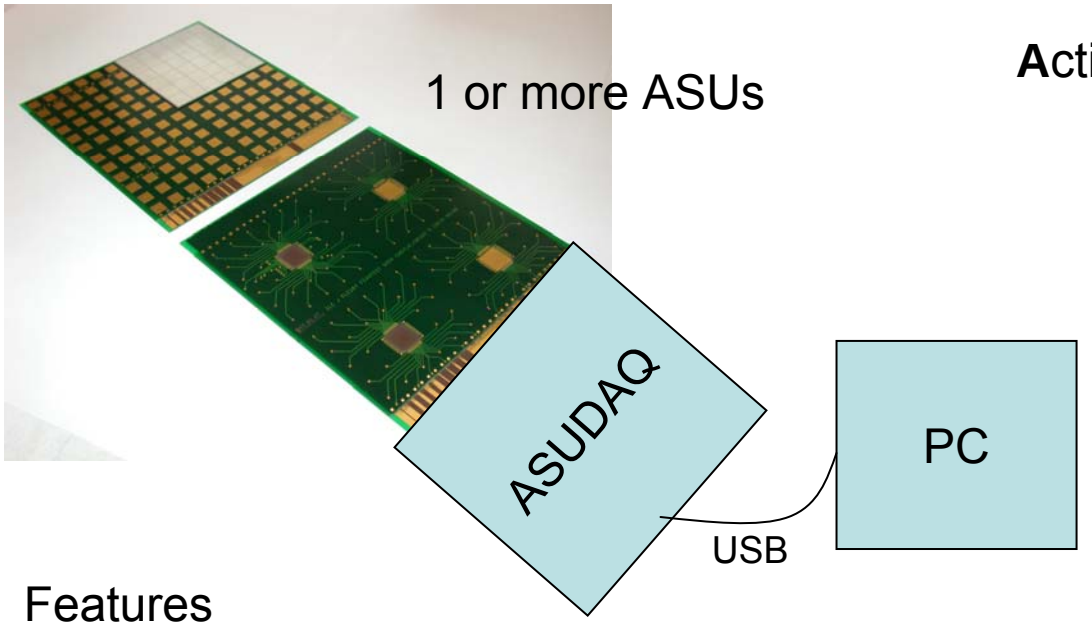
ISDDAQ
- SLAB monitoring



Towards EUDET,
Validation & Test of the whole chain
- R&D test tools for sensor and electronics
- Validation, debugging and maintenance on beam

ASUDAQ for ECAL

R&D on ASU, Cosmic tests of ASU, Wafer+SKiROC production tests



Active **S**ensor **U**nit

Cosmic test bench for ASU characterization.

First R&D step towards EUDET production tests

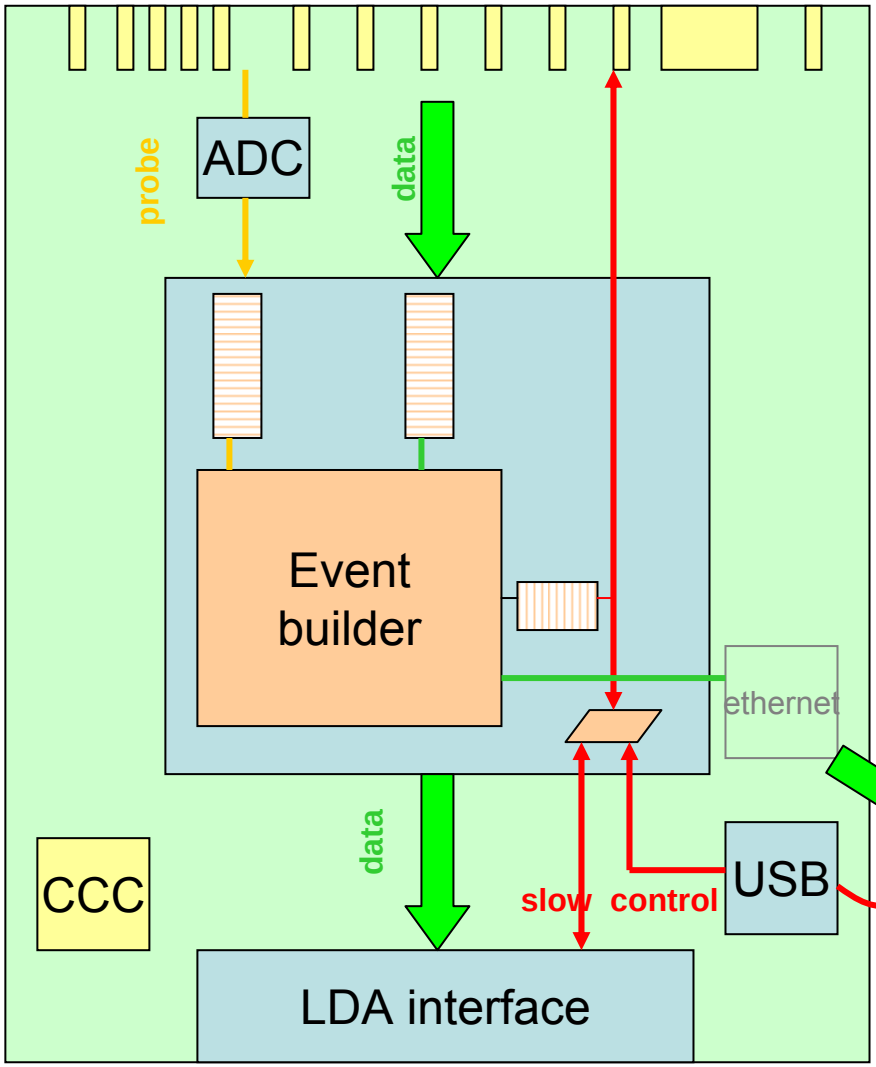
Features

- full **slow control** including internal probing system control
- access to analog test points (embedded ADC)
- **read out** of 4 SKiROC through USB & PC
- cosmic bench environment support (triggers)
- mechanical jaw providing damageless contacts to ASU

A board is being designed

ASUDAQ for ECAL

first prototype schematics are ready



- Generic connectors waiting for final specifications : use of adaptor mezzanines
- Large number of I/O for flexibility
- Various I/O format : LVDS, LVCMOS, NIM, Analog (10b, 40 MHz, ADC included)
- USB for slow control and read-out
- Connector for options : LDAitf, ethernet, debug, …

Very similar to a DIF
Same ASU-DIF interface

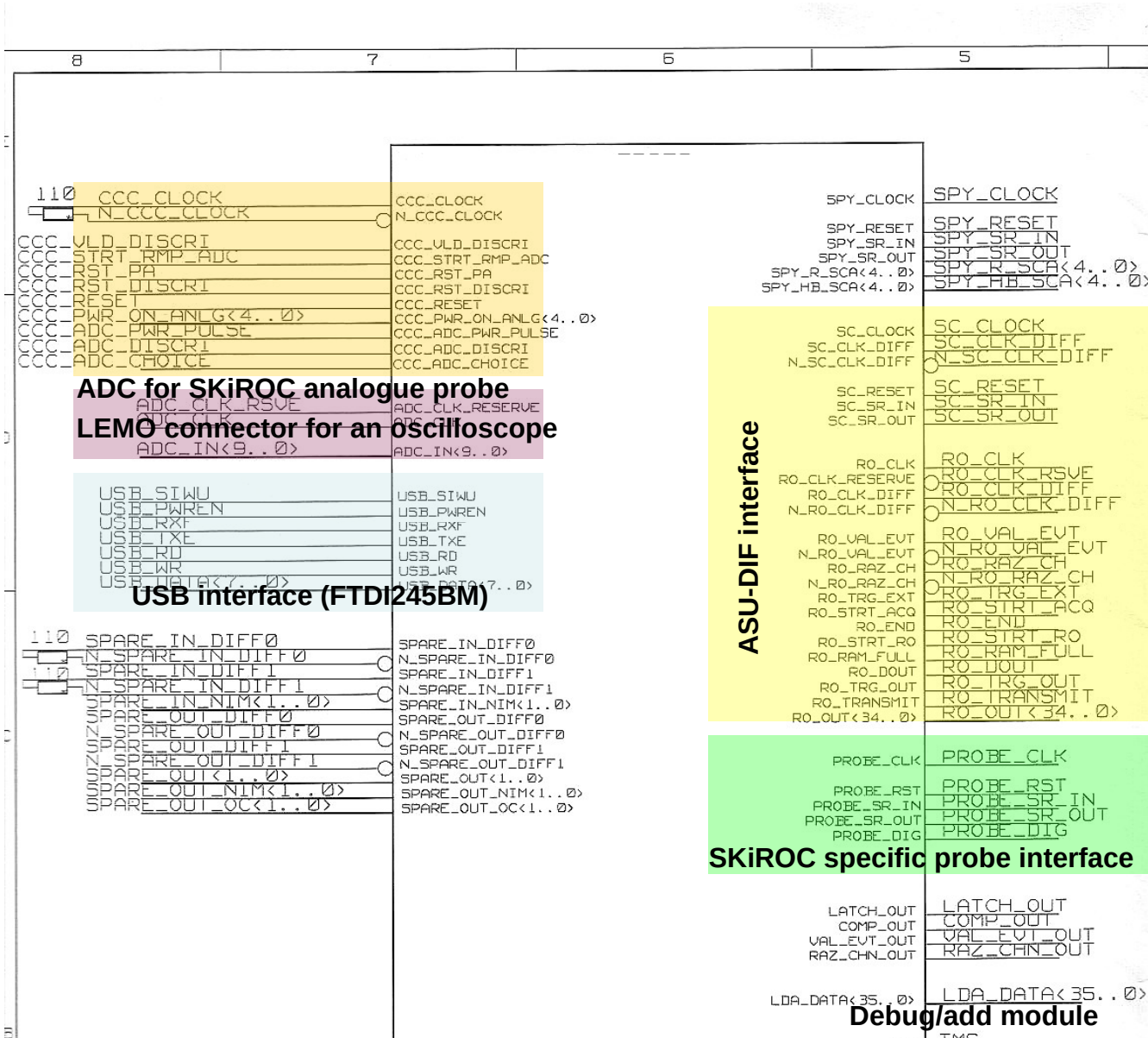
ASUDAQ for ECAL

First prototype compatible with today and future SKiROC

Based on a CYCLONE Fpga from Altera

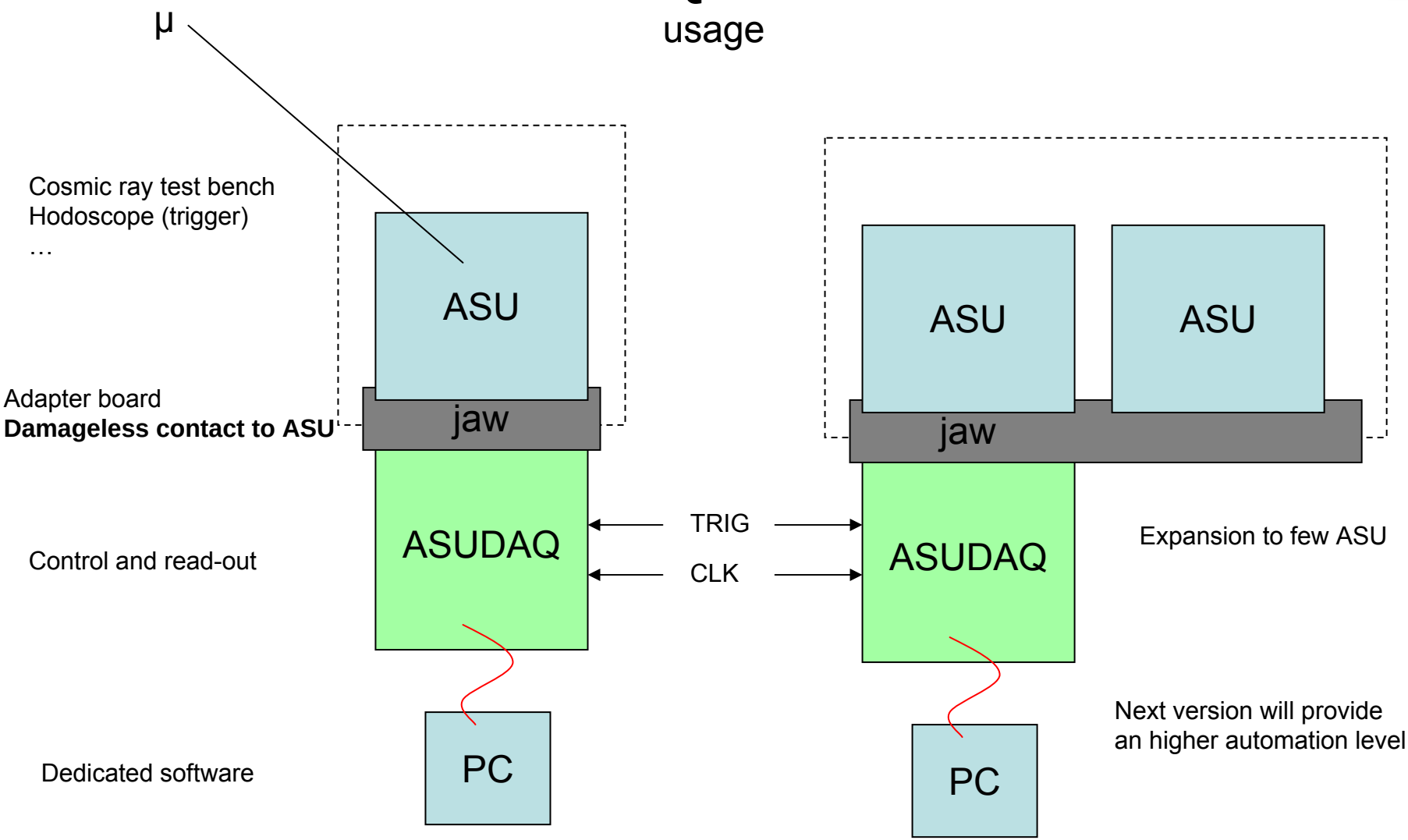
Standard 2.54 mm pitch connectors
- 128 pins for ASU
- 36 pins for debug

Adapter boards to follow design evolvements of external hardware



ASUDAQ for ECAL

usage



ASU/SLAB connector I/O LPC 22/06/07

CAT	NAME			
HV				
POWER	GND	1		
	3.3V	1		
BIAS		0		
REFERENCE		0		
CCC	clkp 40MHz	1 LVDS	O	
	clkn 40MHz			
	Reset	1 OC	OC	
	power_on_xxxx	5 LVTTL	O	new 22/06
	testin	analogue	O	new 22/06
SC	clk_sc	1 LVTTL	O	
	rstb_sc	1 LVTTL	O	
	sroutscbuf	1 LVTTL	I	
	srin_sc	1 LVTTL	O	
PROBE	analogue_probe	analogue	Ain	
	digital_probe	1 LVTTL	I	
READOUT	clkp_5MHz / 1 MHz	1 LVDS	O	
	clkn_5MHz / 1 MHz			
	StartAcq	1 LVTTL	O	
	ValEvtp	1 LVDS	O	
	ValEvtn			
	RazChnp	1 LVDS	O	
	RazChnn			
	StartReadOut	1 LVTTL	O	
	EndReadOut	1 LVTTL	I	
	TransmitOn	1 LVTTL	I	
	Dout (out0)	1 LVTTL	I	
	RamFull	1 OC	OC	
	TriggerExt	1 LVTTL	O	
	TriggerOut	1 LVTTL	I	

ASUDAQ

ASU connector

To be discussed :
see my next talk

Many I/O more added
to current board to follow
SKiROC developments

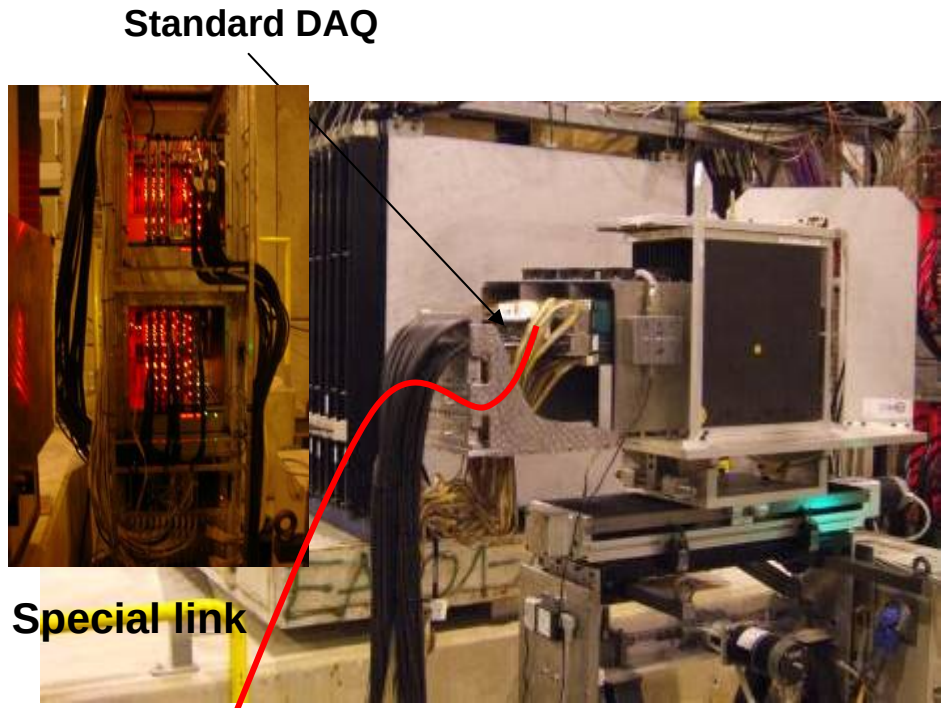
InSituDebugDAQ
concept

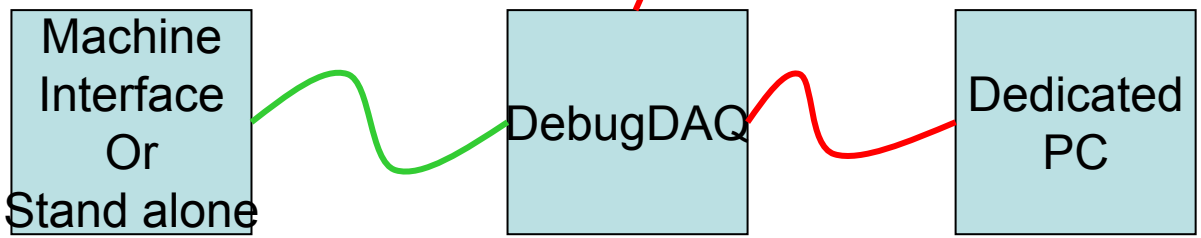
On beam simplified **DAQ devoted to monitor and debug**
a few SLABs
• chip radiation tolerance
• accurate diagnostic
of unexpected behavior
• monitoring (internal probes)
• maintenance

Can run alone, eventually with no beam
• compatible with machine interface
or **specific trigger** and timing

Dedicated Software to ease debugging

Simultaneous DAQ operations allowed

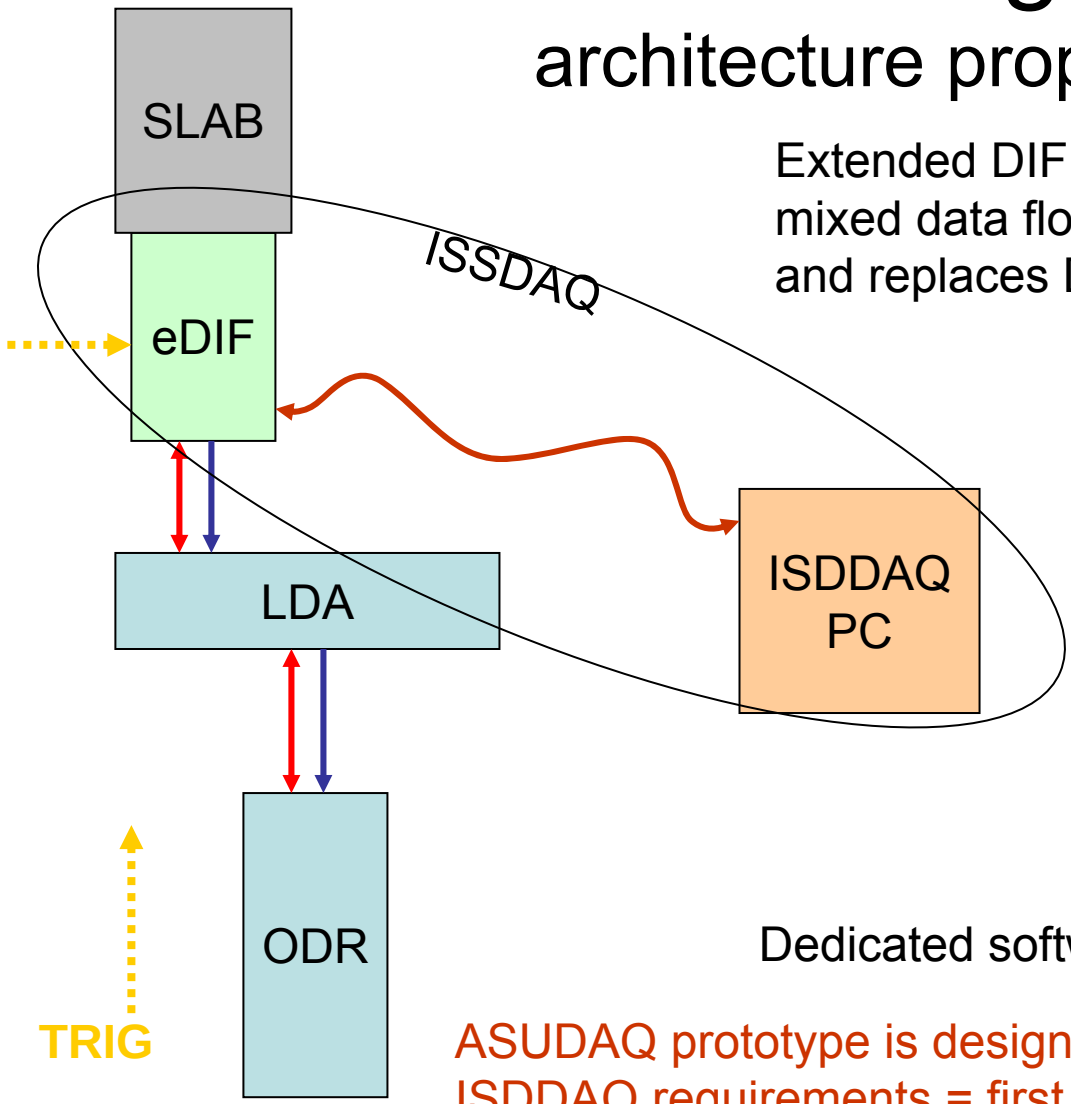




Needs/Replaces DIF !?

InSituDebugDAQ

architecture proposal



Extended DIF is needed for VFE probes and mixed data flow mode (probe+DAQ) and replaces DIF when debugging

Direct connection to LDA would avoid risky cabling operations and highest flexibility

DAQ NI PCI-7811R ?

- FPGA based, 160 I/O to PCI
- buffer flush mode (continuous streaming to PC)

Or Ethernet

Dedicated software tools

ASUDAQ prototype is designed to be compatible with ISDDAQ requirements = first prototyping steps are common

Conclusion

ASUDAQ
- first developments on prototyping board
- ASU connector issue

ISDDAQ architecture issue
- SKiROC Internal probes read-out
- Simultaneous DAQ
- Flexibility (FPGA based)

Common “all in one” prototype is being designed
- generic interfaces
- use of additional adapter board to connect to ASU, SLAB, etc…