IN2P3

Omega

LAL LAL IPN Orsay

STATUS OF SKIROC and ECAL FE PCB

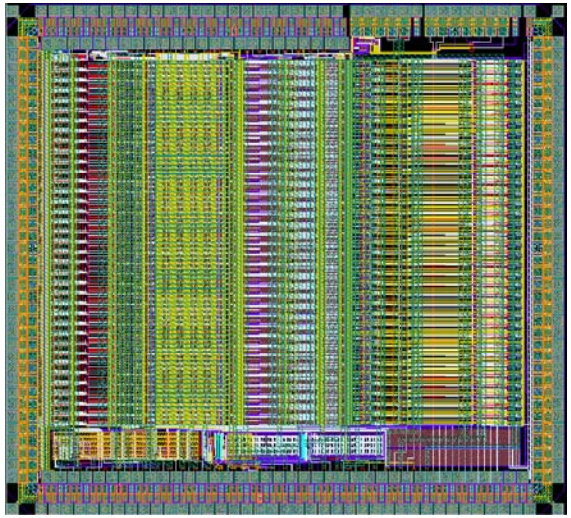
EUDET CALICE Calorimeter for ILC

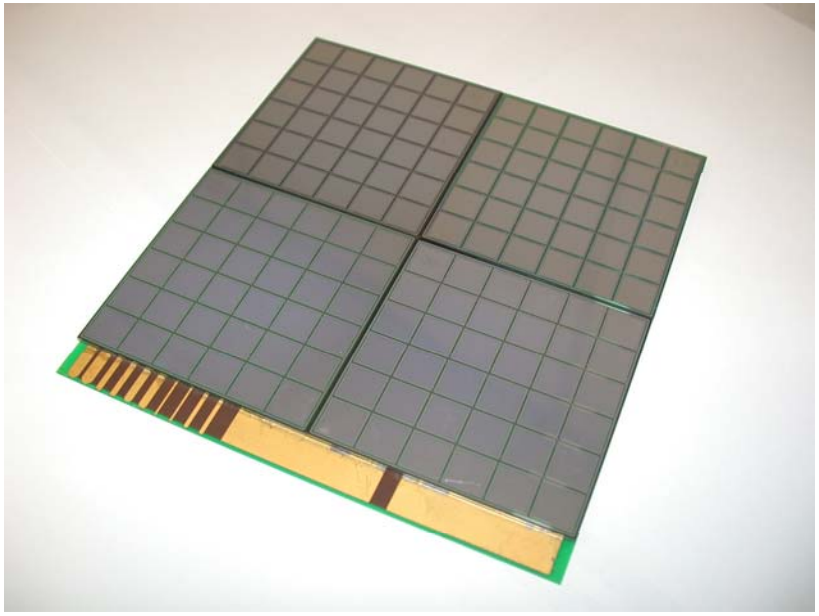
13 September, 2007

Orsay MicroElectronic Group Associated

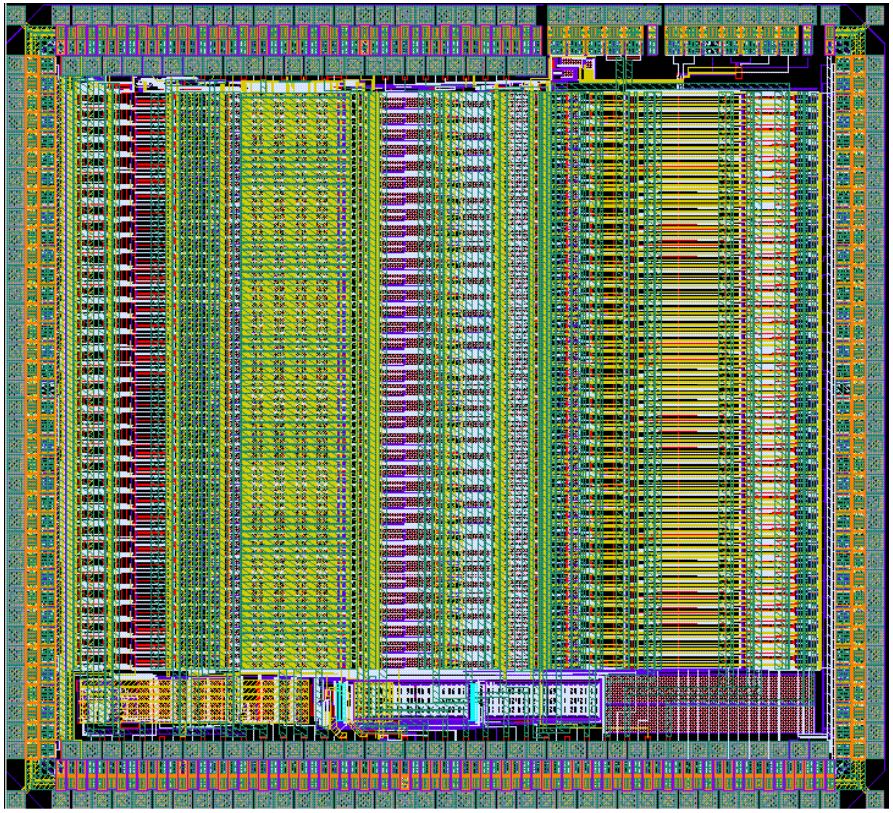
Plan

- ECAL : Skiroc presentation
  - A brief reminder
  - Measurement has started
    - Working features
    - A MIP in Skiroc
- PCB R&D
  - What we have in hand
  - The ASU PCB
- Schedule & conclusion

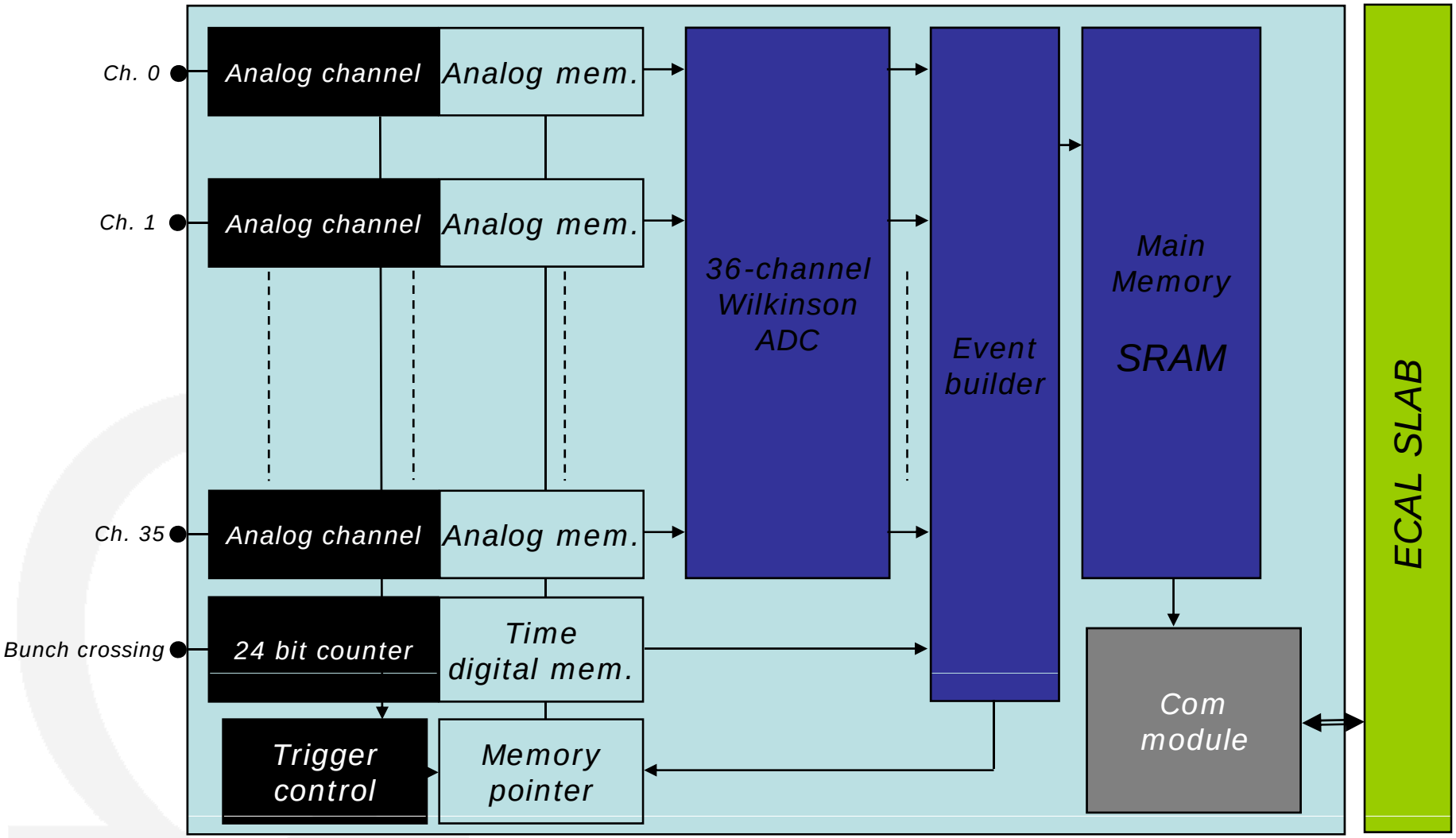




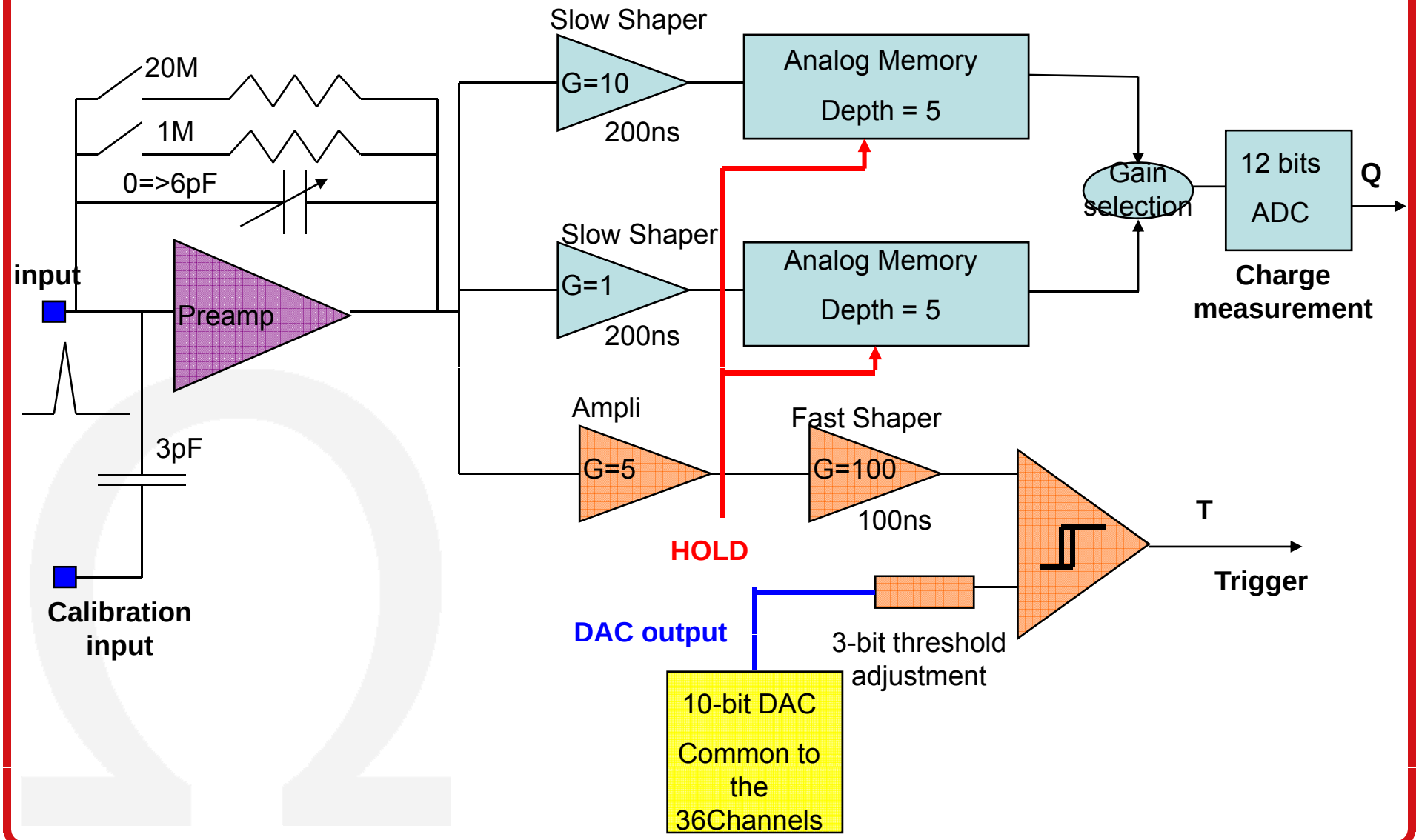
SKIROC STATUS



Reminder : Block scheme of SKIROC



Reminder : One channel



SKIROC : tested features

Preamplifier

- Preamp disable (DC coupled channel OFF – leakage to supply)
- Preamp low Rf (DC coupled degrated mode)

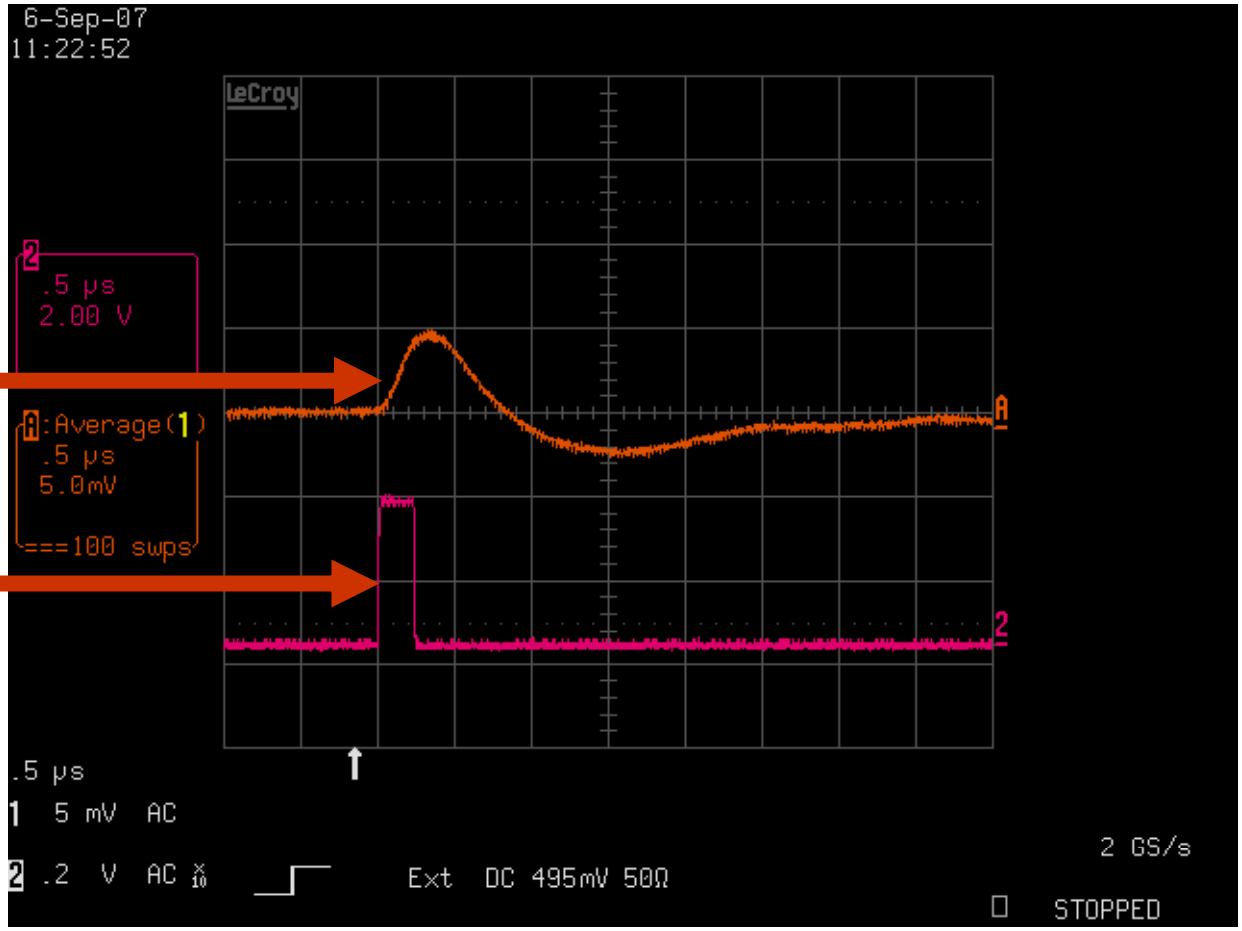
- Auto-trigger
  - Self trigger on a MIP observed in measurement

- Power pulsing
  - Programmable stage by stage
- Calibration injection capacitance
- Embedded bandgap for references
- Embedded DAC for trig threshold
- Serial analogue output
- Probe bus for debug

First measurement

Before any quantitative measurement, some qualitative results to get courage !

1 MIP in SKIROC



Charge measurement

Self trigger

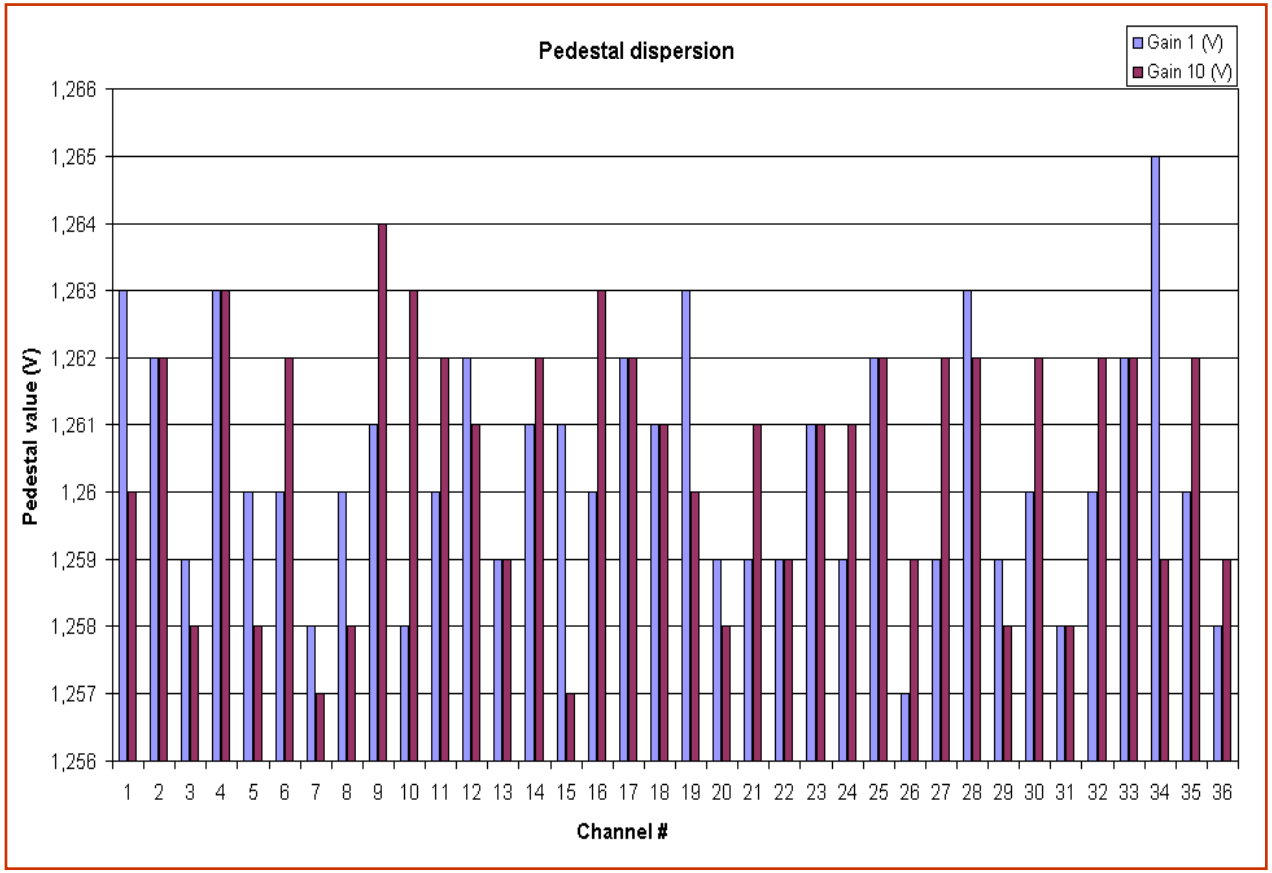
Pedestal dispersion

The pedestal measurement is coherent with what we expect :
-No pedestal pattern (random values according to statistical dispersion)
-Statistical dispersion equivalent to what we get with that technology

Standard deviation :

$\sigma_{Gain\ 1}$= 1.8mV

$\sigma_{Gain\ 10}$= 1.95mV

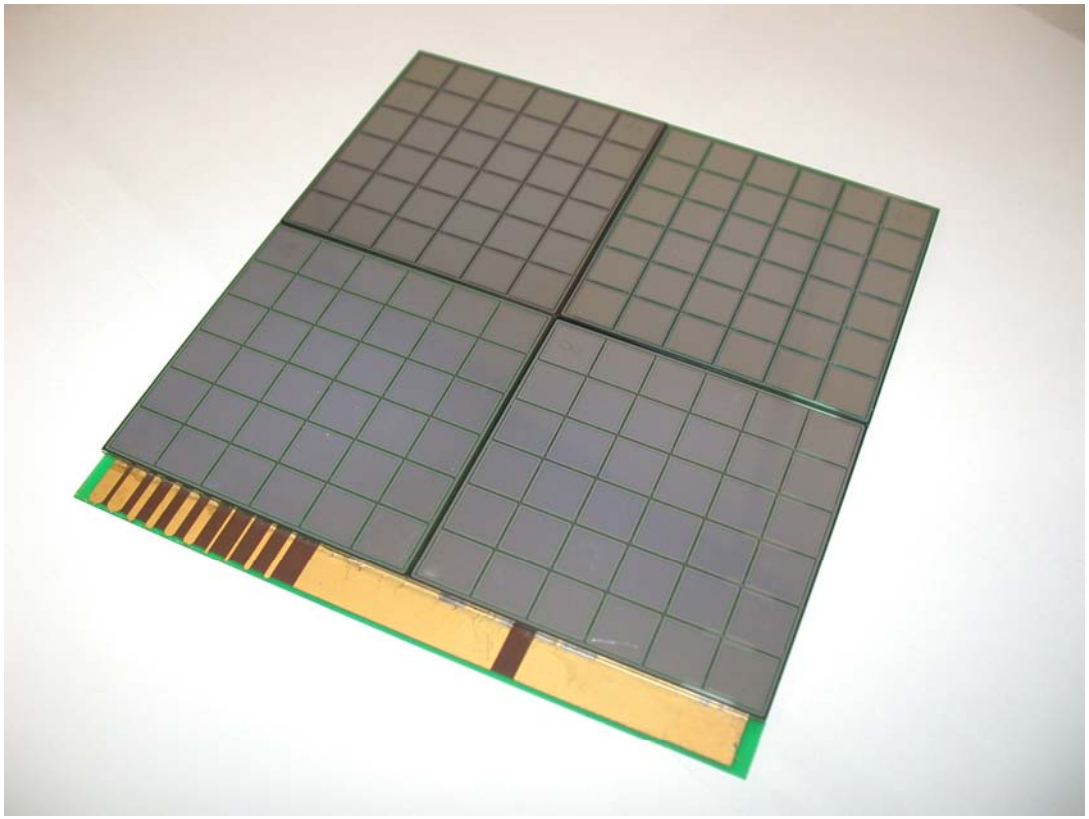


SKIROC : test to be performed

- Dynamic range
- Noise
- Trigger efficiency
- Linearity
- Stability
- Crosstalk
- DAC resolution
- ADC resolution
- Power pulsing & consumption
- DC coupling capability (leakage current swallowing)

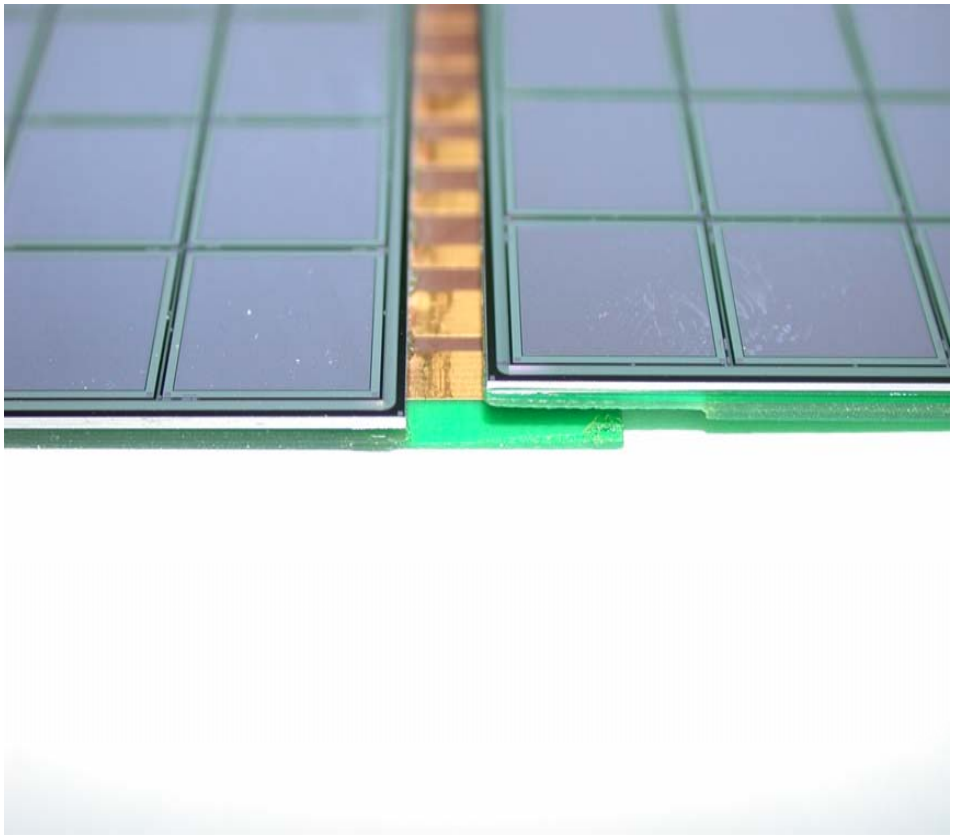
SInce we have debugged the chip control, these tests will be performed ASAP

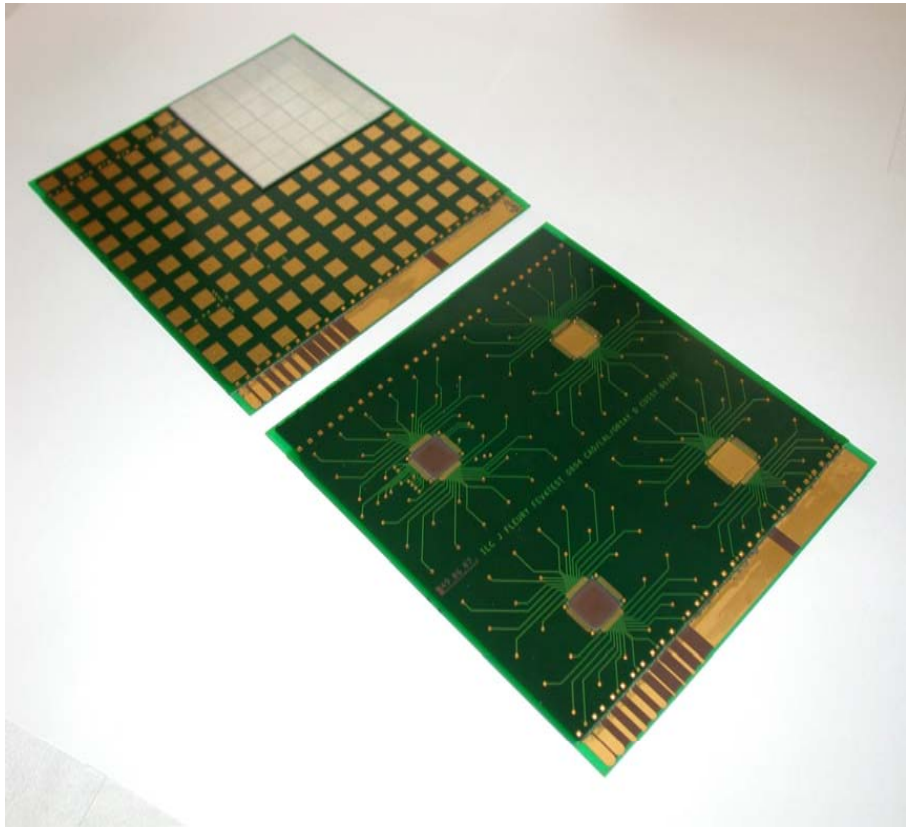
ECAL PCB STATUS



What we have in hand : stitch-test

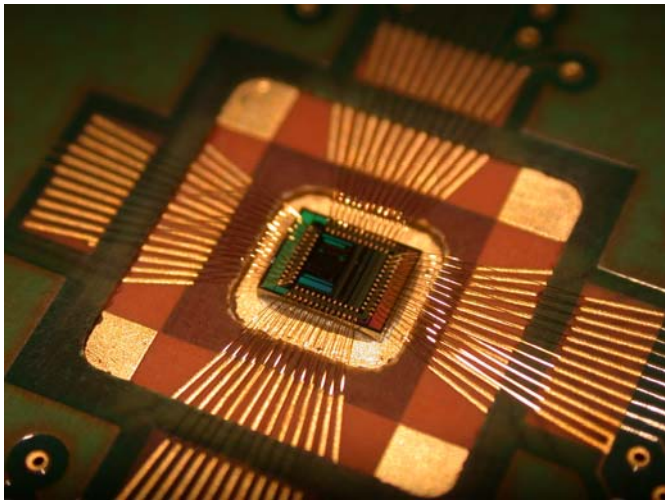
Stitchable PCB :
- Designed only for mechanical and feasibility study
-1*1 cm² pads
-6*6 cm² wafers
- Still a lot of work on « stitching techniques »

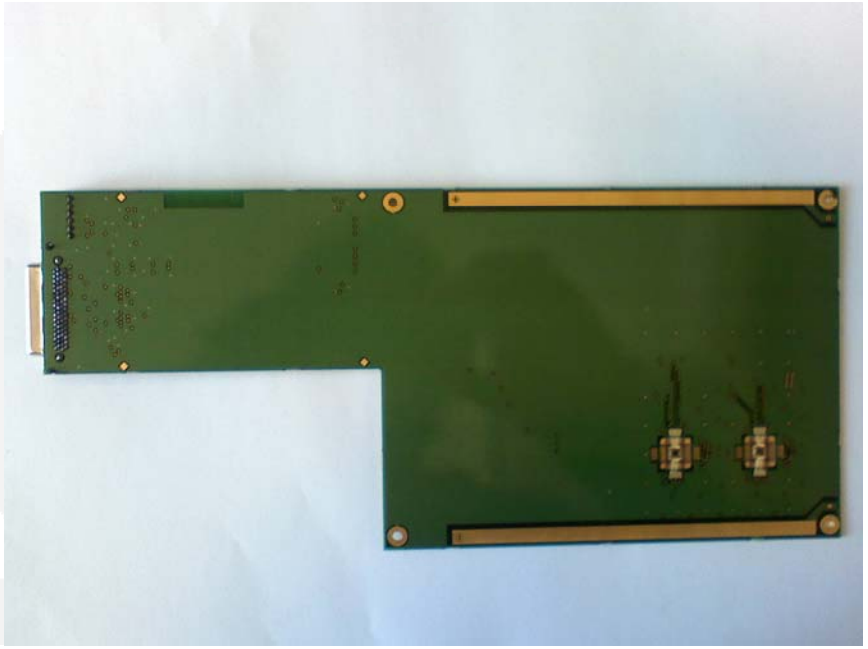


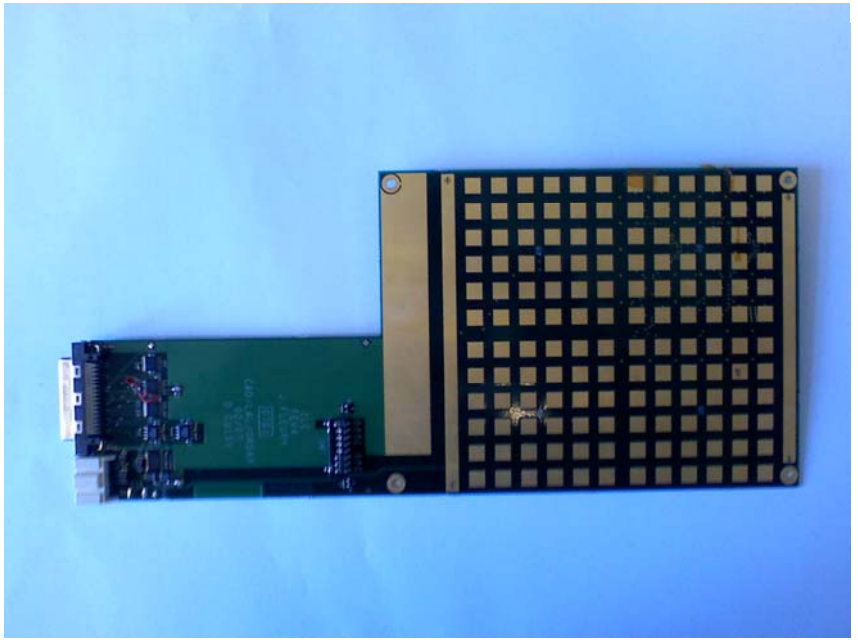


What we have in hand : FEV4

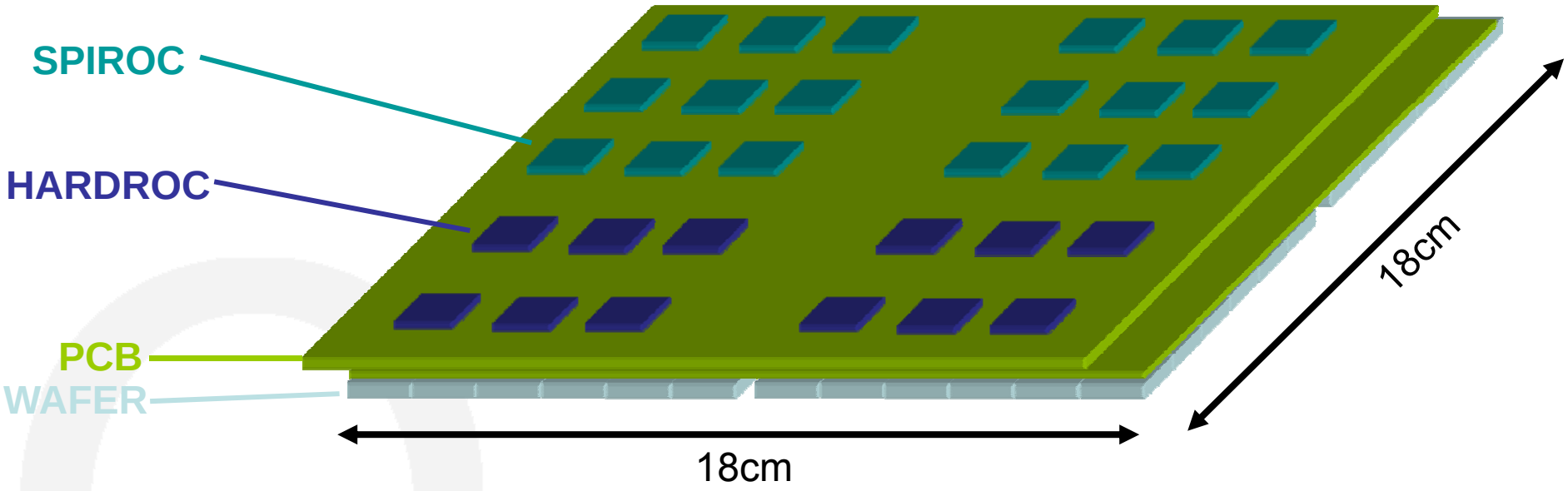
Physics prototype PCB
- Designed to validate the chip embedding
-1*1 cm² pads
-6*6 cm² wafers
-Only one wafer active (36 ch.)
-Under test (ie still not working)
-No probe and no pintest !







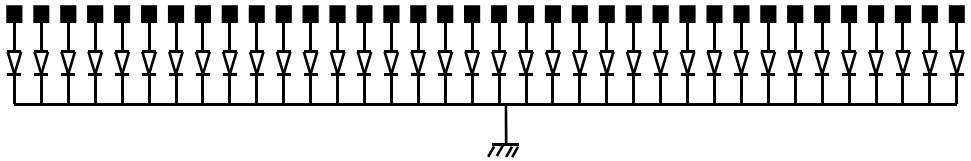
FLC_FEV5 presentation



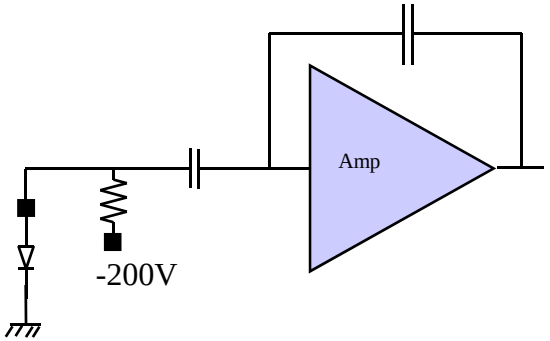
1296 channels. Half SPIROC (18 chips) / half HARDROC (12 chips)

High voltage distribution

AC coupling :

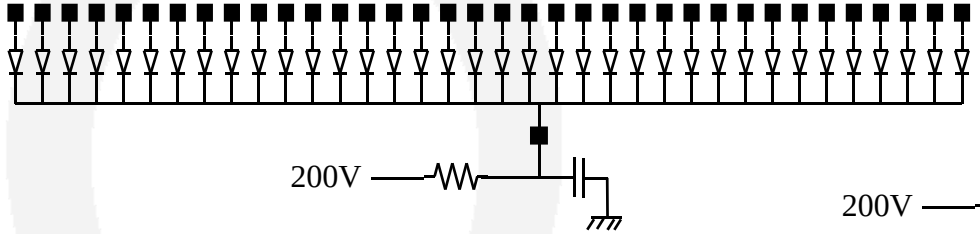


1 Wafer

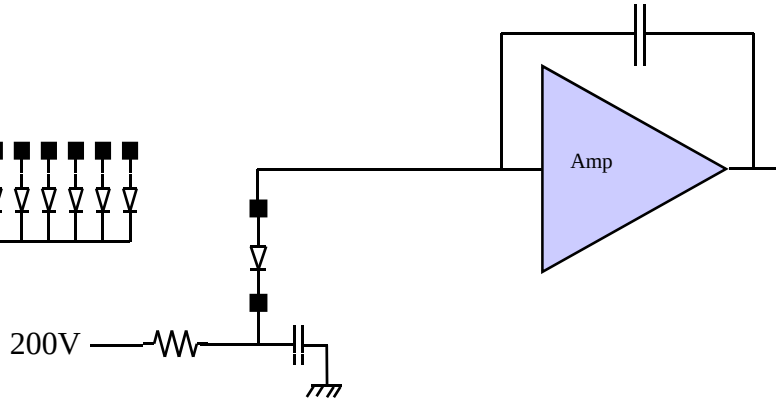


1 Channel

DC coupling :

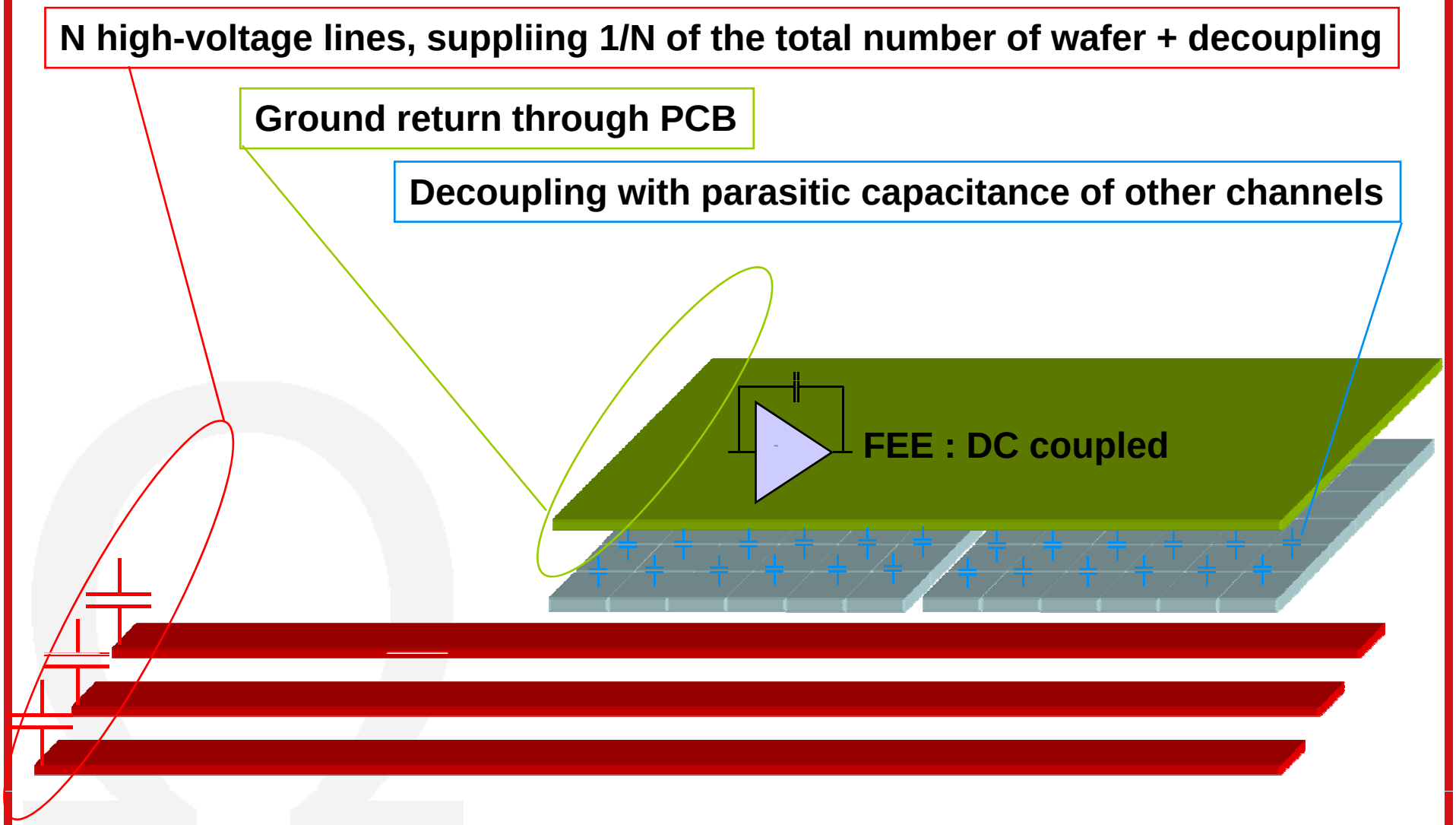


1 Wafer



1 Channel

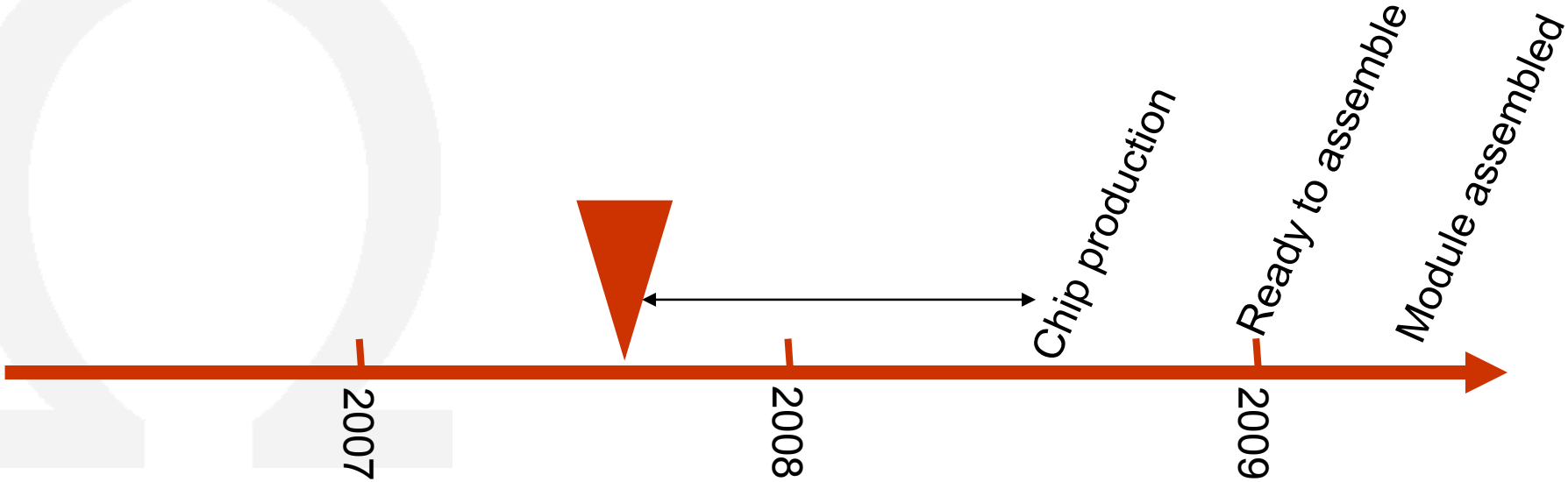
Solution for HV decoupling



Nb of channel/HV line > 1000 → Crosstalk < 1/1000

PCB design schedule

- Schedule
  - ASICs production to be started in summer 2008
  - ASICs have to be tested on PCB to validate daisy-chain
  - « communication module » is the same for the three chips :
    - SKIROC (ECAL)
    - HARDROC (DHCAL)
    - SPIROC (AHCAL)
  - Roughly : PCB R&D finishes when ASIC production starts



Conclusion

- Less than one year to finish the EUDET module design
- All interface have to be defined very soon