High speed 12 bits Pipelined ADC proposal for the Ecal
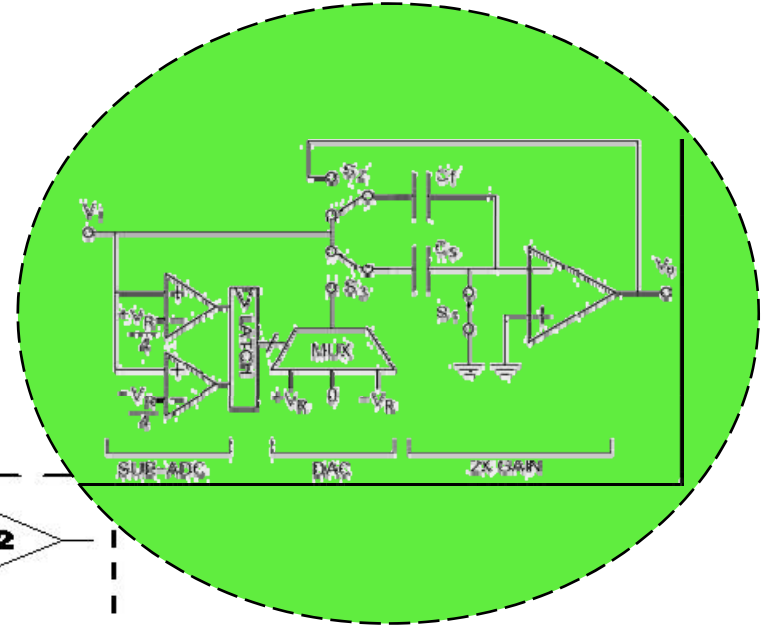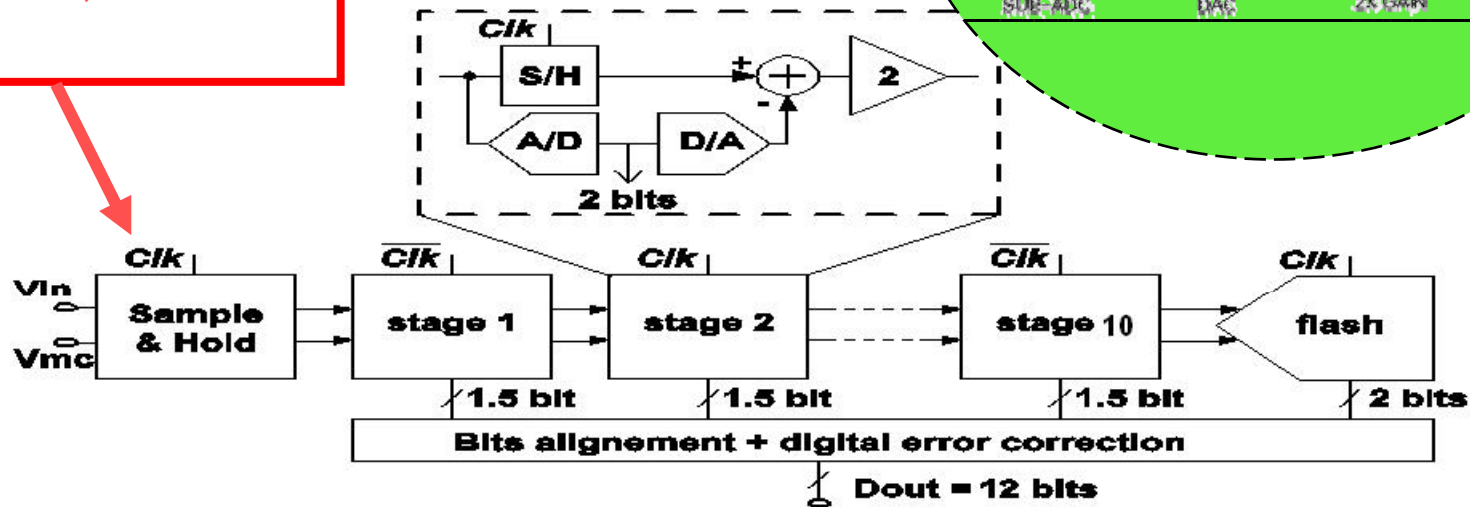
- High speed =>because only config to optimize pipeline power consumption
- Full CMOS even if more difficult
- Low voltage (3.3V)
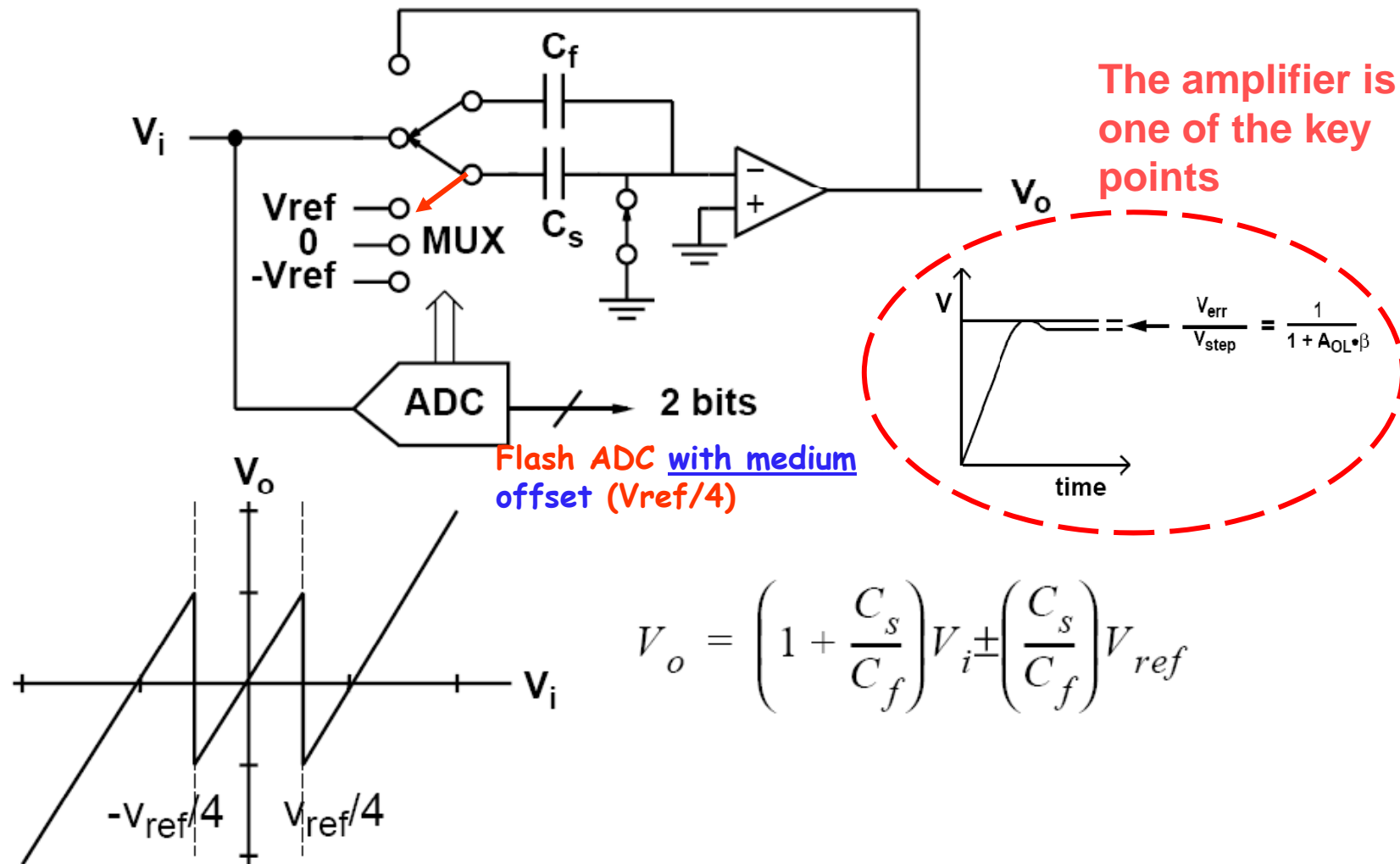- High dynamique range (1.2V to 1.5V)

Pipe line ADC design: the baseline

Very very critical
Must guaranty 12 bits
Offset compensation
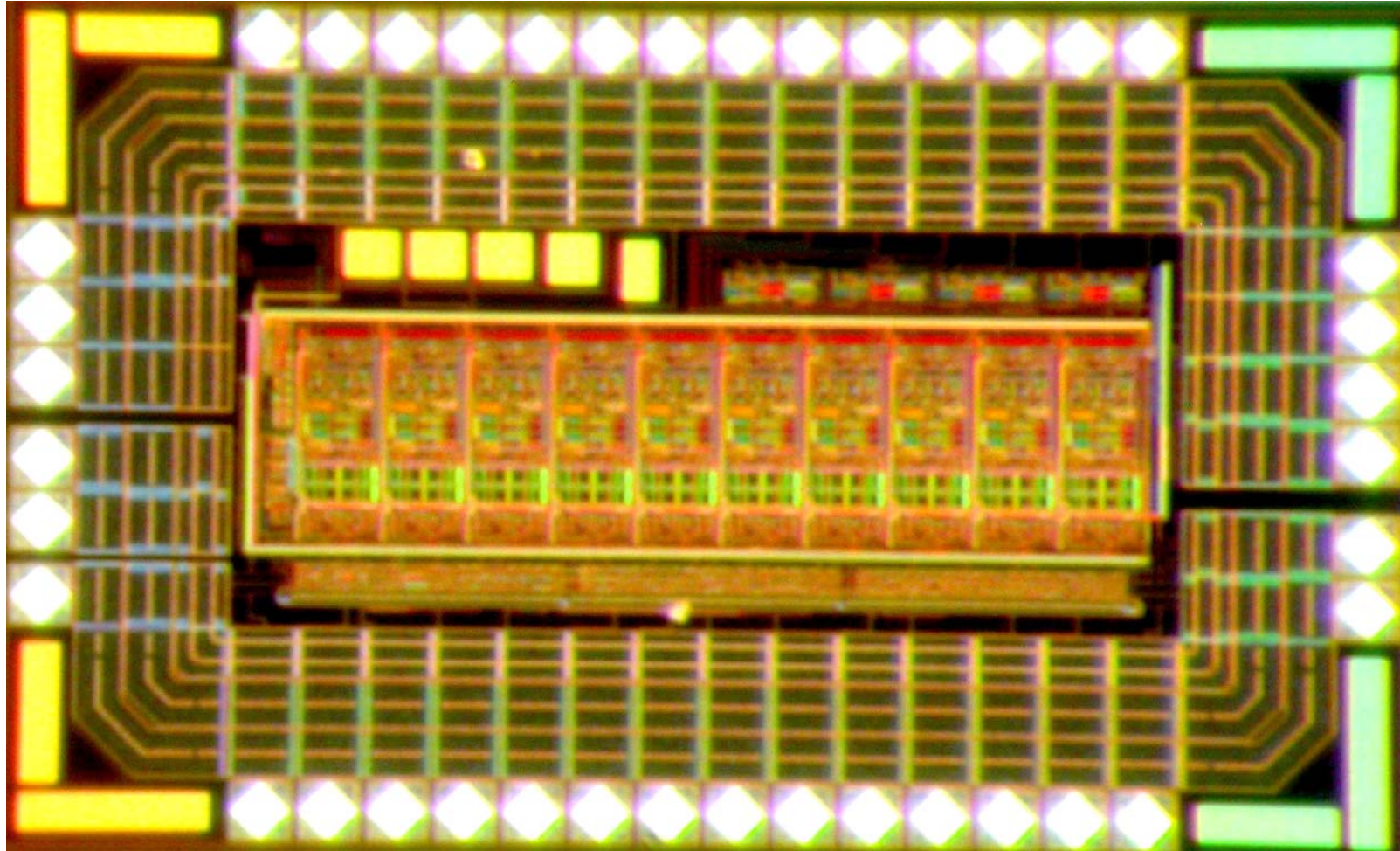CM control
Noise issue, distorsion
....

MDAC Function: Multiplier & DAC

The amplifier is one of the key points

$$\frac{V_{err}}{V_{step}} = \frac{1}{1 + A_{OL} \cdot \beta}$$

Flash ADC with medium offset (Vref/4)

$$V_o = \left(1 + \frac{C_s}{C_f}\right)V_i \pm \left(\frac{C_s}{C_f}\right)V_{ref}$$

# First ADC prototype: 10bits basic features extended to 12bits
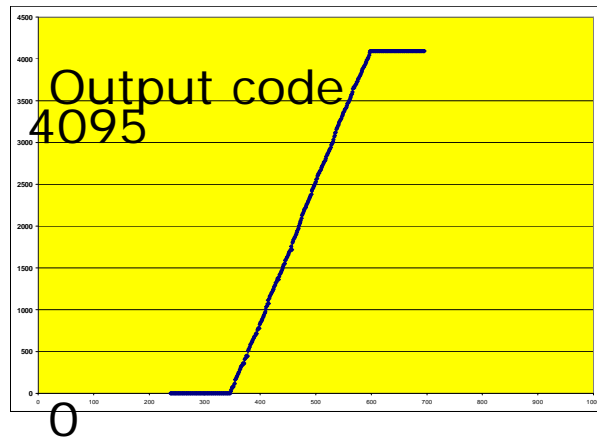
Testing results 1

- The DC power consumption is exactly fitting with our simulations:
    - **27mW** for the actual ADC and 3mW for the Bias stages

- The sampling speed is up to **15Mhz.**

- The very fast power pulsing **1µS, to a ratio better than 1/1000.**
- **No Obvious missing code when averaging, BUT!**
- **INL and DNL: depend on how you measure**

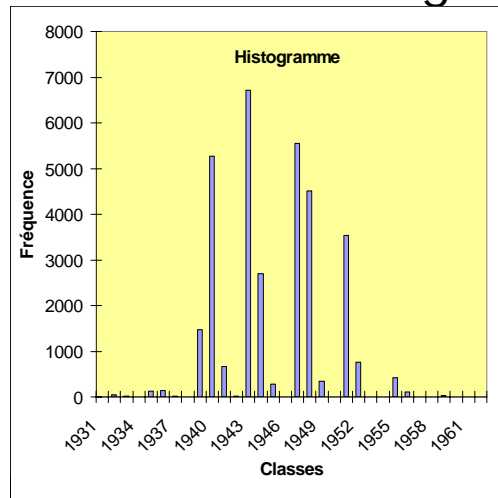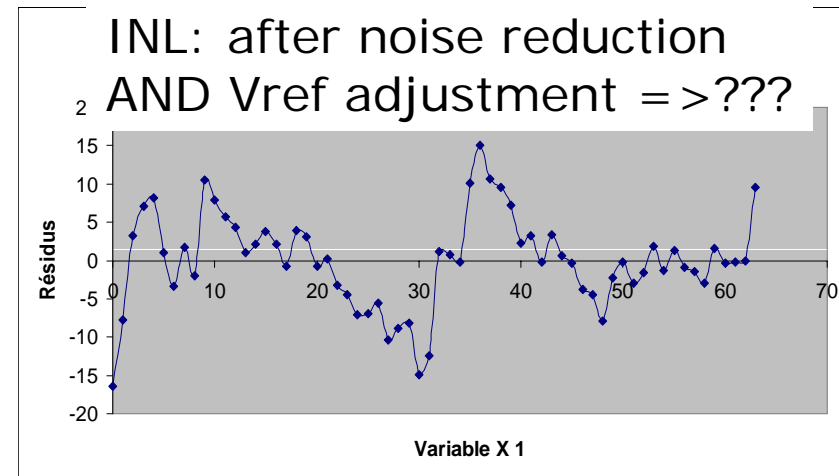# INL results with an input ramp generated by a 12 bits DAC

response to a rampe + fitting extrapolation
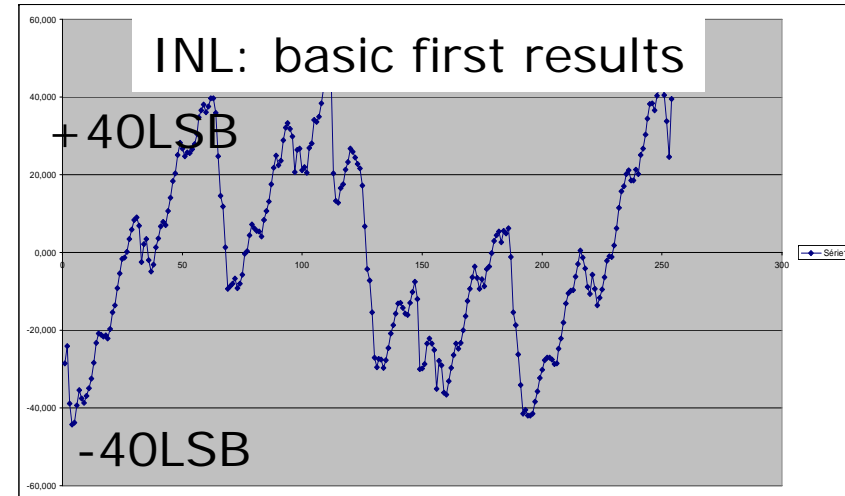
Time parameter
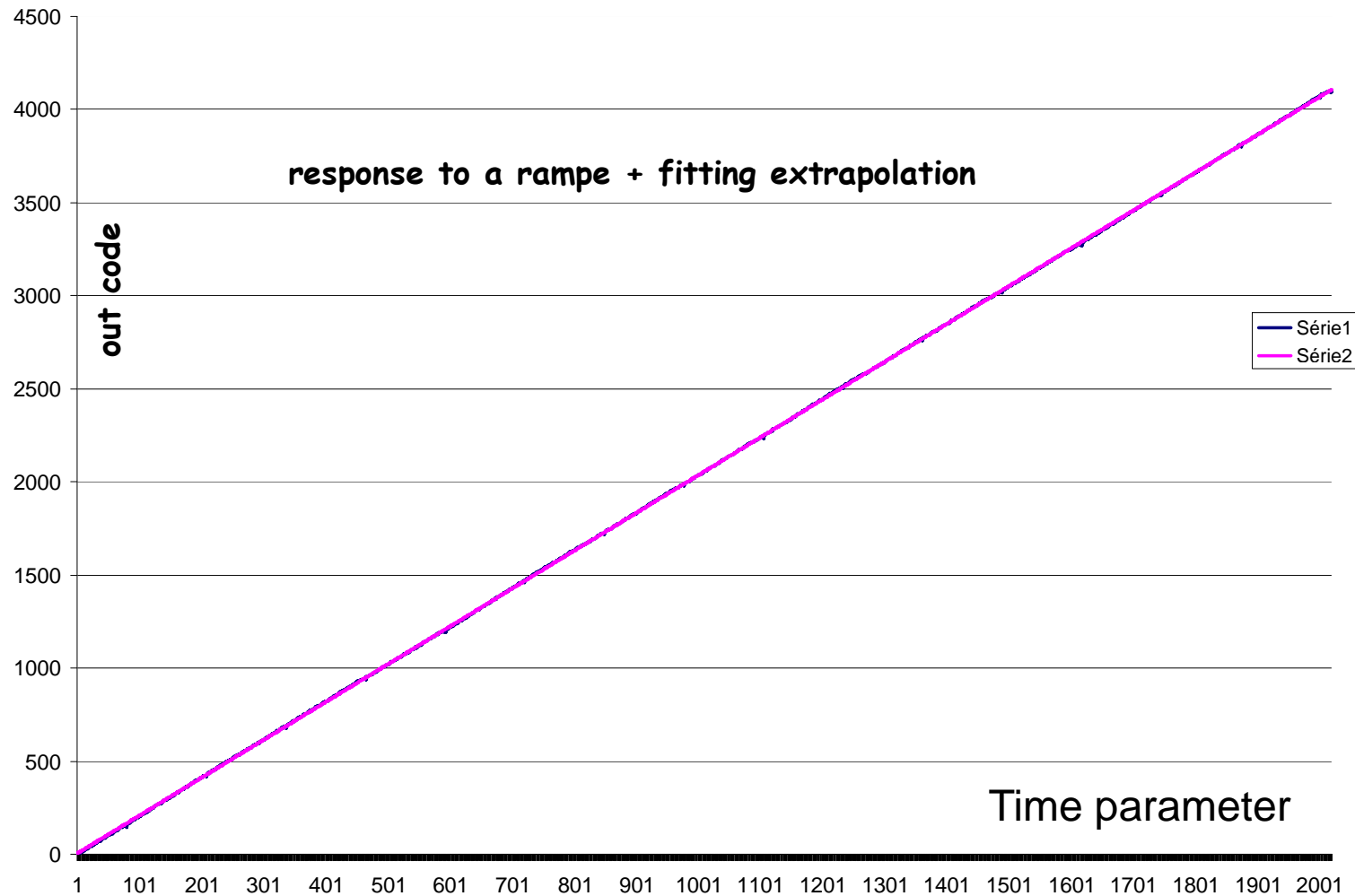
INL first results with onboard S/H Be careful with the set-up !!!!

Output code 4095
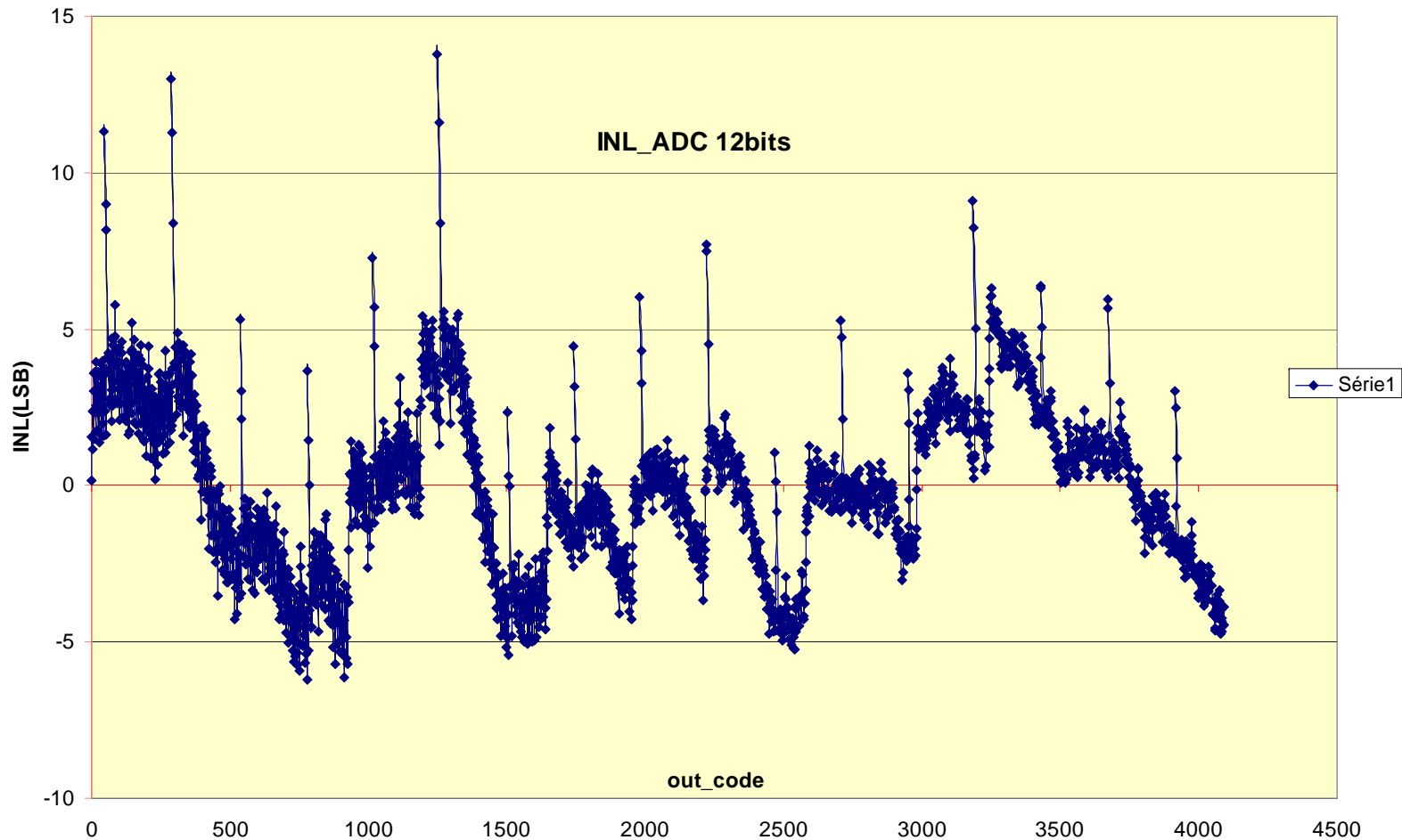
0

Analog input factor

INL: basic first results

+40LSB

-40LSB

Set-up noise >10LSB

INL: after noise reduction AND Vref adjustment =>???

Variable X 1
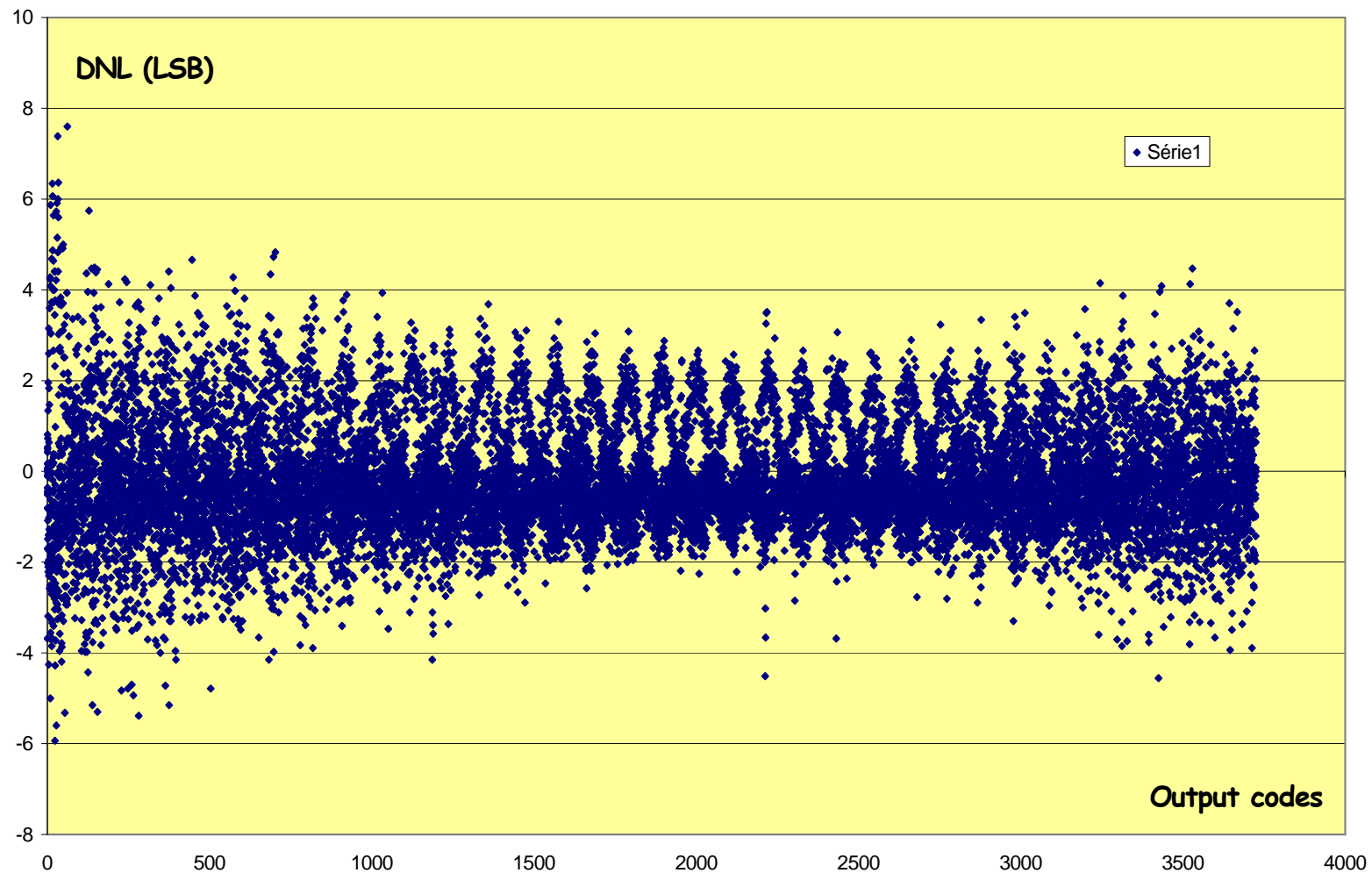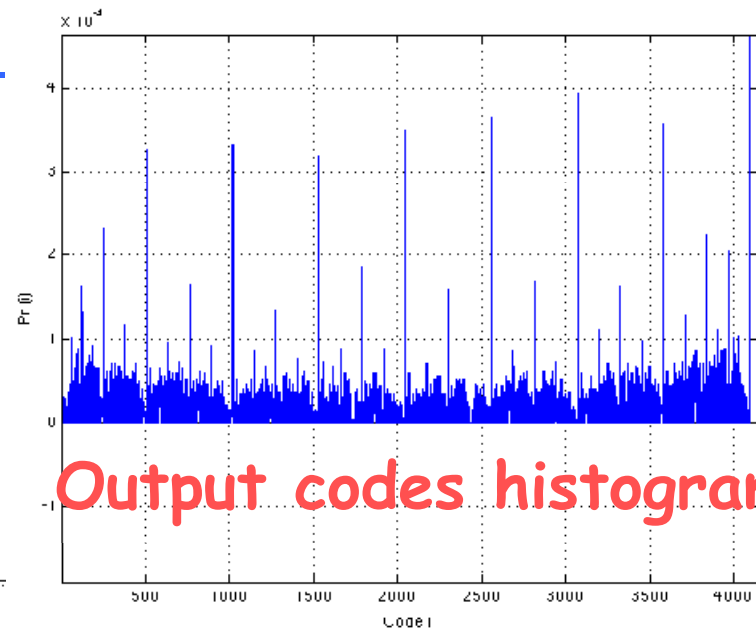
INL results for input ramp and *averaging* => ENOB $\approx$ 9.5 bits ?? Is there a link?

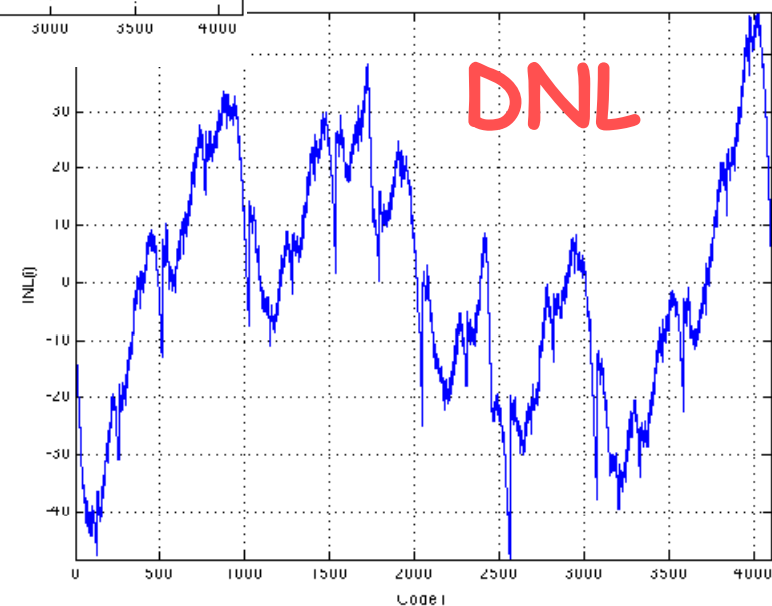# DNL results when differentiating the averaged output code(n)-code(n+1)

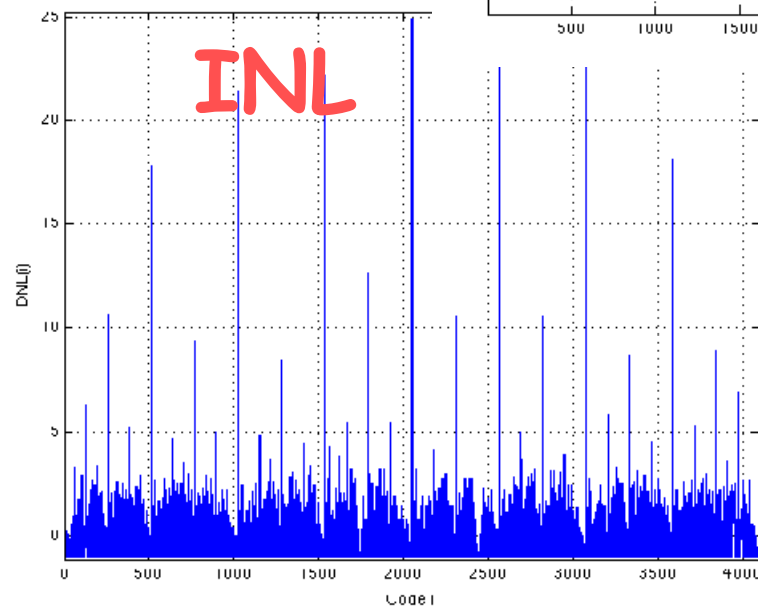# The same output codes after analysis by a dedicated ADC testing software (IXL –D. Dallet)

Output codes histogram

Be careful with the Averaging!

INL
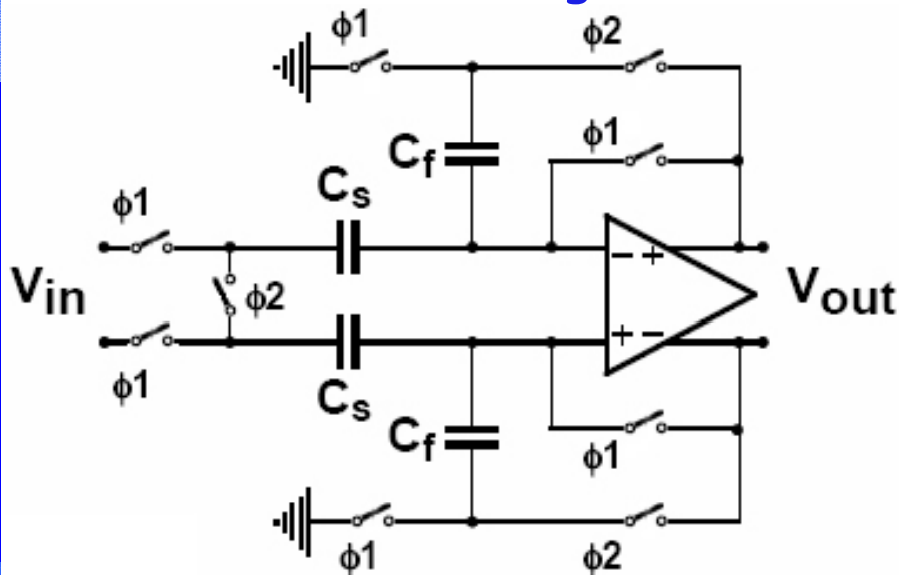

DNL

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Second version design features

- Include the design of the S/Hold stage
- Improving the dynamique range to 1.5V
- Extend the speed beyond 30Mhz
- Include an LVDS clock input
- Improve the capacitors matching.

THE Sample "Track" and Hold

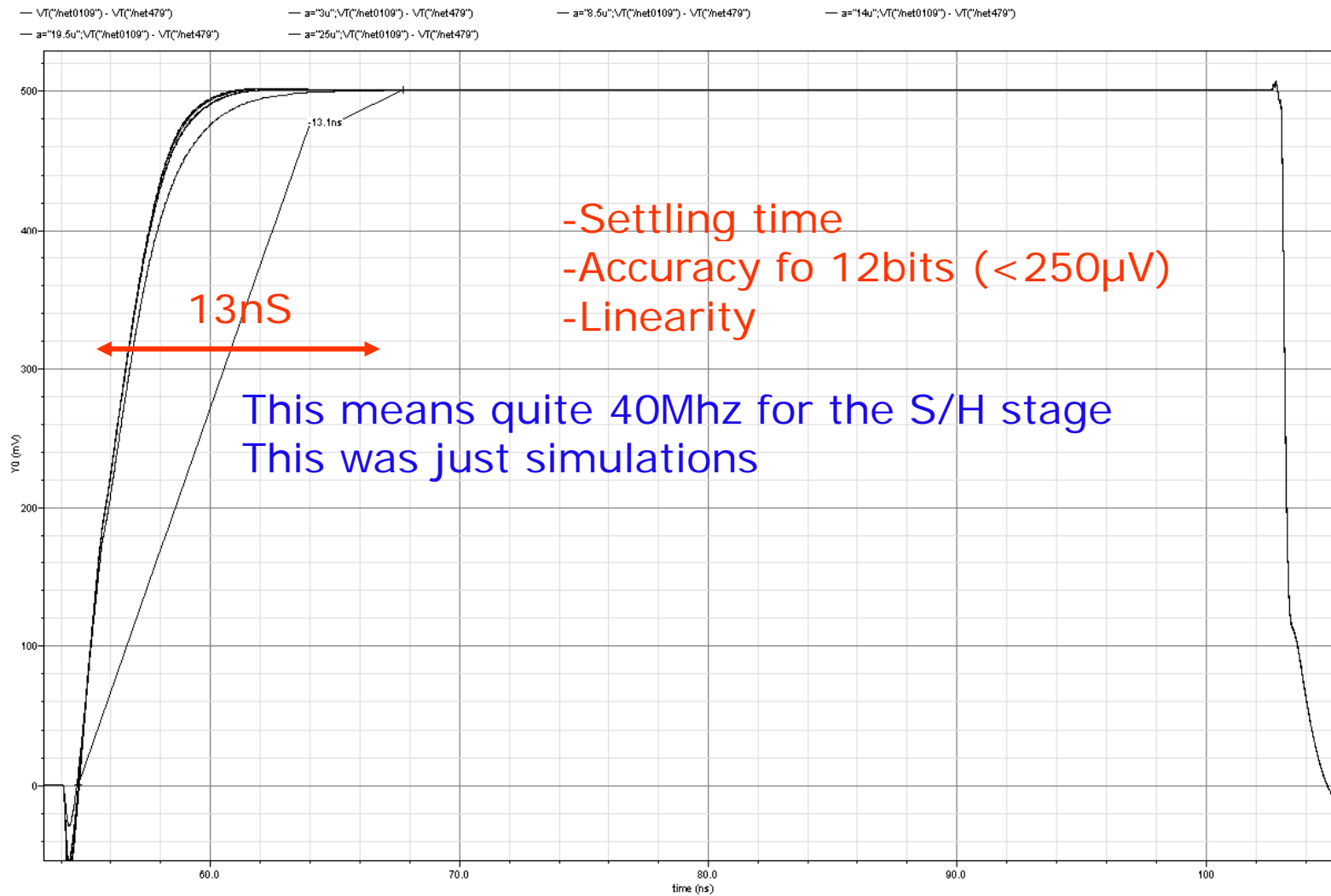We choose this Charge redistribution instead of Flip Flop

+ **single ended to differential**
+ less sensitive to CM error
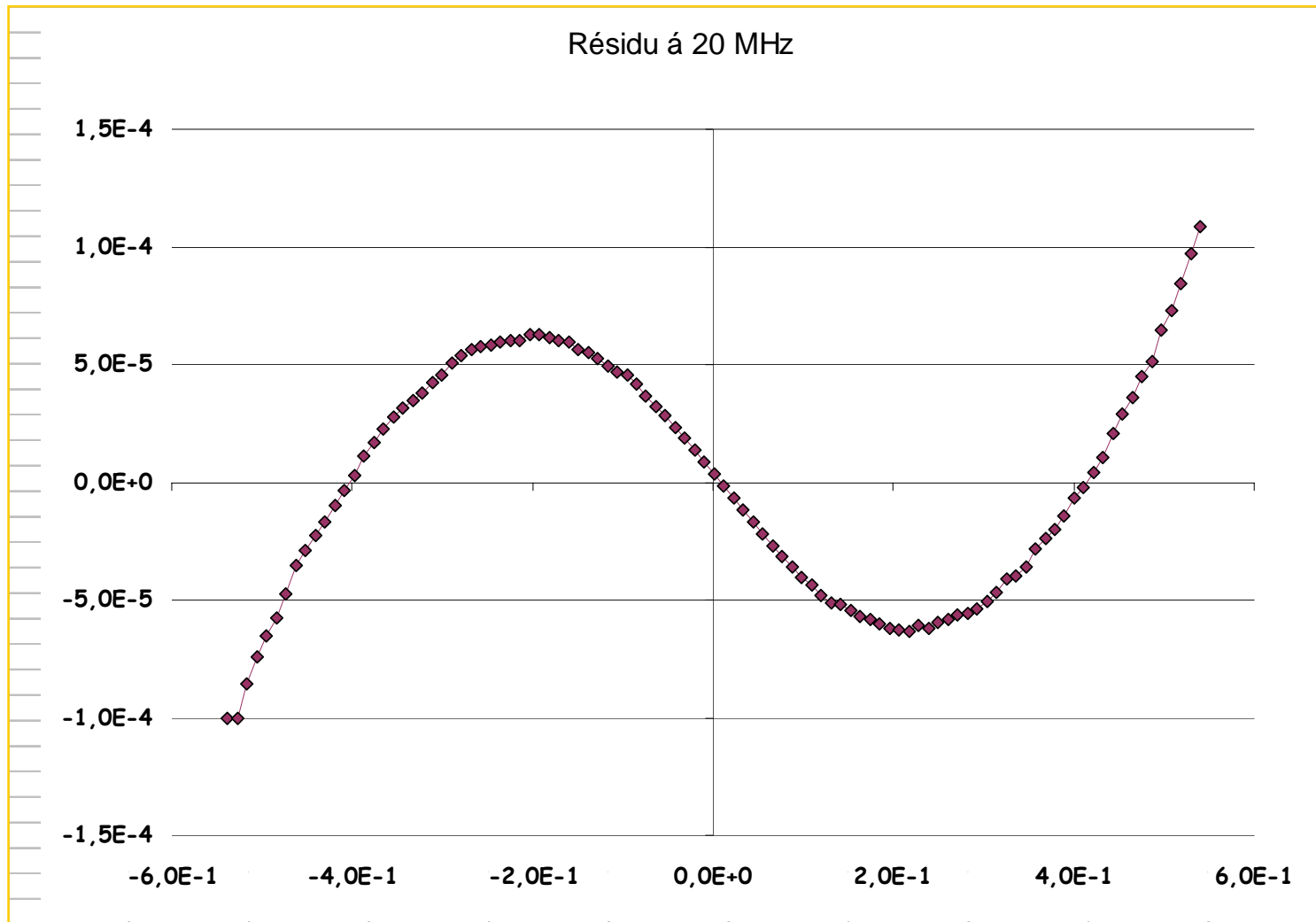+ Offset cancelled (differentially)
- Noise ($\sqrt{2}$ more)
- Gain mismatch
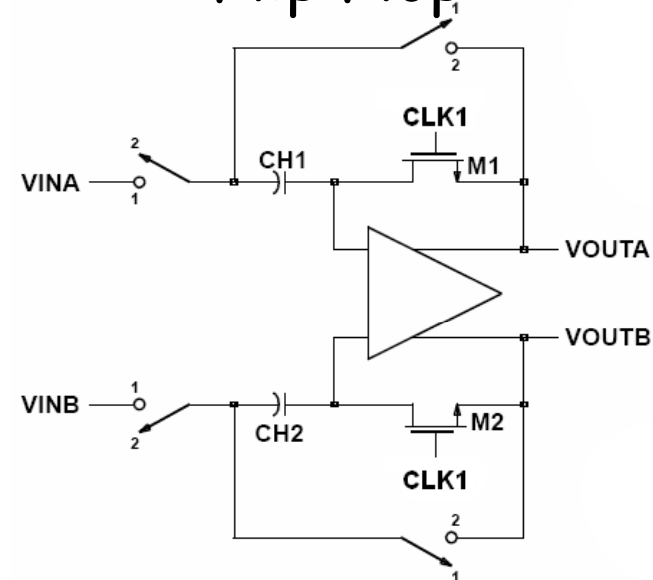
+ Mismatch insensitive; gain=1
+ Less noise
+ Offset cancelled (differentially)
- Sensitive to CM fluctuations
- **Need full differential inputs**

Sample & Hold Simulations

-Settling time
-Accuracy fo 12bits (<250µV)
-Linearity

13nS

This means quite 40Mhz for the S/H stage
This was just simulations

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Improved SH Non linearity @ 25Mhz for the 2nd version of 12 bits ADC
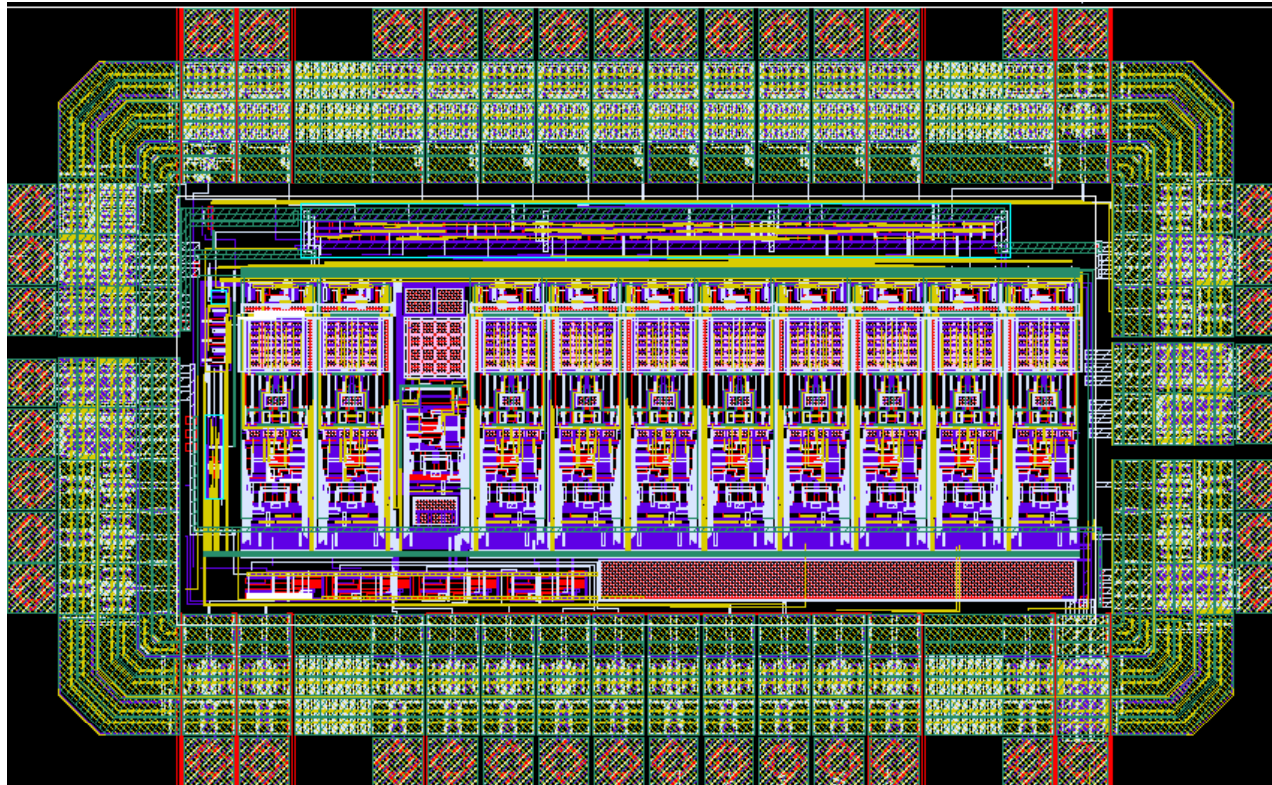

Résidu á 20 MHz

2nd version of __actual__ 12 bits ADC
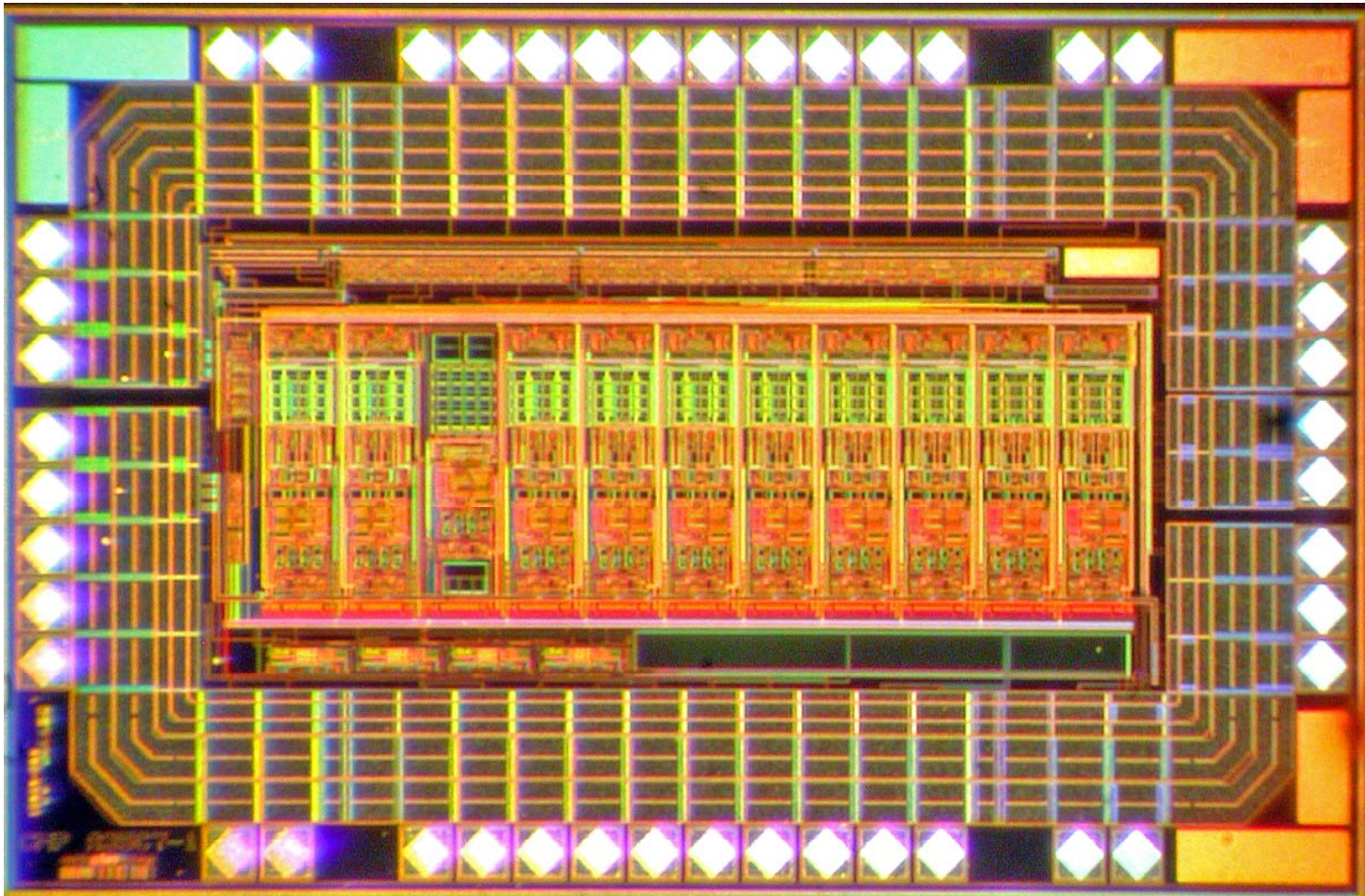## Submitted in January 07

1) **Thru 12 bits** including a **Sample/Hold**
2) Speed: Beyond **30MHz**
3) Power: **35mW** with fast and efficient **standby command**
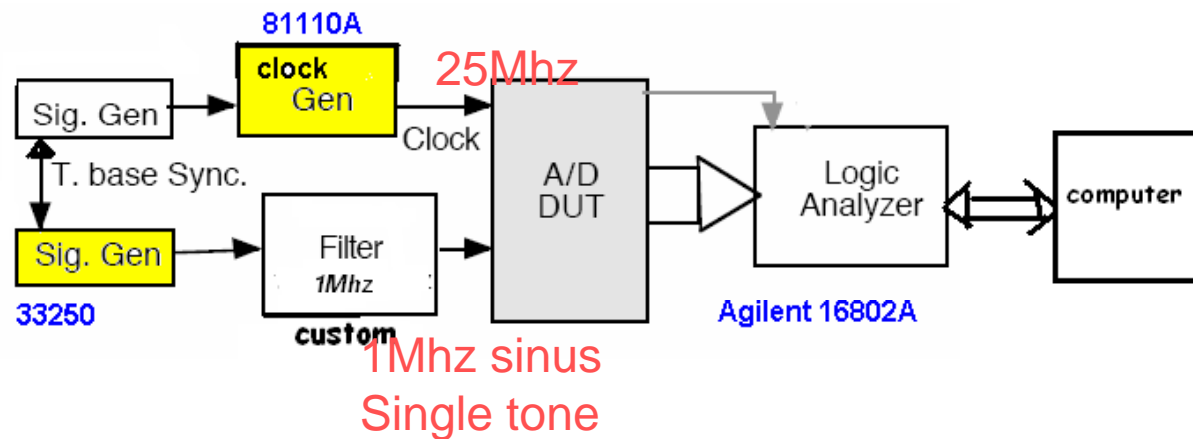
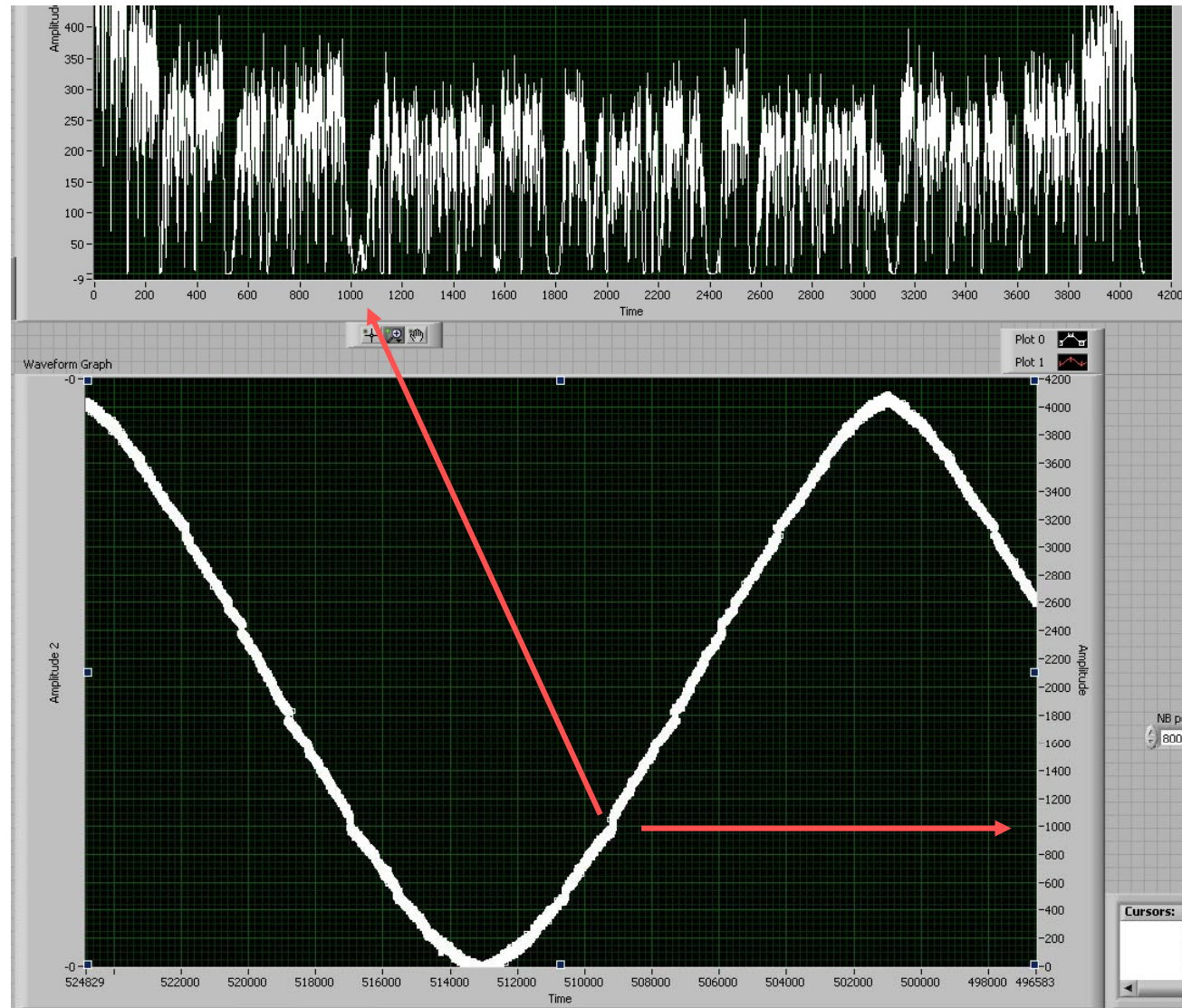# 2nd prototype, die received by June 07
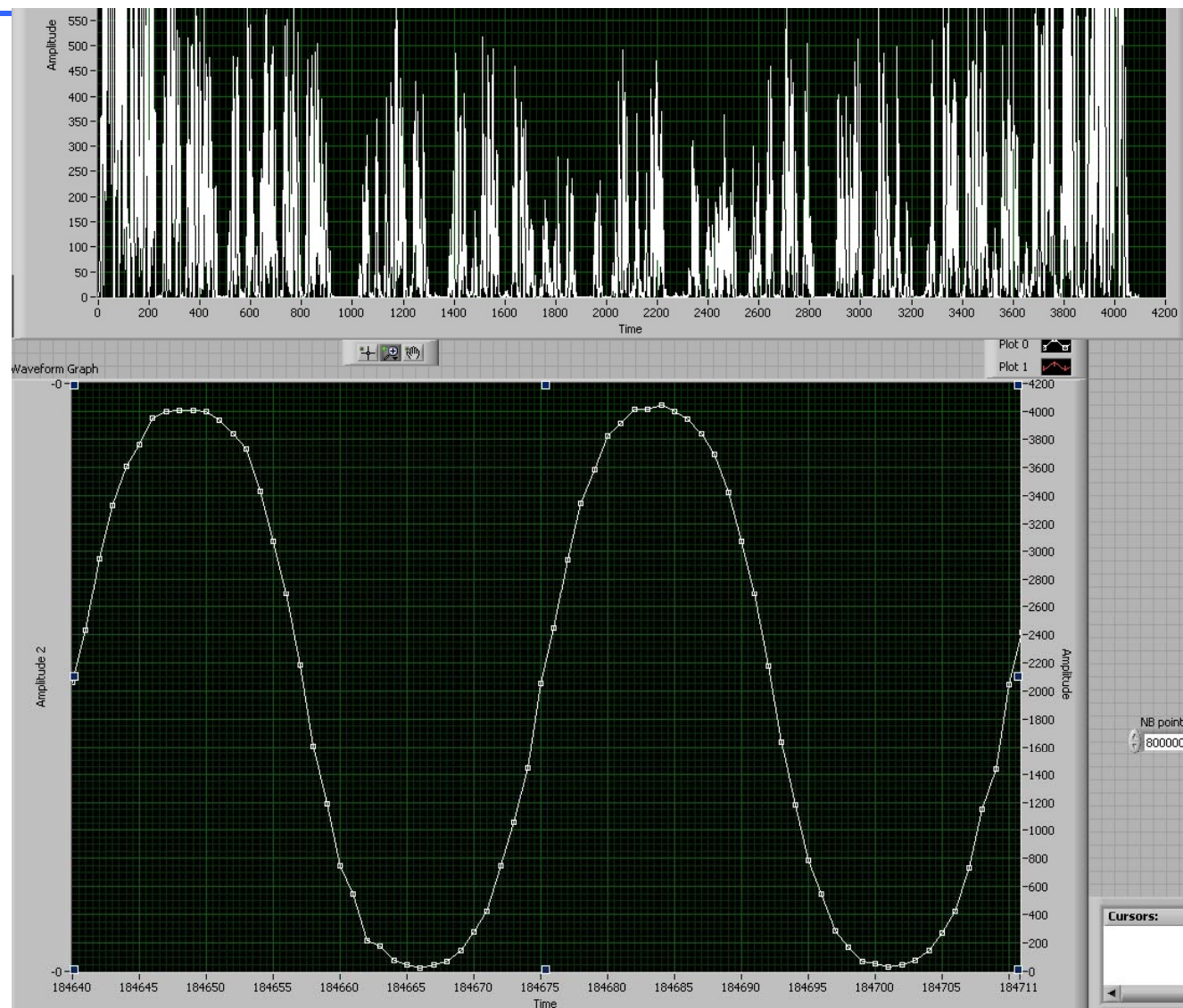
Accurate ADC test bench

-**Be careful with the synchronization of your clock**

-**Pay attention to your input signal spectrum**

- **We need dedicated software to make sure: the FFT windowing + analysis**

Testing results=>missing codes

1Mhz sinus sampled at 35Mhz + histo
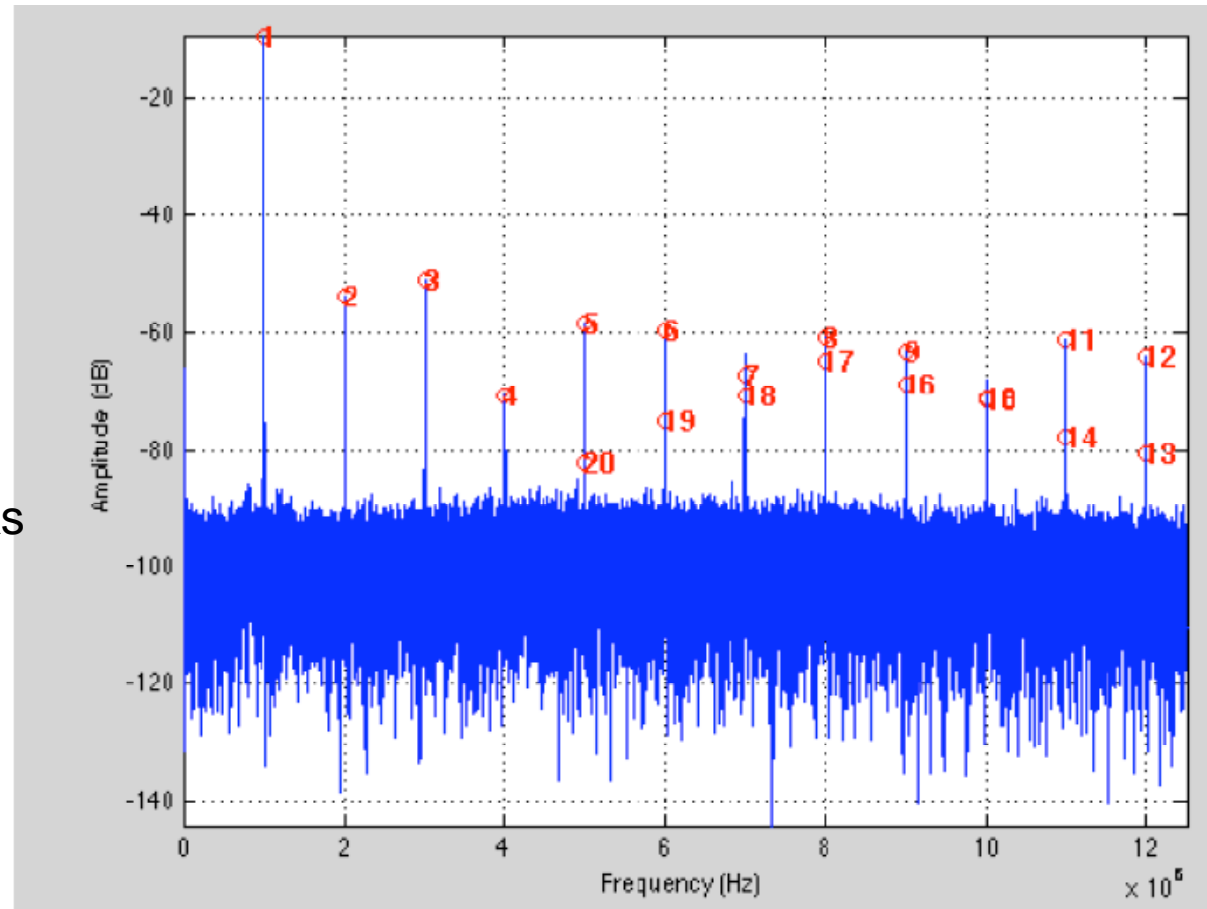
Spectrum analysis (FFT)
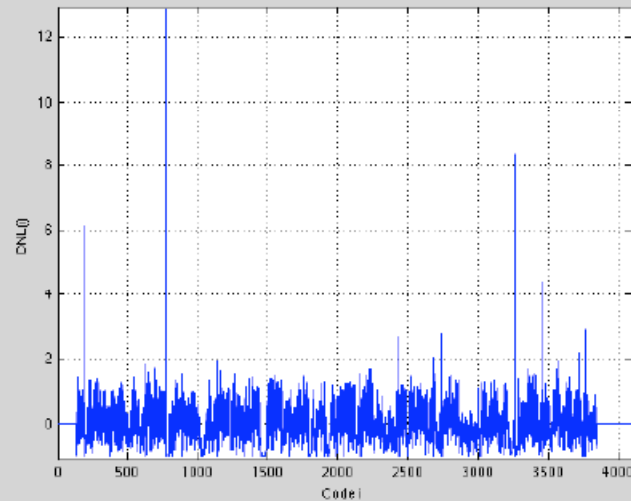
Dynamic range = OK
 (noise floor at -99db)
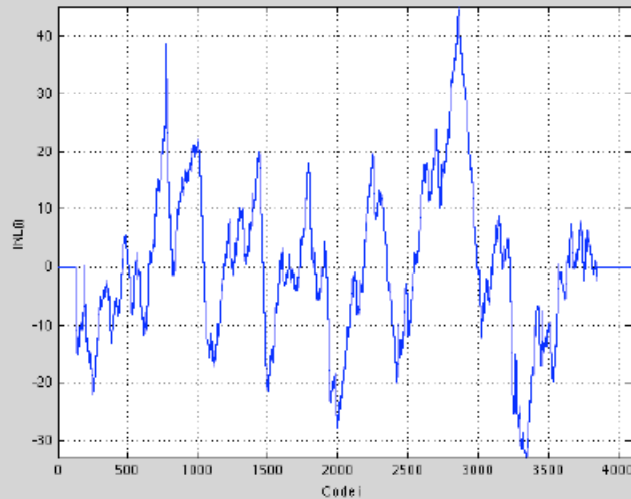
But many distortions peaks

Linearity still to be understood

DNL quite good

resultsDNL =

     mean_DNL: -0.0301
     std_DNL: 0.6361
  peak_to_peak: 13.8093
     peak_min: -1
     peak_max: 12.8093

INL??
Is it the S/H limits
Or the offset error
Founded in the
Design?

Investigations are going on
Some errors found in the MDAC

resultsINL =

     std_INL: 13.7467
     mean_INL: 8.5013e-14
     peak_min: -33.0353
     peak_max: 45.1563
  peak_to_peak: 78.1916

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Summary of the test second proto.

- Speed –OK up to 40Mhz
- DNL -> OK
- Power switching -> OK
- Power dissipation 60mW instead of 40mW and this is fixed
- INL ->NO (investigations are going on: S/H limits? Errors found in the layout)
- The third version will be received in two weeks with some improvements

NEXT STEPS for the "12" bits ADC design

1) The test is really a critical task (3 months)
2) Including a S/H is necessary for accurate test
   But its test is more critical than the ADC….

Design of a 12bits=>digital control of the gain is
   absolutly necessary, and we are working on it.

We found some errors in the layout which are fixed
   (it could have introduce 10LSB errors)