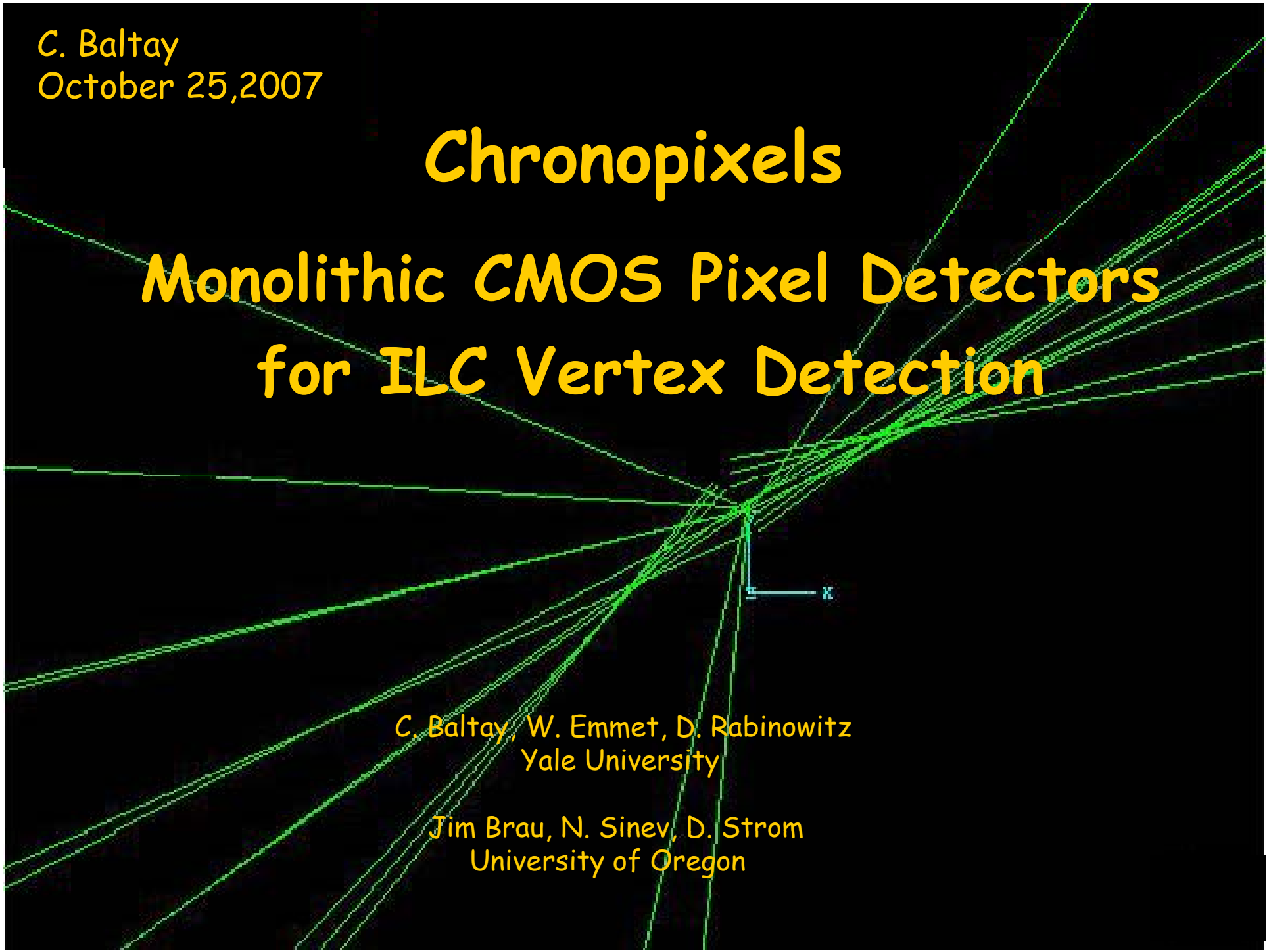
C. Baltay
October 25,2007

Chronopixels

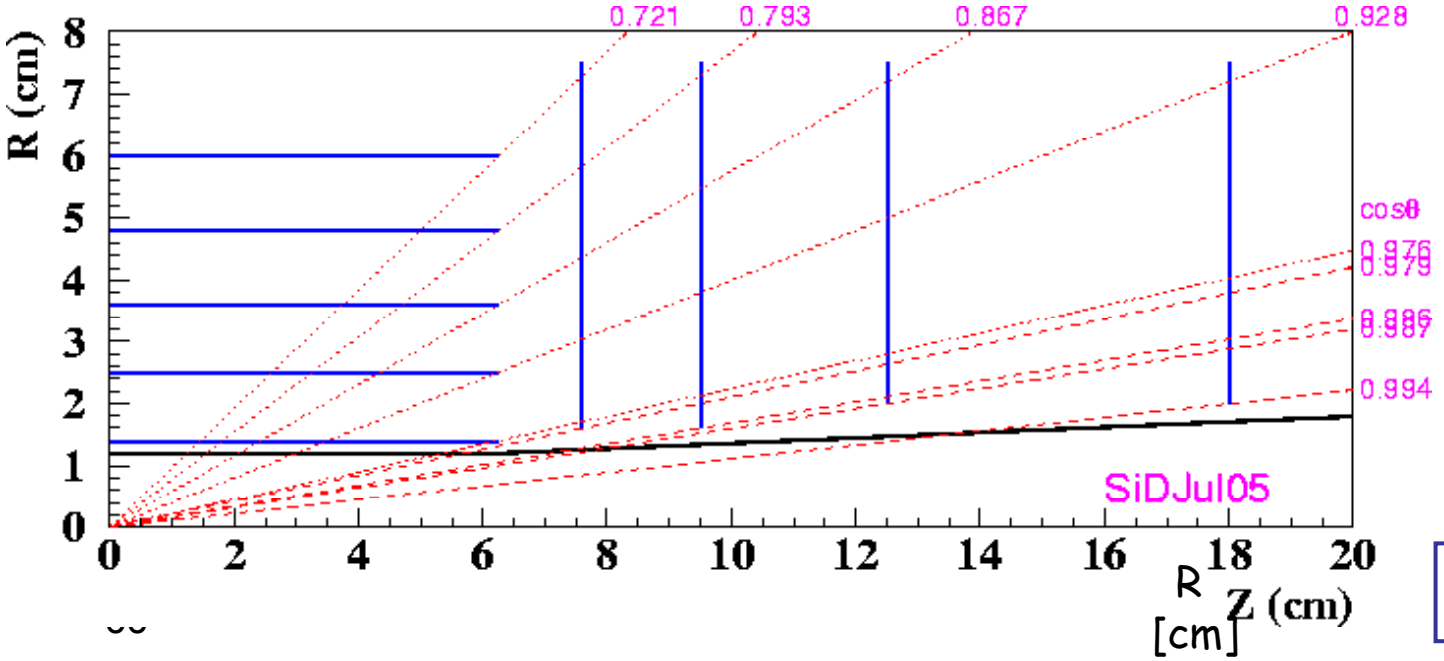
Monolithic CMOS Pixel Detectors for ILC Vertex Detection



C. Baltay, W. Emmet, D. Rabinowitz
Yale University

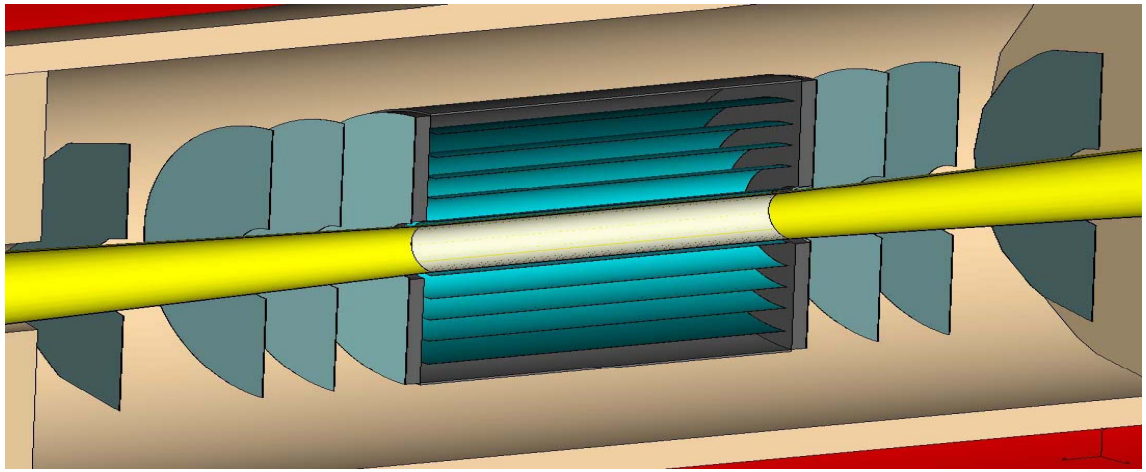
Jim Brau, N. Sinev, D. Strom
University of Oregon

SiD Vertex Detector Layout



5 barrel layers
4 end disks

5 Tesla



SiD Vertex Detector

- BARREL
  - 100 sensors
  - 1750 cm^2
- FORWARD
  - 288 sensors
  - 2100 cm^2

Table I: CMOS Detector Barrel Configuration

Layer	Radius (cm)	Total Length (cm)	No. of Chips	Chip Size (cm^2)
1	1.4	12.5	12	12.5×1.2
2	2.5	12.5	24	12.5×1.2
3	3.6	12.5	20	12.5×2.2
4	4.8	12.5	20	12.5×2.2
5	6.0	12.5	24	12.5×2.2

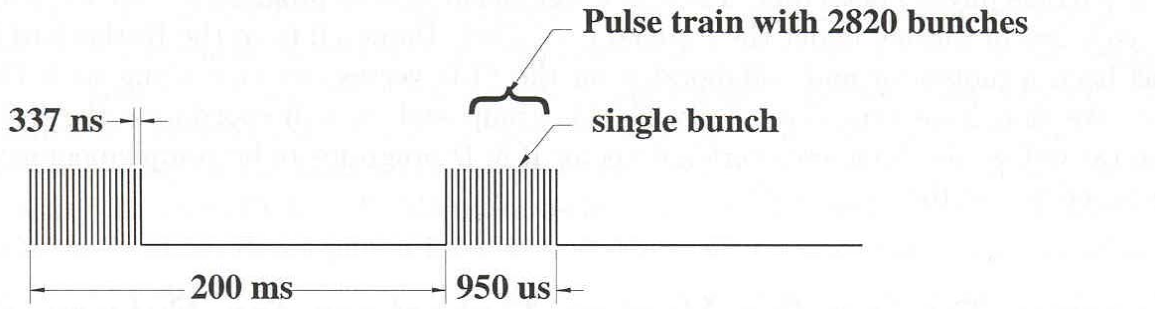
Table II: CMOS Detector Forward Disk Configuration

Annulus	Inner Radius (cm)	Z (cm)	No. of Chips	Chip Size (cm^2)
1	1.6	7.6	24	1.5×0.9
	3.1	7.6	24	4.4×2.2
2	1.6	9.5	24	1.5×0.9
	3.1	9.5	24	4.4×2.2
3	2.0	12.5	24	1.1×0.9
	3.1	125	24	4.4×2.2
4	2.0	18.0	24	1.1×0.9
	3.1	18.0	24	4.4×2.2

Consider Typical Chip of 12.5cmx2.2cm

Time Structure for the TESLA Design

Assume this design for the ILC for Now



Background Calculation:

At 1.5 cm from Interaction Point with 3 Tesla field expect

0.03 hits /mm^2/bunch crossing

Will use this number for the entire detector

Monolithic CMOS Pixel Detectors

➔What are they?

- New CMOS technology makes pixels as small as 10 μ x 10 μ possible
- Each pixel has its own intelligence (electronics) under the pixel
- Unlike CCD's, all pixels are NOT read out in a raster scan
- Reads out x,y coordinates only of pixels with hit (i.e., exceeding an adjustable threshold) at 50 MHz
- Monolithic design – photosensitive detector pixel array and read out electronics for each pixel on the same piece of silicon – can be quite thin (less then 50 μ)

Conceptual Design

- During the past years, working with SARNOFF, we developed a conceptual design that:
  - we believe will work for an ILC Vertex Detector
  - that SARNOFF believes they can build.
- Plan to integrate over pulse train and readout during 200 msec between trains to avoid EMI (Electromagnetic Interference) during train.
  - Occupancy would be too high
  - BUT – for each hit, readout x,y, AND time of hit (time to better than 300 nsec precision effectively tagging each hit with its bunch crossing number)
  - In analyzing Vertex detector data look only at hits which occurred in the same single bunch crossing

➔ Occupancy ~ 10^{-6} at 0.03 hits/mm^2!!

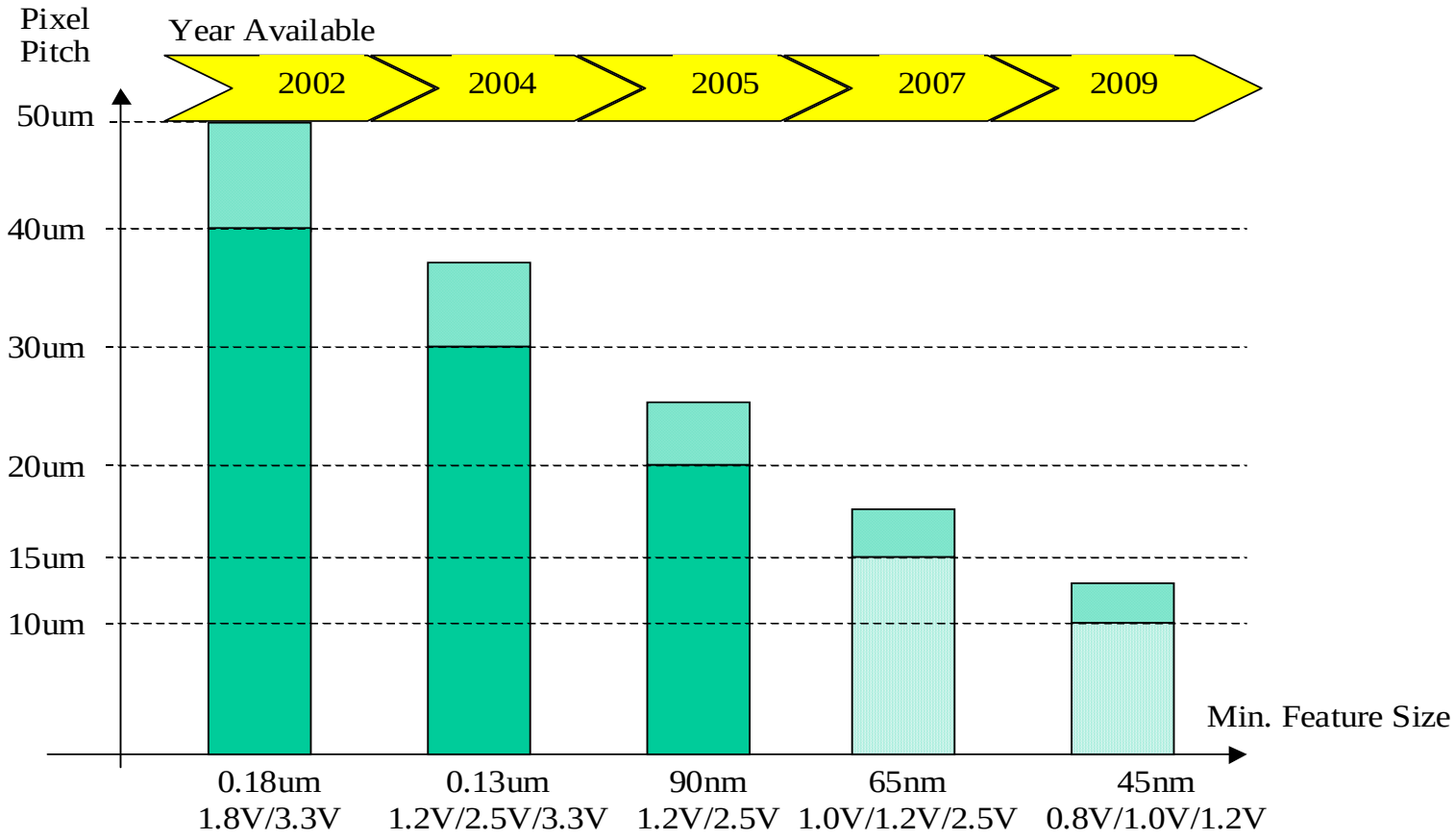
What Limits the Pixel Size

How small can we make the pixels and still store the hit time information of up to 4 hits/pixel

a) Area needed with present technology (0.18 µ) is 50micronsx50microns for:
   - Comparator/counter/latch, etc., circuit
   - Storage of up to 4 hits, i.e., 14 bits 4 deep

b) Process Technology – how does pixel size scale as process technology goes from 0.18 µ to .13 µ to . . .?
   - What do you need to go to 10 µ x 10 µ pixels?
   - Can you estimate the progress of this technology
     - What's available today?
     - Much more interesting – what will be available ~ 5 years from now when we need to fabricate the actual devices?

Technology Roadmap: Macropixel size estimation vs. Mixed-signal Process Technologies

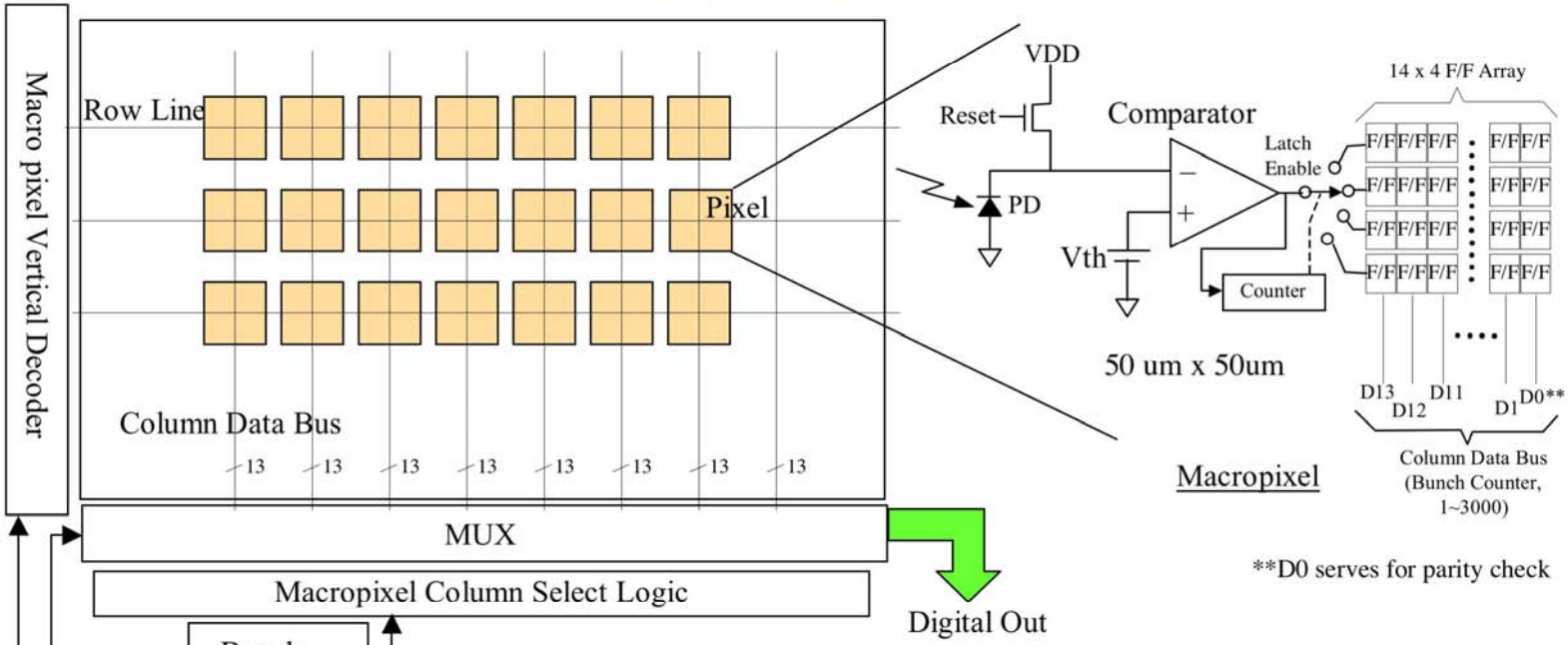


Current Design

- Monolithic CMOS Process (0.045 micron technology)
- Single Layer of Pixels,in the range of 10umx10um to 15um to 15um
- Detect Hits above adjustable Treshhold
- Store time of Hit, up to 4 hits/pixel
- Integrate over Bunch Train, Readout during 200 msec between trains
- Digital Readout(no Analog)

Chronopixel Design

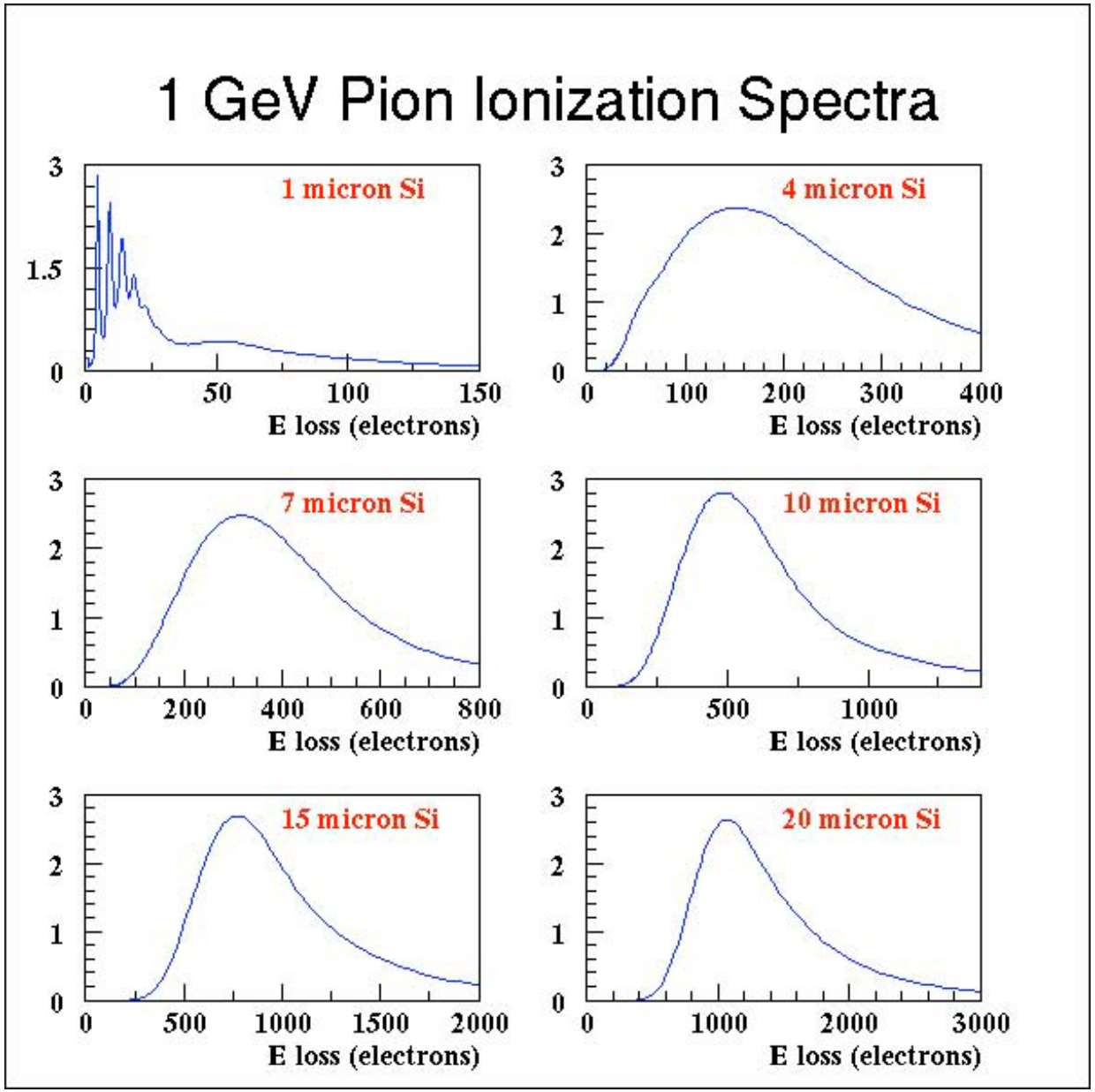
Macropixel Array Architecture



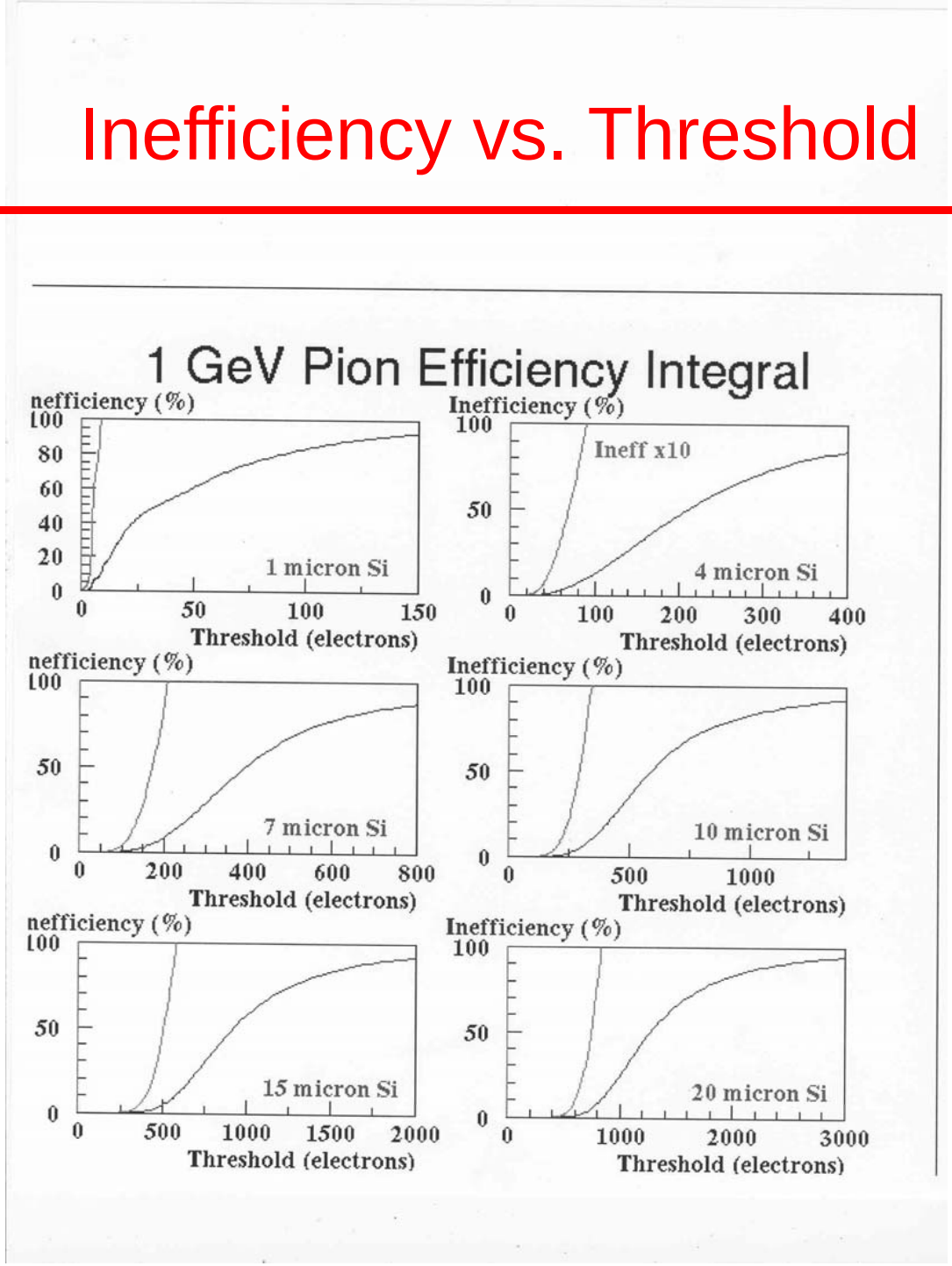
- As a local digital memory to store the time stamp, F/F's are used. To express 3000 bunches, 12 bits are needed and 13th and 14th bits are for checking the parity. Since average multiple impact probability per pixel is assumed to be 4, 14 (H) x 4 (V) F/F's are needed in this architecture.
- When a particle impacts, a pixel's signal rises above the threshold level and comparator out switches from '1' to '0', enabling the F/F's to latch the time stamp data supplied by the global bunch counter. When the data is latched, the pixel is reset.
- If next particle impacts the same location, comparator out enables next set of F/F's to preserve the previous time stamp data. This is implemented using a counter which increments the row address of the F/F array.
- Time stamp information is read out in the random access mode from the pixels of interest which stored nonzero time stamp data.

Signal to Noise

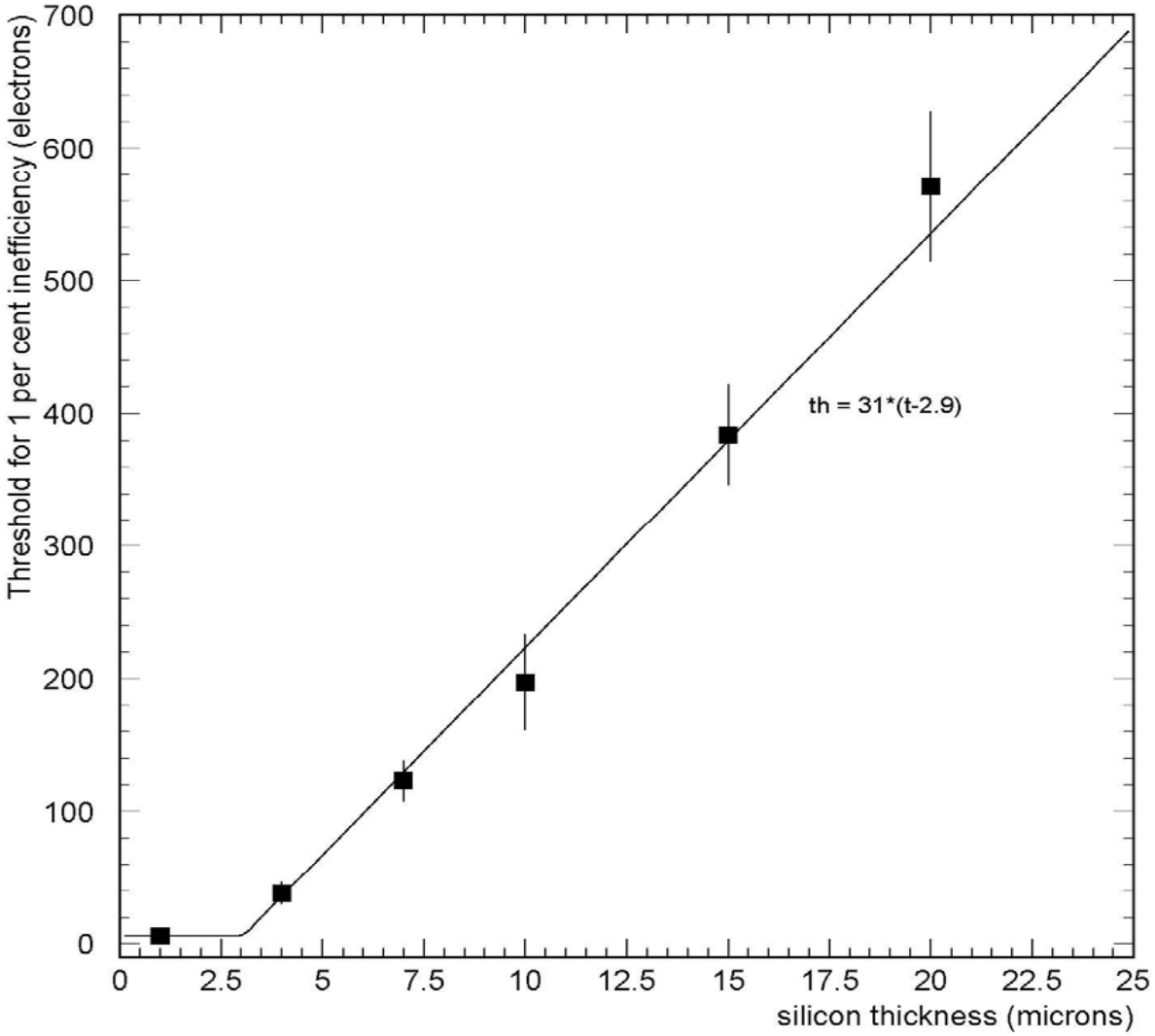
- Signal due to particle crossing Silicon has a broad distribution
- Peak or mean signal is not the relevant consideration
- Question to ask is at what signal level(I.e. at what threshold) do we detect >99% of the particles
- Charge may be shared between two pixels


1 GeV Pion Ionization Spectra
1 micron Si
4 micron Si
7 micron Si
10 micron Si
15 micron Si
20 micron Si
E loss (electrons)

Inefficiency vs. Threshold



Threshold for 99% Efficiency vs.Epilayer Thickness



Signal to Noise Considerations

- Would like 99% efficiency even for particles whose charge is shared evenly between two pixels.
- Would like threshold to be at 5 sigma of the noise to keep fake hits to below 1/3 of the real hits I.e. <0.01hits/mm**2 or 10e-6/pixel

Si thickness	electrons at 99%	threshold	acceptable noise
4	40	20	4
7	125	63	13
10	250	125	25
15	400	200	40
20	550	275	55

Readout Procedure and Speed

- Expected hit rates:
  - Consider chips 22 mm x 125 mm = 2750 mm^2
  - Total no. of 10 µ x 10 µ pixels = 27.5 x 10^6 pixels/chip
  - Total hits .03 x 2820bunches x 2750mmsq = 2 x 10^5 hits/chip
- Number of bits to read out one hit pixel

  X info (up to 2200) – 12 bits + parity = 13 bits
  Y info (up to 12500) – 14 bits + parity = 15 bits
  Time (up to 3000) -12 bits +2 parity = 14 bits
  42 bits total
- 2 x 10^5 hits/chip x 42 bits/hit/50 MHertz = 168 msec.
- This should work,but not much safety margin in case the background is much higher then anticipated.
- Preferred Readout scheme-
  - Divide device into 40 segments,read these out in parallel into a FIFO buffer at 50MHertz (~4msec)
  - Read out FIFO buffer at 1/2 Ghertz (~16 msec)
  - This has a factor of ~10 safety margin!
- The 42 bits/hit and the readout time can be further reduced by a more clever readout scheme.

Charge Spreading

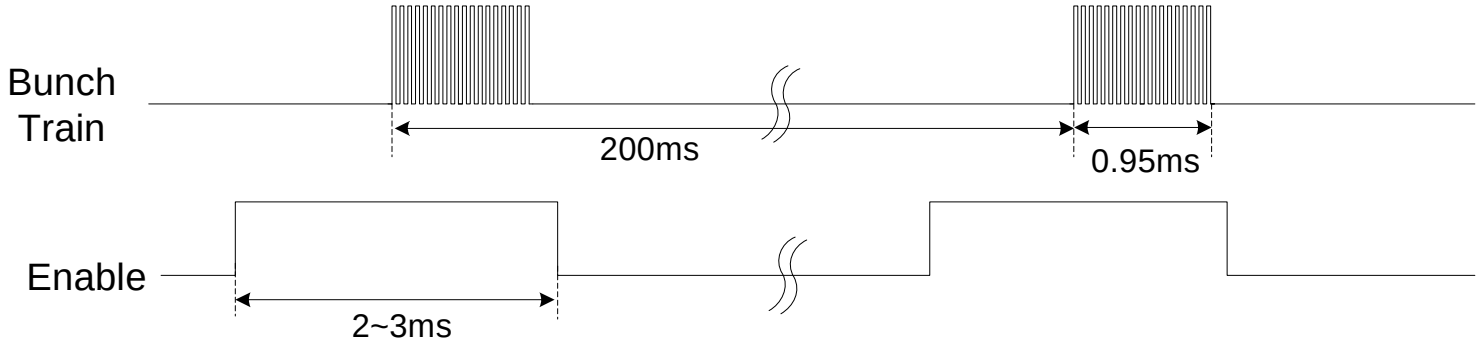
- It is important to keep charge spreading to much smaller than the pixel size so that we can give up on the analog information.
- How small can we keep the charge spreading
  - Thickness of expitaxial layer – 15 μ
  - Deplete expitaxial layer – need high resistivity, ~ 10 Kohm cm
  - -- Can keep charge spreading to a few microns

3D Simulations under way to study these effects (Nick Sinev)

Power Dissipation Analysis

	Component	Optimized Power Dissipation	Before Optimization
Analog	Detector	9.9uW	11.7uW
	Comparator	27.0uW	35.1uW
	Sub_total	36.9uW	46.8uW
Digital	Timing Logic	0.05uW	
	Counter/Decoder	0.07uW	
	Mem. Array	~ 0uW	
	IO Interface	0.01uW	
	Sub_total	0.13uW	
	Total	37.03uW	

Power Reduction Method



* Activate the Detector and the Comparator during the Bunch Train (~2msec) and deactivate during the Readout time(~200 msec)
* Power reduction Ratio of ~ 1/100
* 0.37 Watts per 2cmx12.5cm chip(15mWatts/sqcm)
* We expect that this can be further reduced

Other Considerations

- Dark Current
  - Will reset array after each bunch crossing so dark current should not be a problem during 337 nanosec
- Operating Temperature
  - Sarnoff expects modest cooling (<0°C adequate)
- Device Thickness
  - Thinning to ~ 50 um looks feasible

The First Prototype

- The ultimate design calls for
  - 45 nm Process Technology
  - 10 to 15 micron pixels
  - 15 micron thick epilayer
  - High resistivity Silicon
- Whats easily available now for prototype
  - 180 nm Process Technology
  - Can do 50 micron pixels
  - Readily available Si with routine TSMC fabruns has 7 micron epilayer and low resistivity

The First Prototype

- In order to get first prototype quickly and for a cost we can afford we opted for the TSMC process with the readily available Si with 7 micron epilayer and low resistivity
- The main purpose of this first prototype is to test the electronics performance of the chronopixel design such as noise performance,comparator accuracy and stability,scan speed and power dissipation
- Fab started,expect batch of 40(minimum order) devices in February of 2008

Parameters of the First Prototype and the Ultimate Devices

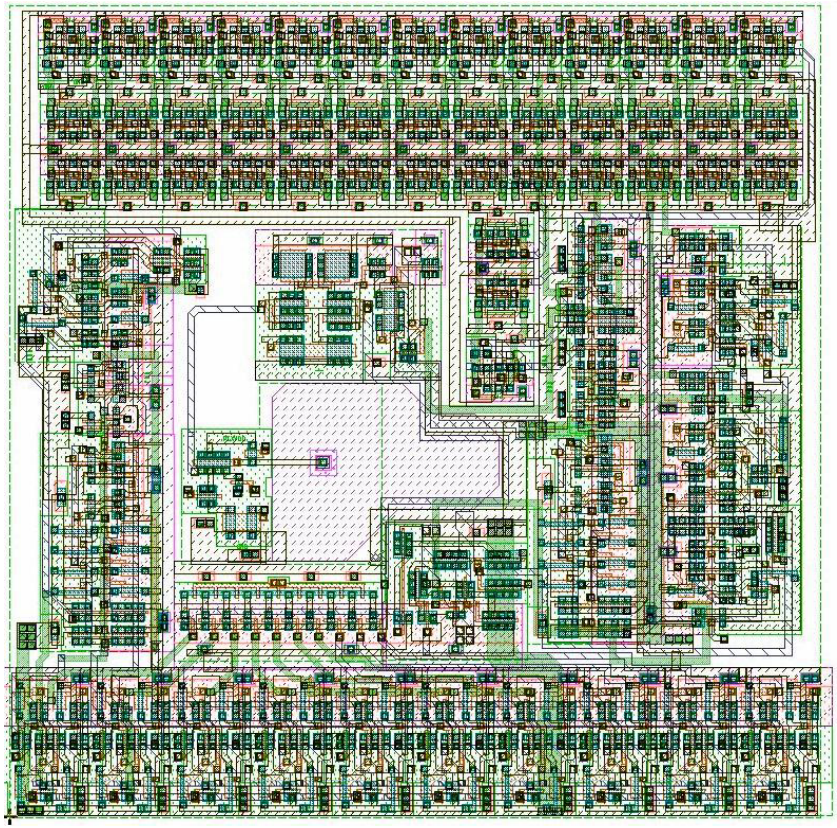
Design Values

Parameter	Ultimate Device	First Prototypes
Chip Size	125 mm x 20 mm	5 mm x 5 mm
Array Size	12,500 x 2000 pixels	80 x 80 pixels
Pixel Size	10 µ x 10 µ	50 µ x 50 µ
Memory Depth	14 bits x 4 deep	13 bits x 2 deep
Epilayer Thickness	15 µm	7 µm
Epilayer Resistivity	10 kilo ohm cm	10 ohm cm
Detector Sensitivity	10 µ V/e	10 µ V/e
Detector Noise	25 electrons	25 electrons
Comparatory Accuracy	0.2 mV rms	0.2 m V rms
X-scan Speed	25 MHz	25 MHz
Power Dissipation	0.15 m W/mm^2	0.15 m W/mm^2
Chip Power	0.4 W/chip	4 m W/chip
Process Technology	45 nm	180 nm mixed signal CMOS TSMC Process

Completed Layout

- Completed Layout of Sarnoff fits 563 transistors into 50 μm x 50 μm pixels for 180 nm technology

- Detector sensitivity
  10 μV/e (eq. to 16 fF)
- Detector noise
  25 electrons
- Comparator accuracy
  0.2 mV rms (cal in each pixel)
- Memory/pixel
  2 x 14 bits each
- Ready for 5mmx5mm array submission
- Designed for scalability
  eg. no capacitors in signal path



Progress and Plans

Calendar Year 2007

- Completed Chronopixel Design
- SARNOFF Completed detailed design of first prototype Jan 31 2007,detailed report in hand
- Started Fabrication of prototypes Oct 15 2007-delay due to late arrival of 2007 funding
- 3D simulations of charge collection efficiency and overall design performance.This effort will continue for the next few years…

Progress and Plans

Calendar Year 2008

- Expect delivery of first batch of prototypes in February of 2008
- Plan to test prototypes at Oregon,Yale,and SLAC
- Test electronics is being designed and built by the Oregon group with help of Marty Breidenbach's group at SLAC
- Start design of second set of prototypes based on test results.Details like process technology,pixel size,epilayer thickness and resistivity will depend on what SARNOFF and the foundries can do at that time.

Progress and Plans

Calendar Year 2009

- Complete design of second prototype by SARNOFF
- Fabricate second set of prototypes
- Test second prototypes
  - Electronics tests
  - Beam tests?
  - Radiation tests?

Issues and concerns for future R&D

- Can power consumption be reduced further? How will it scale as we go to 10 micron pixels?
- What redesign will be needed to go to prototype 2,based on what we learn from prototype1(readnoise,comparator accuracy and stability,etc…).
- How will voltages to deplete epi-layer scale to the 45 nm technology(issues of charge collection efficiency etc)