Chronopixel: Design and Prototyping

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- Chronopixel Pixel Design
- Chronopixel System Design
- Prototype Plans
- Summary

Chronopixel Project:

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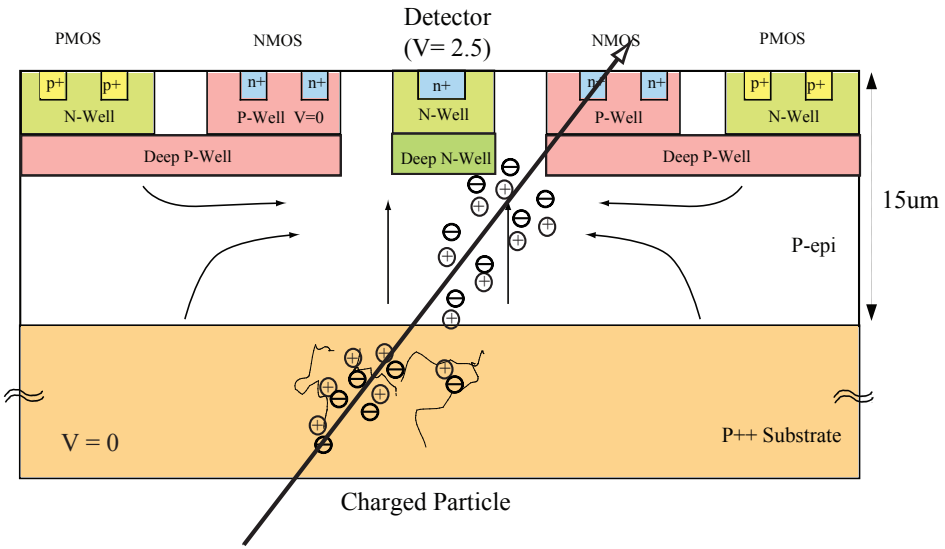
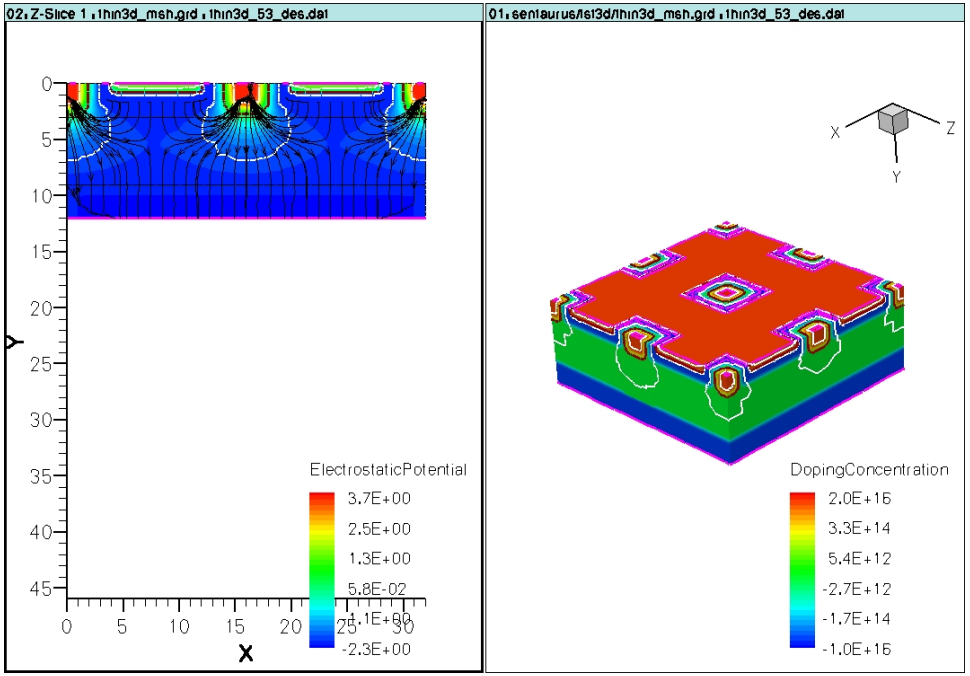
Yale University

EE work is contracted to Sarnoff Corporation

Pixel Design

• Use a deep P-well to isolate the charge collection region from the N-wells of the PMOS transistors:



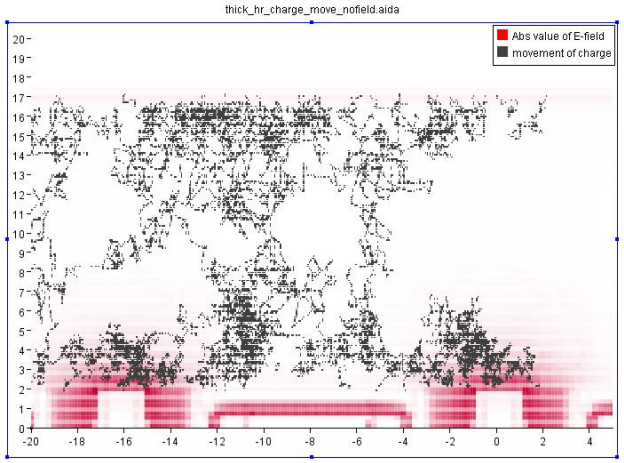


• Possible bias voltages for the detector node are usually limited to highest voltage allowed by the process. For small feature sizes, this voltage may be quite small.

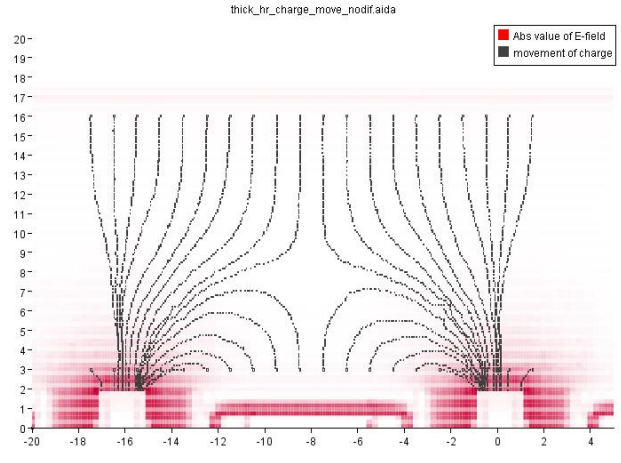
• It is likely that most of the charge we collect will be via diffusion. We are investigating the role of the weak field in the undepleted epi-layer and configurations of the p-implants that will help reflect the charge to the charge collection input.

• We have developed an option for the SiD Monte Carlo that can use the output of the field map from the 3D TCAD DESSIS calculation to calculate the fraction of charge that will be collected.

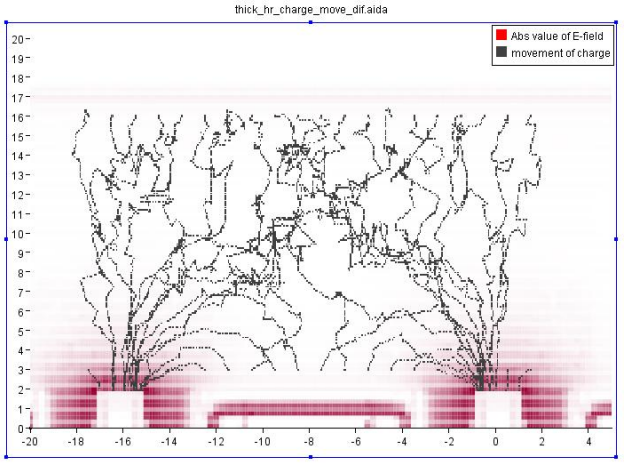
•Thus far, our assumption that over most of the cell, at least 50% of the charge will be collected by the node closest to the track, is confirmed in simulation.



Diffusion Only



No Diffusion



Diffusion + Field

• Examples of Nick Sinev's simulation – in high resistivity epilayer, there is apparently enough field in the undepleted region to efficiently collect the charge.

• In high resistivity epilayer transition between depleted and undepleted region if fairly large – increasing the charge collection region.

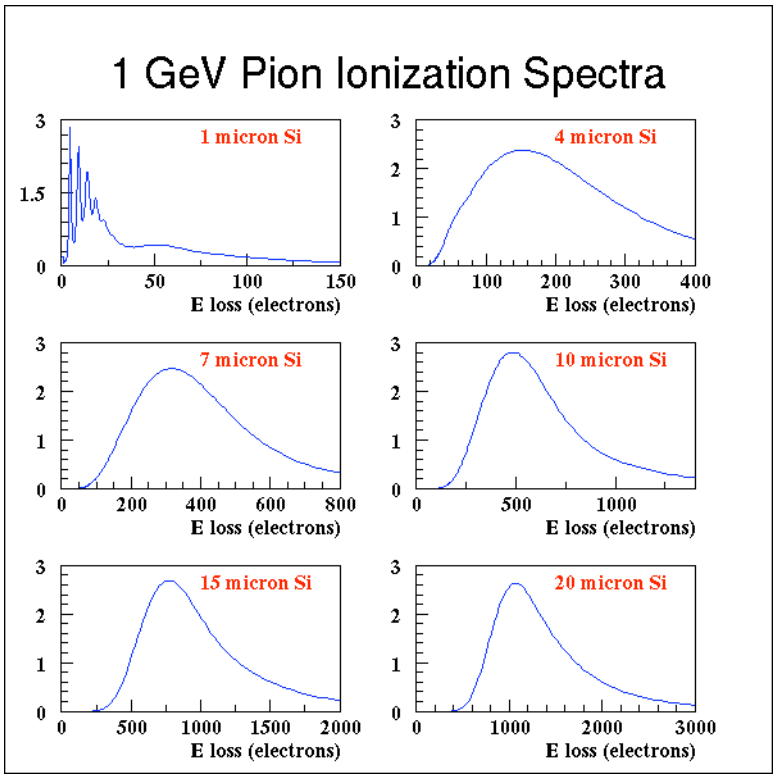
High efficiency and low hit multiplicity is possible:

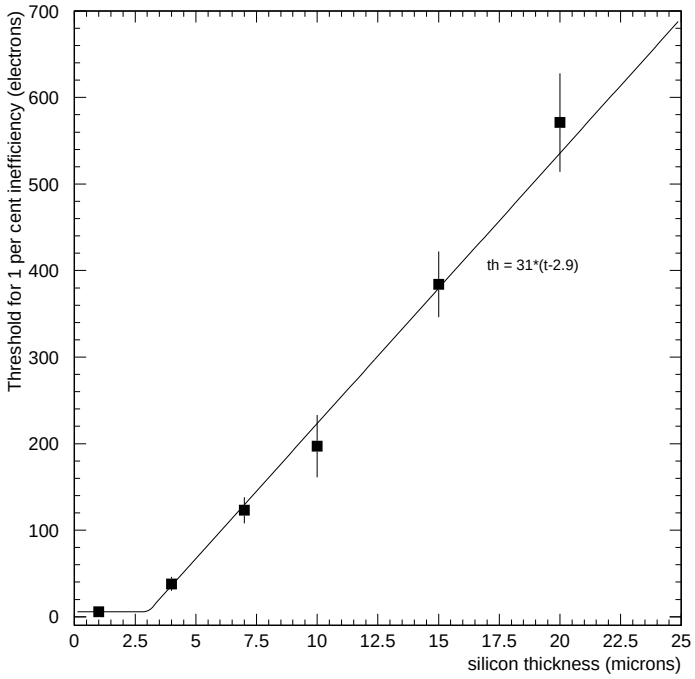
Pixel size (μ)	Tan(λ)	EPI layer 20μ thick				EPI layer 12μ thick			
		100e	125e	160e	200e	100e	125e	160e	200e
16x16	0.	100.	100.	100.	99.95	99.0	98.1	94.4	88.0
	0.2	100.	100.	100.	99.6	98.8	97.7	94.5	89.0
	0.4	100.	100.	100.	99.9	99.1	98.4	95.3	90.9
	0.7	100.	100.	100.	99.95	99.7	99.0	97.6	94.5
	1.0	100.	99.95	99.87	99.64	99.7	99.45	98.7	97.2
12x12	0.	100.	100.	99.95	99.65	99.2	97.5	95.0	87.6
	0.2	100.	100.	99.95	99.75	99.0	98.2	96.5	93.
	0.4	100.	99.95	99.85	99.6	99.1	97.8	95.6	90.6
	0.7	100.	100.	99.9	99.9	99.75	99.1	97.9	94.7
	1.0	100.	100.	100.	100.	99.9	99.7	98.7	96.5
8x8	0.	99.95	99.85	99.55	98.8				
	0.2	100.	99.9	99.5	98.0				
	0.4	99.95	99.85	99.65	98.7				
	0.7	100.	99.95	99.6	98.7				
	1.0	100.	100.	99.9	99.5				

Pixel size (μ)	Tan(λ)	EPI layer 20μ thick				EPI layer 12μ thick			
		100e	125e	160e	200e	100e	125e	160e	200e
16x16	0.	1.46	1.38	1.30	1.23	1.22	1.15		
	0.2	1.51	1.44			1.24	1.16		
	0.4	1.64	1.56			1.25	1.18	1.09	1.0
	0.7	1.85	1.75			1.35	1.28	1.18	1.08
	1.0	2.12	2.0			1.48	1.4		
12x12	0.	1.66	1.55			1.21	1.14		
	0.2	1.71	1.60			1.23	1.18		
	0.4	1.89	1.76			1.25	1.19	1.1	1.01
	0.7	2.14	1.99			1.38	1.30		
	1.0	2.53	2.36			1.56	1.45		
8x8	0.	2.43	2.12	1.7	1.47				
	0.2			1.77	1.53				
	0.4			2.06	1.76				
	0.7	3.17	2.79	2.43	2.08				
	1.0	3.72	3.28	2.84	2.41				

N.B. Set thresholds to give at least 99% efficiency (green area)

Expected Charge Collection

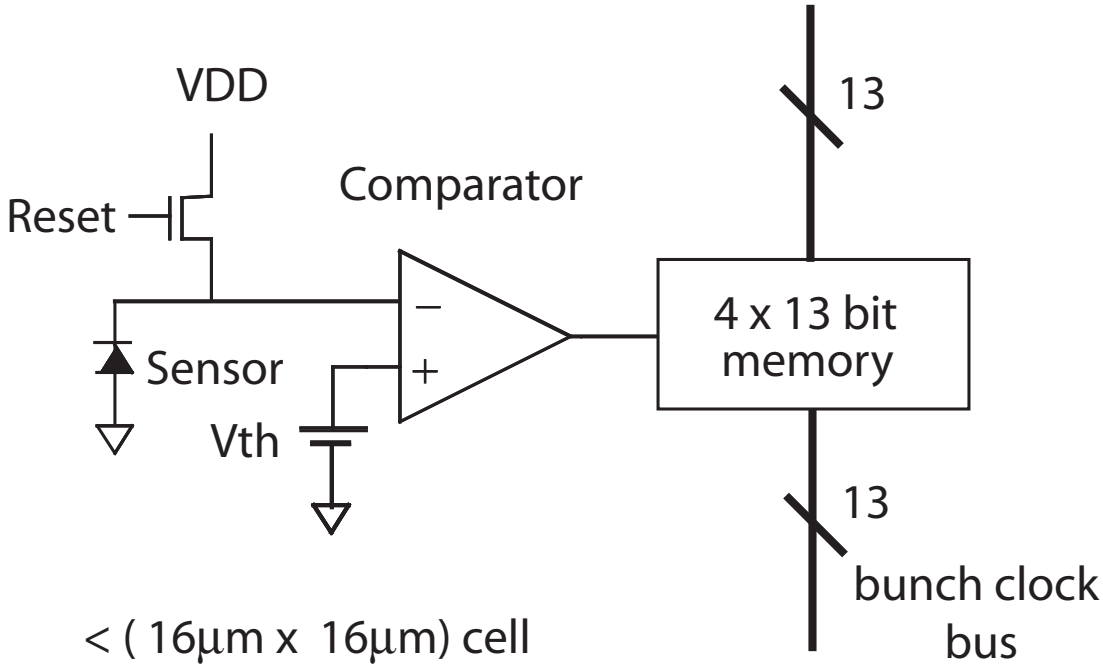




Epilayer Thickness (microns)	Electrons at 99% Efficiency (electrons)	Threshold (electrons)	Acceptable Noise (noise)
4	40	20	4
7	125	63	13
10	250	125	25
15	400	200	40
20	550	275	55

In Pixel Electronics

Functional schematic:



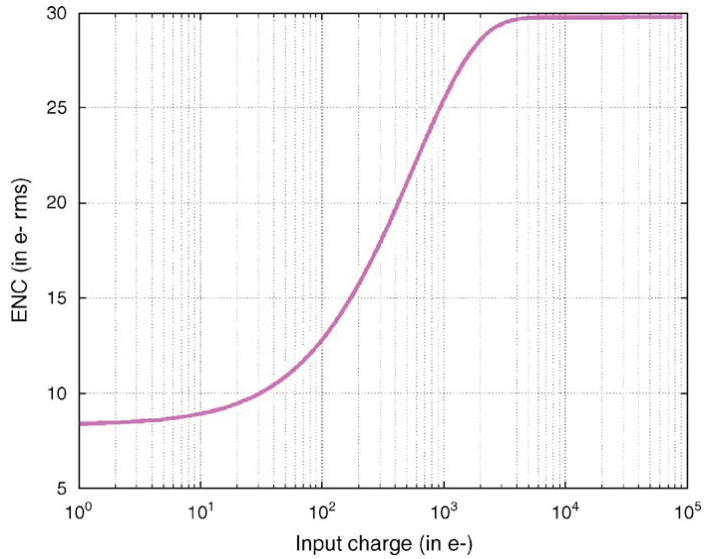
N.B. number of bits in memory depends on bunches in ILC and error correction, if any.

Is this noise achievable?

Main source of noise is due to reset.
$\Rightarrow$ We expect the total capacitance at the input node to be less than 16 fF, naively giving reset noise:

$$\sqrt{kTC} = 50 \text{ electrons}$$

To reduce this noise we use a soft reset and feedback: see NIMA 560(2006)139, well suited to our low occupancy situation.



- Other sources of noise, e.g. 1/f and thermal noise in the first transistor, are expected to be < 10 electrons.

- **SARNOFF expects prototype noise to be 25 electrons**

How precisely do we need to set the threshold?

- Assuming a noise target of 40 electrons, we need

$$\sigma_{Vth} \simeq \frac{40e}{16\,\mathrm{fF}} = 0.4\,mV$$

Expected total variation is $\sim 6\,\mathrm{mV}$ – will have two components:

–local random (2 mV)
–slowly global variation

SARNOFF solution:

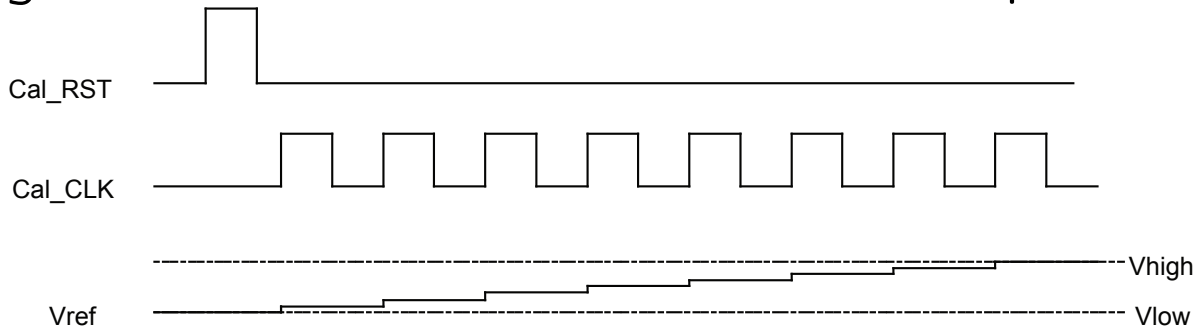
⇒ use a resistor ladder with 10 taps for local variations
⇒ Allow for several different zones for global thresholds

Final threshold precision 0.2 mV

Calibration Procedure

1. Set overall threshold offset to zero

2. Scan through resistor ladder values and find tap corresponding to Vth



   $\Rightarrow$ This could be done before every bunch train

3. Add an offset to all channels in a given zone corresponding to

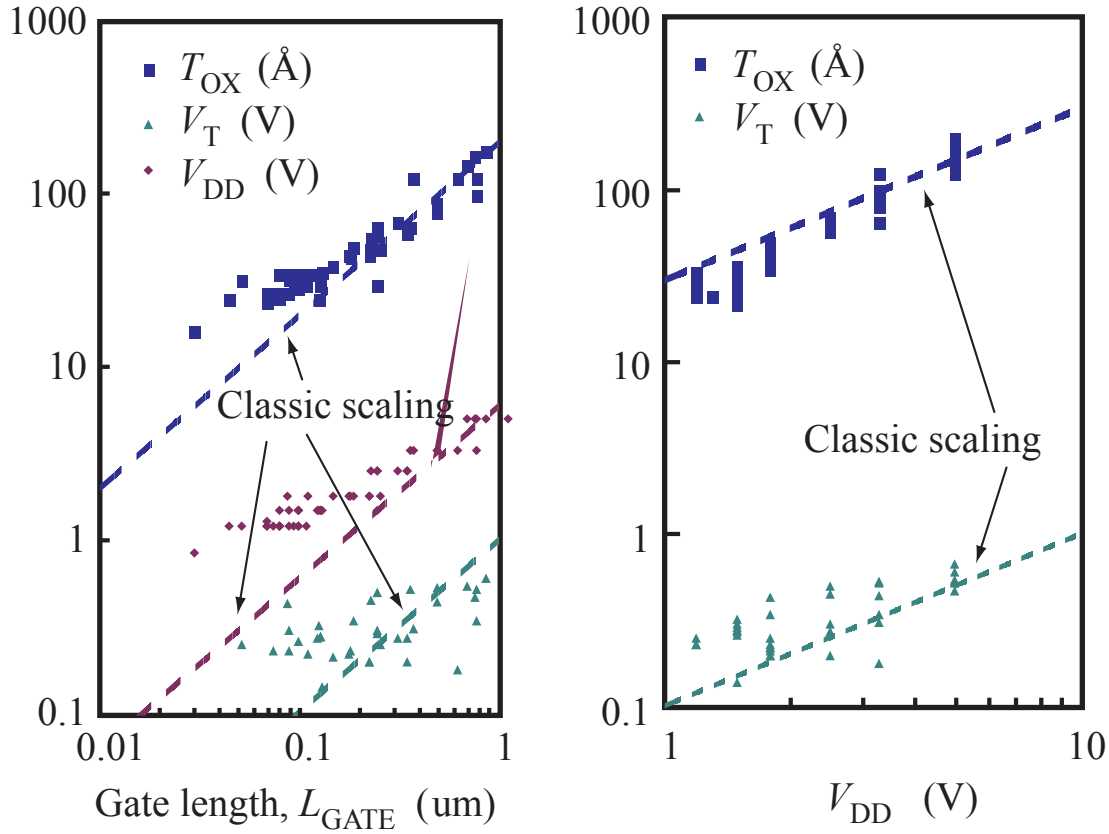
$$5 \times 40 \sim 200 \quad \text{electronthreshold} \sim 2\,\text{mV} \times C/e$$

   c.f. SARNOFF noise estimate 25 electrons.

Will calibration procedure work at smaller feature size?

- Don't expect thresholds to get worse at smaller feature size

- Can use thicker oxide for analog part of circuit



Novak IBM J. RES. & DEV. VOL. 46 NO. 2/3 MARCH/MAY 2002

SARNOFF calibration procedure should work at 45 nm

Power

- Sarnoff estimates analog prototype power will be

$$\sim 40\,\mu\text{W} \times f/\text{channel}$$

or 16mW/cm^2 for $f = \frac{1}{100}$ and 50μm $\times$ 50μm pixels.

- In the prototype power is estimated to be 0.4μW/ pixel

- Power must be reduced for the final devices. Scaling the prototype: $\sim$ 0.4 W/ladder, peak current $\sim$ 16 A.

$\Rightarrow$ power in the circuit is dominated by the comparator
– Can reduce current by 10 without hurting noise
– Explore with prototype
$\Rightarrow$ Noise limit on power is $\propto C_{tot}^4$
– power/area should decline with feature size

Will it fit?

• The prototype design (180nm 50μm $\times$ 50μm) with 2 memories has 600 transistors allocated as:

Item	Fraction
memory	30%
calibration circuit	33%
i/o interface	18%
analog cicruit	3%
digital logic	16%

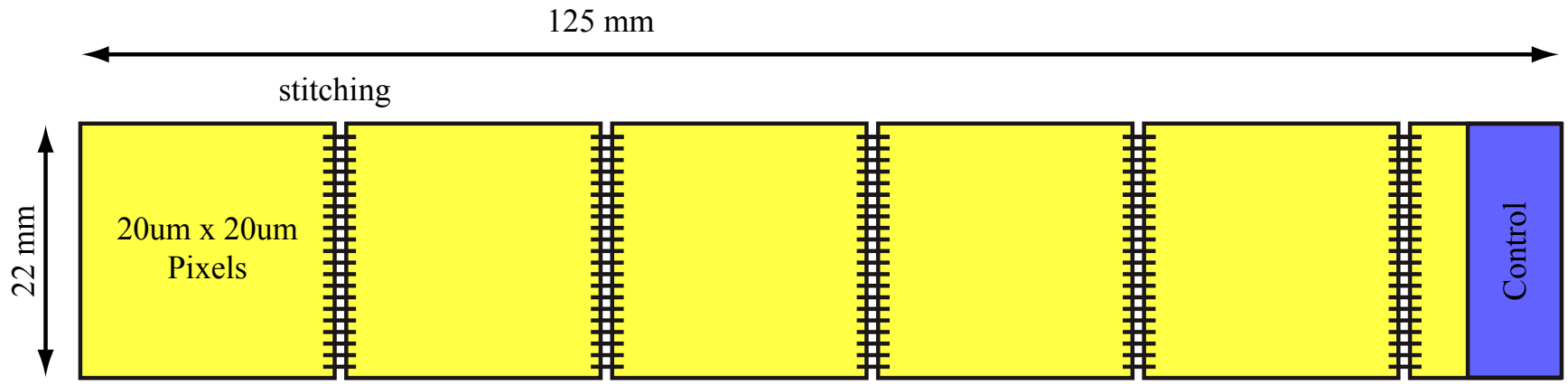
• For the final device with 4 buffers about 800 transistors are needed. To reach a pixel size of 14μm $\times$ 14μm, a factor of 4 in feature size is needed (45 nm).

• Even smaller pixels can be achieved by reducing dead space near charge collection, perhaps reduce to 3 buffers

• Prototype has 12 bits + 2 bits for error checking. Error checking may not be needed in final version: **Final version range 10-15 μm**

Prototype design is scalable (e.g. no capacitors in signal path)

Possible barrel ladder layout:



- Basic pixel unit fits in a single reticle

- Sarnoff stitching technique used to connect pixels buses to control logic.

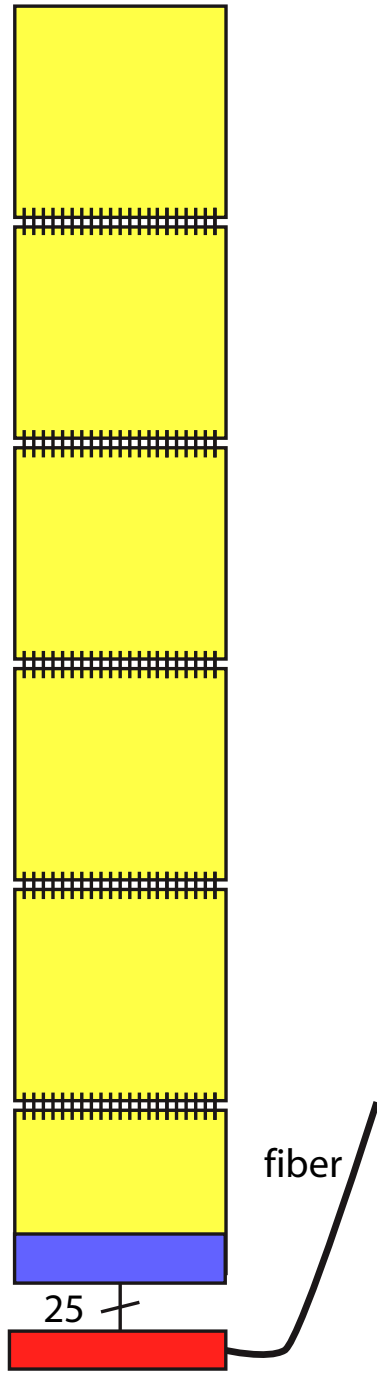
- Power and readout from one end of ladder ($\sim$ 100 connections)

Data Rates

- At baseline occupancy, we expect 250k hits-clusters/ladder/train, ∼1 M hit-clusters/ladder/sec
- Parallel readout of chip at 50MHz gives factor of 40 safety margin for multiple hits and increased occupancy
- Possible data structure (10μm pixels)

Row & Ladder (25bits)	
Column (12 bits)	Bunch No. (13 bits)
. . .	
Column (12 bits)	Bunch No. (13 bits)
End of Row (25bits)	

- Readout 25 bits in parallel, serialize on optical fiber, ∼ 1.25Gbits/s

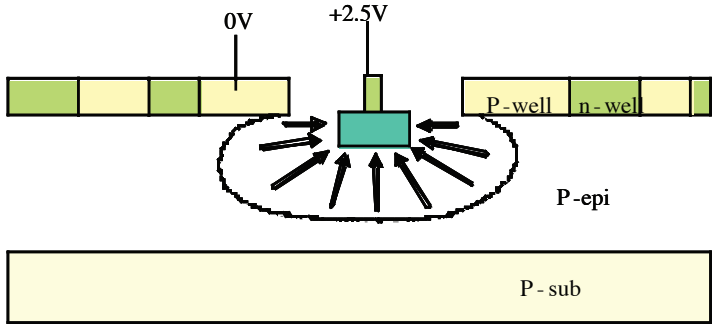


Prototype

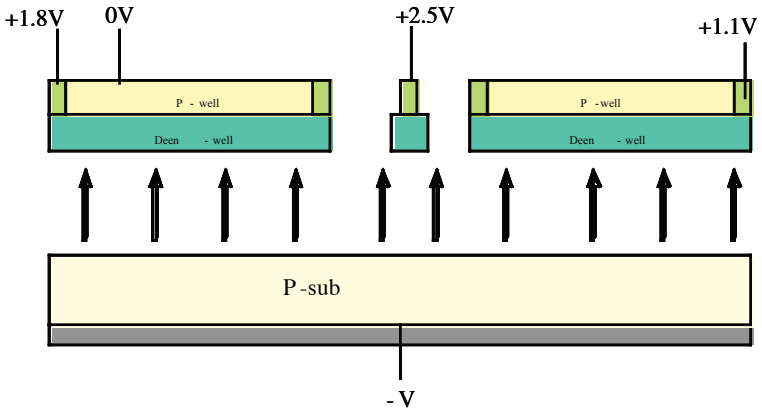
• Initial prototypes will made at TSMC, which currently does not offer deep p-wells or thick 15 μm thick epilayers

• Will use two pixel geometries to allow tests for pixel circuit with an IR laser and with ^{55}Fe:

Pixel -A

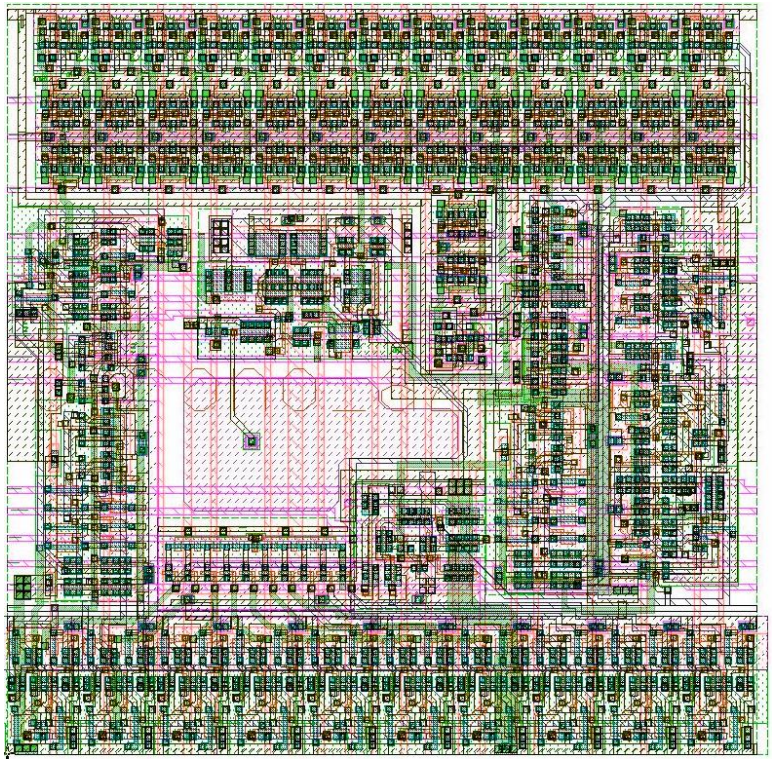


Pixel -B

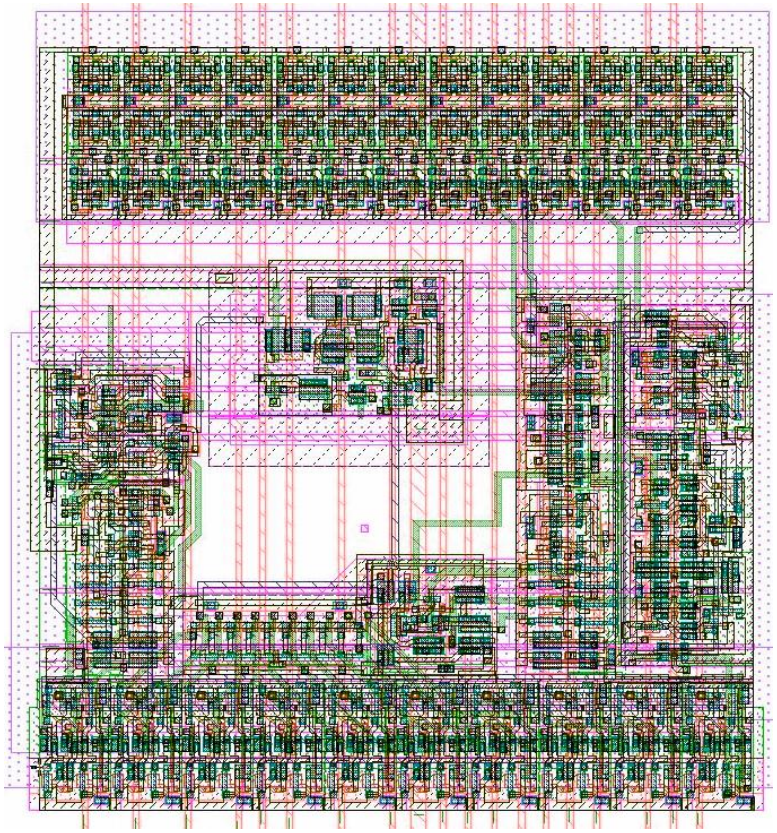


Note pixel b takes more space to keep currents from the 1.1V and 2.5 V n-wells small

Prototype layout is finished and ready for fab.

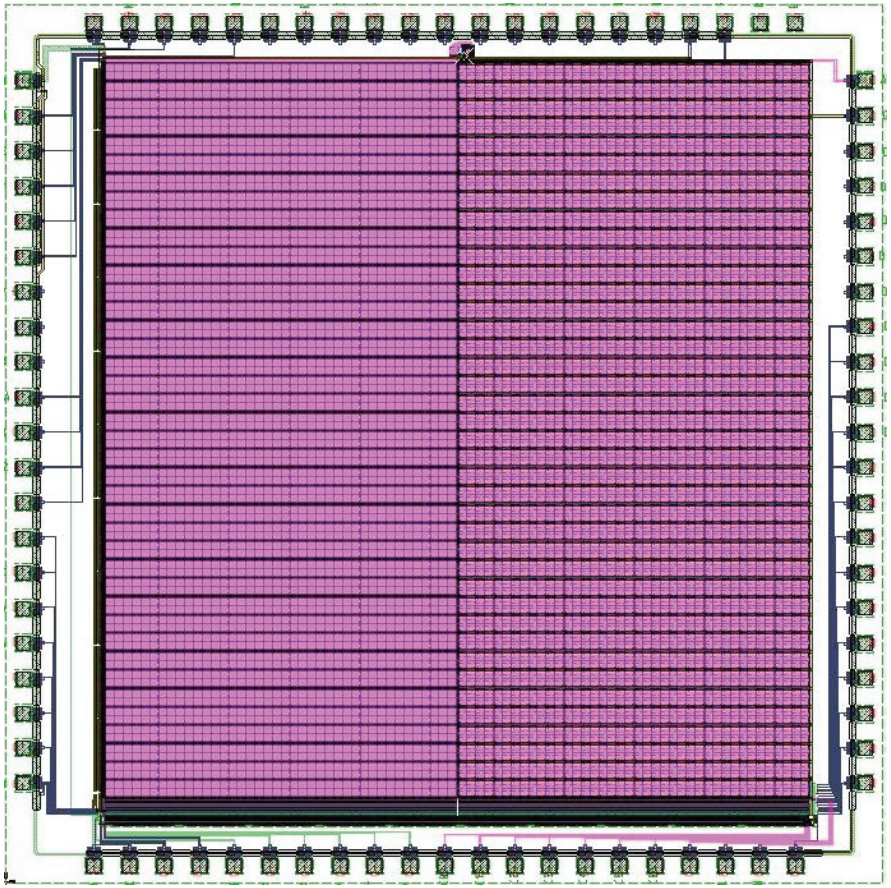


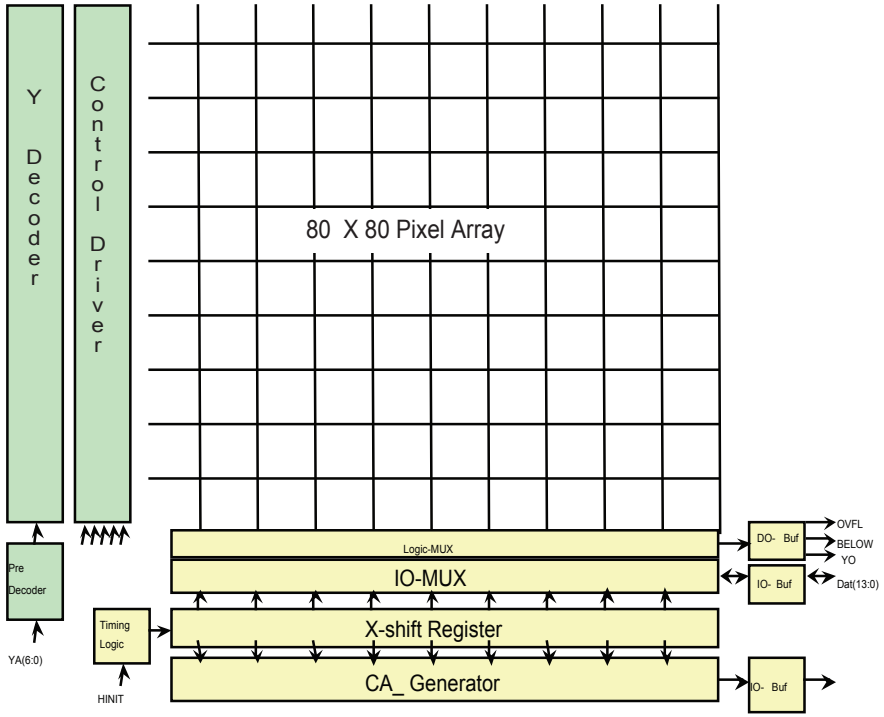
Pixel A



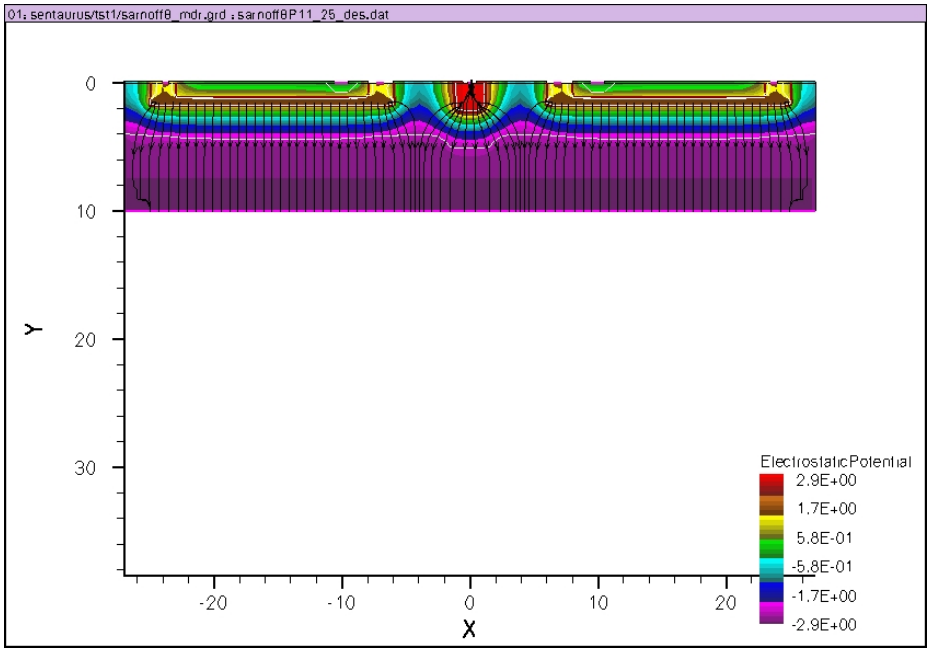
Pixel B

Final Chip is 80 $\times$ 80 pixels (also includes individual test pixels)

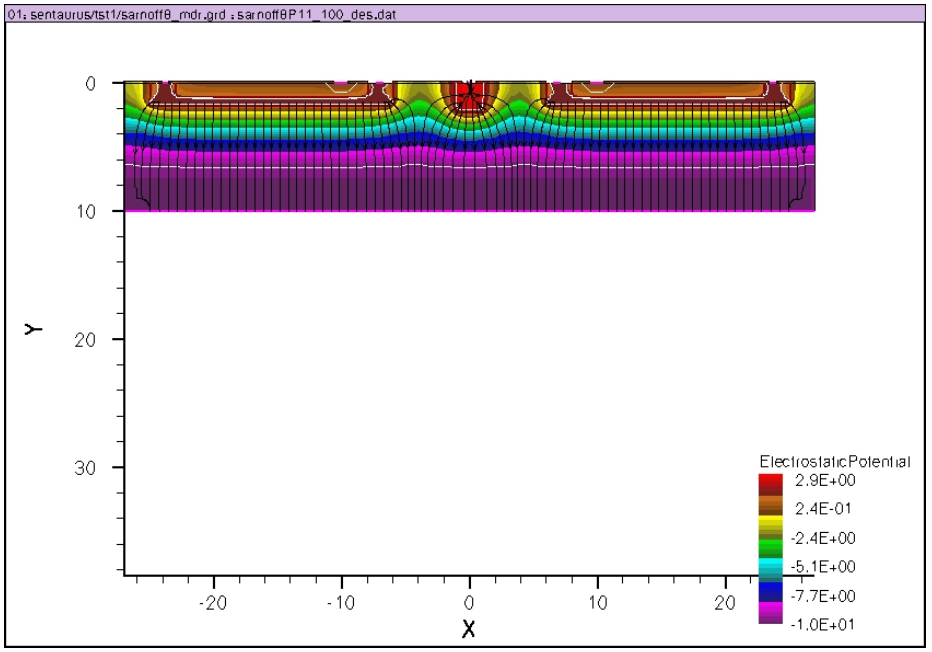




Prototype Simulation – Pixel B



2.5 V bias



10.0 V bias

We can vary bias voltage in experiment and simulation and compare the collected charge

Prototype Testing

- Use MIMOSA-18 devices to check that we can get expected results with lasers and ^{55}Fe.

- As soon as Chronopixel goes to FAB (now) will start work on the electronics board needed to read it out in conjunction with our SLAC colleagues.

- Measurements to be made include:
  - Measure noise with S curve technique
  - Measure sensitivity with ^{55}Fe
  - Measure position dependent response with laser

Conclusions

- The design and layout of a 50μm $\times$ 50μm *scalable* Chronopixel device is complete

- Scaling the Prototype design to 45 nm gives 10μm - 15μm pixels.

- There is considerable scope to reduce the power from that of the first prototype

- We expect that the Chronopixel project will result in a detector that meets ILC specifications