Deep N-well 130nm CMOS MAPS for the ILC vertex detector

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ILC Vertex Detector Review

October 22 – 27, 2007 – Fermilab

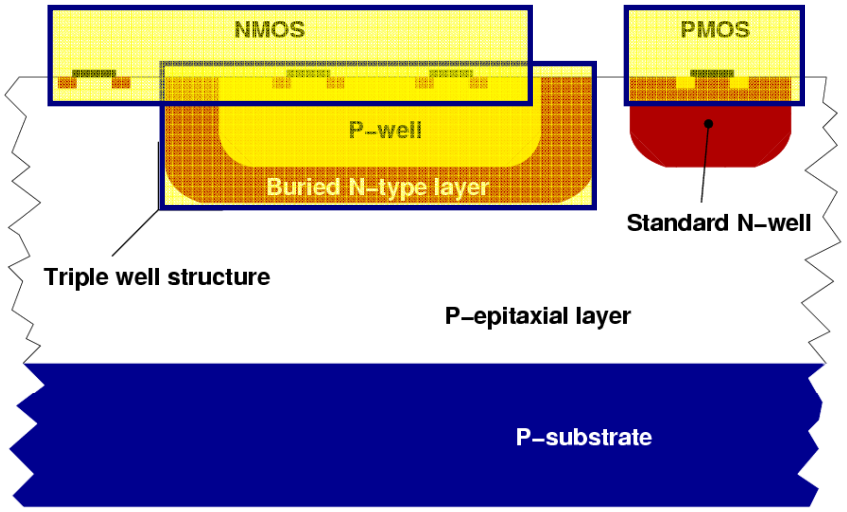
Outline

- Deep N-Well MAPS in 130nm CMOS technology and ILC Vertex Detector requirements
- Pixel analog signal processing
- Digital section and digital readout architecture with sparsification and time stamping
- Experimental results
- Workplan

Deep Nwell sensor concept

- Developed by the SLIM5 collaboration (INFN, Universities of Bergamo, Bologna, Pavia, Pisa, Trento, Trieste)

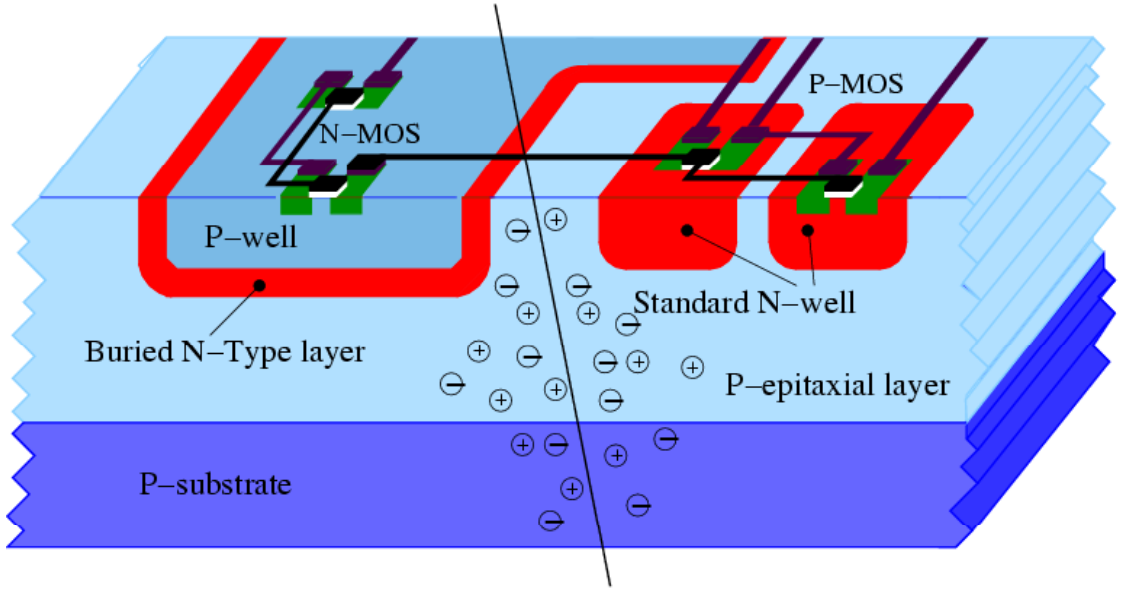
- In triple-well CMOS processes a deep n-well is used as a shielding frame against disturbancies from the substrate to provide N-channel MOSFETs with better insulation from digital noise



The new design features of our CMOS pixels:

- The deep n-well (DNW) can be used as the collecting electrode
- NMOSFETs can be integrated both in the epitaxial layer or in the nested p-well.
- PMOSFETs are integrated in standard n-wells
- A full signal processing circuit can be implemented at the pixel level overlaying the NMOS transistors on the collecting electrode

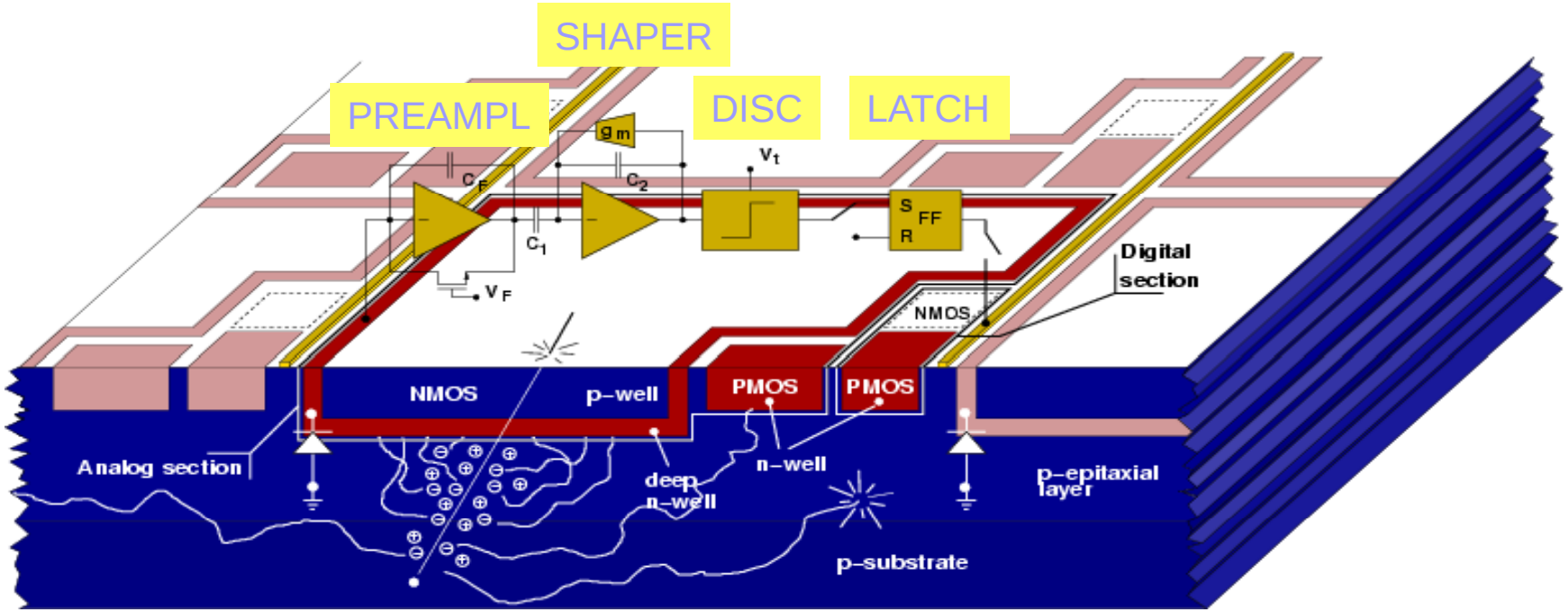
Deep Nwell sensor concept



- DNW MAPS is based on the same working principle as standard MAPS
- A DNW is used to collect the charge released in the epitaxial layer
- DNW may house NMOS transistors
- Using a large detector area, PMOS devices may be included in the front-end design → charge collection inefficiency depending on the ratio of the DNW area to the area of all the N-wells (deep and standard)

Deep Nwell sensor concept

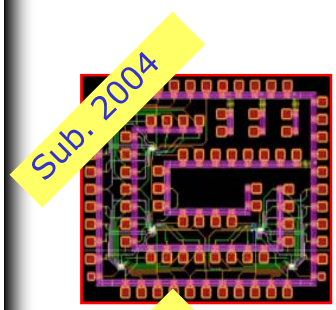
Classical optimum signal processing chain for capacitive detector can be implemented at pixel level:

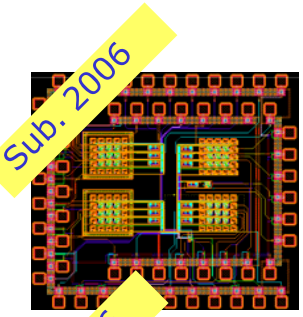


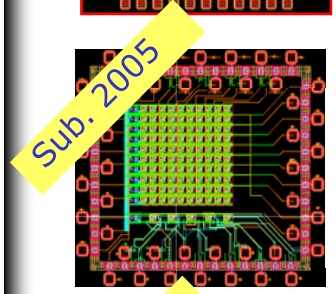
- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance)

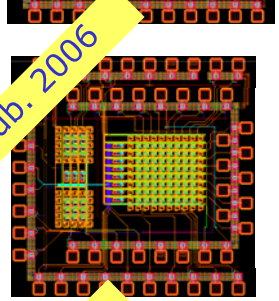
Technology: 130nm CMOS HCMOS9GP by STMicroelectronics

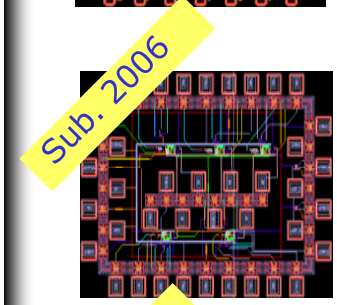
APSEL series chips

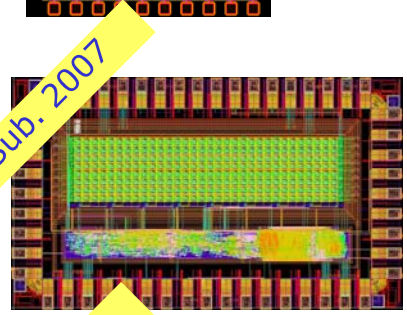


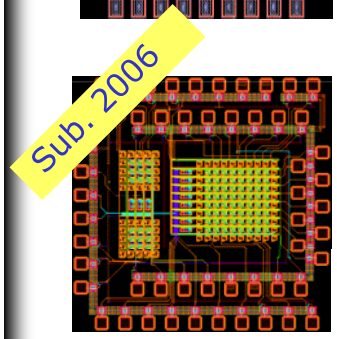


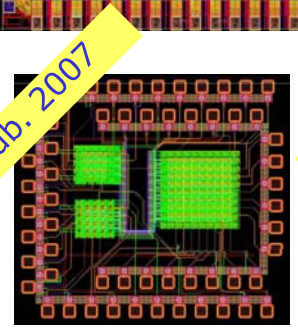


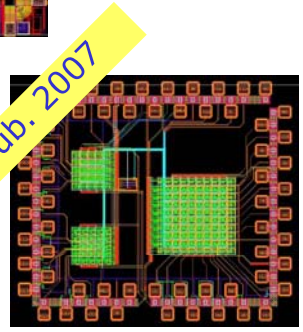








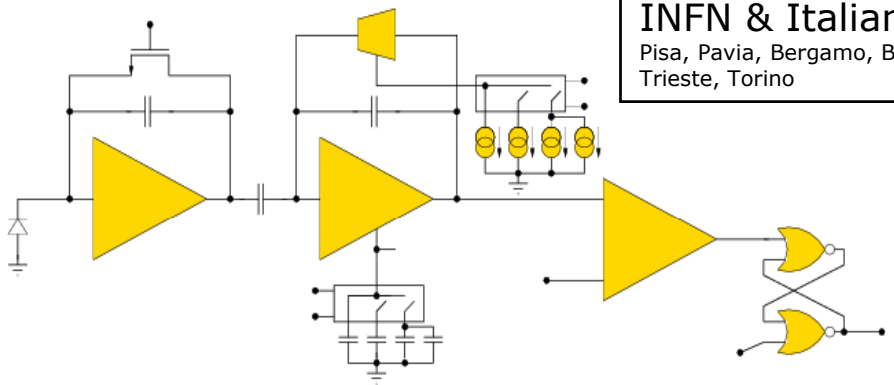




SLIM5 Collaboration:

INFN & Italian Universities

Pisa, Pavia, Bergamo, Bologna, Trento, Trieste, Torino



Full in-pixel signal processing:
PA + shaper + comparator + latch

Prototypes fabricated with the STMicroelectronics 130nm triple-well technology

High sensitivity charge preamplifier with continuous reset + RC-CR shaper with programmable peaking time

A threshold discriminator is used to drive a NOR latch featuring an external reset

Pixel size about 50μm x 50μm

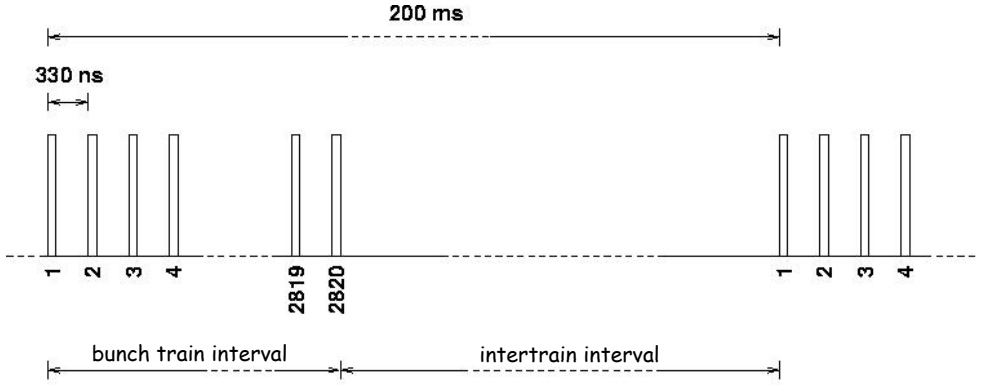
The first prototypes proved the capability of the sensor to collect charge from the epitaxial layer

130nm CMOS DNW MAPS for the ILC vertex detector

- INFN program (Milano, Pavia) started in 2006; design DNW MAPS according to ILC specifications
- Same concept as in the APSEL chips, but reduced pixel pitch and power dissipation
- Digital readout architecture with in-pixel sparsification logic and time stamping, taking into account the beam structure of ILC

Design specifications for the ILC vertex detector

- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a duty-cycle of 0.5%



  - assuming maximum hit occupancy 0.03 part./Xing/mm^2
  - if 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
  - if a digital readout is adopted 5μm resolution requires 17.3 μm pixel pitch
  - 15 μm pitch → $O_c \approx 0.056$ hits/train → 0.0016 probability of a pixel being hit at least twice in a bunch train period

- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

Sparsified readout architecture

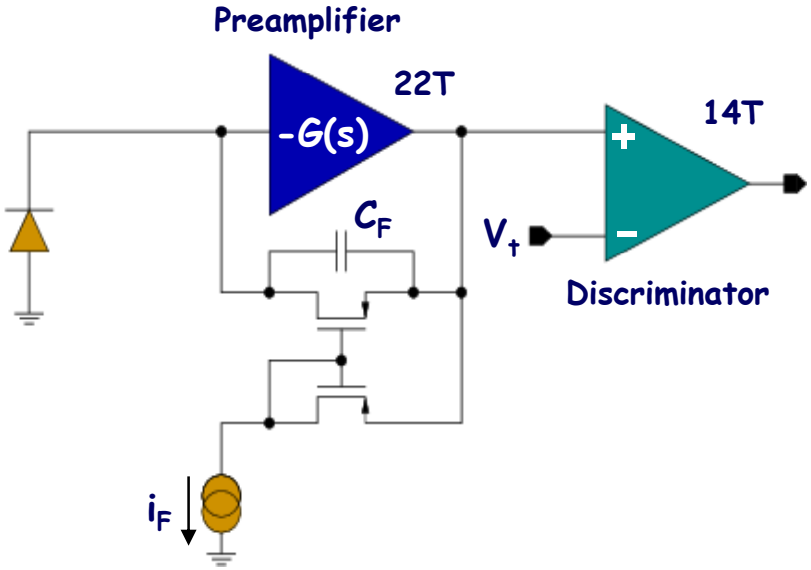
- In DNW MAPS sensors for ILC sparsification is based on a token passing readout scheme suggested by R. Yarema (FNAL)

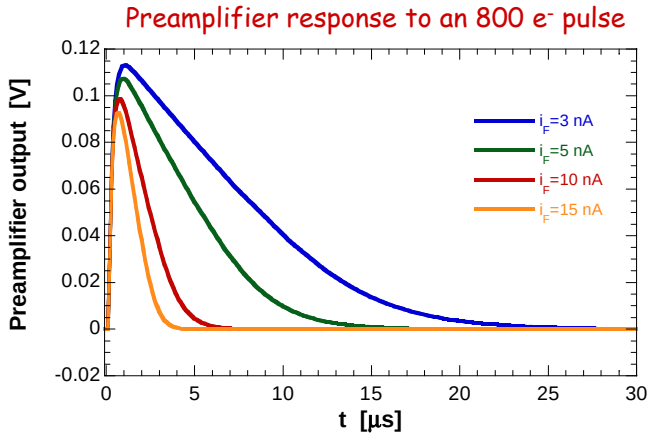
  (R. Yarema, "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", *ILC VTX Workshop at Ringberg*, May 2006)

- This architecture was first implemented by Fermilab ASIC designers Jim Hoff, Tom Zimmerman and Gregory Deptuch in the VIP1 chip (3-D MIT LL technology, see Fermilab presentation on Wednesday)

- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)

Pixel level processor





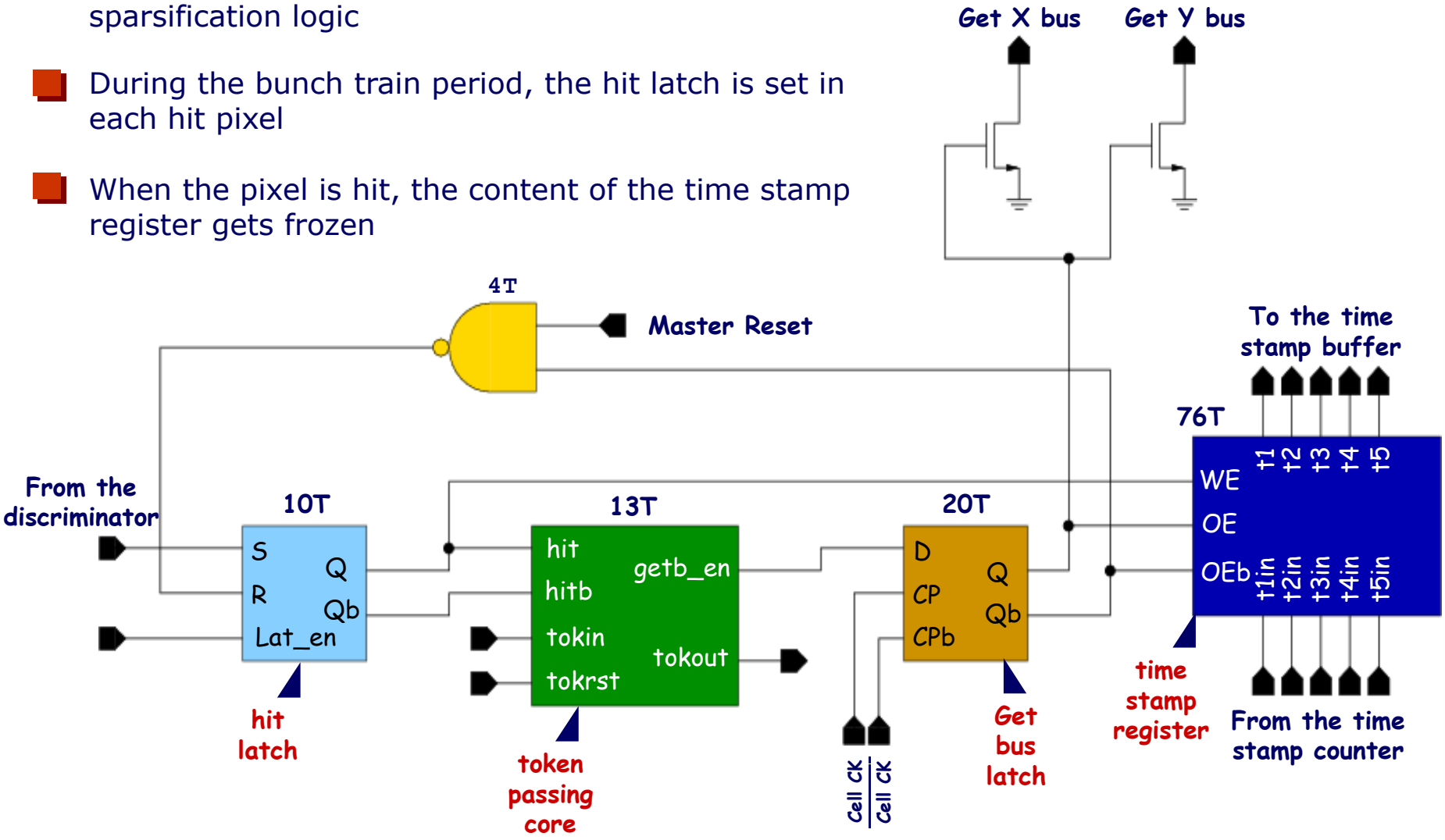
- C_F obtained from the source-drain capacitance
- High frequency noise contribution has been reduced limiting the PA bandwidth

From simulations:

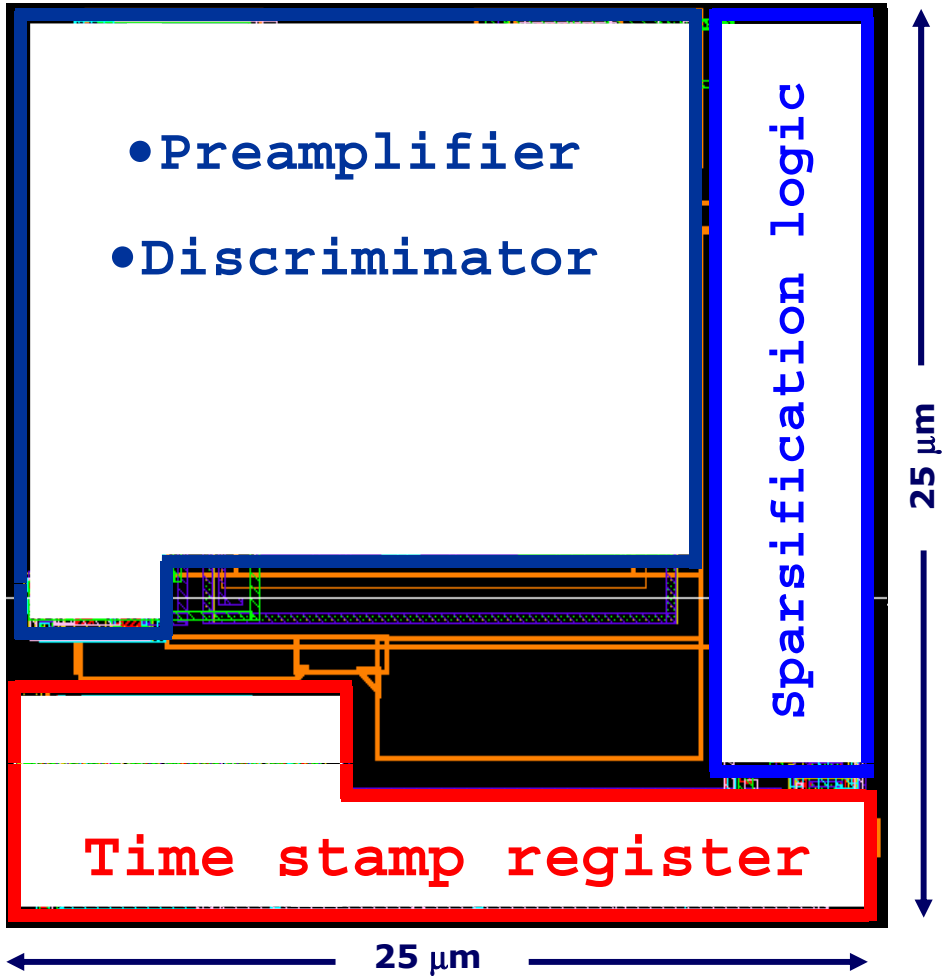
- ENC=**25 e⁻ rms@C_D=100 fF**
- Threshold dispersion ≈ **30 e⁻ rms**
- Power consumption ≈ **5 µW**
- Features power-down capabilities for power saving: the analog section cell can be switched off during the intertrain interval in order to save power (**1% duty-cycle** seems feasible)

Cell digital section

- Includes a 5 bit time stamp register and the data sparsification logic
- During the bunch train period, the hit latch is set in each hit pixel
- When the pixel is hit, the content of the time stamp register gets frozen

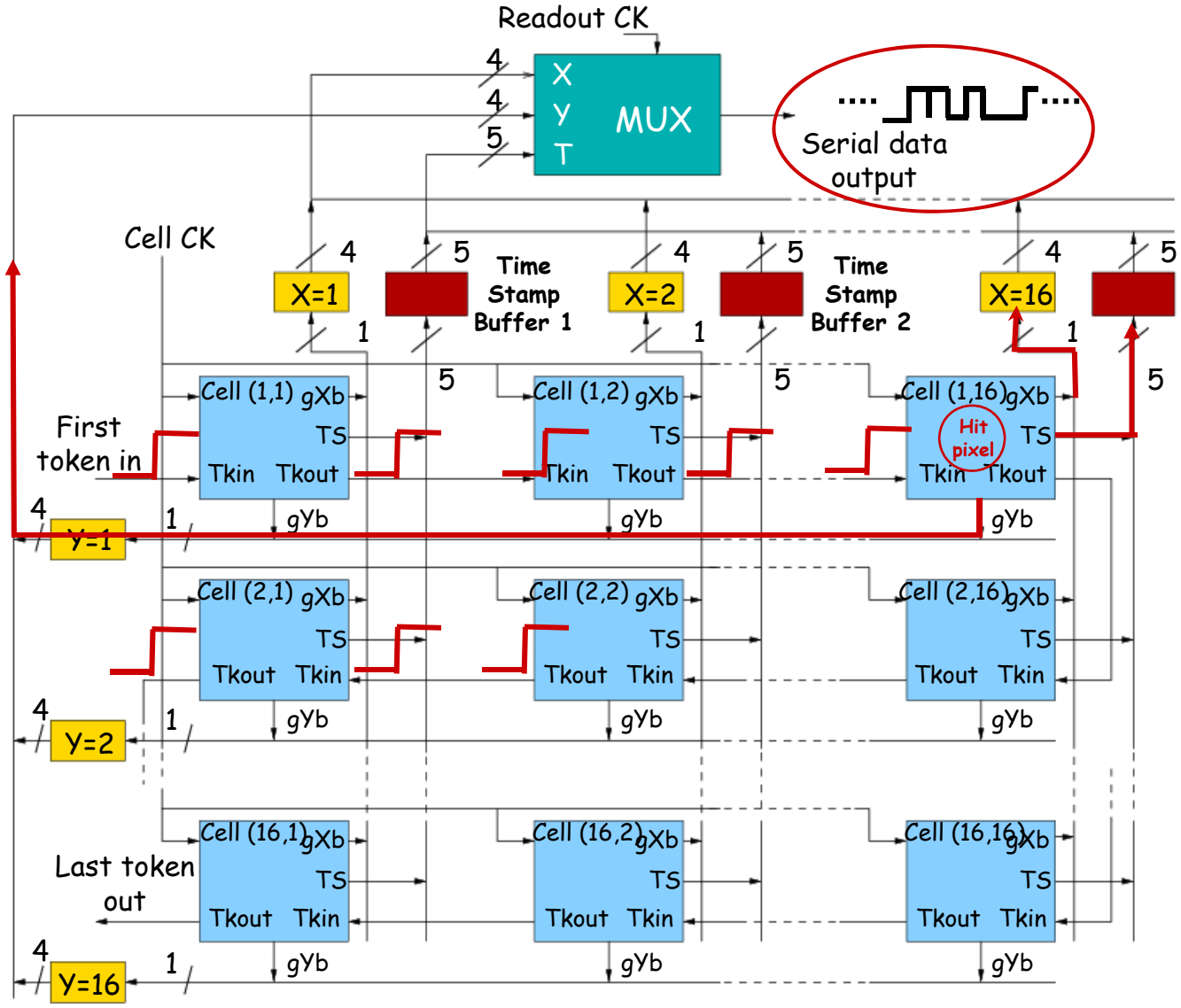


ILC DNW elementary cell



analog front-end
+
digital section
↓
164 transistors

Digital readout scheme



Readout phase:

- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

Power dissipation analysis

- Because low material budget is necessary, there is little room for cooling system ⟶ very low power operation
- Analog power: $P_{an,pix} \approx 5\mu W$/pixel (dissipated in the analog PA)
- Digital power: $P_{DC,pix} \approx 7$ nW/pixel (leakage currents of the digital blocks)

  $P_{dyn,pix} \approx 20$ nW/pixel (to charge the input capacitance of the time stamp register blocks during the detection phase)

  (power in the periphery neglected since it grows as the square root of the number of matrix cells)

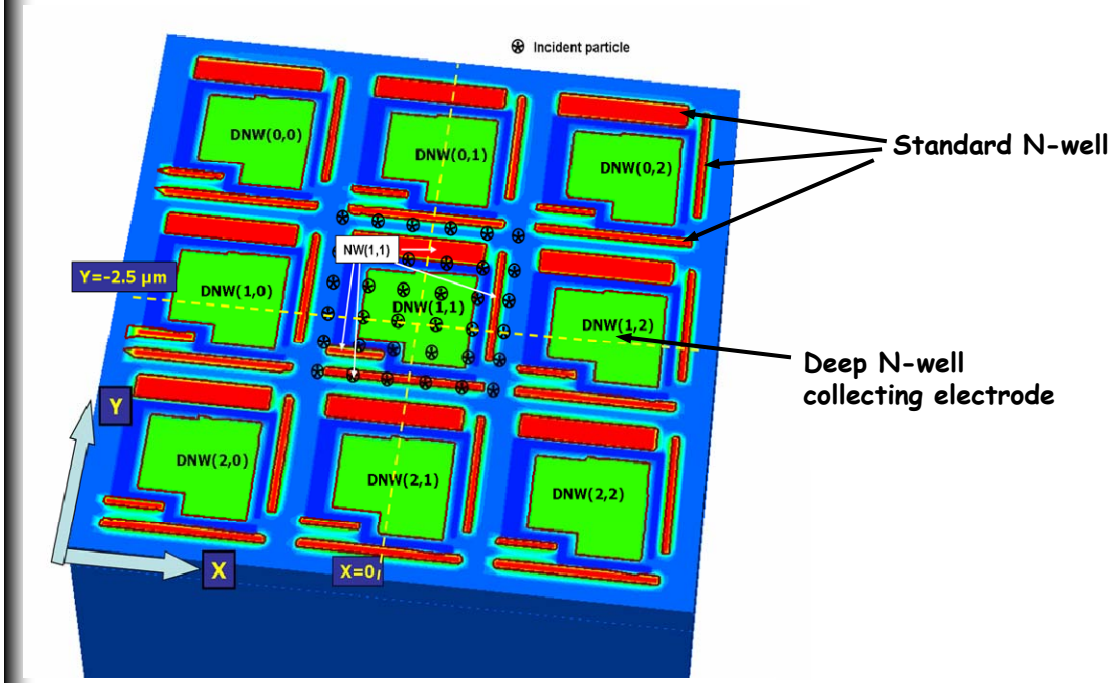
$$P_{tot} = P_{an,pix} \cdot N \cdot M \cdot \delta_P + P_{DC,pix} \cdot N \cdot M + P_{dyn,pix} \cdot N \cdot M \cdot \delta_P$$

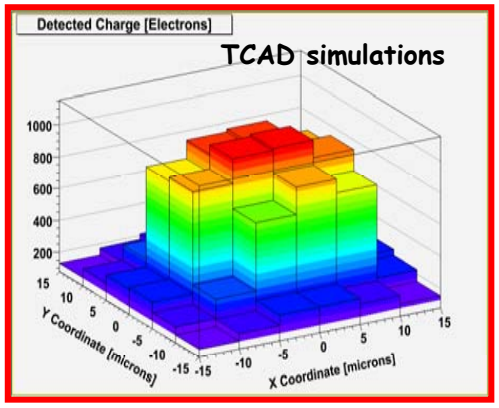
$\approx$ **15.5 W** | **13.6 W** | **1.9 W** | **0.05 W**

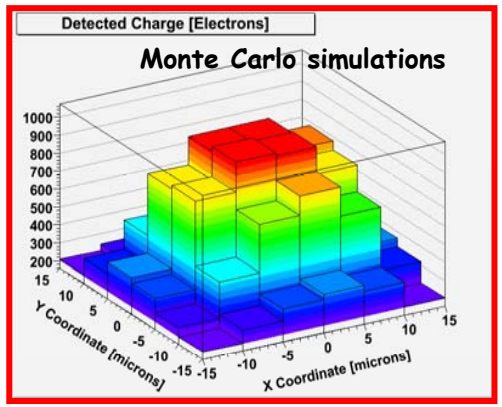
Assuming:
- 170000mm^2 total vertex detector area (pixel pitch of 25 μm);
- 1 Mpixel chips;
- δ_P=0.01 power supply duty cycle

N= number of cell per pixel
M= number of chips composing the detector

3D device simulations







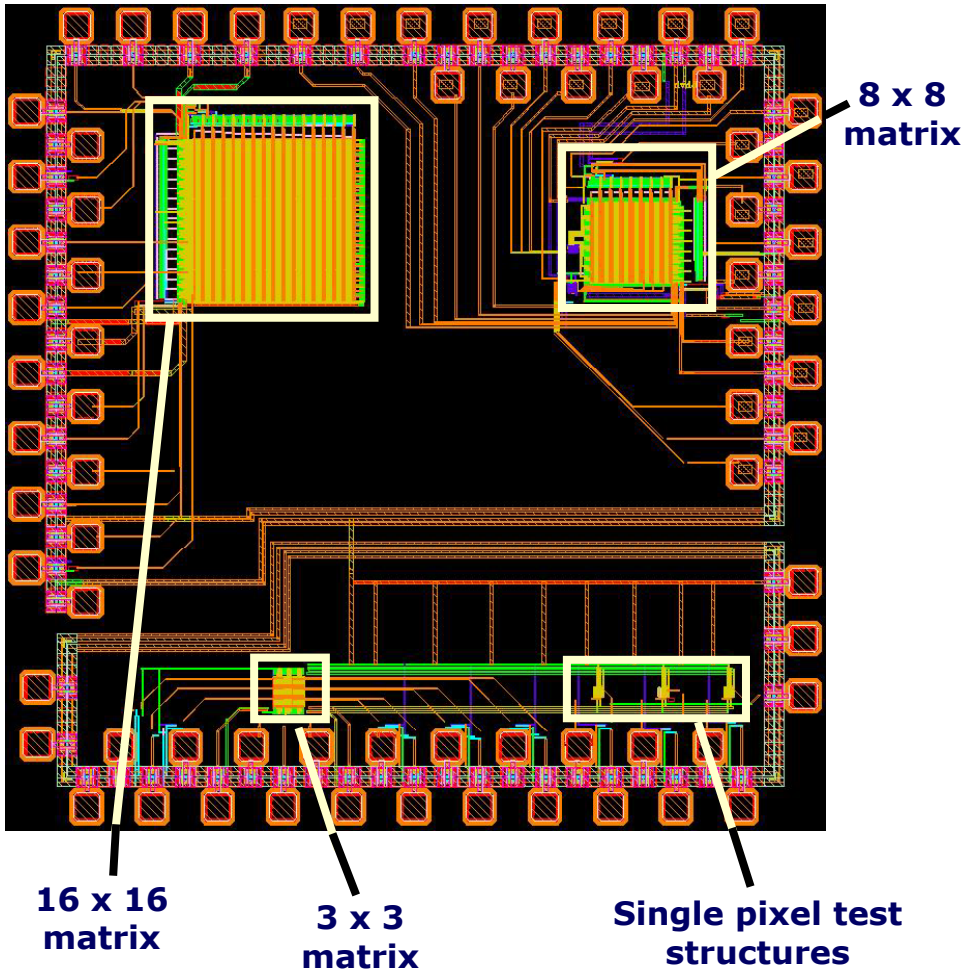
Charge collected by the central pixel in the 3×3 SDR0 matrix

Physical simulation performed by E. Pozzati - University of Pavia (Italy)

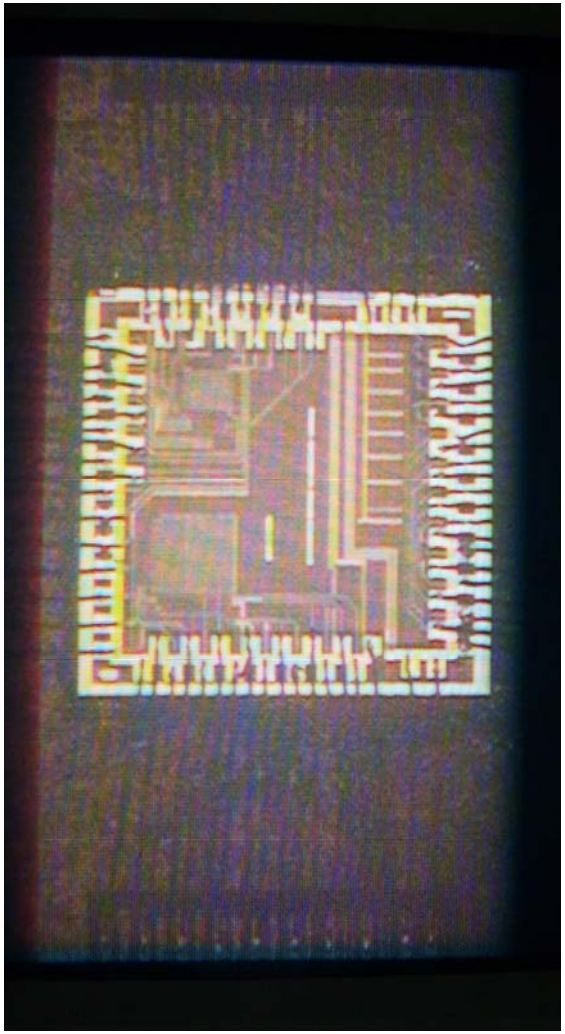
- The simulated structure (with TCAD) required a mesh with 165000 vertices. Because of the really long computation time only 36 simulations, each involving a different MIP collision point, have been performed
- MAPS operation is mainly diffusion driven → computing power required by TCAD may not be needed
- Monte Carlo code based on random walk developed (results of a collaboration with D. Christian – Fermilab)
- Activity presently focused on finely tuning a three-dimensional diffusion model for Monte Carlo simulations of MAPS by comparison with TCAD simulation results
- Advantage: dramatic reduction in computing time
- Next step: take advantage of fast Monte Carlo simulator to maximize detection efficiency through suitable layout choice

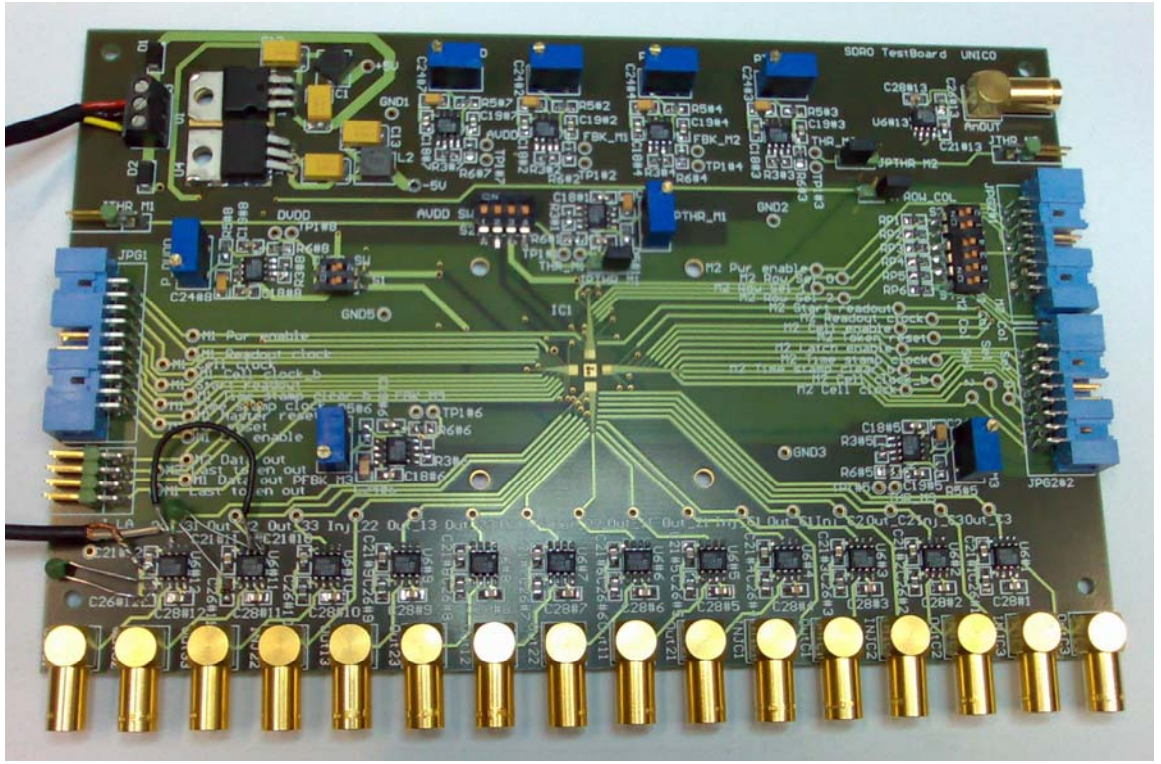
The demonstrator chip (SDR0)

- The chip includes:
  - a 16 by 16 MAPS matrix (25 μm pitch) with digital sparsified readout
  - an 8 by 8 MAPS matrix (25 μm pitch) with digital sparsified readout and selectable access to the output of the PA in each cell
  - a 3 by 3 MAPS matrix (25 μm pitch) with all of the PA output accessible at the same time
  - 3 standalone readout channels with different C_D (detector simulating capacitance)
- Delivered end of July 2007



SDRO chip and test board



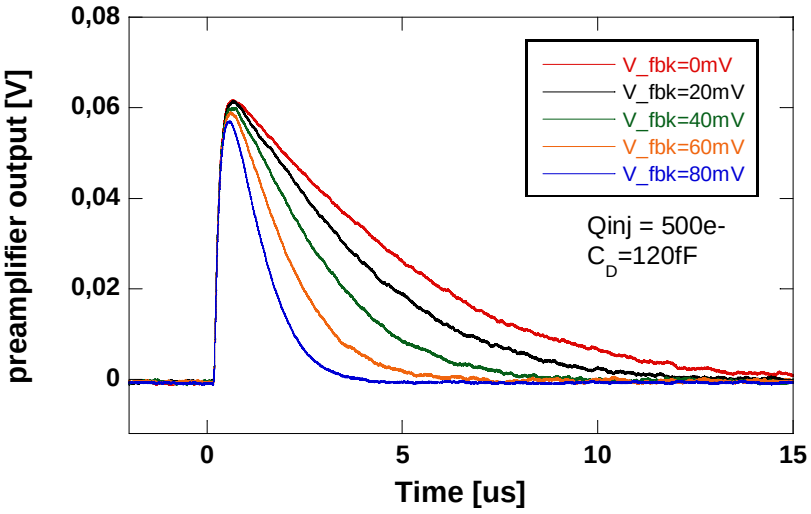


Test board designed by Marcin Jastrzab
University of Science and Technology, Cracow (Poland) and University of Insubria, Como (Italy)

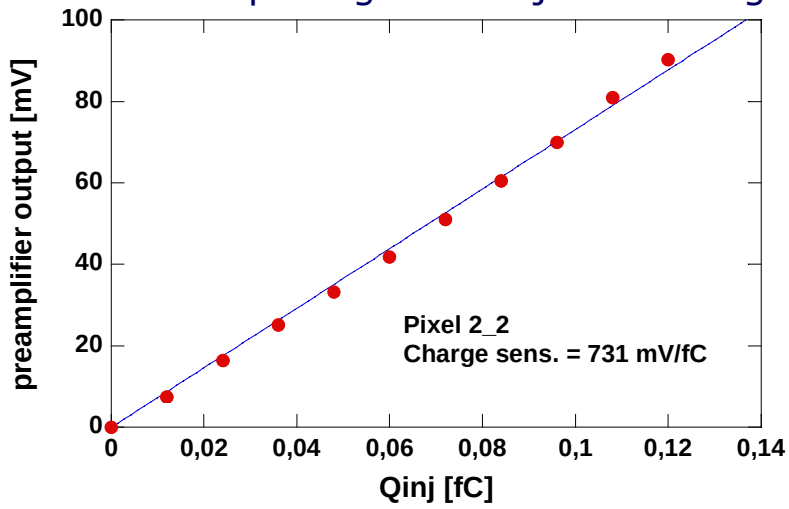
Credit: Fabio Risigo University of Insubria, Como (Italy)

SDRO experimental results

Preamplifier response
to an external calibration signal



Pixel output signal vs injected charge



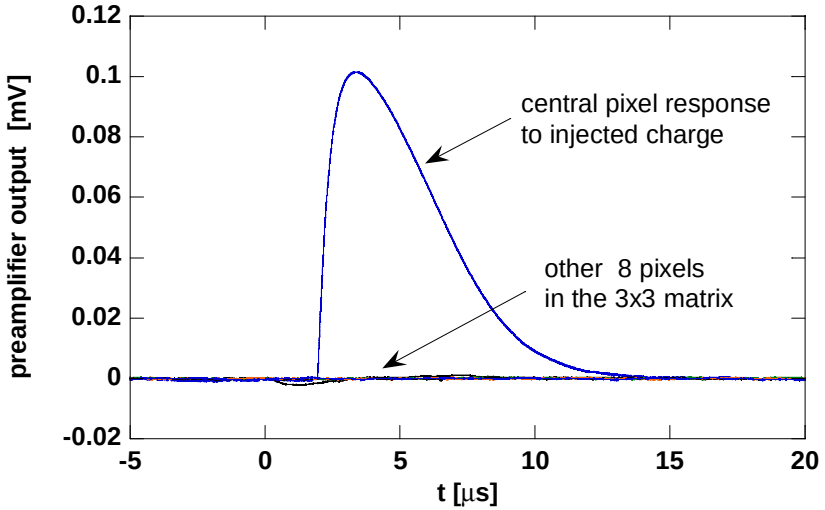
- Tests on the analog section with injection of external calibration signals and with an infrared laser scan (single channels, 3x3 pixel matrix)

Preliminary results:

- Average **charge sensitivity ≈ 0.7 V/fC**
- ENC = **40 e rms @ C_D=120 fF**

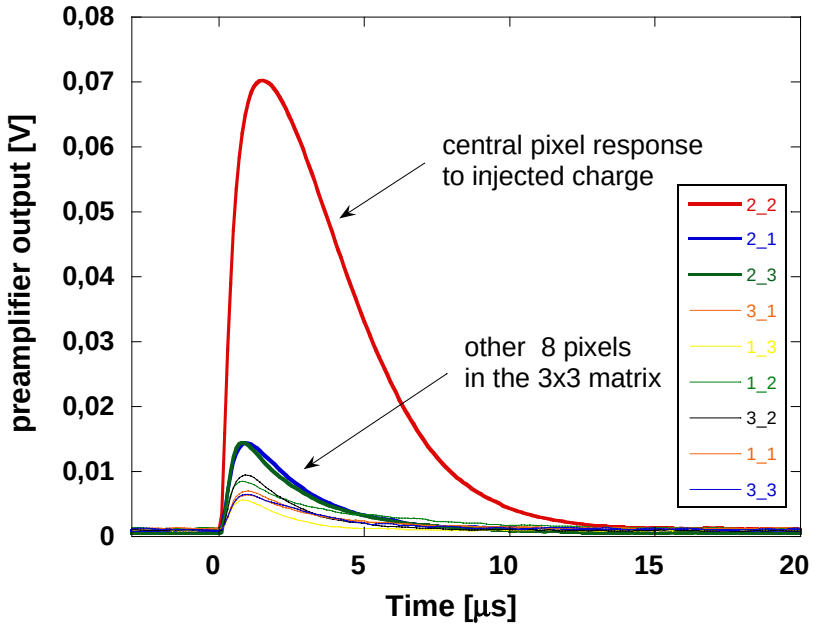
  (preamplifier input device: I_D = 1 μA, W/L = 22/0.25)

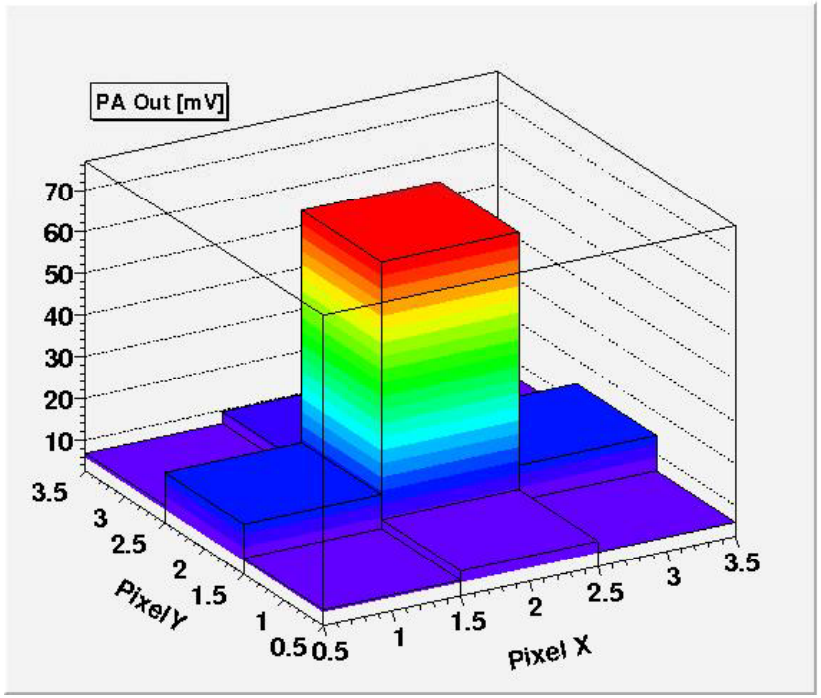
No crosstalk between pixels,
no correlated noise



SDR0 experimental results

3x3 matrix response to infrared laser





- Plans for the next few weeks:

  Absolute calibration with a ^{55}Fe source

  Tests of the 16x16 matrix with digital readout

Performance of DNW MAPS and ILC specifications

Sensor thinning

DNW 130nm CMOS MAPS may take advantage from chip and wafer thinning technologies which are being developed by the microelectronic industry, as for other MAPS R&D activities.

Pixel pitch

SDR0 prototype: pixel pitch = 25 μm.
Binary readout: ILC VTX demands a pixel pitch < 20 μm.

→ Optimization of the pixel cell layout planned in the next prototypes. Possible design changes: in-pixel digital time stamp register replaced by an analog time stamp measurement (sampling and holding the value of analog ramp voltage until its converted by an off-pixel ADC).

The reduction of the pixel pitch may be also achieved by using a more scaled technology, such as 90 nm CMOS. Test structures have already been fabricated in this process.

Performance of DNW MAPS and ILC specifications

Detection Efficiency

SDR0 readout architecture: compatible with foreseen hit rate if pixel pitch is reduced below 20 μm.
TCAD simulations and experimental charge collection data gathered on SLIM5 structures (same 130nm process): the pixel detection efficiency may approach ILC requirements if the layout of the collecting electrode is optimized.
The option of a deep P-well shielding regular N-wells will be explored.

Radiation hardness

According to tests on performed on SLIM5 devices, DNW 130nm CMOS MAPS appear to be radiation tolerant to the ionizing radiation levels (< 1 Mrad) foreseen in ILC. Optimization of the sensor layout and of the preamplifier can lead to a further improvement of ionizing radiation hardness.

Power dissipation and cooling

The power dissipated by the analog and digital sections is already complying with ILC requirements in the present SDR0 version. This requires an experimental verification of the sensor operation in power cycling mode, which appears feasible from simulations.
An actual cooling system for a DNW MAPS module in 2009 may also take advantage from similar developments in other MAPS R&D activities.

Workplan

Year	Sensor design and fabrication	Experimental results	Personnel and funding for Italian groups involved in R&D for ILC Vertex Detector (manpower/equipment = FTEs/k$)	
			Italian	EUDET
2004	Design and submission of test structures with deep N-well pixels and associated electronics in 130 nm CMOS (SLIM5)		4/50	
2005	Submission of the first prototype MAPS matrix in 130 nm CMOS (SLIM5)	Electrical and radiation source tests of first test structures (SLIM5)	4/50	
2006	Submission of a 16x16 MAPS prototype (SDR0) aimed at proving feasibility of 130 nm CMOS MAPS for ILC VTX	Complete test of SLIM5 130 nm CMOS matrix (charge collection, noise, threshold dispersion)	7/60	3.5/50

Workplan

Year	Experimental results	Plans	Personnel and funding for Italian groups involved in R&D for ILC Vertex Detector (manpower/equipment = FTEs/k$)	
			Italian	EUDET
2007	Tests of the SDR0 prototype (under way)	Optimization of the design of the pixel cell and of the readout circuits	7/30	3.5/35
2008		Submission of a 256x256 matrix (SDR1); beam test with EUDET facilities	8/150	3.5/50
2009		Design of a detector module with SDR1 or with an upgraded version; mechanical and cooling studies	Pending INFN approval	2/32

Conclusions

- INFN R&D program aims at developing 130nm CMOS MAPS with sparsified readout and time stamping for the ILC vertex detector
- DNW MAPS structures have been fabricated in a 130 nm, triple well CMOS technology; preliminary tests are encouraging
- Several issues have to be addressed to meet ILC specifications (pixel pitch, detection efficiency)
- Plans for the future:
  - design of a 256 x 256 matrix for beam test (2008)
  - evaluation of more scaled technologies (90 nm CMOS)

Acknowledgments

I want to thank the ILC pixel R&D group at Fermilab for the very useful discussions that helped us to choose the SDR0 chip architecture.

Backup slides

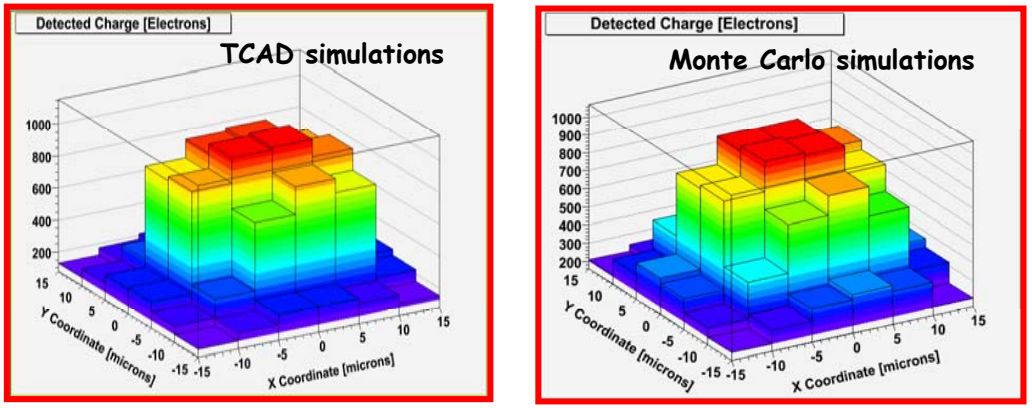
Design specifications for the ILC vertex detector

SDR0 prototype

Hit rate [particles/bco/mm^2]	Detector pitch [μm]					
	5	10	15	20	25	30
0.03	99.99%	99.97%	99.84%	99.52%	98.87%	97.76%
0.06	99.99%	99.87%	99.39%	98.20%	95.91%	92.26%
0.09	99.98%	99.72%	98.69%	96.20%	91.70%	84.93%
0.12	99.97%	99.52%	97.76%	93.68%	86.66%	76.75%
0.15	99.95%	99.26%	96.62%	90.75%	81.13%	68.36%

Detection efficiency for different sensor pitch and hit rate values

3D device simulations



Charge collected by the central pixel in the 3×3 SDR0 matrix
Physical simulation performed by E. Pozzati - University of Pavia (Italy)

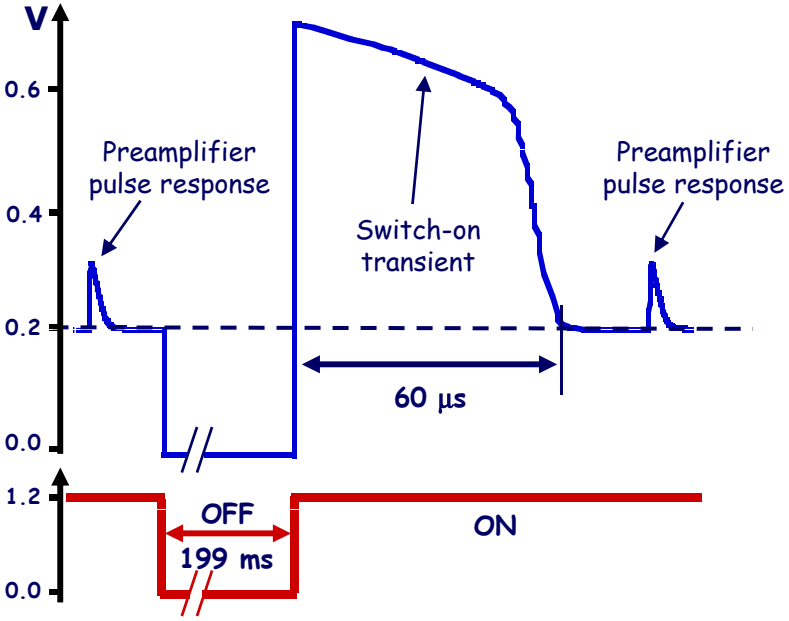
Simulations with Monte Carlo code have been performed with the following assumption:

- 80 e-h/μm are generated uniformly along a linear track which is normal to the device surface and feature a gaussian distribution in the plane normal to the track itself (σ=0.5 μm).
- The SDR0 simulation volume is 85x85x80 μm^3.
- Electron lifetime, according to the Scharfetter model is about 9.2 μs at the considered doping levels (10^{15} cm^{-3}) and sets a limit to the random walk duration for each carrier.

▪E. Pozzati, M. Manghisoni, L. Ratti, V. Re, V. Speziali, G. Traversi: "*MAPS in 130nm triple-well CMOS technology for HEP applications*" Topical Workshop on Electronics for Particle Physics, TWEPP 2007, Sept. 3-5, Prague, Czech Republic

Power cycling simulations

- Power cycling can be used to reduce average dissipated power by switching the chip off when no events are expected
- Example:
  - ✓ILC bunch structure: ~330 ns spacing, ~3000 bunches, 5Hz pulse
- The analog section in the elementary cell can be switched off during the intertrain interval in order to save power (analog power is supposed to be predominant over digital)



- Based on circuit simulations, power cycling with at least **1% duty-cycle** seems feasible