DEPFET Devices

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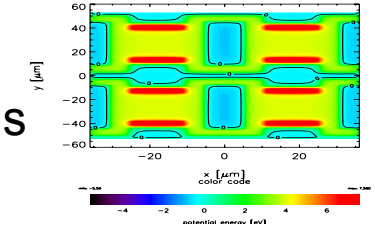
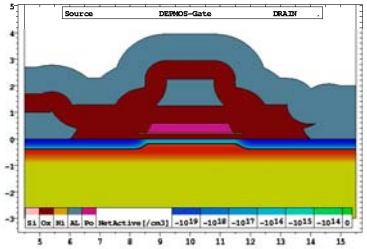
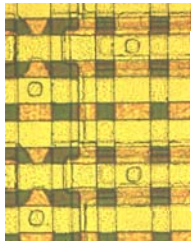
for the DEPFET Collaboration
(www.depfet.org)

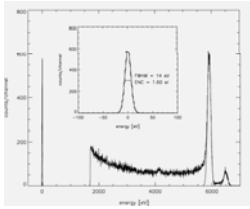
Outline

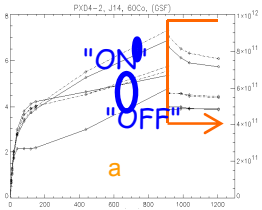
- Design and Simulations
- Technology
- DEPFET Production
- Single Pixel Results
- Radiation Tolerance
- Ladder Concept & Thinning
- New Production

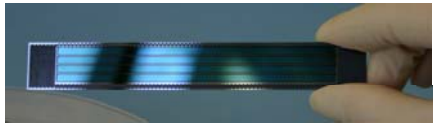


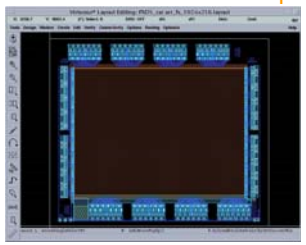




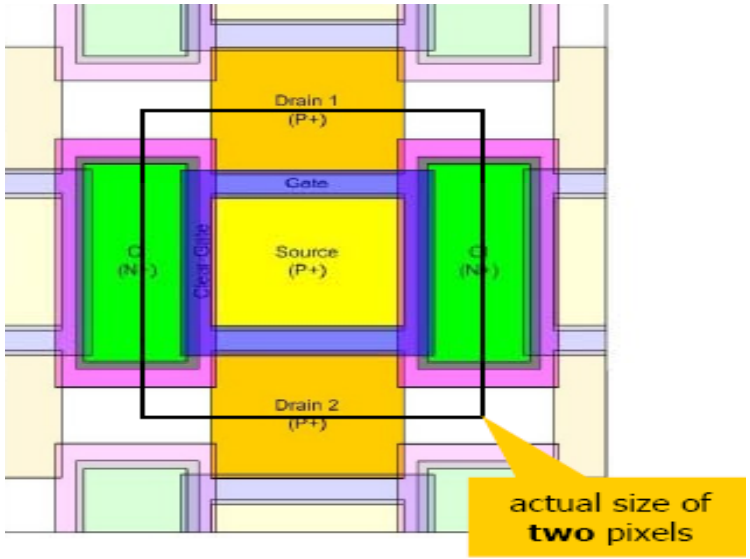


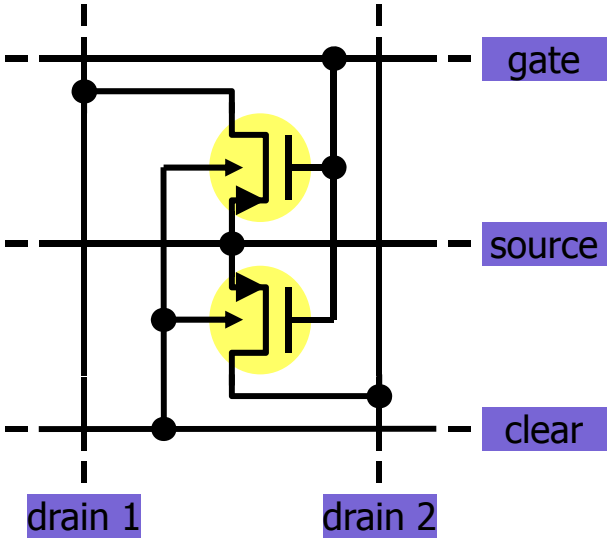






Design: Double Pixel





Compact layout: sharing of source, gate, and clear, less metal lines, more equally distributed in x and y

=> smaller pixel size possible

Simultaneous readout of two lines:

=> doubles readout speed (needs more readout channels, however)

Device Simulation

Charge -> current conversion factor (g_q) as function of gate length

$$g_q = \frac{-\mu}{L^2}(V_{GS} - V_{th})$$

Confirmed by measurements

For L_{eff} = 4 µm (actual devices)

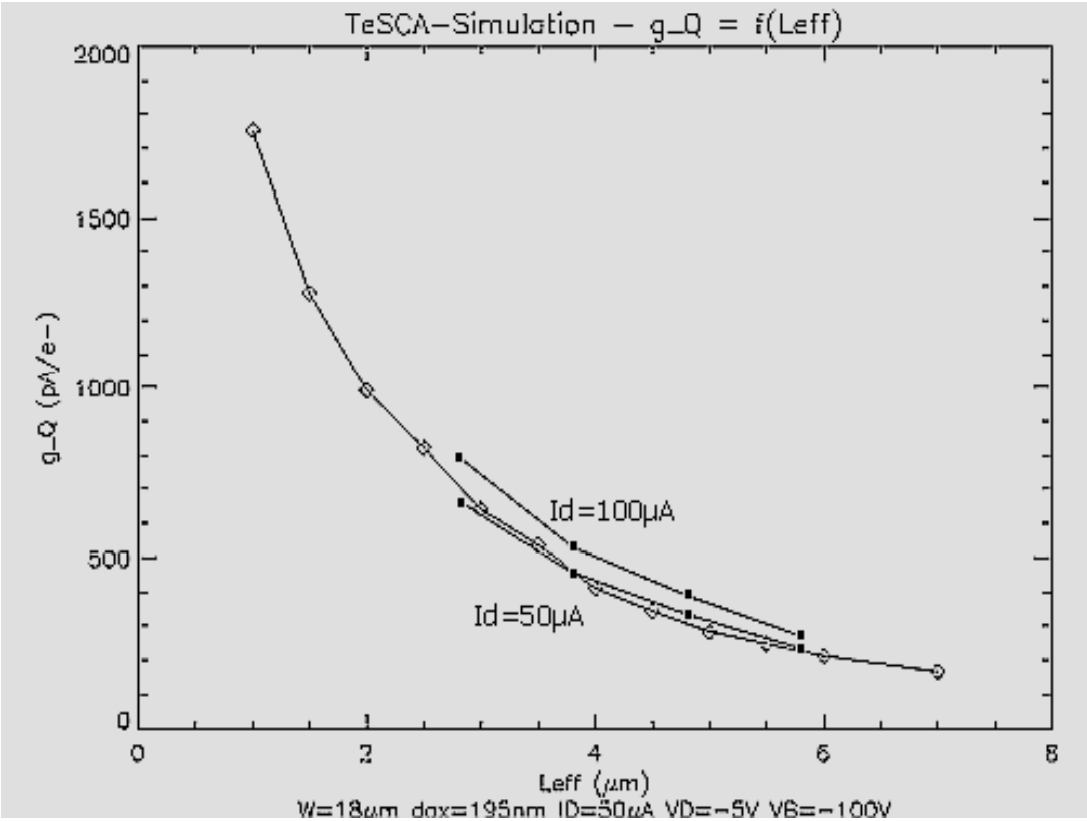
g_q = 500 pA/e

With reduced gate length:

g_q > 1nA/e possible

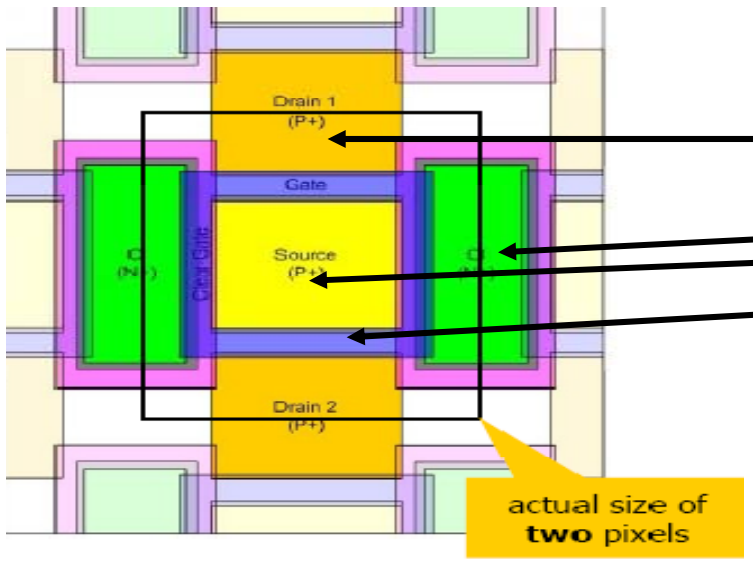
Larger g_q improves S/N

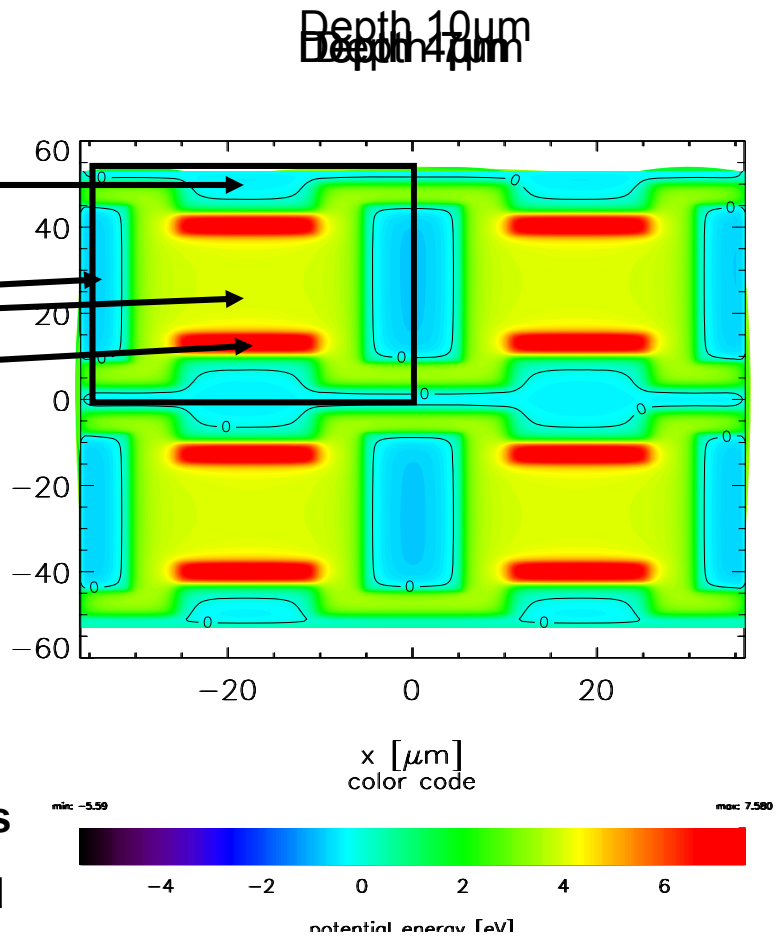
Less sensitive to external noise sources



Device Simulation

Potential in a DEPFET array in accumulation mode

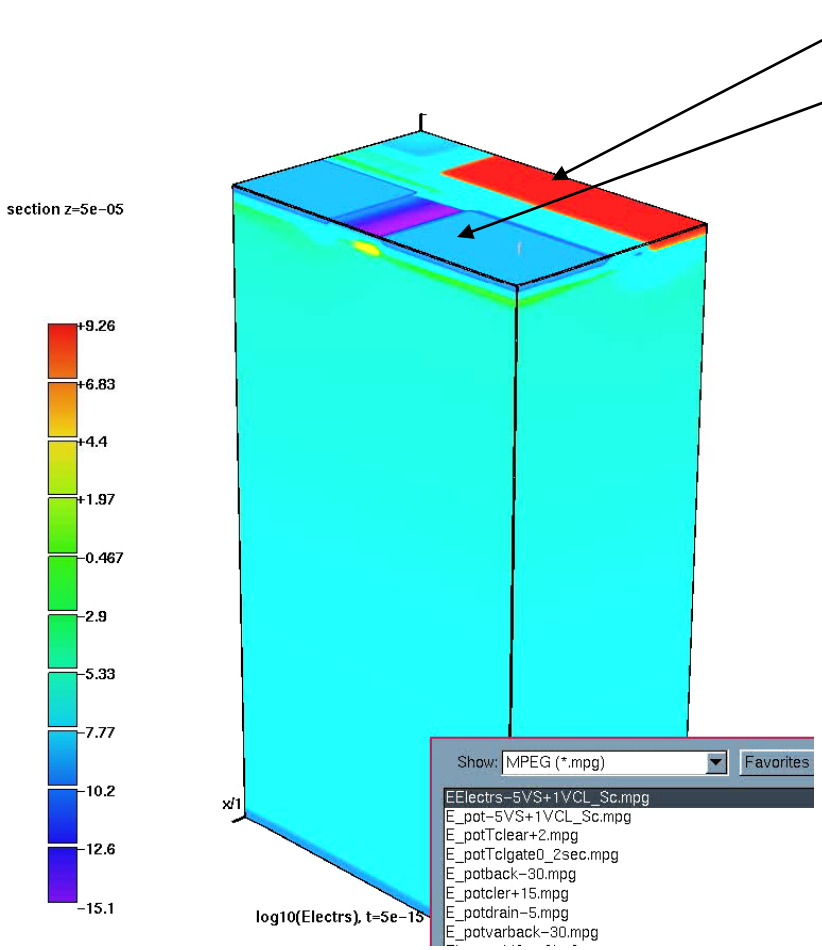




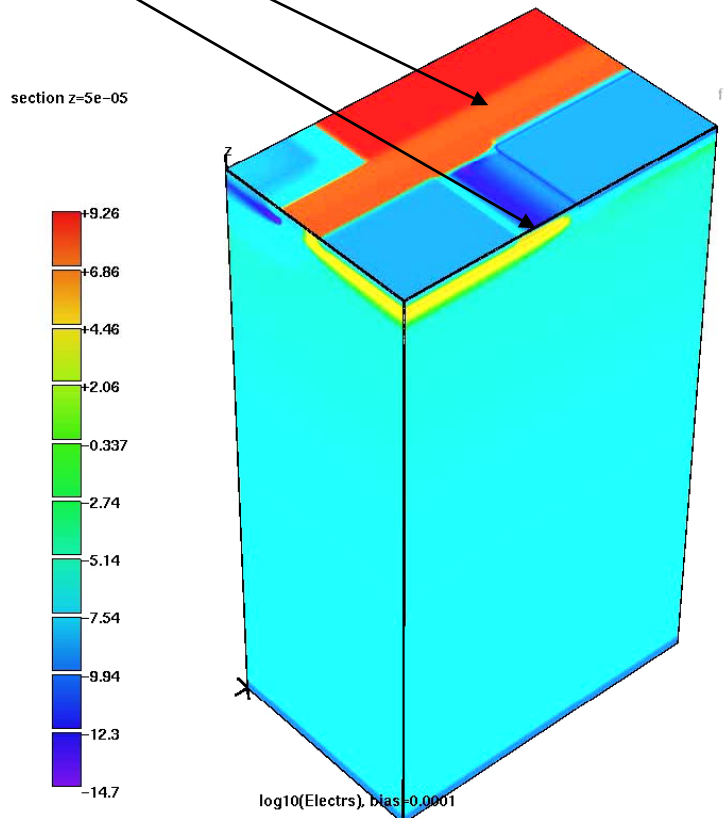
Well defined potential minima under FET gates

=> Good charge collection efficiency expected

Device Simulation: Charge collection and clear



Charge collection



Clear mechanism

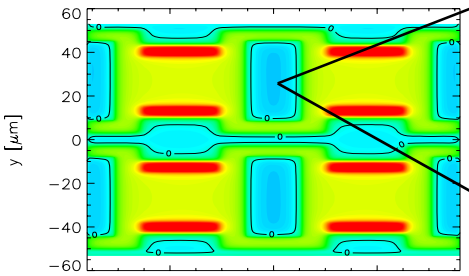
Simulation: Collection time and charge losses

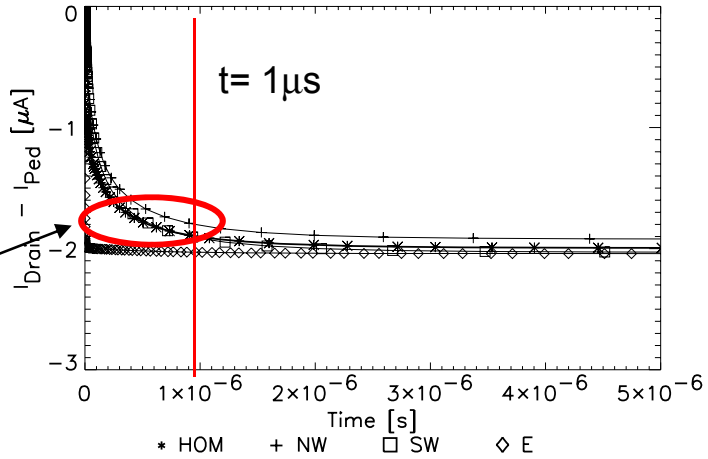
Charge collection usually fast (~ ns for 45 µm)

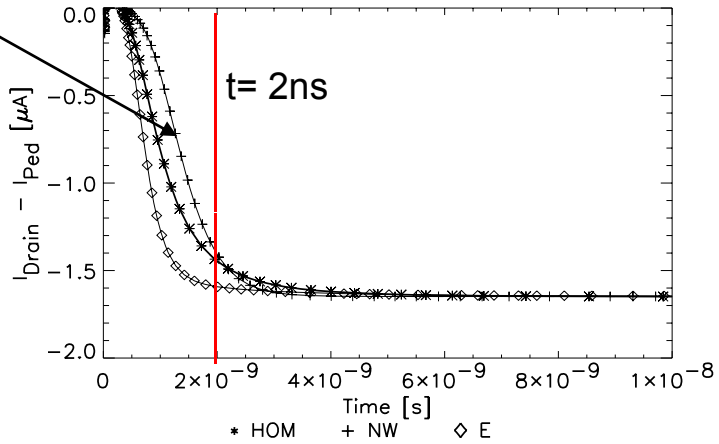
Except: interface at clear region (low lateral field)

Long collection times (~µs)

Losses due to trapping likely







Remedy: HE (deep) n-implant:

-> charge kept away from interface

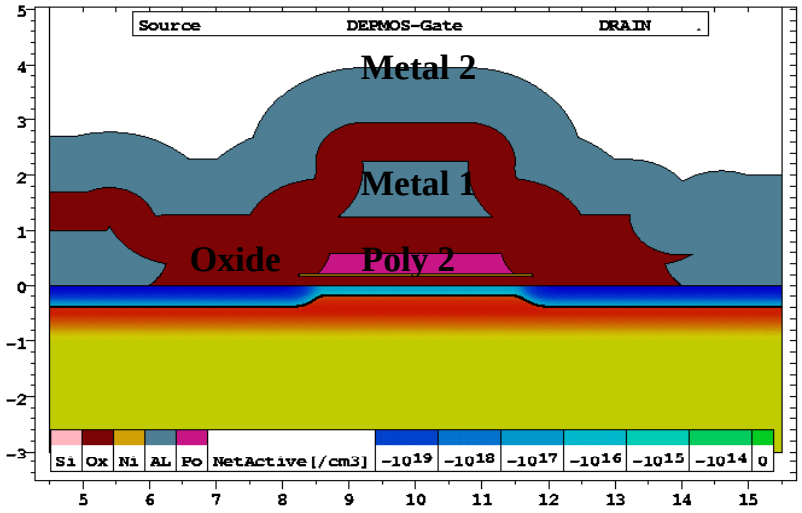
Introduction of lateral drift fields

-> fast charge collection also under clear

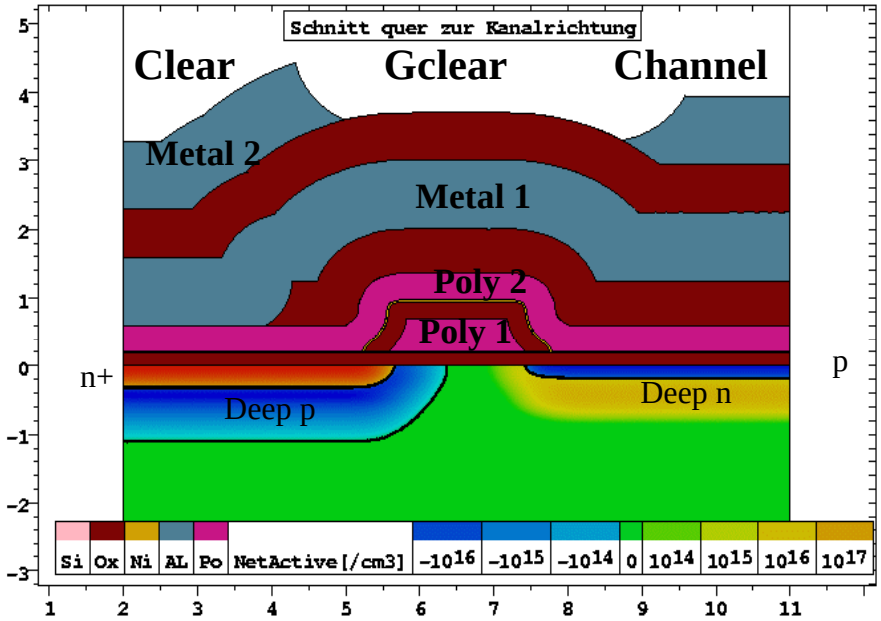
No significant charge losses expected

DEPMOS Technology at the MPI Semiconductor Laboratory

Double Poly / Double Al Technology
on high ohmic 150mm substrate



along the channel



perpendicular to the channel
(Clear region)

Double metal necessary for matrix operation
Self-aligned implantations with respect to polysilicon electrodes =>
Reproducible potential distributions over large matrix areas
Low leakage current level: < 200pA/cm² (fully depleted – 450µm)

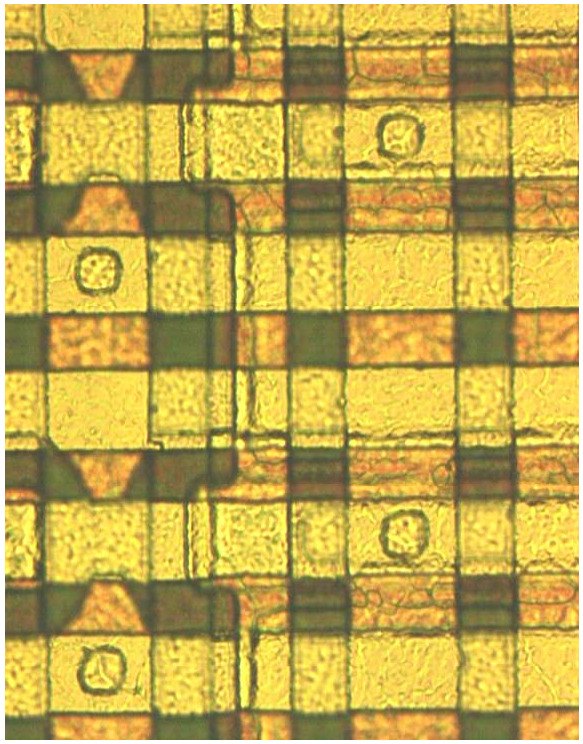
PXD4 Production: 1st Iteration of DEPFET Matrices

Production in the MPI semiconductor laboratory

Various test structures & single pixels

Test-Matrices (amongst others):

Array	area	Pixel Size	Clear
64 x 128	7x7 mm^2	33x24 μm^2	common gate
64 x 128	7x7 mm^2	36x22 μm^2	common gate
64 x 128	7x7 mm^2	36x29 μm^2	pulsed gate



Clear mechanisms:

Clear gate: potential barrier between gate and clear contact:

Pulsed: can be lowered during clear: lower clear voltages

Common: fixed potential, simpler layout (smaller pixels)

HE implant: internal gate deeper in bulk:

-> lower clear voltages (better clear performance)

-> lower amplification

Single Pixel Tests

Tests of basic DEPFET parameters

- gain (g_q)
- clear efficiency
- intrinsic noise
- radiation hardness

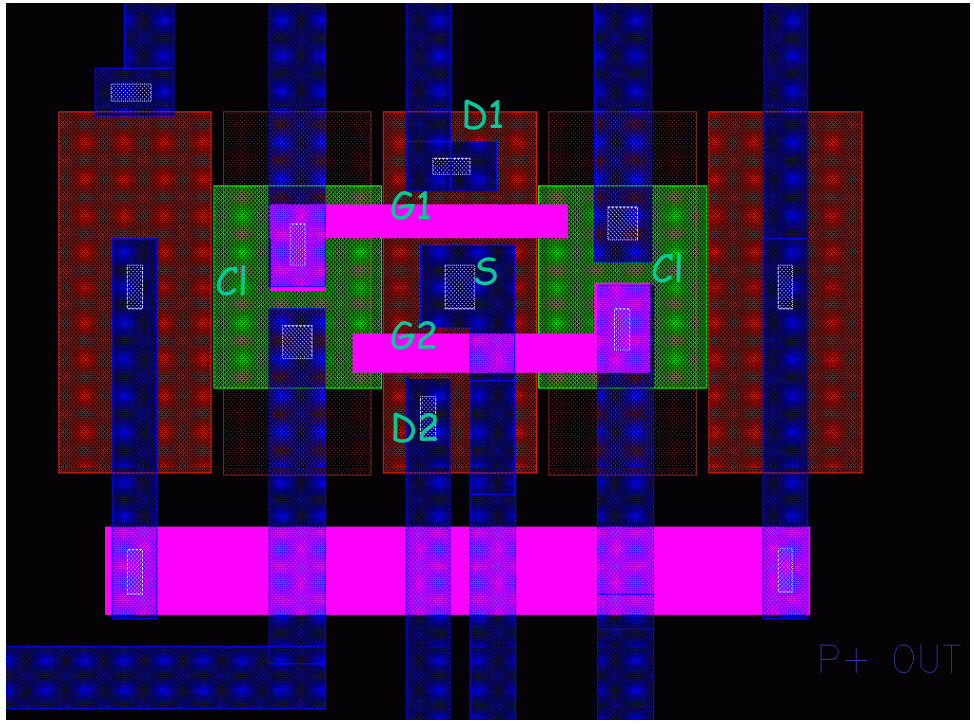
Single "double" pixel

S: source (common)

D1, D2: drain

G1, G2: gate

C1, C2: clear contacts



Single Pixel Test: g_q (charge -> current conversion)

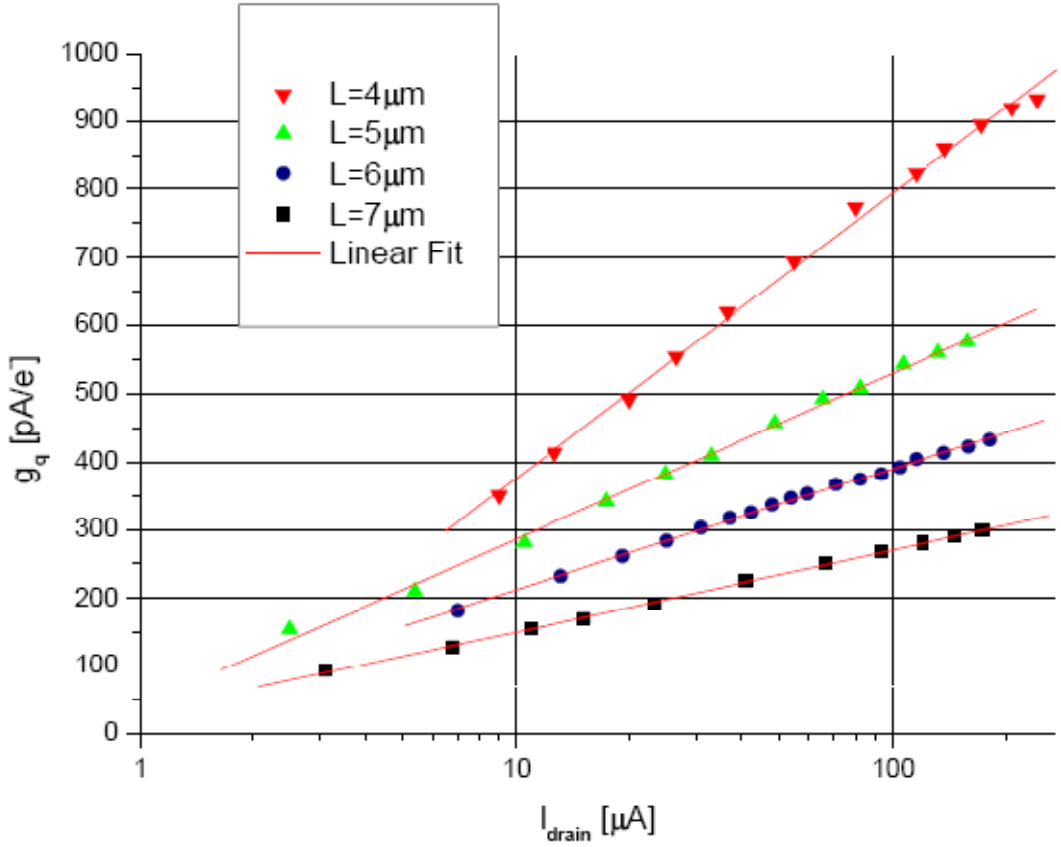
$$g_q = \frac{-\mu}{L^2}(V_{GS} - V_{th})$$

$$= f(I_d)\frac{1}{L^2}$$

Expected dependence of g_q on gate length confirmed

Future: reduce gate length to increase gain to ~ 1 nA/e

(L: design parameter, L_{eff} smaller due to underetching)



Single Pixel Tests: Clear Efficiency

Complete clear:

-> necessary for low noise operation

Incomplete clear -> some charge remains

Fluctuations of left over charge -> reset noise

Noise as function of clear parameters

-> Complete clear in large parameter space

Fast clear:

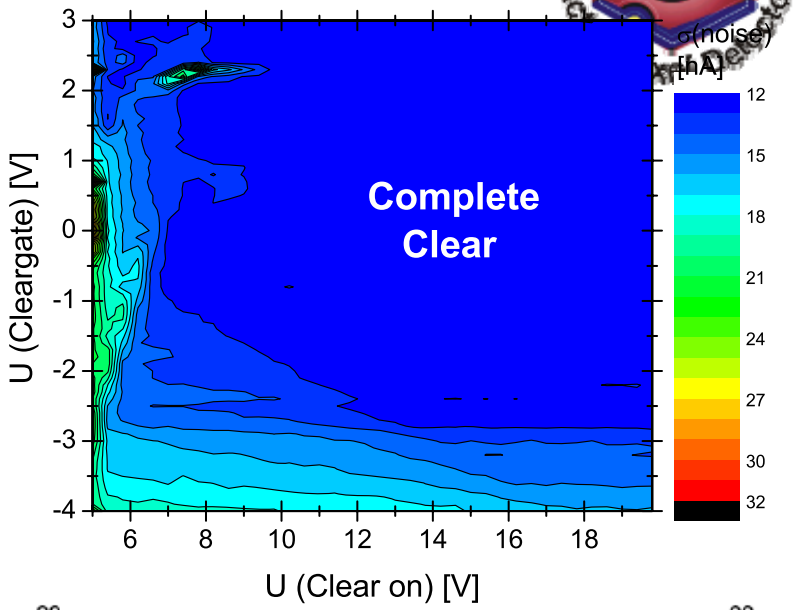
-> necessary for high speed operation

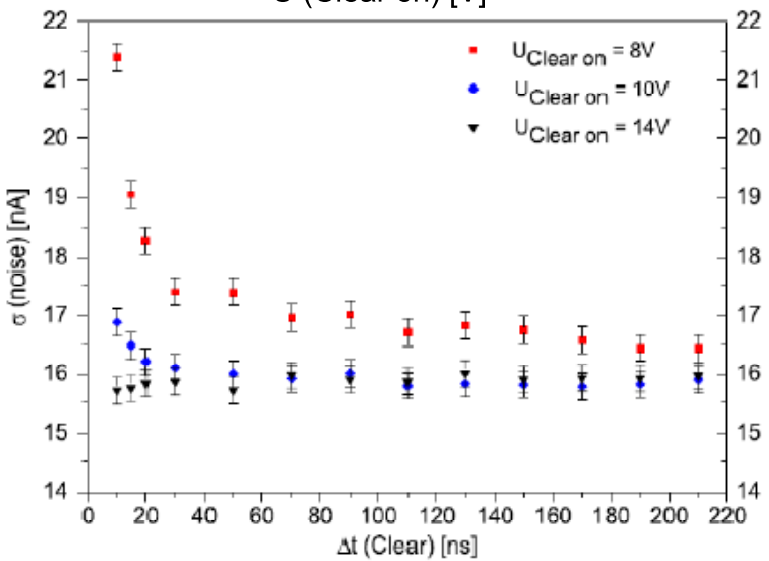
Complete clear achievable in < 10 ns

Present clear voltages rather high (>10V)

Design goal: lower clear voltages

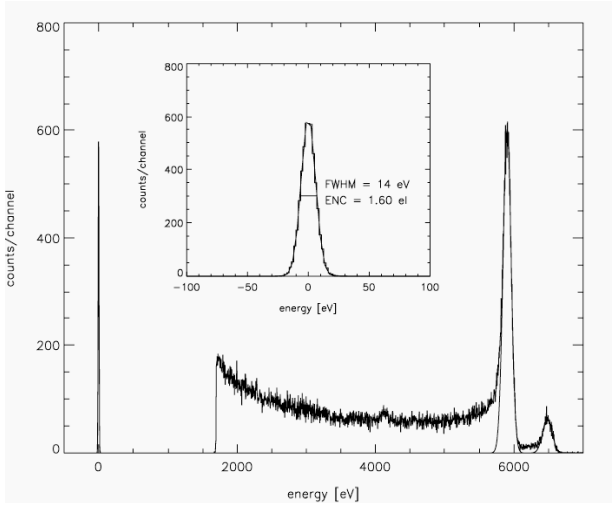
(U > 10V not compatible with rad. hard CMOS)



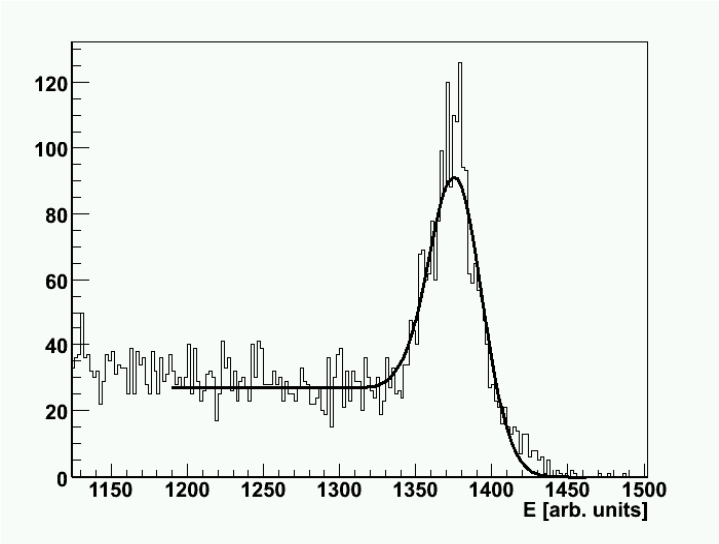


Lab Tests: Noise versus bandwidth

High speed readout => high bandwidth => short shaping times
Thermal noise of the DEPFET transistor ~ 1/SQRT(τ)



1.6 e ENC at τ=10 μs



25 e ENC at τ=33ns (30MHz)

$$ENC = \sqrt{\alpha \frac{8kT g_m}{3g_q^2}\frac{1}{\tau} + 2\pi a_f C_{tot}^2 + qI_{Leak}\tau}$$

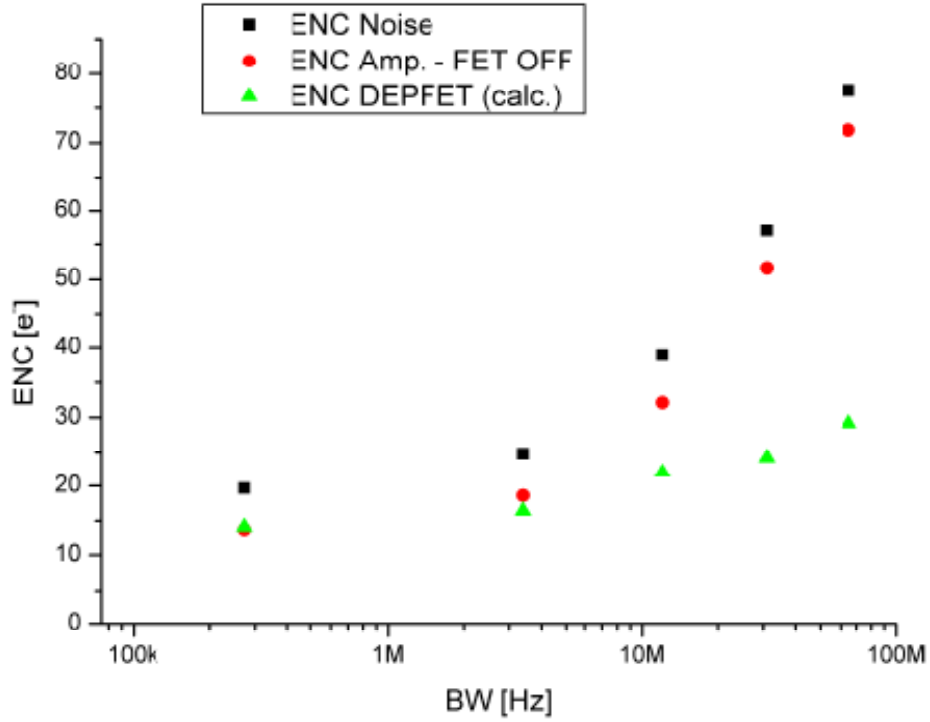
Measurements of a single pixel with an external high bandwidth amplifier.

Lab Tests: Noise versus bandwidth

For 20 MHz line readout rate: 50 MHz bandwidth for single measurement (sample-clear-sample)

@ 50 MHz: rms ~ 30 e-

Aim for S/N ~ 40/1 (~ 100 e-): sufficient headroom for external noise sources!



Intrinsic DEPFET noise sufficiently low for high speed operation at ILC

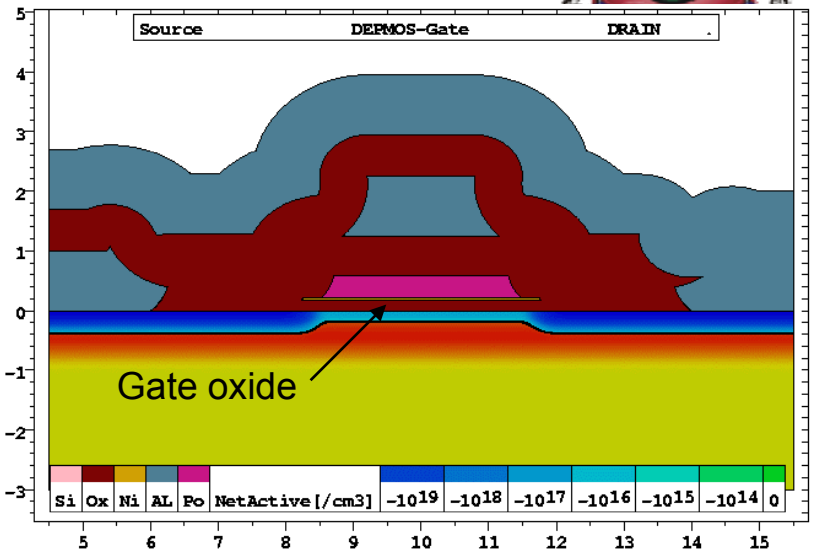
Radiation Hardness

Ionising radiation (γ, e from beamstrahlung).

Creation of fixed positive charge in gate oxide.

Shift of flatband voltage (more negative to compensate oxide charge).

Shift of transistor threshold voltage



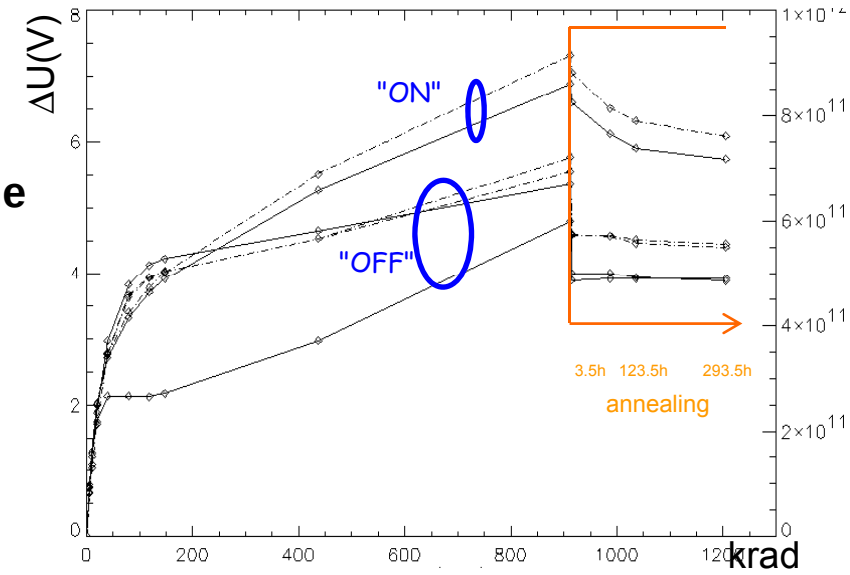
Irradiation with Co^{60} γ: ~ 1 MRad

Transistor off: ΔU ~ 4V

Transistor on: ΔU ~ 6V

DEPFET operation: transistor off most of the time (1000/1).

Threshold voltage can be compensated adjusting switcher voltages.

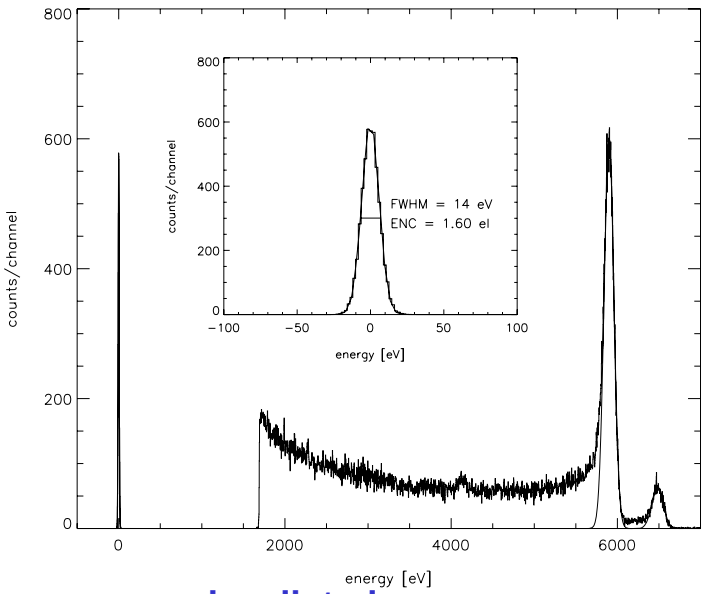


Radiation Hardness

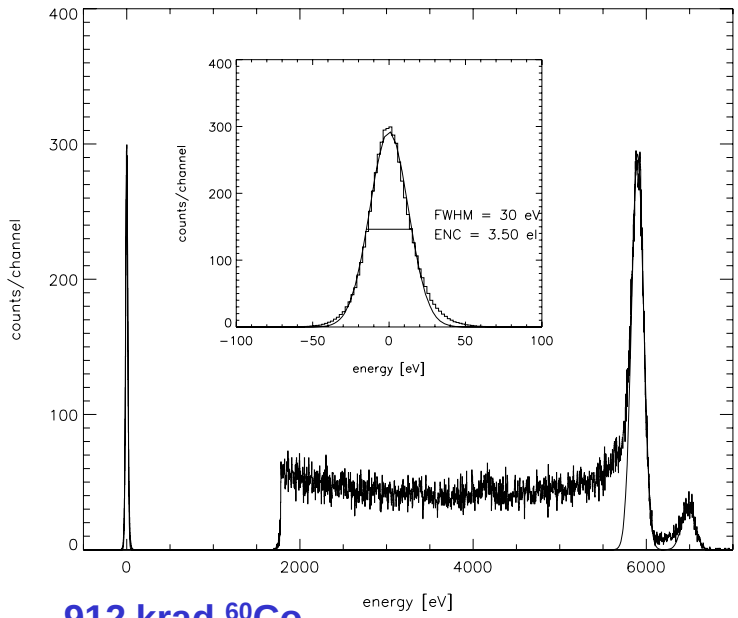
Oxide damage: introduce traps at interface, reduce mobility

-> increase of 1/f noise

-> change of transistor gain: g_m, g_q



non-irradiated
V_{thresh}≈-0.2V, V_{gate}=-2V
time cont. shaping τ=10 µs



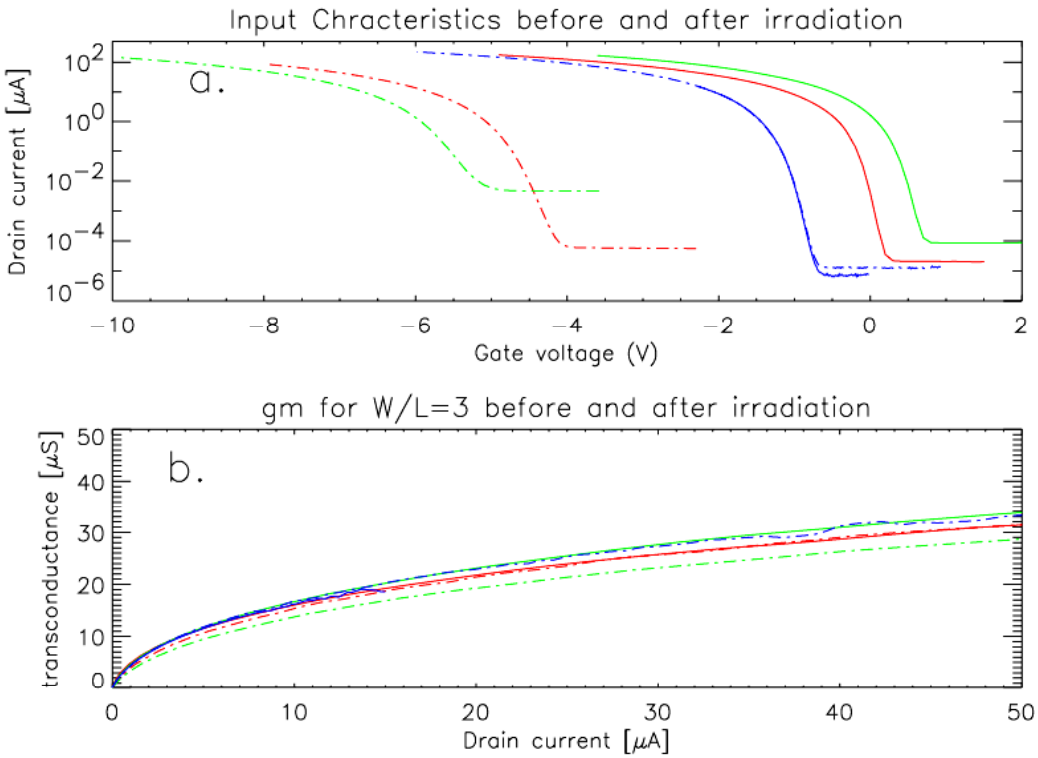
912 krad ^{60}Co
V_{thresh}≈-4.0V
time cont. shaping τ=10 µs

Noise ENC=1.6 e^- (rms)
at T>23 degC

Noise ENC=3.5 e^- (rms)
at T>23 degC

Negligible noise increase observed (1/f noise does not scale with 1/Sqrt(τ))

Radiation Hardness: protons, neutrons



gamma,
neutron*
proton*,
irradiations
*** @ Berkeley**

NIEL: increase of leakage current => shot noise

$3x10^{12}$ n/cm^2 (~ 35 ILC years !):
95e$^-$ ENC @ 20^{0}C
22e$^-$ ENC @ 0^{0}C

With Δt = 50 μs (frame rate)

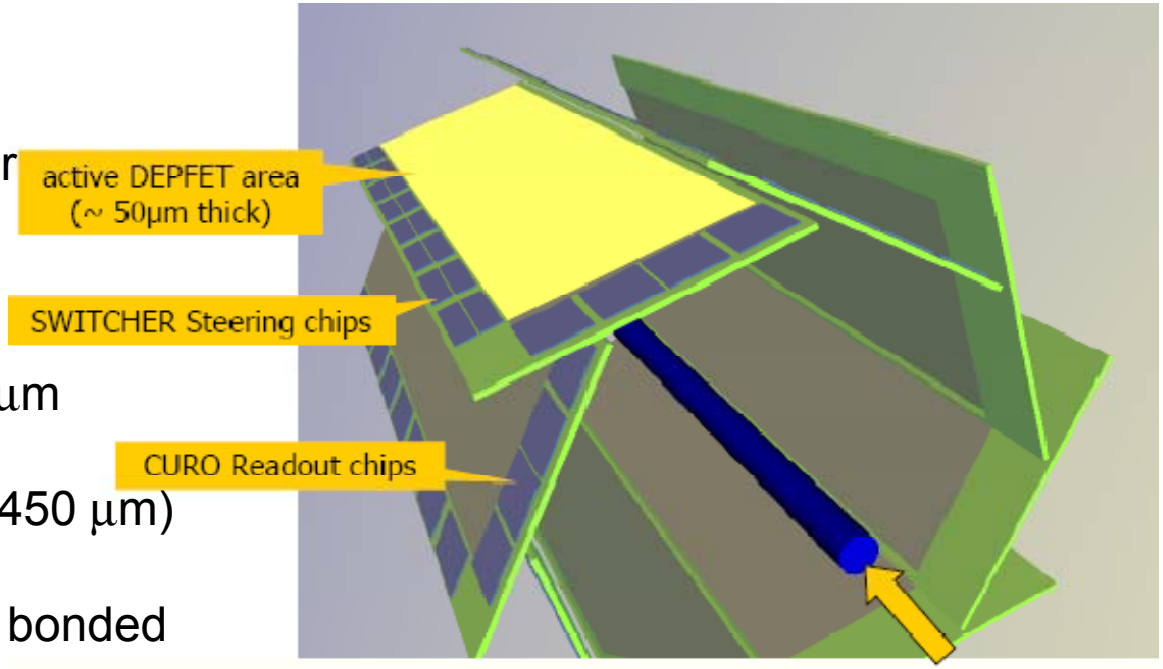
Type	fluence	ILC years	ΔV_{thresh}	g_m	I_{leak} (pixel)*
Gamma	913 kRad	~30	~4V	=	~100fA
Neutron	$2.4x10^{11}$ n/cm^2	~2	0V	~	1.4 pA
Protons	$3x10^{12}$ n/cm^2~ & 280 kRad	~35	~5V	-15%	25.9 pA

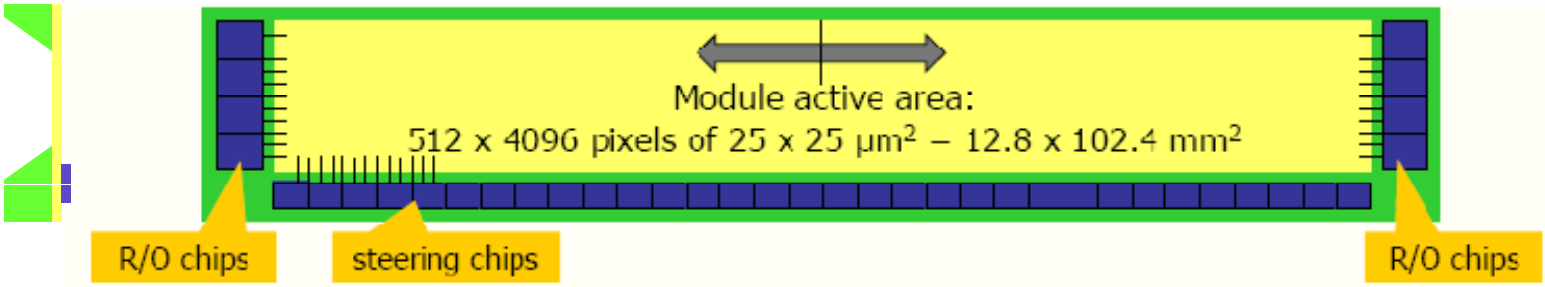
*unirradiated: ~5-22 fA

Module Concept & Material Budget

Innermost Layer:

- One self supporting Si-sensor
- Readout at both ends
- Sensitive area thinned to 50 µm
- Support frame not thinned (~450 µm)
- Thinned (50 µm) ASIC bump bonded





Thinning Technology at MPI Semiconductor Laboratory

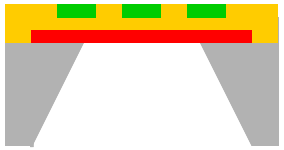
1) **Process backside of thick detector wafer (structured) implant.**

2) **Bond detector wafer on handle wafer (SOI).**

3) **Thin detector wafer to desired thickness (grinding & etching).**

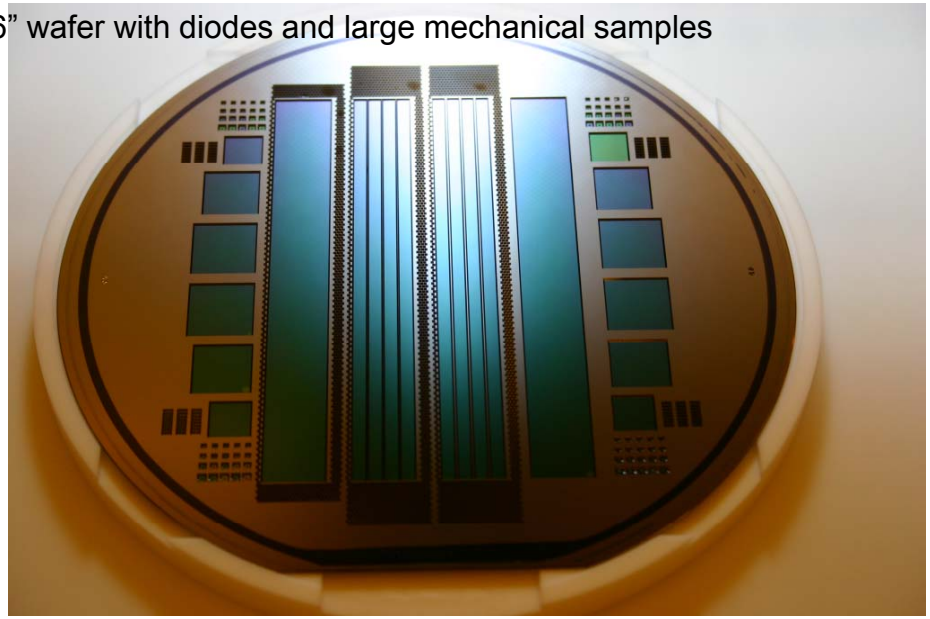
4) **Process front side of the detector wafer in a standard (single sided) process line.**

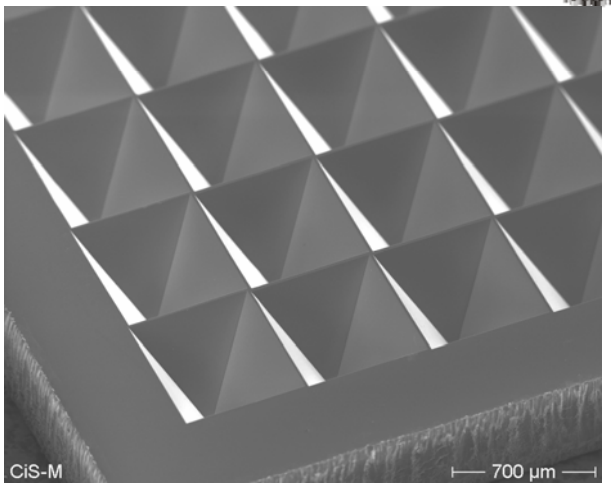
5) **Etch handle wafer.**
If necessary: add Al-contacts
Leave frame for stiffening and handling, if wanted

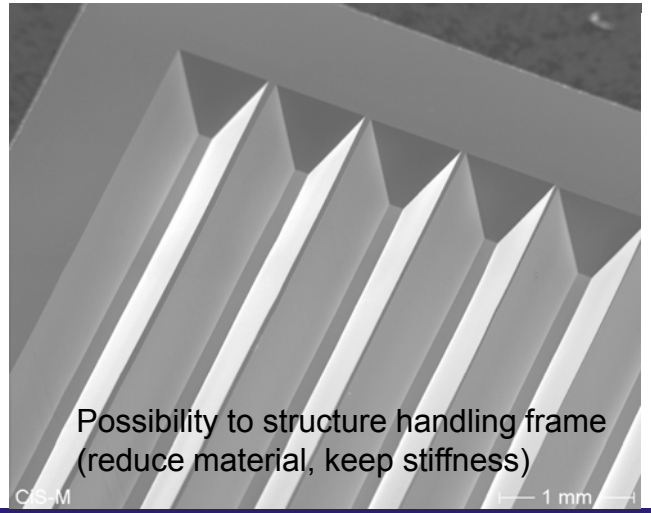


Thinning : mechanical samples

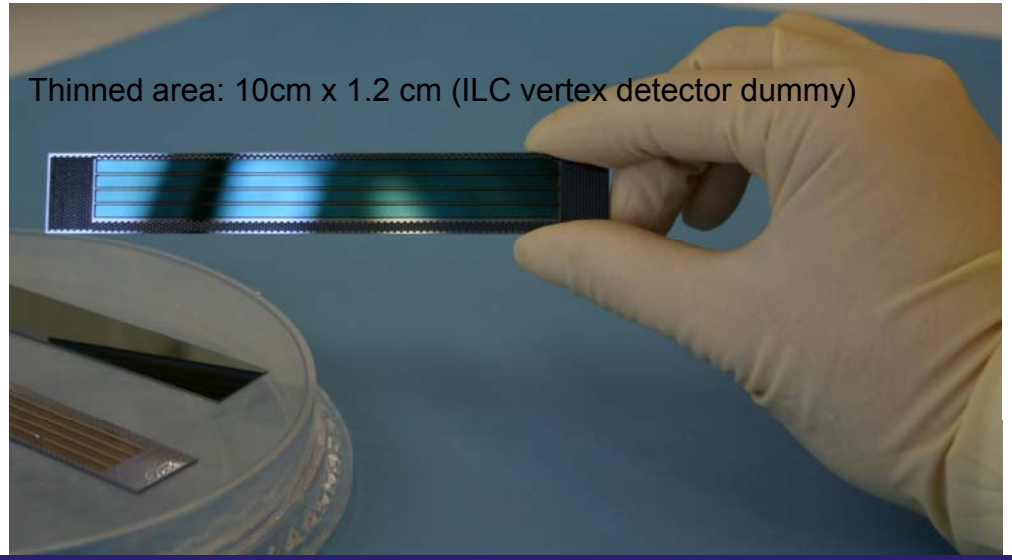
6” wafer with diodes and large mechanical samples





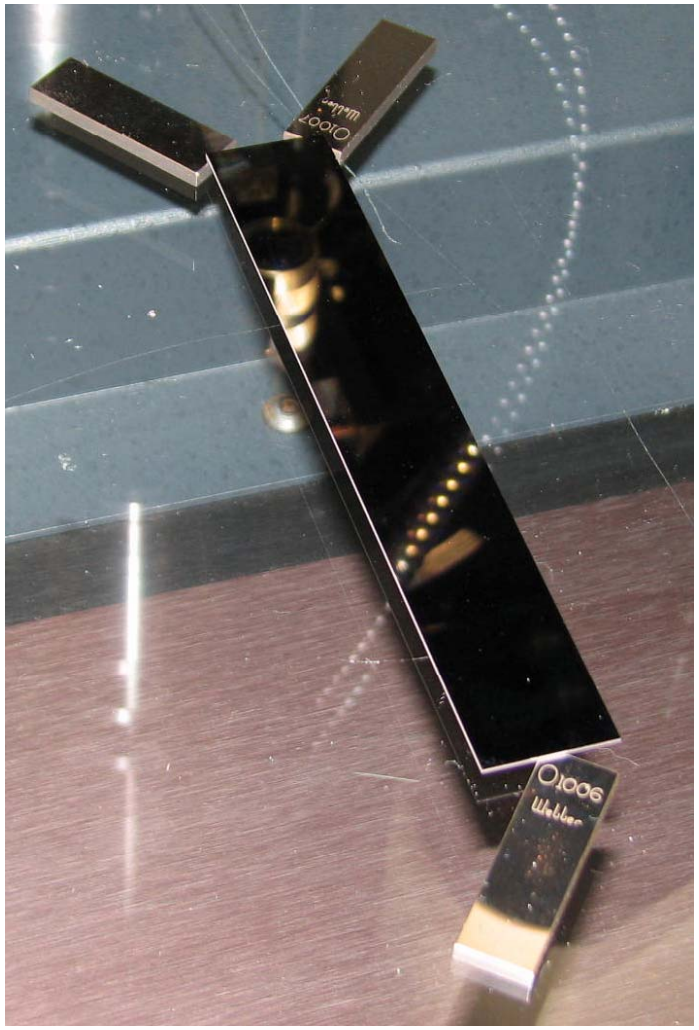


Possibility to structure handling frame
(reduce material, keep stiffness)

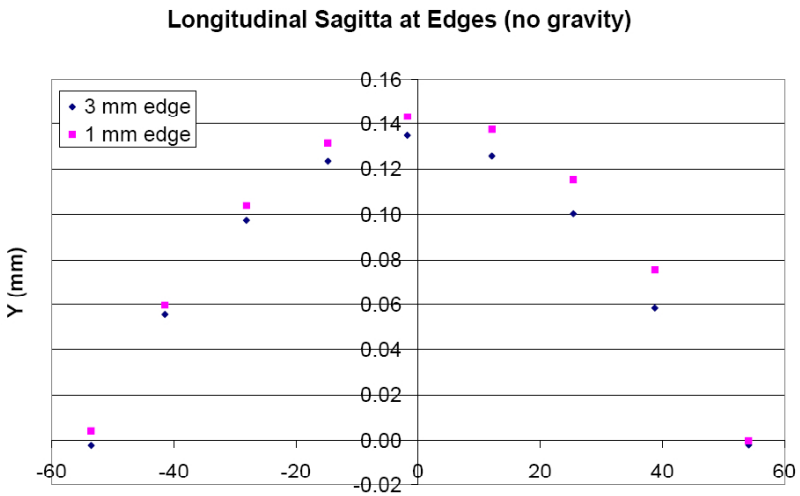


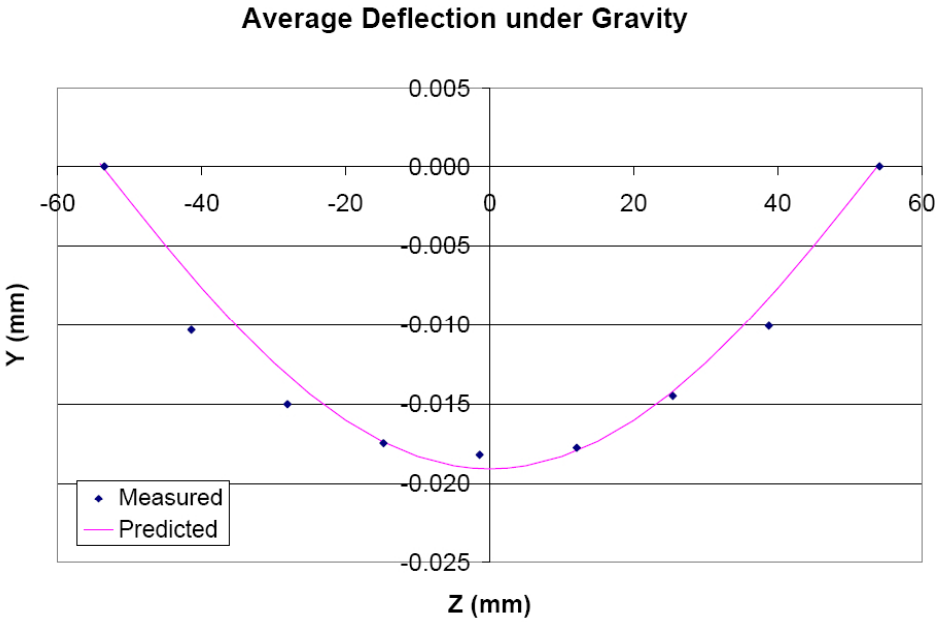
Thinned area: 10cm x 1.2 cm (ILC vertex detector dummy)

Mechanical Properties

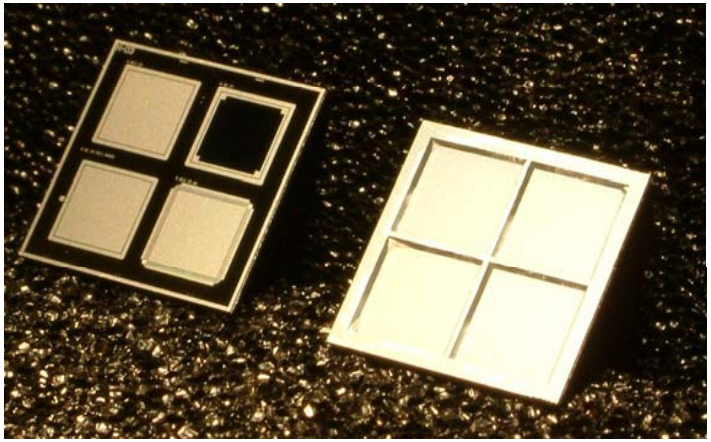


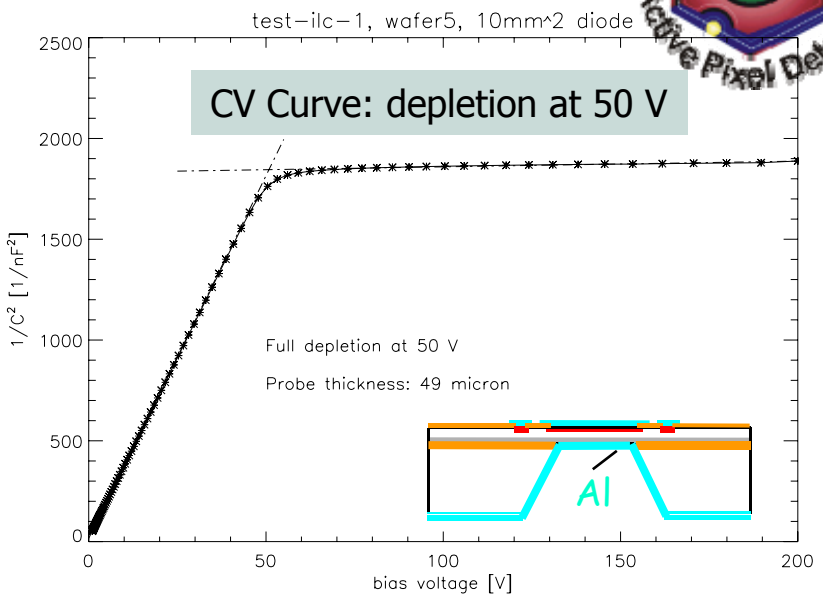
Bill Cooper, Fermilab

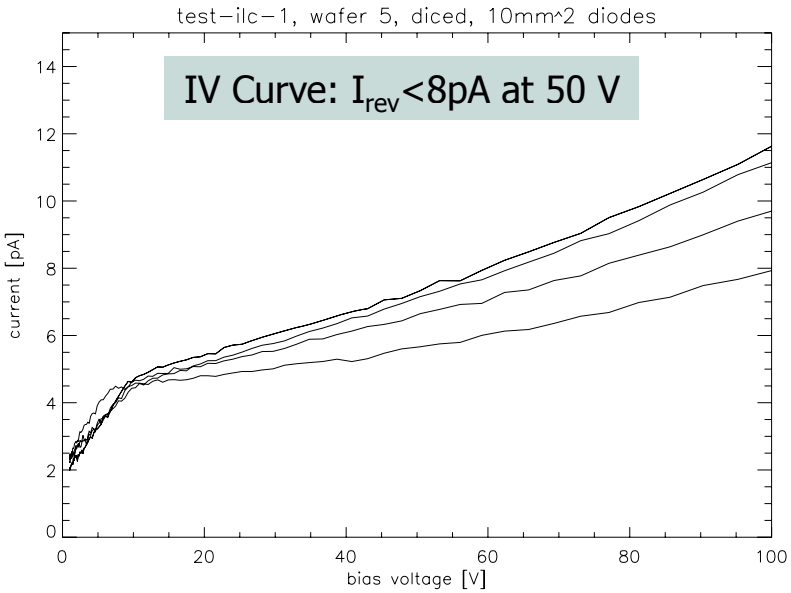


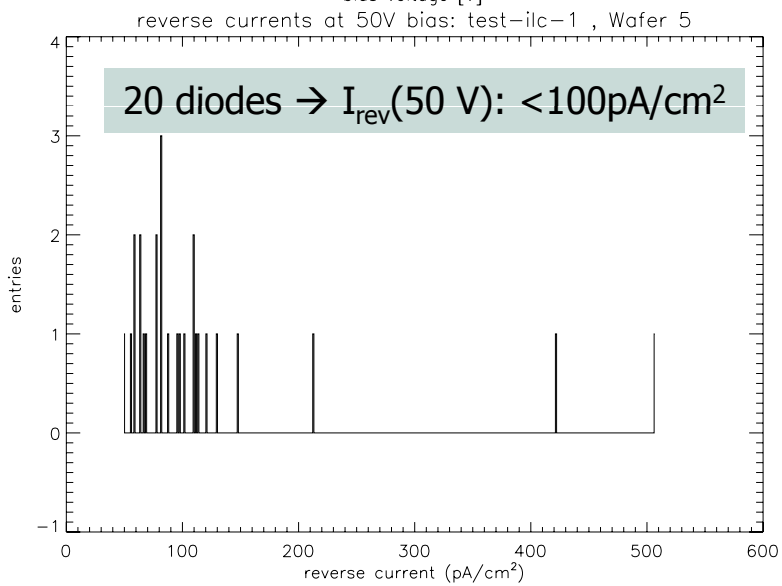


PiN Diodes on thin Silicon





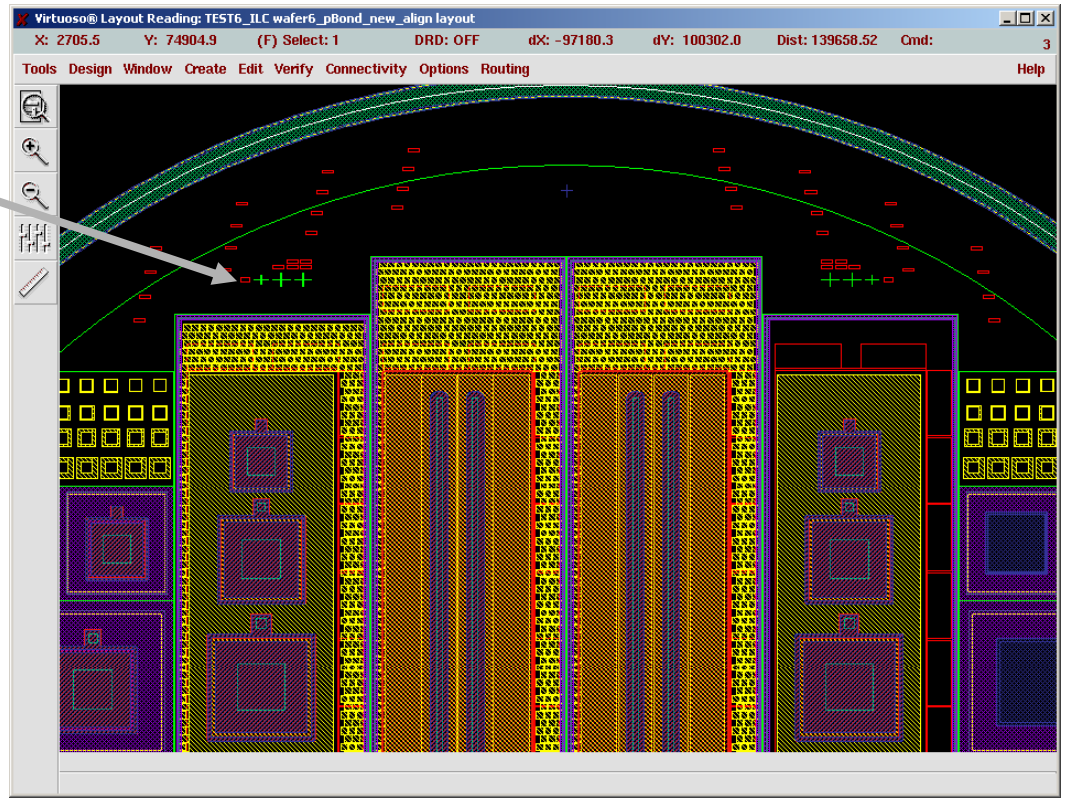




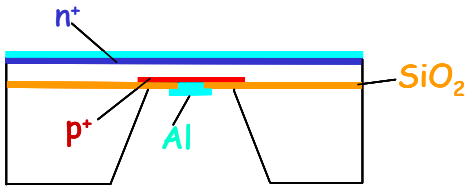
Actual Projects: Large ILC type structures

- Large (10cm x 1.2cm) ILC module like structures, 50 µm thick
- Instrumented with MOS diodes and strip-like patterns
- Smaller test diodes and MOS structures
- Backside implant like needed for DEPFETs (structured p-implant)
- Processing of real thinned DEPFETs scheduled for 2008/2009

Alignment marks in BOX to find the partial p-implant after bonding



Implants like DEPFET config.

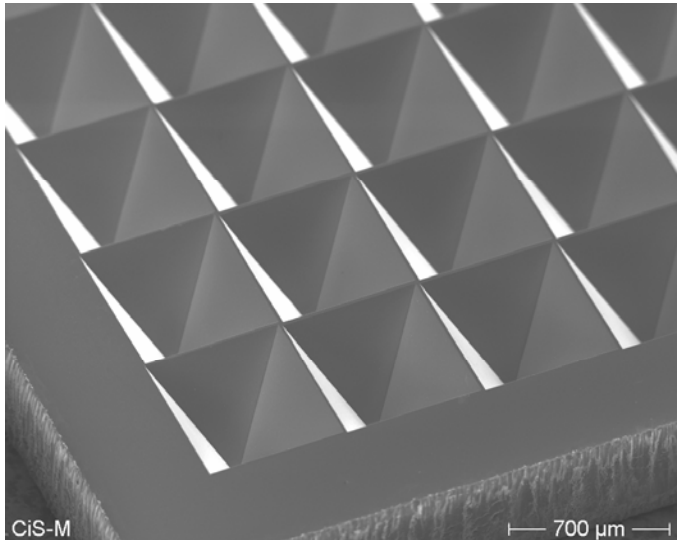


unstructured n+ on top
structured p+ in bond region

Material Budget

Material budget (within acceptance)

Sensor:	50 μm Si:	0.05% X_0
Frame:	450 μm Si	0.05 % X_0
Switcher:	50 μm Si	0.01 % X_0
Gold bumps:		0.03 % X_0
Total:		**0.12 % X_0**



Frame perforated to reduce material keeping mechanical strength

All silicon module:

-**Low material budget**

-**Mechanical rigidity**

-**Easy handling**

-**Minimal CTE effects**

-**Single module scale sensor**

New Pixel Production

New Pixel Production: PXD5

-Larger matrices:

512 x 512 (1.6 x 1.2 cm²)
128 x 2048 (0.3 x 4.9 cm²)

-optimization clear ⇔ gain
lower clear voltages

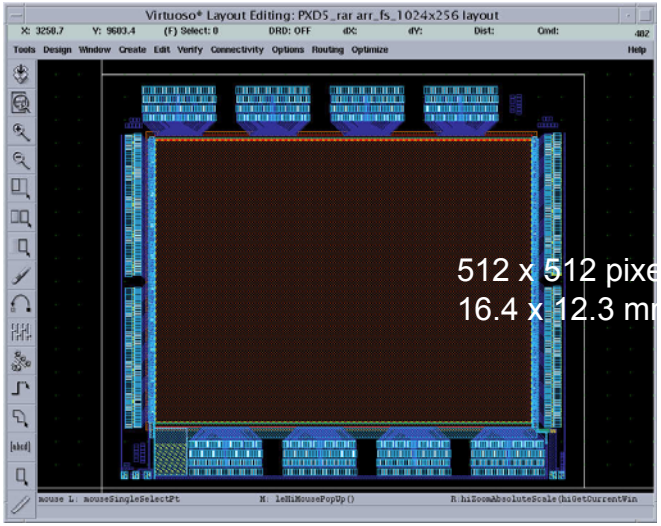
-variants:

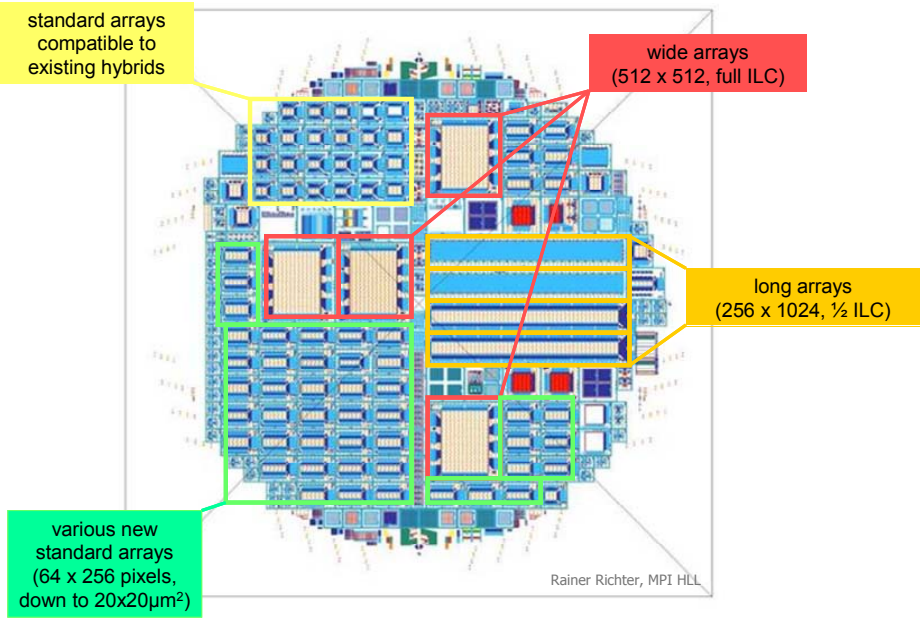
small pixels (20x20 μm²)
shorter gate -> higher g_q

-Test structures for bump bonding

-Ready since June 2007

-First matrices in a lab and beam test





Summary and Conclusions

DEPFET pixel detectors for ILC have been designed, simulated and fabricated at the MPI semiconductor laboratory

Measurements of single pixels demonstrate:

- charge-current conversion as expected from simulations
- fast and complete clear
- low noise even at high bandwidth
- sufficiently radiation tolerant for use at ILC

All silicon module/ladder concept: based on thinned sensors

- thinning technology demonstrated
- thinned samples/diodes have good mechanical and electrical properties
- 0.1% radiation length per layer in reach

2nd generation pixel matrices produced

- larger (ILC scale) array
- smaller pixel size
- improved properties (gain, clear behaviour)
- evaluation in progress

Hans-Gunther Moser

for the DEPFET Collaboration
(www.depfet.org)

R G B	R G B	R G B
44, 31, 113	120, 101, 213	194, 186, 236