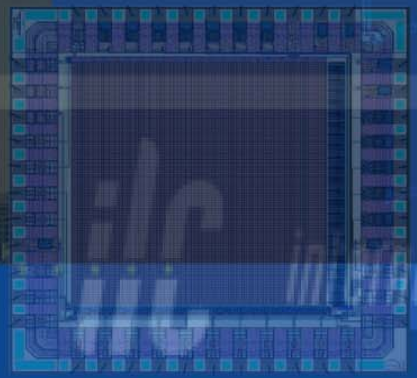
ILC Vertex Tracker

From Instrumentation R&D to Physics Benchmarking

A *LNBL* and *UC Berkeley* Program in collaboration with *Purdue U*, *INFN Padova* and *INFN Torino*

M Battaglia
UC Berkeley and LBNL



WWS ILC Vertex Review
October 22-27, 2007

LAWRENCE BERKELEY NATIONAL LABORATORY

Collaborators

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VTX Simulation, Reconstruction, Analysis

Physics Benchmarks

G4/Mokka

lcio

Sensor Simulation

PixelSim

lcio

ALS & FNAL Beam Test Data

Jet Flavour Tagging + CDF Vtx Fit

Marlin

Cluster Reconstruction

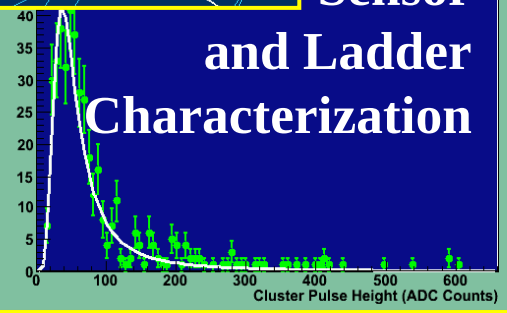
PixelAna

lcio

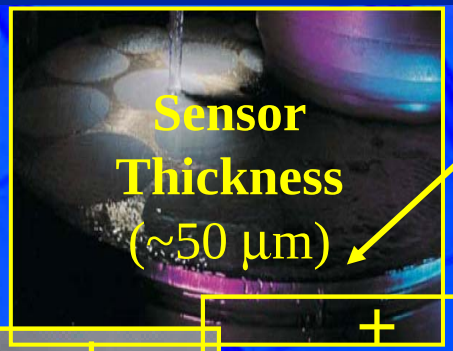
Track Fit and Extrapolation

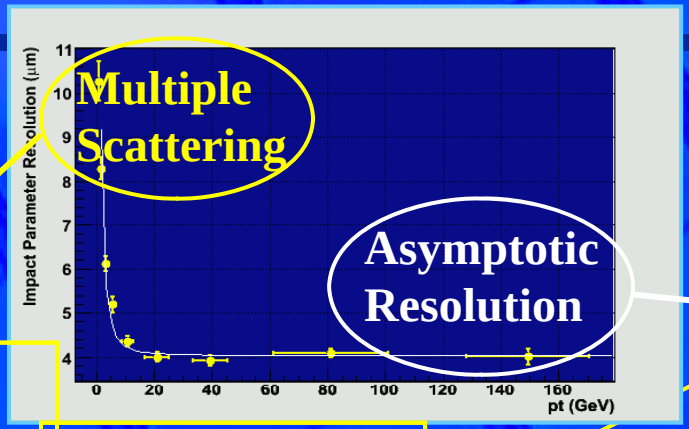
VTX Pattern Recognition

Sensor and Ladder Characterization



ILC Vertex Tracker: Requirements and R&D Streams





Pixel Size
(10-20 μm)

+
Services
Cooling
[80 mW/cm²]

Power
Dissipation
[<1mW/ADC]

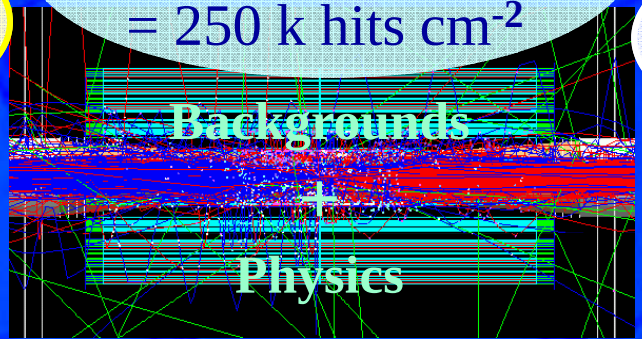
ADC
Resolution
[~5 bits]

Readout
Speed
[25-50 MHz]

Airflow removes
70-100mW/cm²
< 0.5 mW/ADC

5 hits/BX
x 9 (20 μm pixels)/hit
= 250 k hits cm⁻²

25 MHz r/o
25 μs/512 pixel col
O(1 %) occupancy

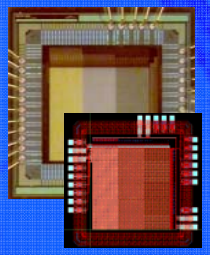


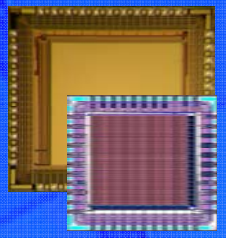
(demonstrated)
[R&D in progress]

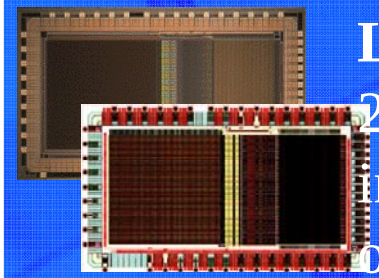
Monolithic Pixel Sensor Development

Analog Pixel Architecture

- Charge Interpolation [$\sigma \sim a/(S/N)$]
- In-pixel CDS & On-chip Digitisation
- Fast Readout







AMS 0.35µm-OPTO

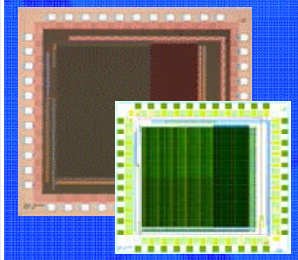
LDRD-1 (2005):
10, 20, 40µm pixels

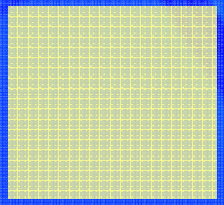
LDRD-2 (2006):
20µm pixels,
in-pixel CDS
3T and SB pixels

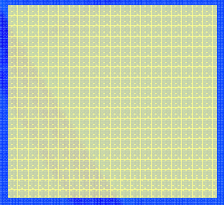
LDRD-3 (2007):
20µm pixels,
in-pixel CDS
on-chip 5-bit ADCs

Binary Pixel Architecture

- Small Pixels [$\sigma = \text{pitch}/\sqrt{12}$]
- In-pixel Discr. & Time Stamping
- In-situ Charge Storage







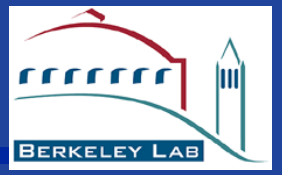
OKI 0.15µm FD-SOI

LDRD-SOI-1 (2007):
10µm pixels,
analog & binary pixels

OKI 0.20µm FD-SOI

LDRD-SOI-2 (2008):
10µm pixels,
analog & binary pixels
(in-pixel time stamp)

• • •



WP-1 Benchmarks and Physics Tools for Vertex Tracker Optimisation

WP-2 CMOS Pixel Sensors with in-pixel CDS, in-chip ADC and Fast Readout

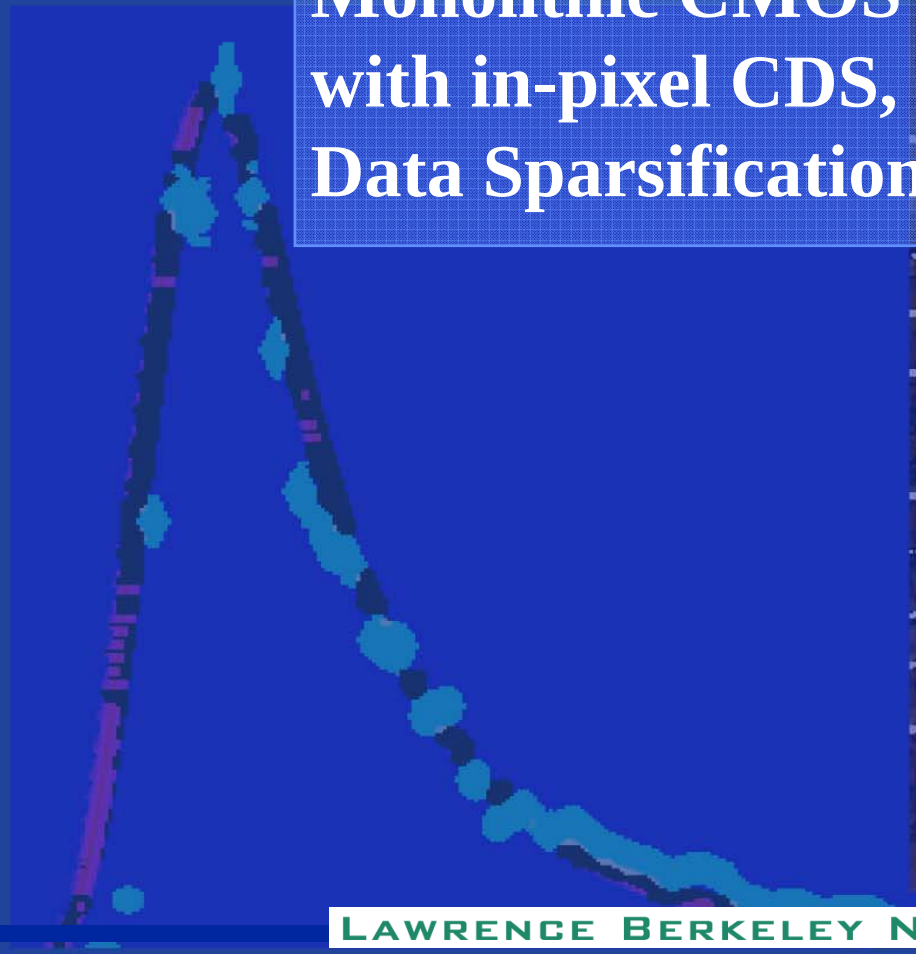
WP-3 SOI Pixel Sensors with Binary Output and Time Stamping

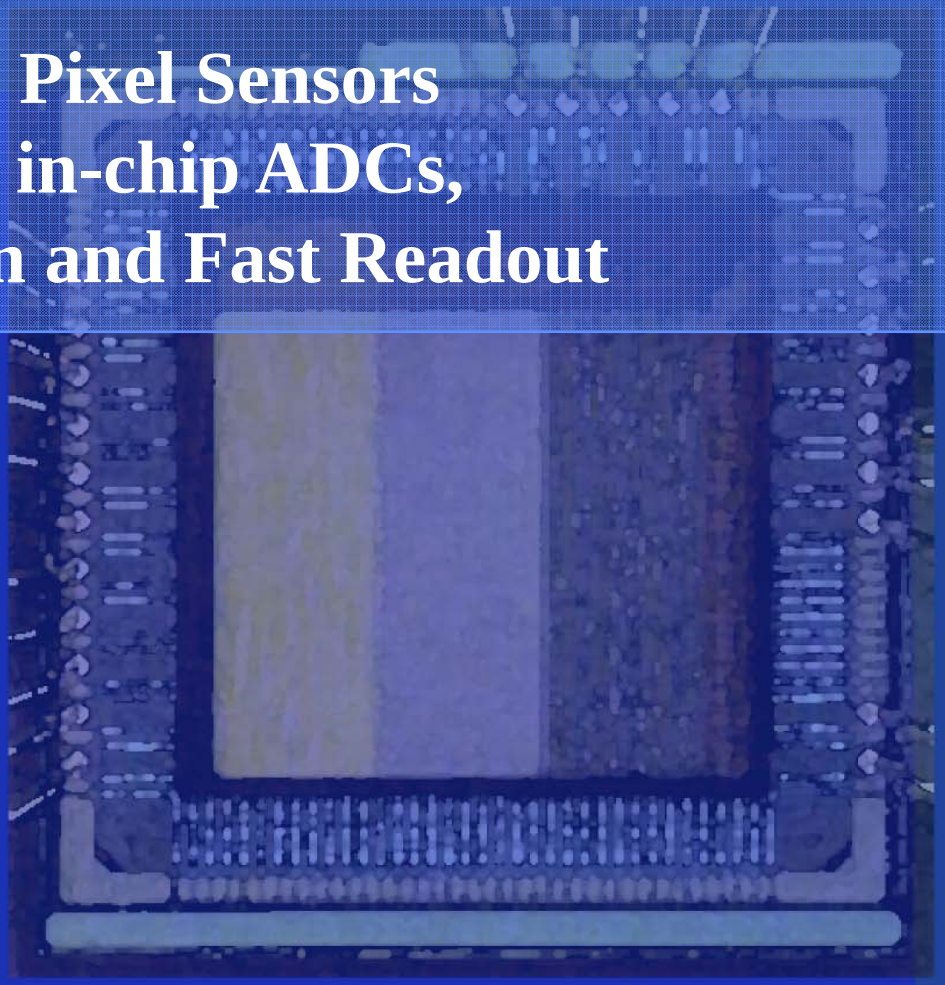
WP-4 Low Mass Vertex Tracker Ladder

WP-5 Vertex Tracker Prototype

WP-6 ILC Vertexing and Tracking: Simulation, Reconstruction and Validation

WP-2
Monolithic CMOS Pixel Sensors with in-pixel CDS, in-chip ADCs, Data Sparsification and Fast Readout





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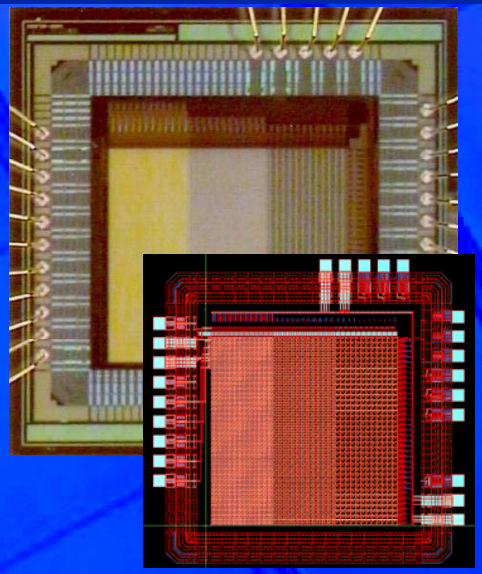
LDRD-1 Chip

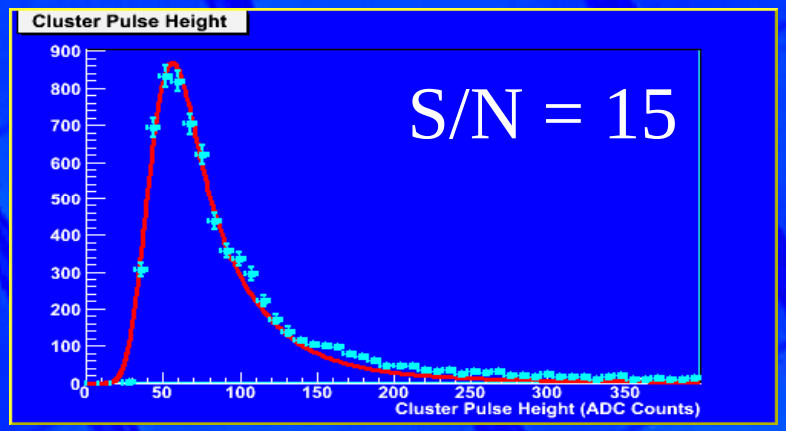
LDRD-1 Chip:

First LBNL test structure, simple 3T pixels, analog output, 3 matrices with 10x10 μm^2, 20x20 μm^2 and 40x40 μm^2 pixels;

AMS 0.35 OPTO process

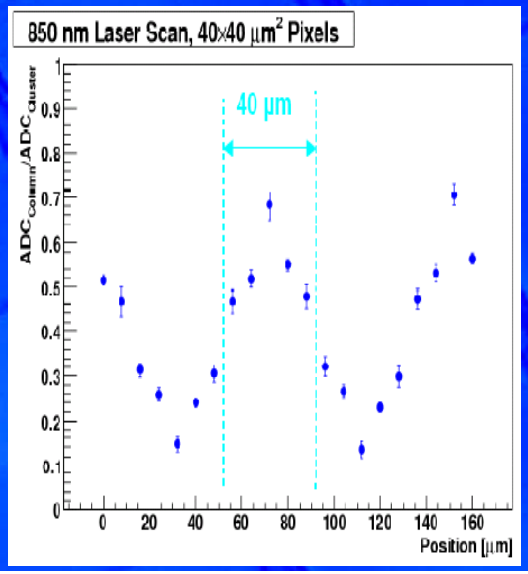


m.i.p. response with 1.5 GeV e^- beam at ALS

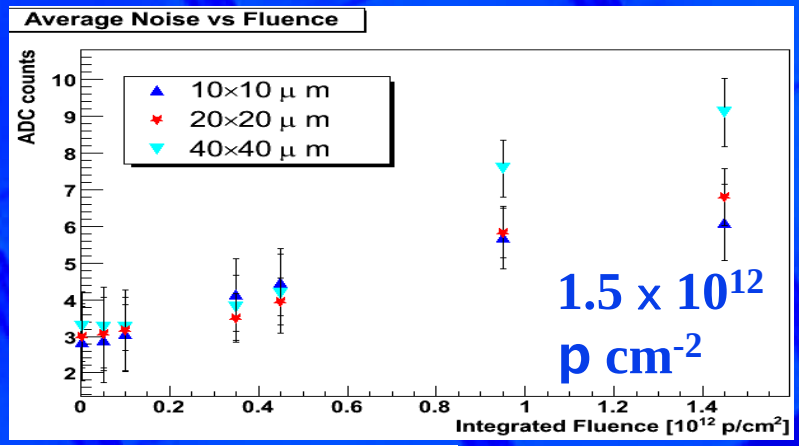


Resolution Study (focused laser spot)

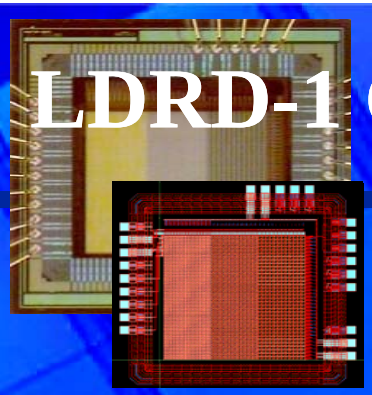
Pitch (μm)	Laser Scan	Pixel Sim
10	2.0	1.5
20	3.3	3.2
40	5.1	5.0



Radiation Hardness Test with 30 MeV p and n at 88" Cyclotron



LDRD-1 Chip: Charge Collection Time

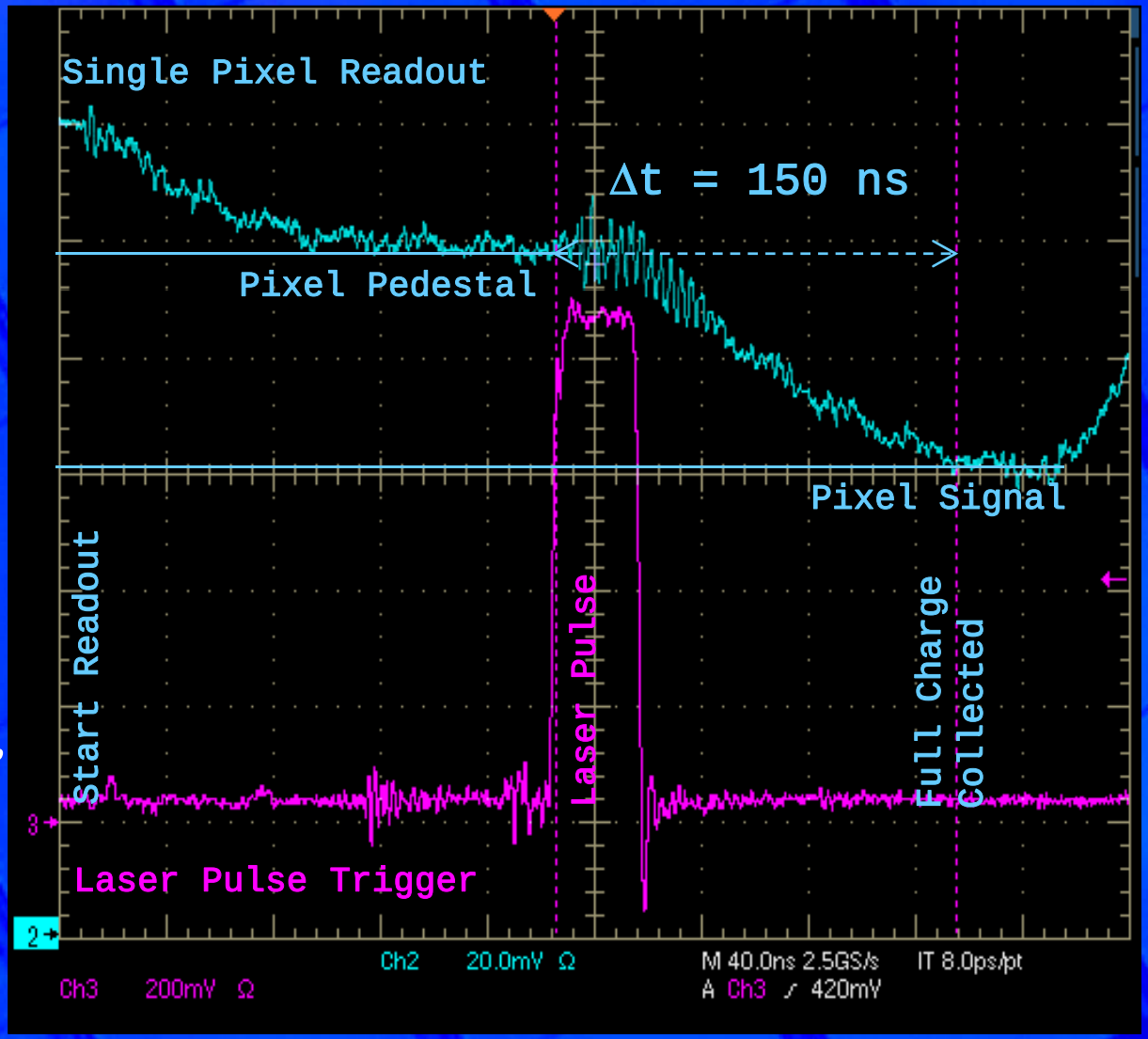


Charge carriers collected by diffusion in almost field-free epitaxial layer;

First measurement of charge collection time in AMS 0.35-OPTO process;

1 ns 1060 nm Laser pulse collimated on 20x20µm pixel, charge = 1 m.i.p.

Charge collection time
Δt ~ 150 ns



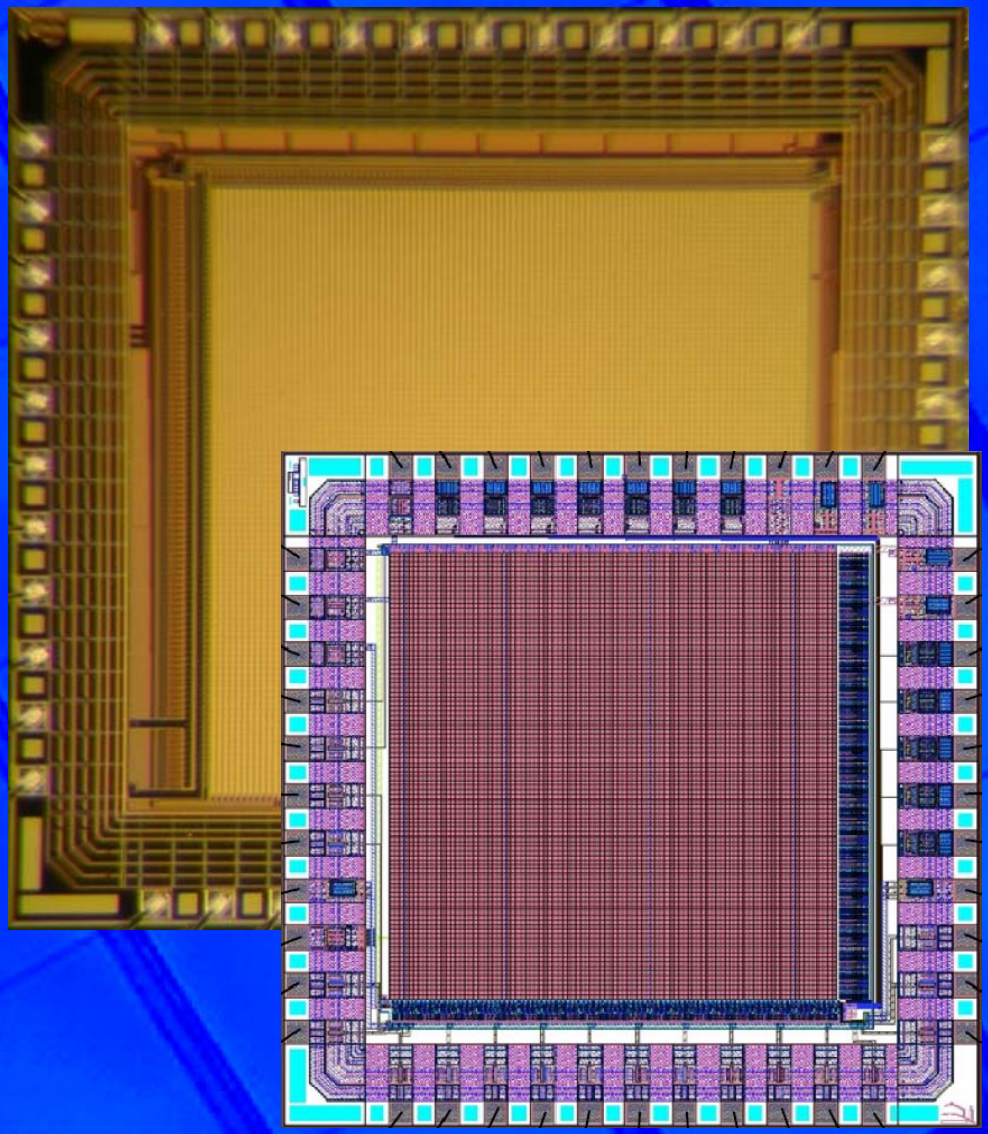
LDRD-2 Chip

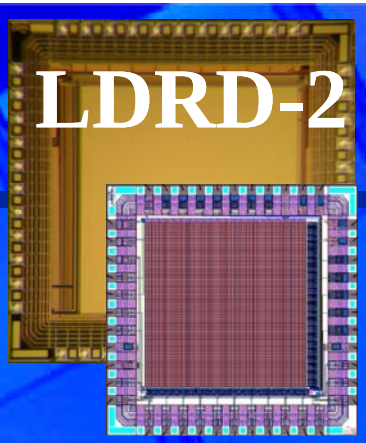
LDRD-2 Chip:

Second generation chip features more complex pixel architecture (20 transistors) with in-pixel CDS, power cycling, different bias options and diode sizes, two parallel outputs of 48 x 96 pixels.

Size: 1.5x1.5 mm^2
6 matrices of 20x20 μm^2 pixels;

AMS 0.35-OPTO process, received October 2006

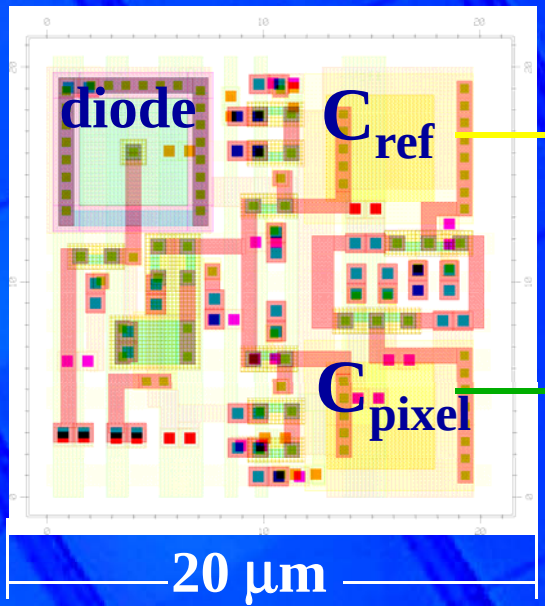


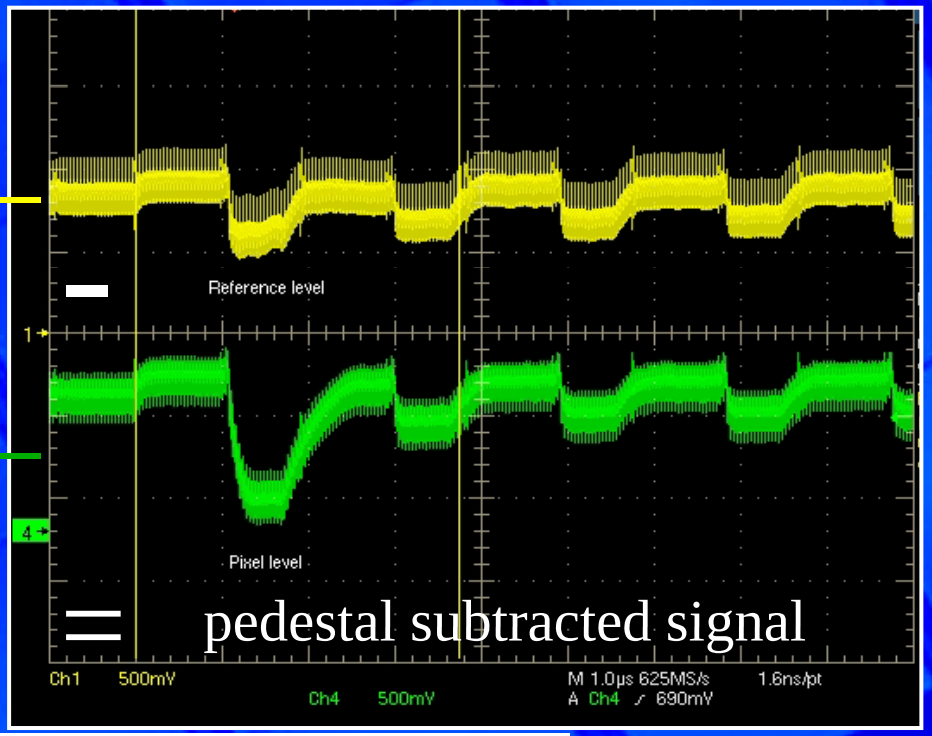


LDRD-2 Chip: In-Pixel CDS

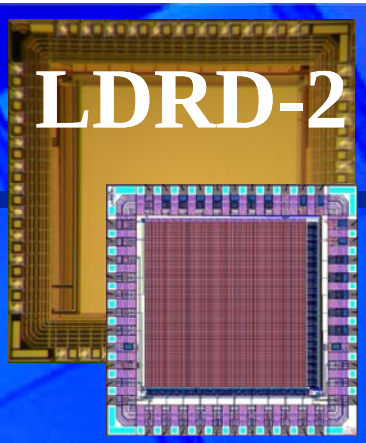
Digitisation at end of pixel column limited in precision by speed and power dissipation: advantageous to subtract pedestal level in-pixel with correlated double sampling.

Stored reference and **pixel level** with pulsed laser light:





LDRD-2 Chip: ALS Beam Test

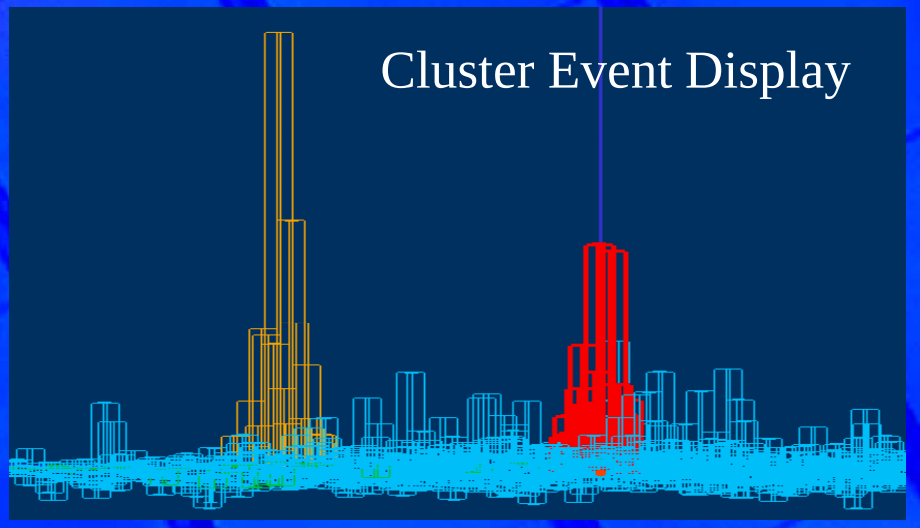


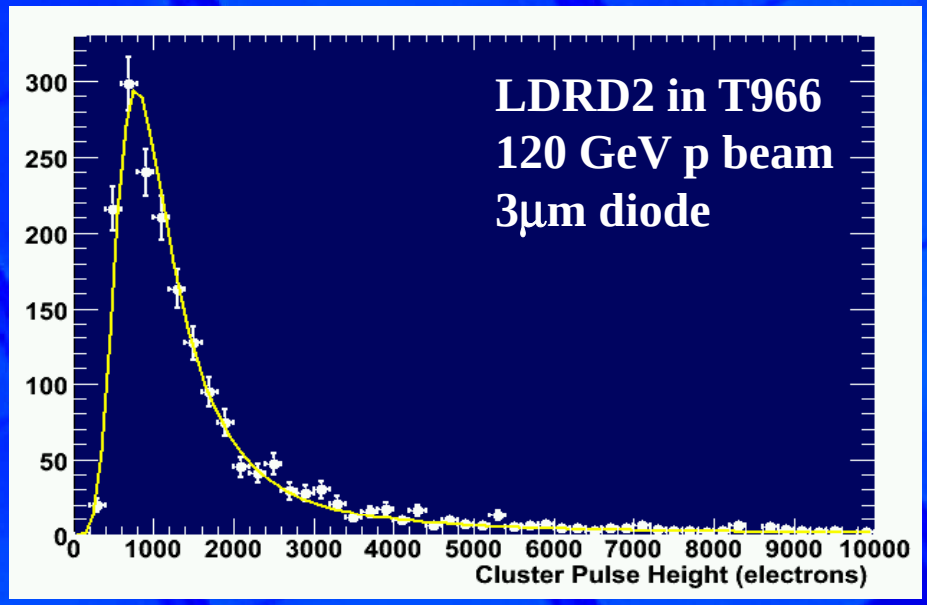
LDRD-2 tested on ALS 1.3 GeV e^- and MTest 120 GeV p beams;

Operated in rolling-shutter mode, CDS from in-pixel stored ref. charge, 1.25 - 25 MHz r/o speed, noise stable up to 25 MHz and limited by r/o board:

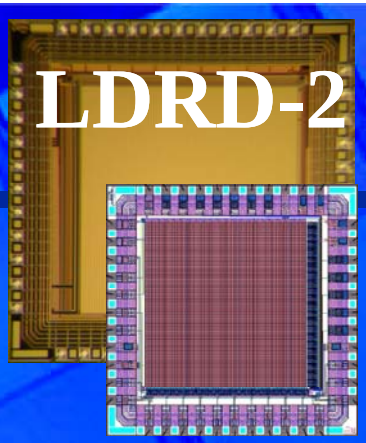
Preliminary results @ 21°C at 1.25 MHz

<Nb. of Pixels in Cluster>	**4-5**
<S/N>	**~16**





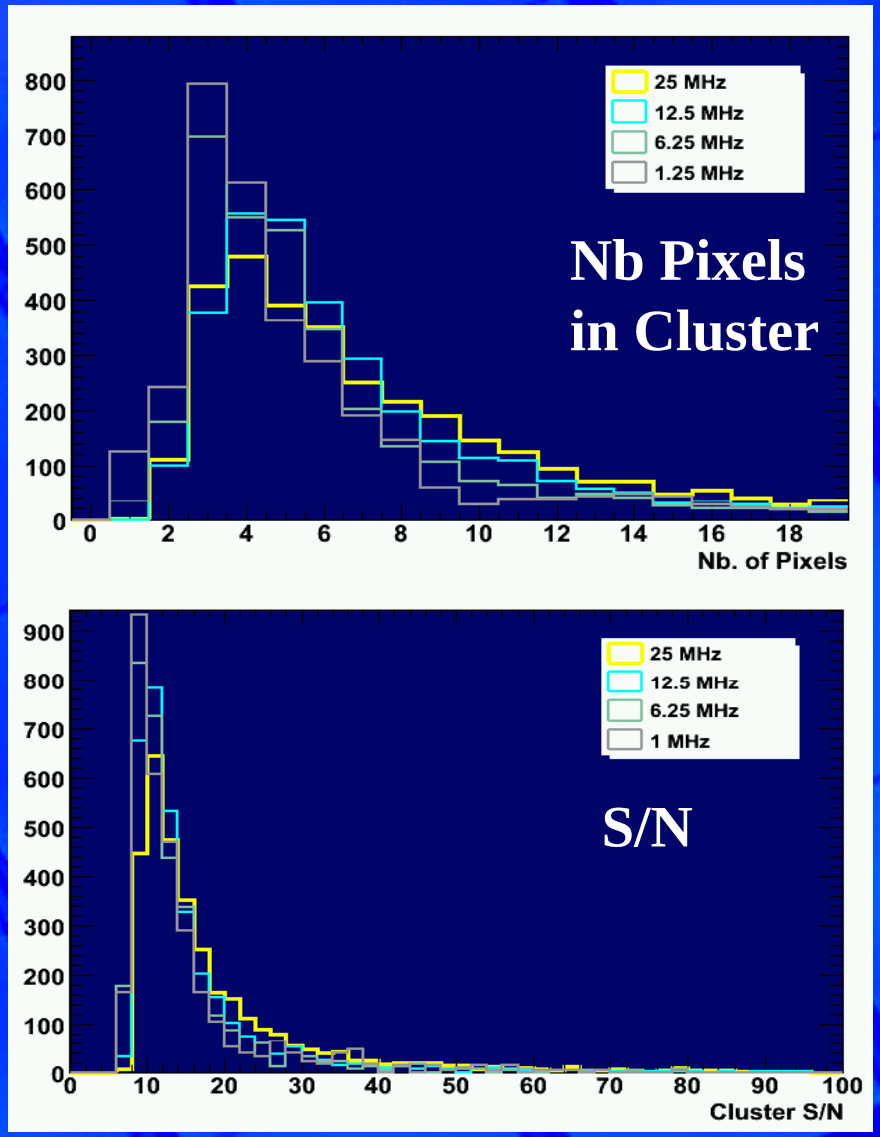
LDRD-2 Chip: 25 MHz readout



ALS BTS 1.35 GeV e^- beam

Operate LDRD-2 at different r/o frequencies under same beam conditions;

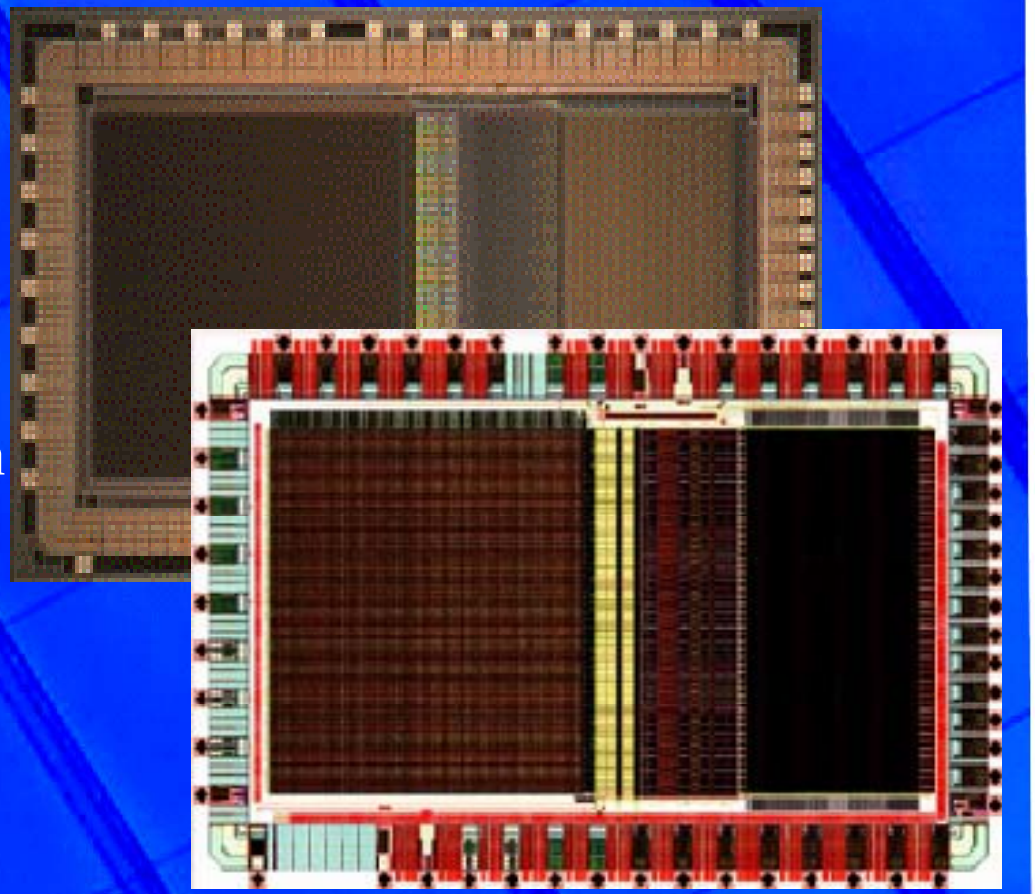
Results show no appreciable degradation of response up to maximum tested frequency of 25 MHz (integration time 184 μs)



LDRD-3 Chip

LDRD-3 Chip:

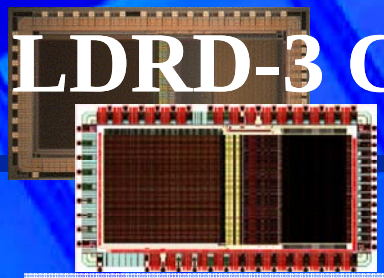
Third generation chip features same pixel cell as LDRD-2 with in-pixel CDS and 5-bit successive approximation fully differential ADCs at end of columns. CDS subtraction performed at digitisation level;

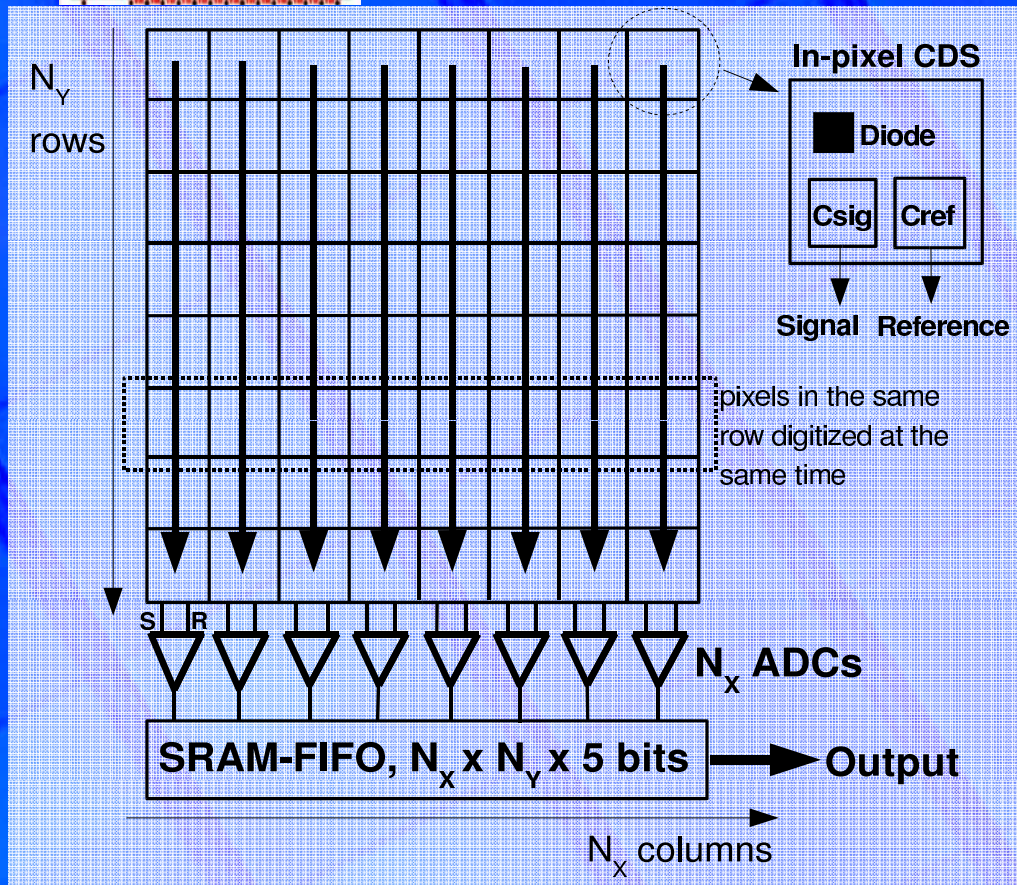


Size: 4.8x2.4 mm²
matrix of 96x96 of
20x20 µm² pixels;

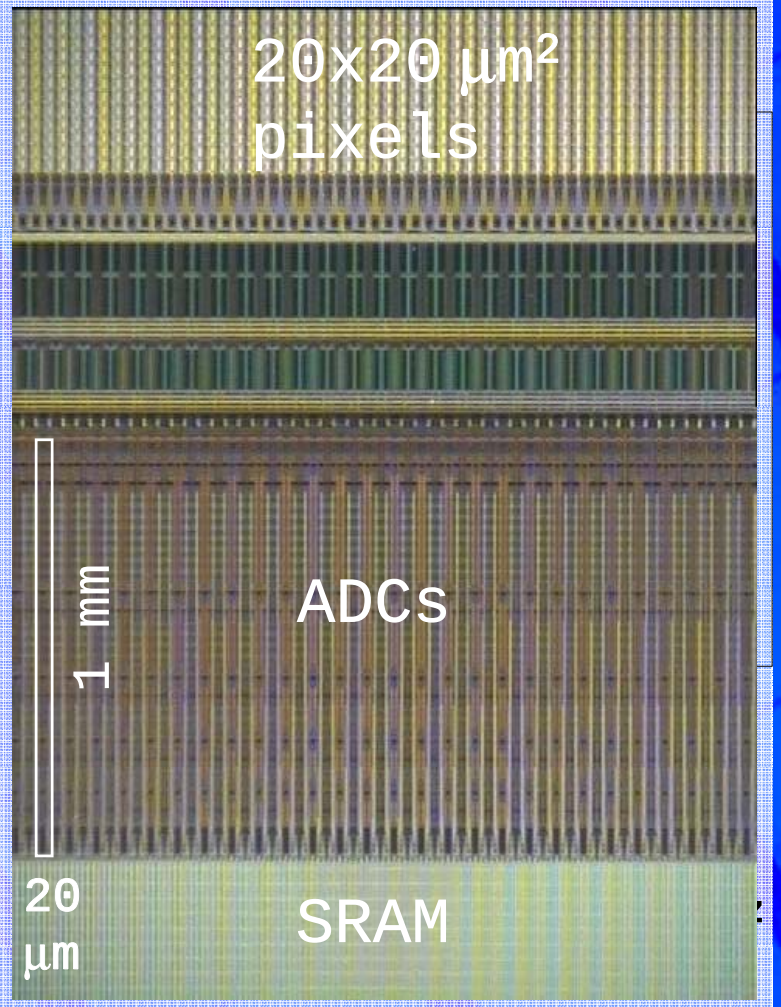
AMS 0.35-OPTO process,
received October 2007

LDRD-3 Chip





(a) Sketch of the LDRD-3 chip architecture

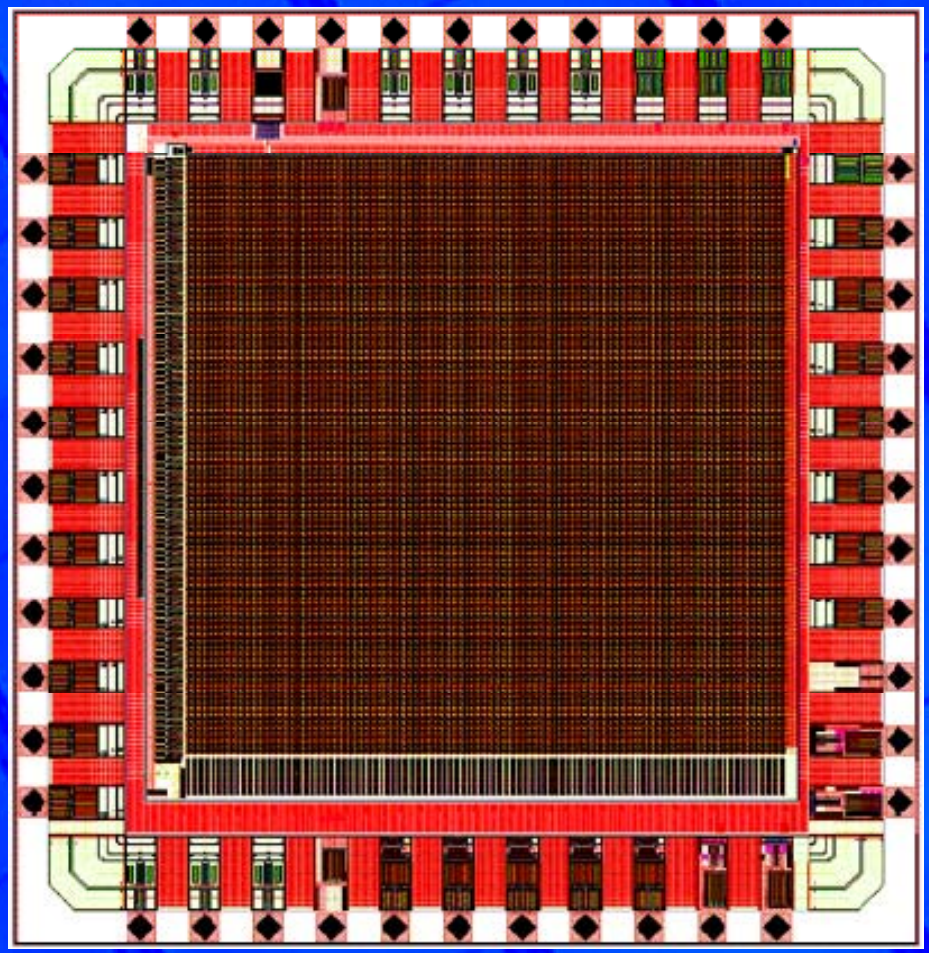


LDRD-2-RH Chip

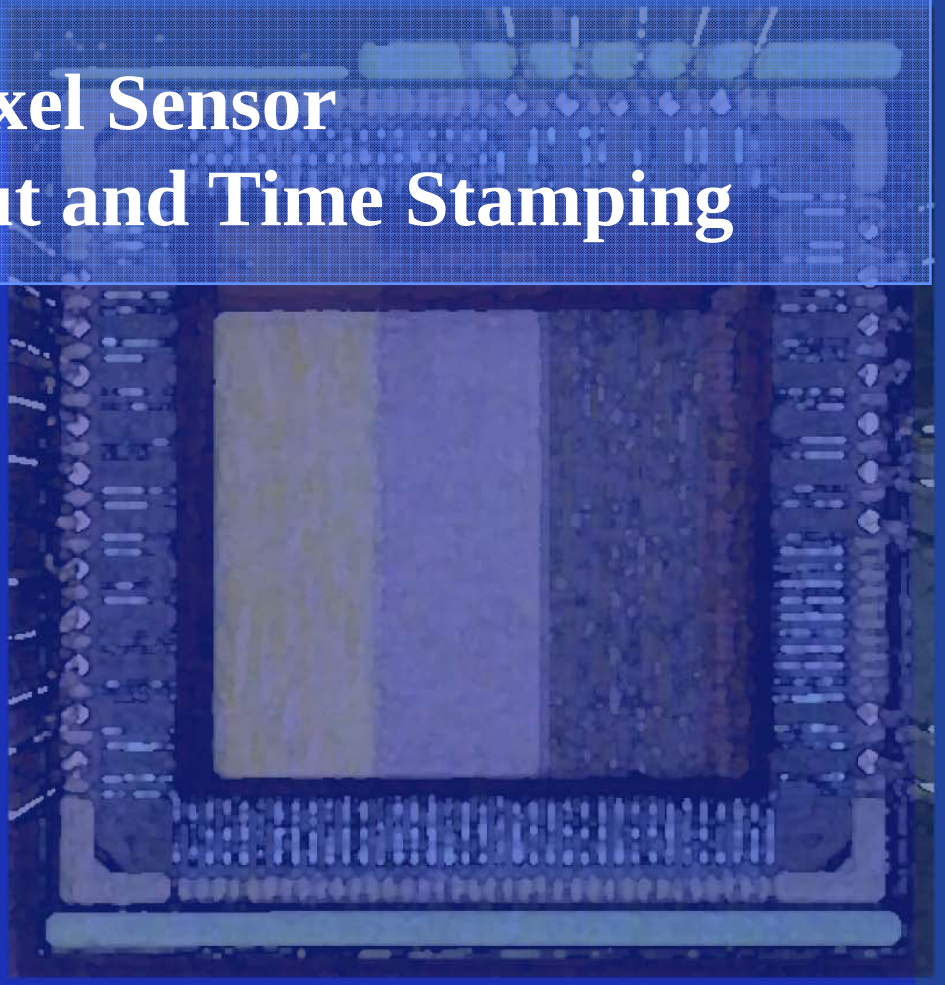
Radiation-hard test version of LDRD-2 chip;

Enclosed transistors, various diode designs (standard, extended thin oxide, same with poly guard ring, ...)

Chip submitted in October 2007 in AMS 0.35 OPTO process, to be characterised and irradiated with 200 keV e^- (NCEM), 30 MeV p and 14 MeV n (88" cyclotron)

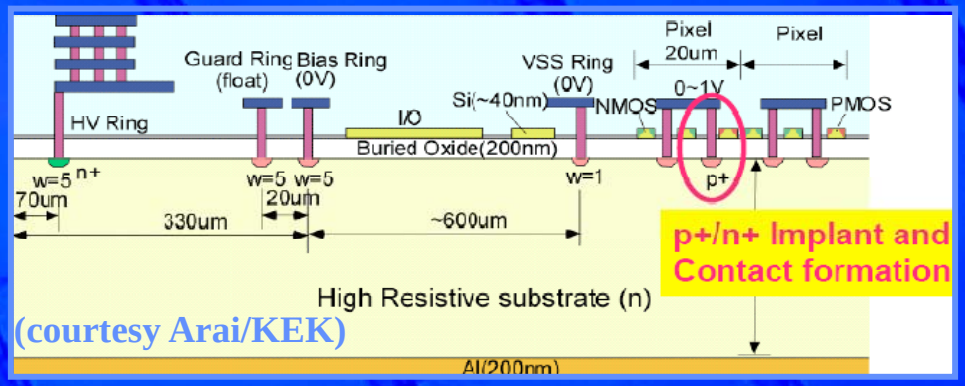


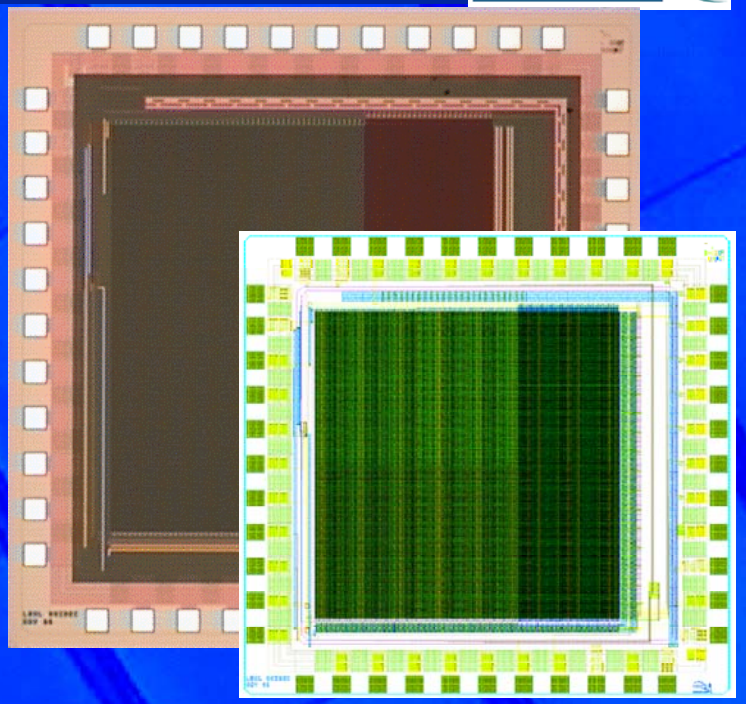
WP-3
SOI Monolithic Pixel Sensor with Binary Output and Time Stamping



LDRD-SOI Chip

SOI process offers appealing opportunity for monolithic pixel sensors, removing limitations from commercial CMOS;



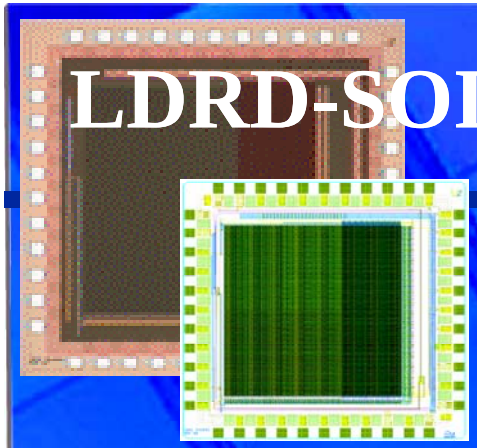


SOI appealing to industry for low-power devices, ultra-low power stand-by;

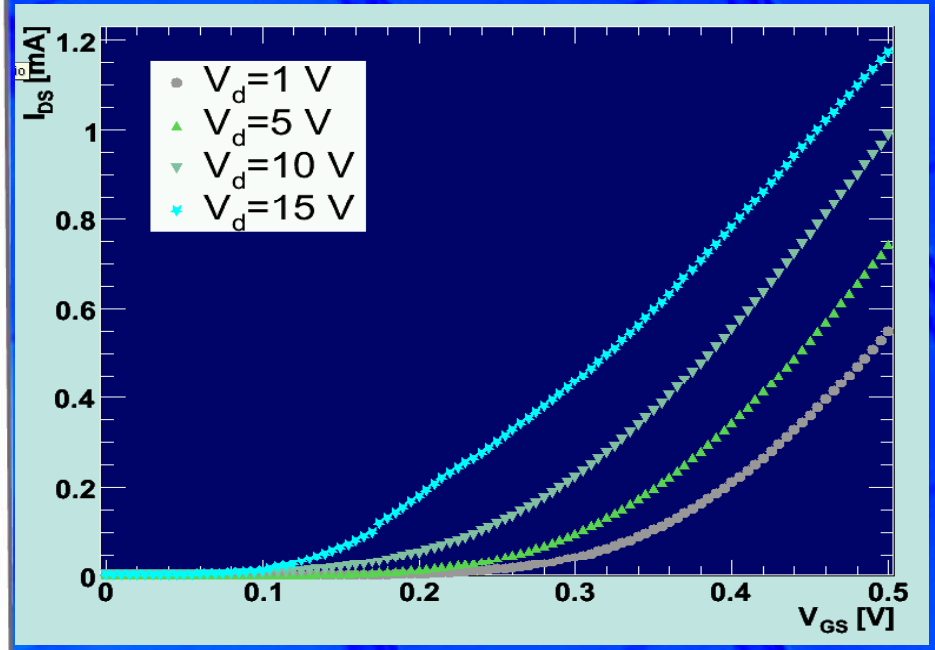
Specialized 0.15µm FD SOI process with high resistivity bulk and vias offered through KEK within R&D collaborative effort;

Chip with 10x10 µm² pixels, both **3T analog** and **digital** architectures;

LDRD-SOI-1:Tests and Irradiation

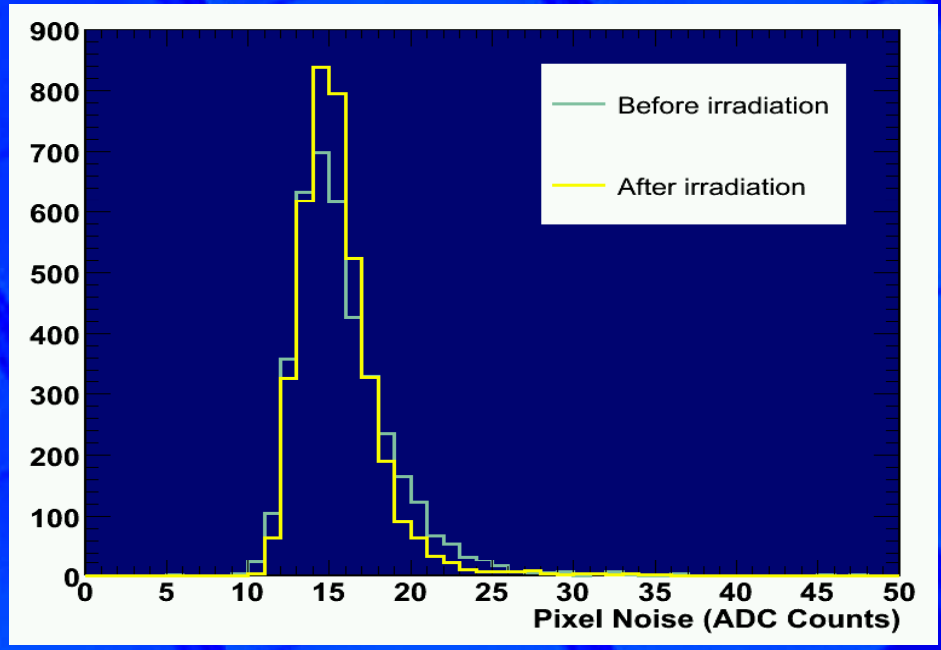


Significant backgating effect observed in single transistor test, expect analog chip section functional for $V_d < 20$ V

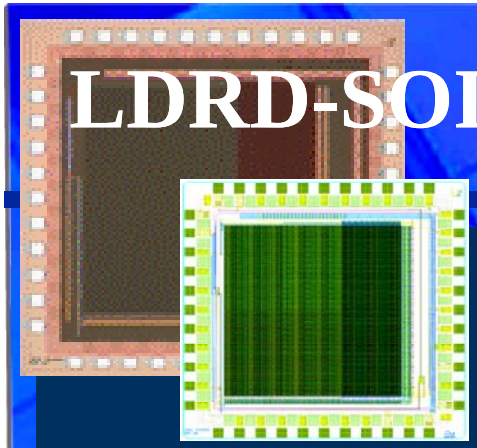


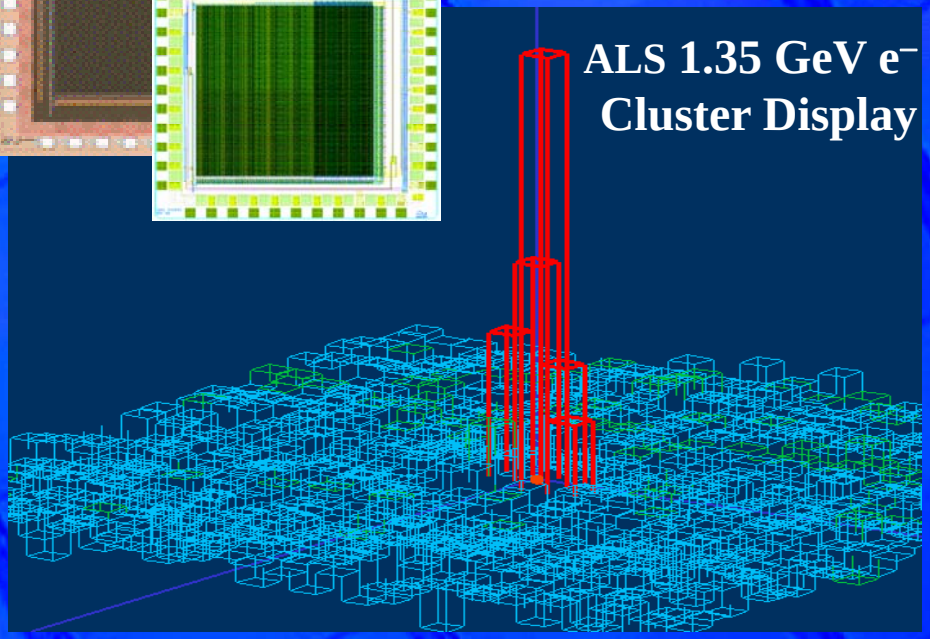
First irradiation performed with 30 MeV protons (2.5×10^{12} **p/cm^2**) show evidence of charge build-up in BOX;

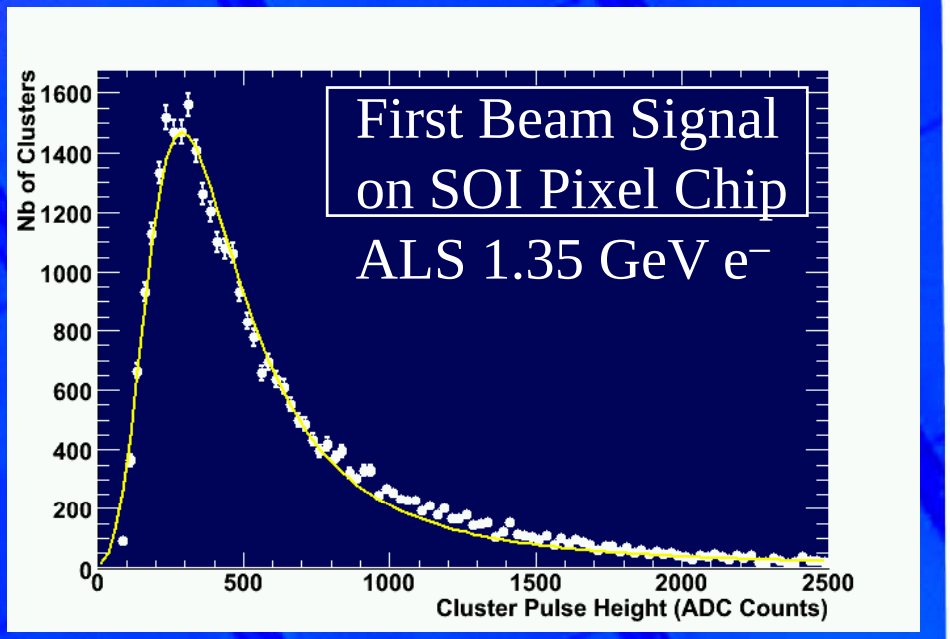
Exposure to 1-20 MeV neutrons (10^{11} **n/cm^2**) shows no appreciable degradation of noise:



LDRD-SOI-1 Analog Pixels: Beam Test



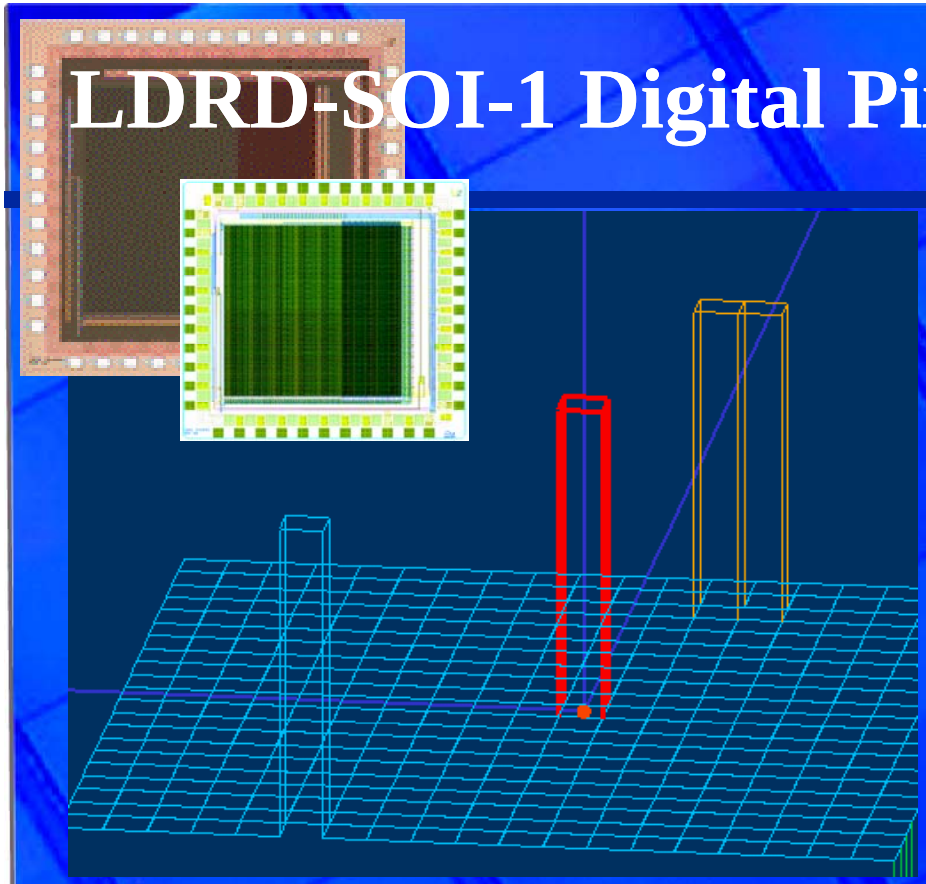


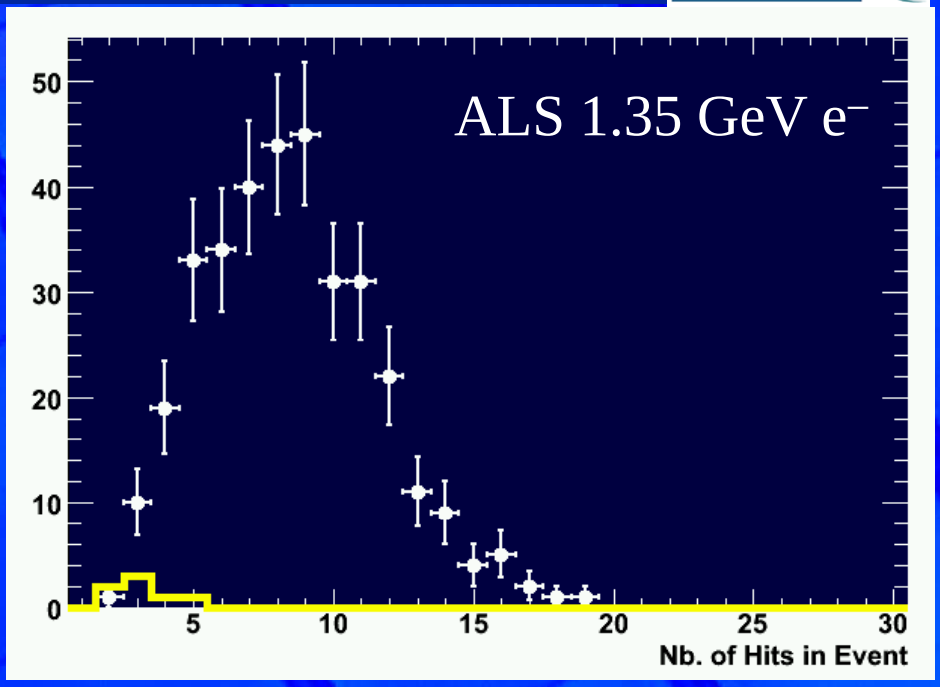


V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>	Signal MPV (ADC)	S/N
1	9.7	0.05	3.31	132	8.9
5	14.0	0.12	3.39	242	14.9
10	7.8	0.20	3.31	316	15.0
15	3.9	0.01	2.45	301	13.6

to appear in NIM A (2007)

LDRD-SOI-1 Digital Pixels: Beam Test

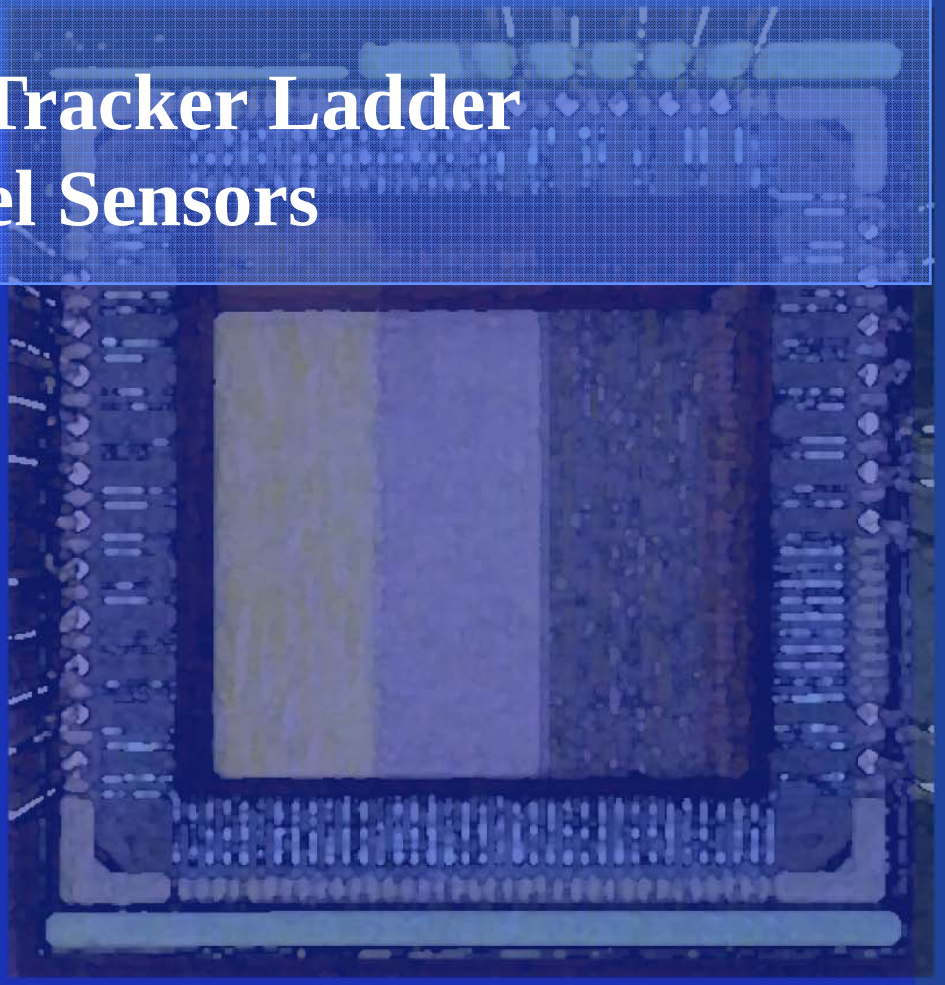


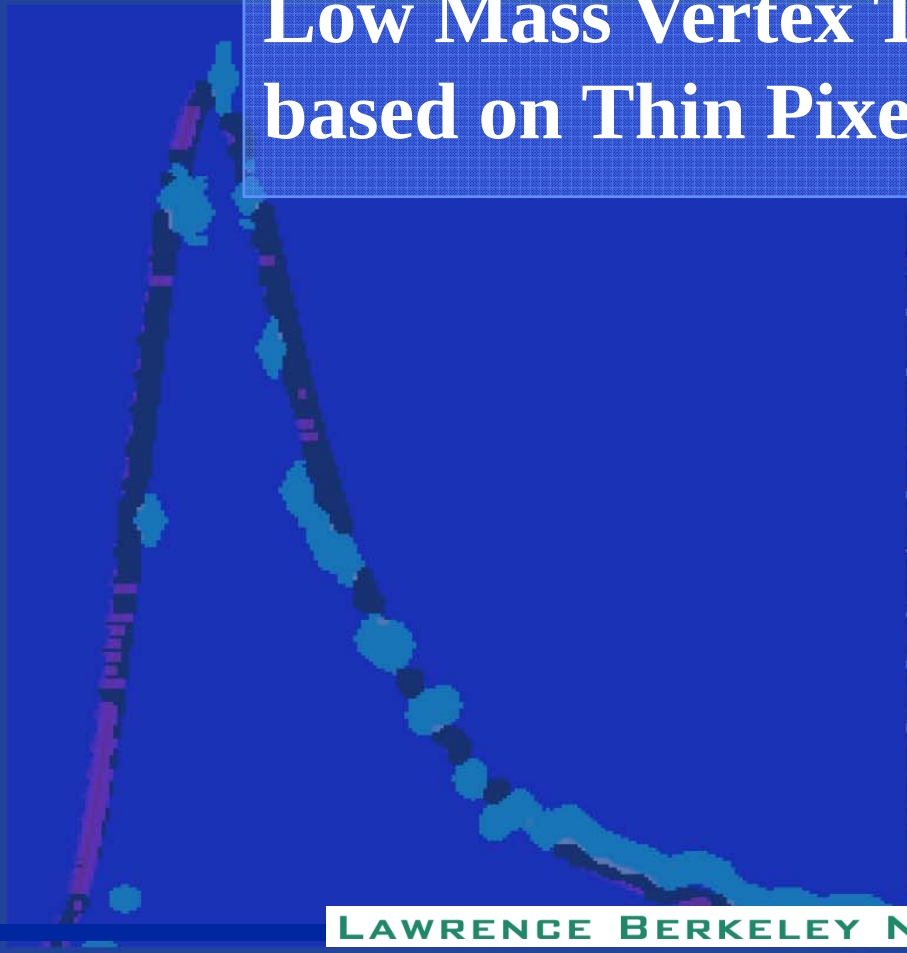


V_d (V)	Clusters/Evt w/ beam	Clusters/Evt w/o beam	<Nb Pixels>
20	3.62	0.04	1.78
25	5.81	0.04	1.32
30	8.31	0.04	1.26
35	1.60	0.01	1.14

Digital pixel consists of 3T + comparator and latch, no internal amplification for minimum power dissipation, total 15 transistors in 10x10μm²

WP-4
Low Mass Vertex Tracker Ladder based on Thin Pixel Sensors





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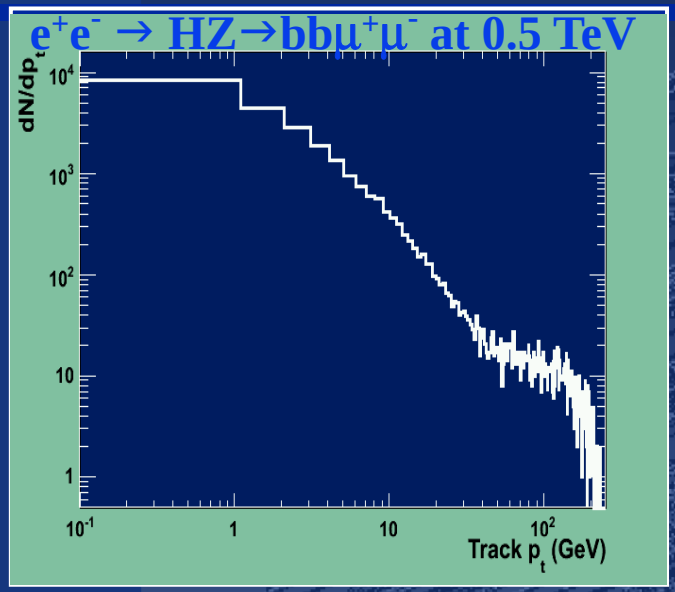
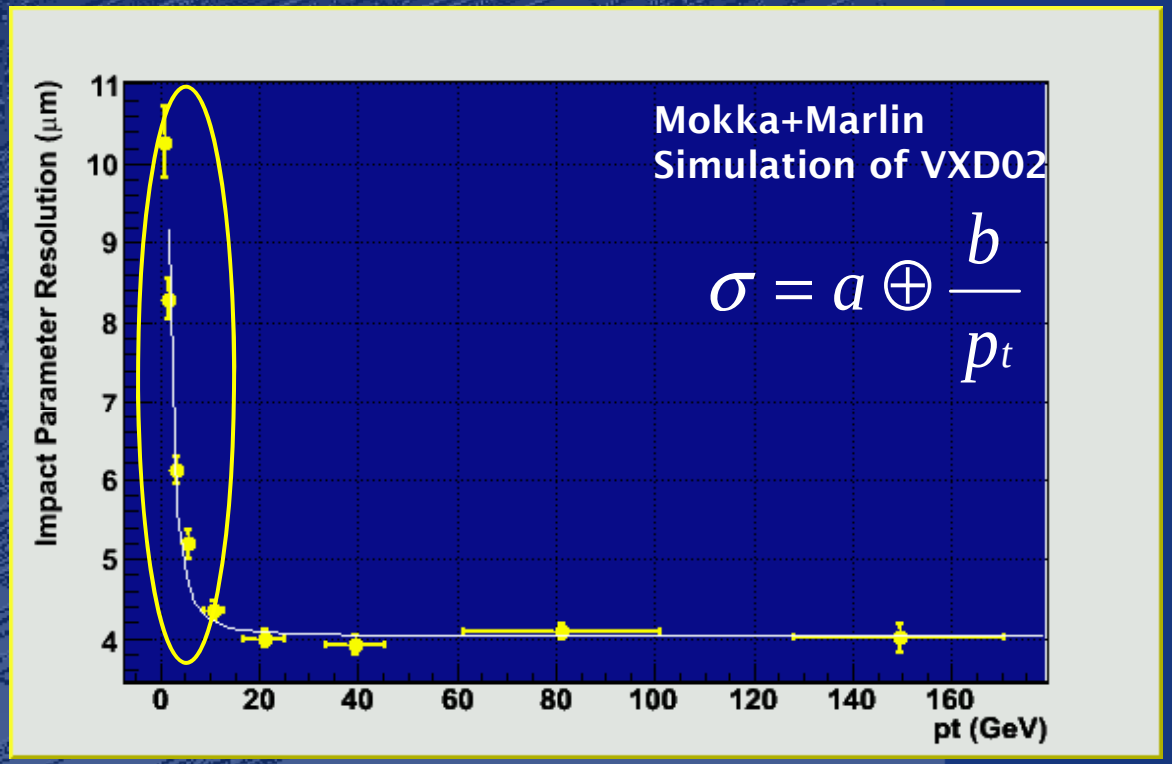
Multiple Scattering and Sensor Thickness



Preserving track extrapolation accuracy to bulk of particles at low momentum requires ultra-thin sensors and mechanical support:

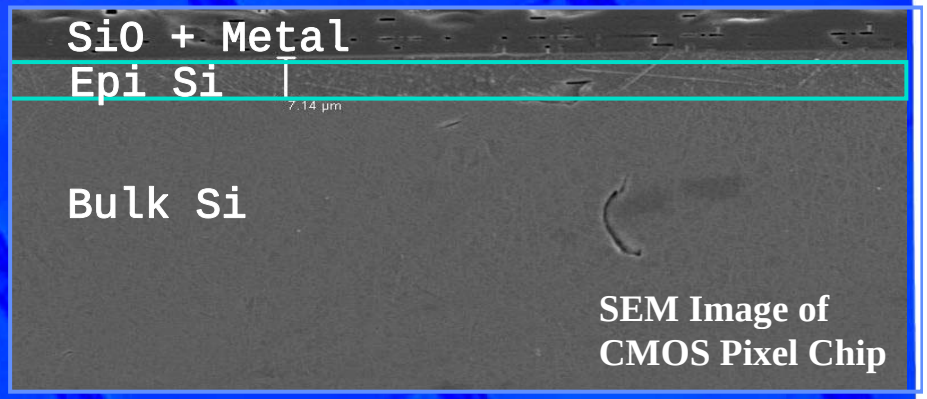


Sensor Thickness μm	a μm	b μm
25	3.5	8.9
50	**3.7**	**9.6**
125	3.8	11.7
300	4.0	17.5

→ need thin monolithic pixel sensor.

CMOS Sensor Back-thinning

Thin sensitive epi-layer makes CMOS Pixel sensors in principle ideally suited for back-thinning w/o significant degradation of performance expected (especially S/N), but questions arise from earlier results;

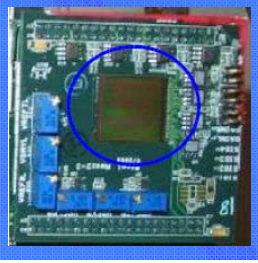


SEM Image of CMOS Pixel Chip

Back-thinning of diced CMOS chips by partner Bay Area company: Aptek.
Aptek uses grinding and proprietary hot wax formula for mounting die on grinding plate:

Backthinning yield ~ 90 %, chip thickness measured at LBNL after processing:
"50 µm" = $(50 \pm 7)\mu m$, "40 µm" = $(41 \pm 6)\mu m$; three chips fully characterised:

Chip mounted on PCB with reversible glue and characterized



Chip removed from PCB

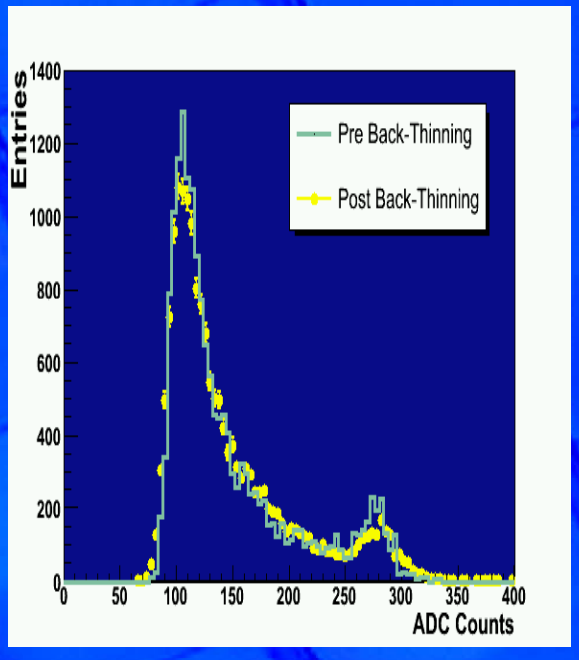
Back-thinning

Chip re-mounted and re-characterized

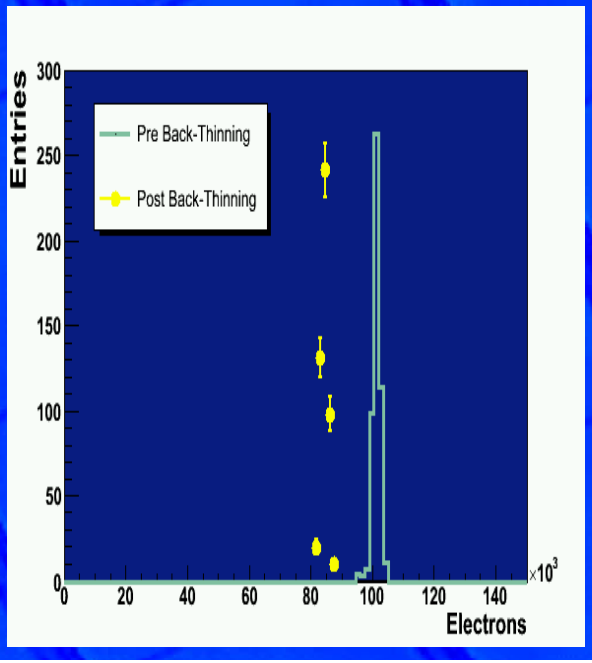
40 μm Back-thinned Sensor Tests

Study change in charge collection and signal-to-noise before and after back-thinning:
Mimosa 5 sensors (IPHC Strasbourg), 1 M pixels 17 μm pitch, 1.8x1.8 cm² surface

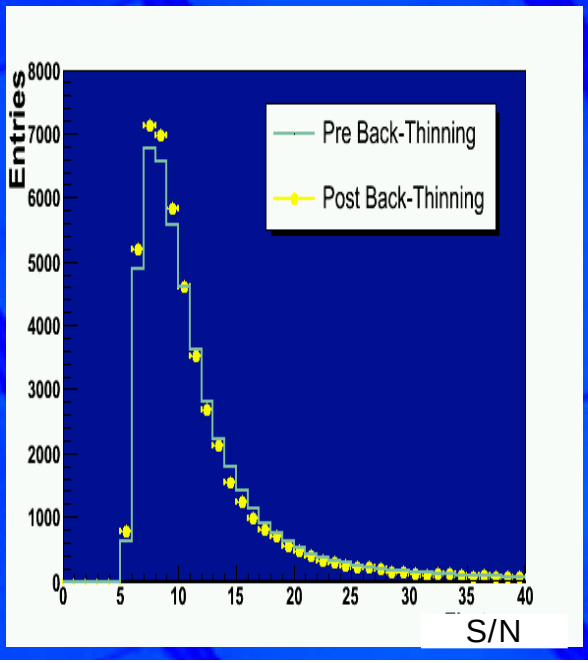
^{55}Fe
Determine chip gain and S/N for 5.9 keV X rays



Collimated Laser
Compare charge collection in Si at different depths



1.5 GeV e⁻ beam
Determine S/N and cluster size for m.i.p.



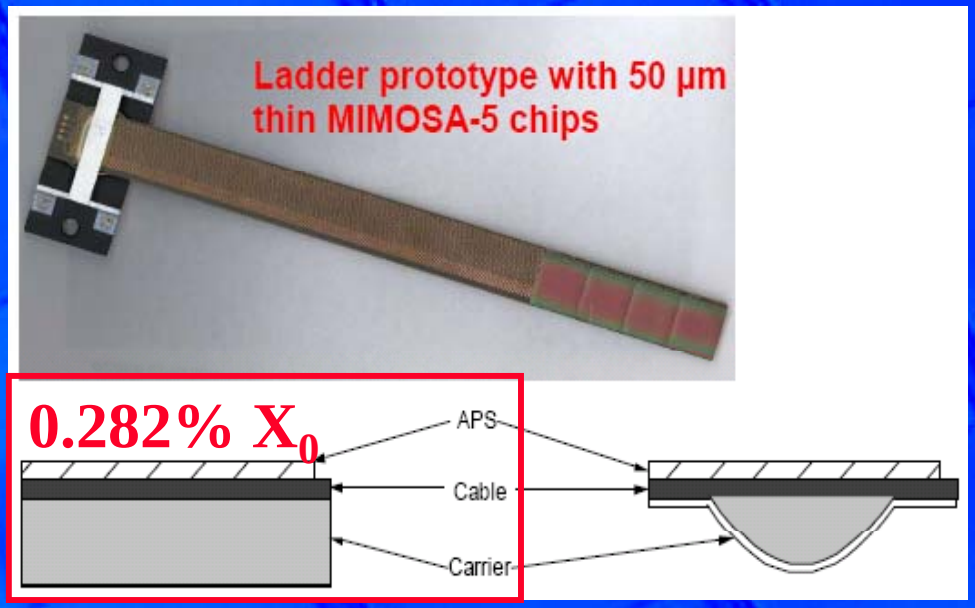
Published in
NIM A579 (2007) 675

CMOS sensors back-thinning demonstrated

VTX Ladder Design & Testing

Program of engineering design, construction and characterization of full ladder equipped with back-thinned CMOS pixel sensors based on experience from STAR HFT project and in collaboration with them;

- STAR Low mass carrier: 50μm CFC+3.2mm RVC+50μm CFC (=0.11%X_0);



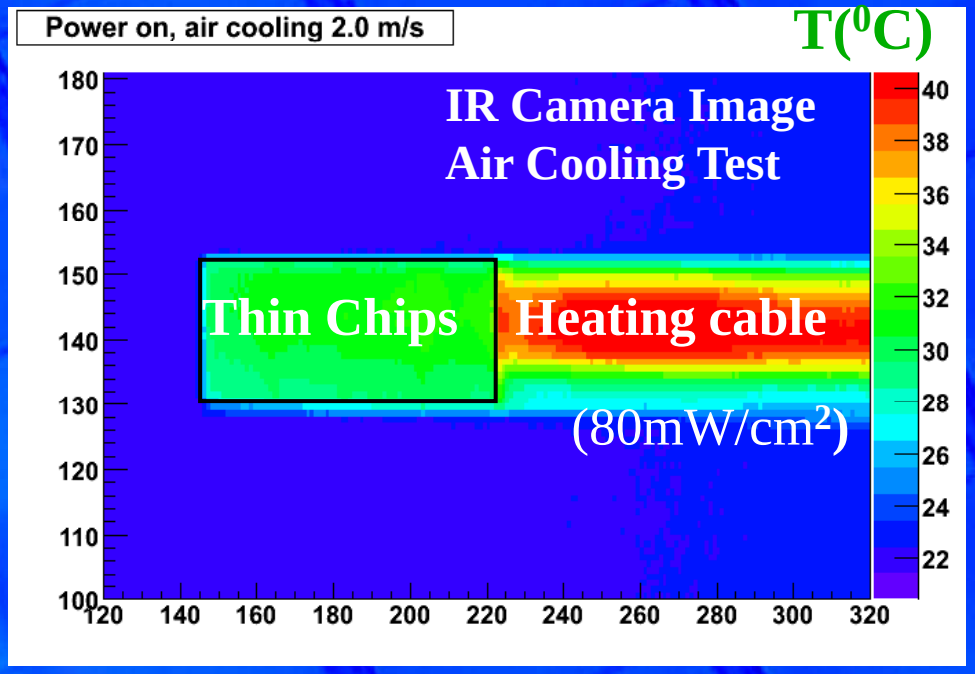
Component	Thickness (% X_0)
Pixel Chip	0.054
Adhesive	0.014
Kapton Cable	0.090
Adhesive	0.014
Carrier	0.110
Total	**0.282**

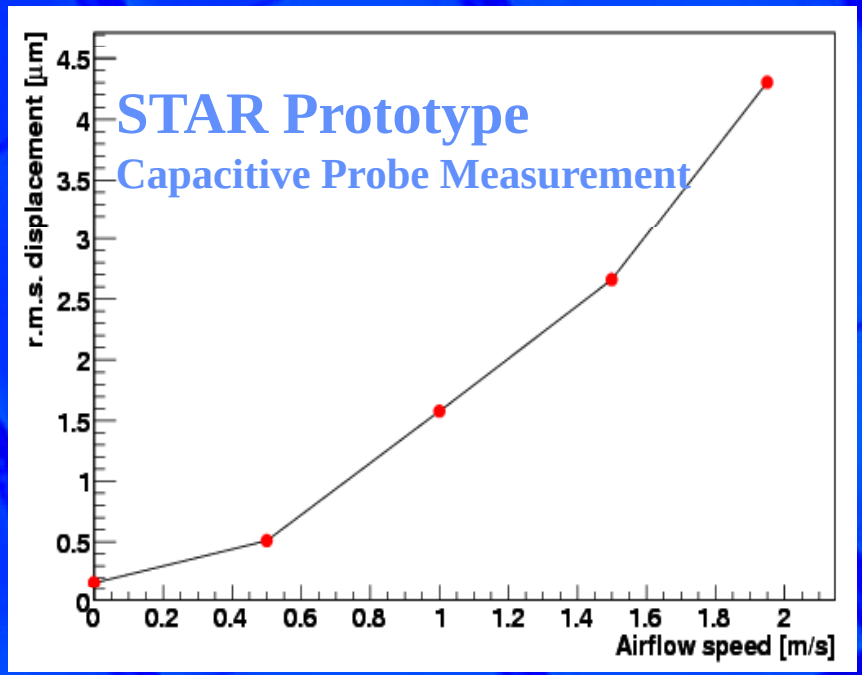
VTX Ladder Design & Testing

Mechanical and thermal characterization of STAR prototype,

study of heat removal using low-speed airflow;

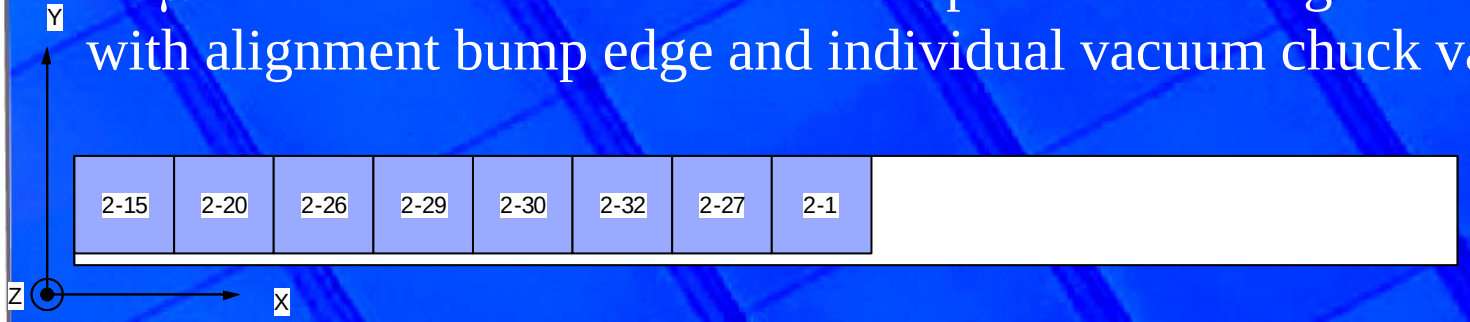
r.m.s displacement on unsupported end of ladder mounted at one end, w/ quasi-laminar airflow at 20^{o} angle



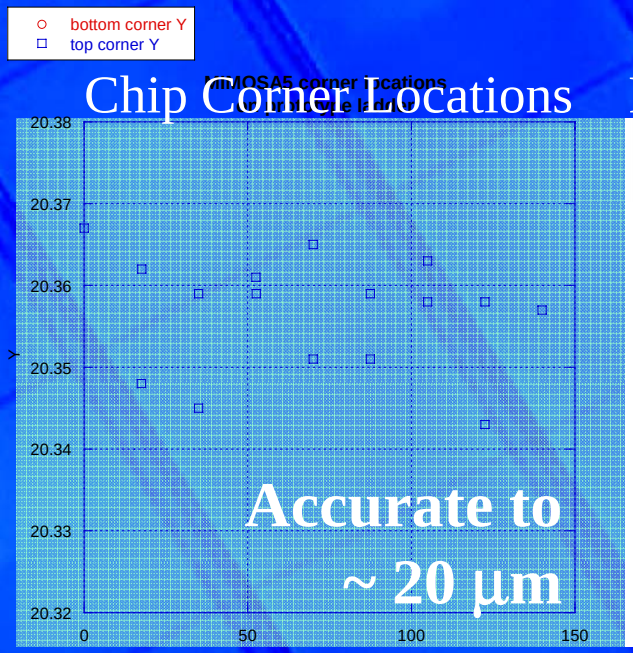


VTX Ladder Design & Testing

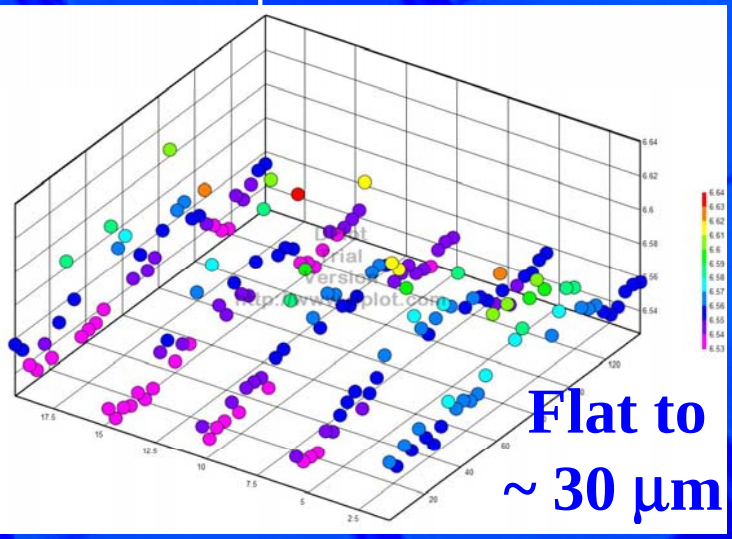
STAR study of accuracy of chip positioning on carrier:
50 μm back-thinned MIMOSA5 are positioned using a vacuum chuck with alignment bump edge and individual vacuum chuck valves;



Chip Corner Locations



Profile of Chip Elevation on Carrier

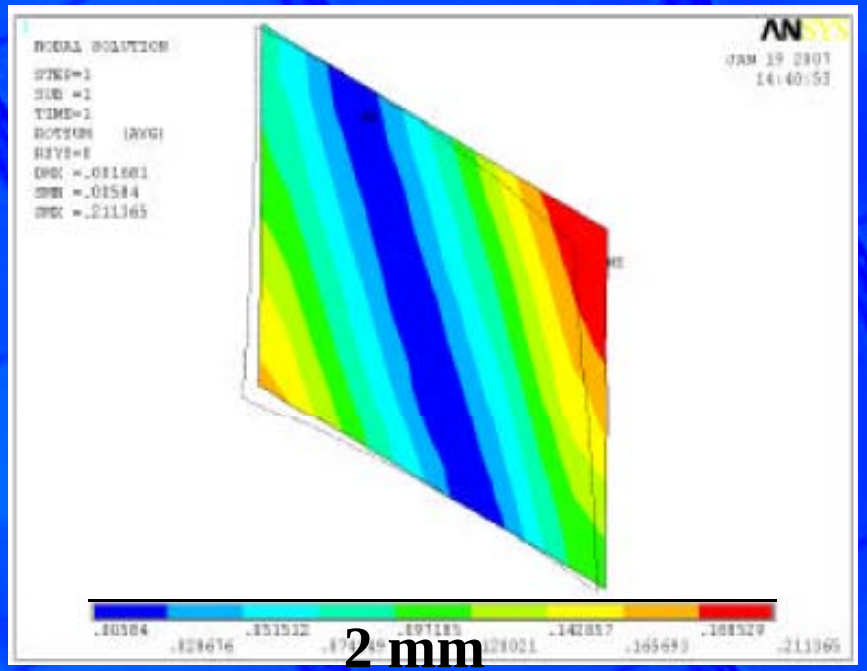


Measurements using Optical Survey Machine with ~ 1 μm accuracy.

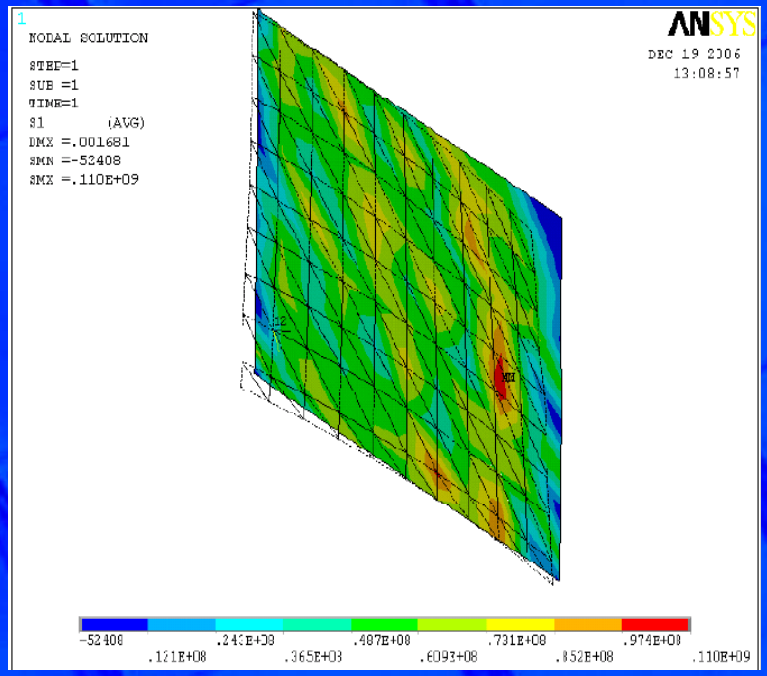
VTX Ladder Design & Testing

- Performed surveys of 40 μm and 50 μm thin chips and FEA analysis of stress on flattened chip, results suggest sandwich ladder design;

Measured Surface Map of 50 μm thin chip



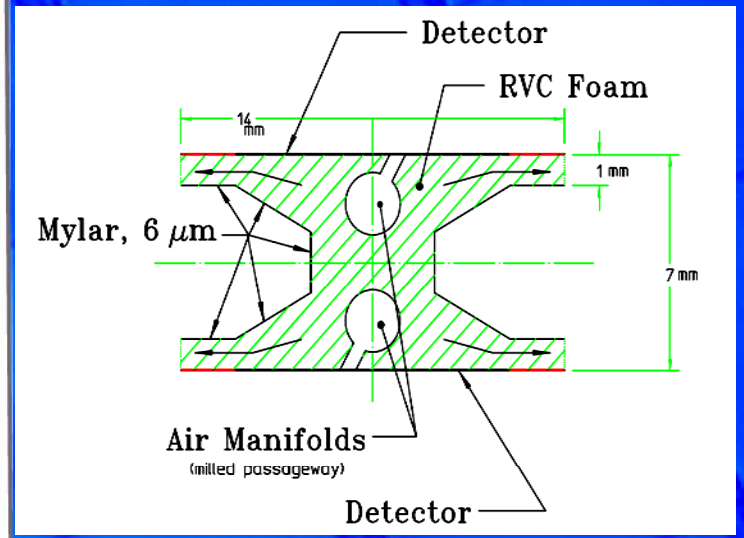
FEA stress analysis of flattened 50 μm chip

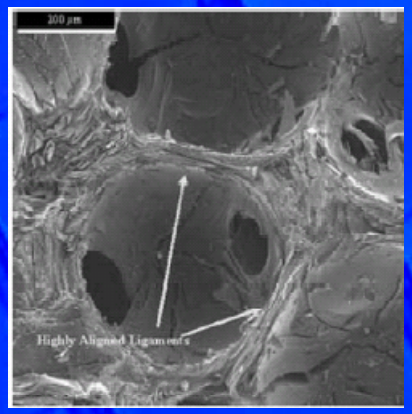


VTX Ladder Design & Testing

- FEA of prototype structures: (core-cooled Si/CF/RVC sandwich, Si/Al/RVC sandwich, CVD coated CF);
- Core-cooled ladder concept is promising, optimisation in progress to move to prototyping in 2008;

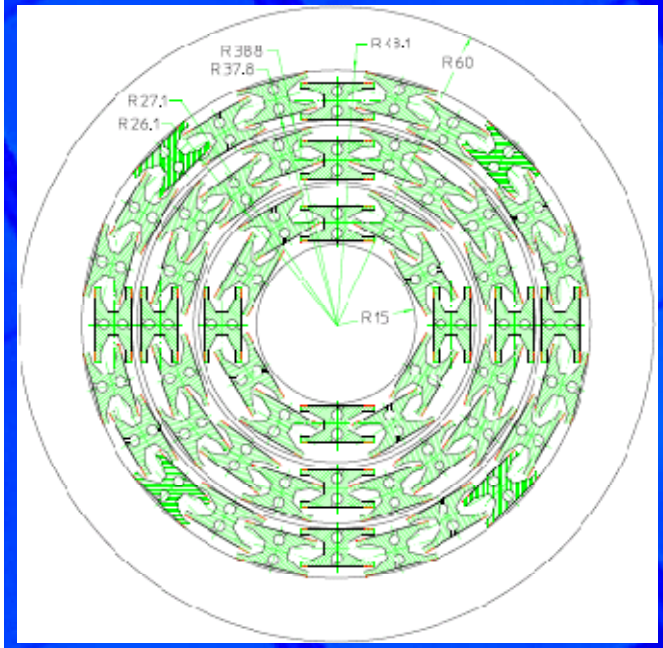
Concept for Symmetric Ladder Sandwich Support with Air Cooling through Core



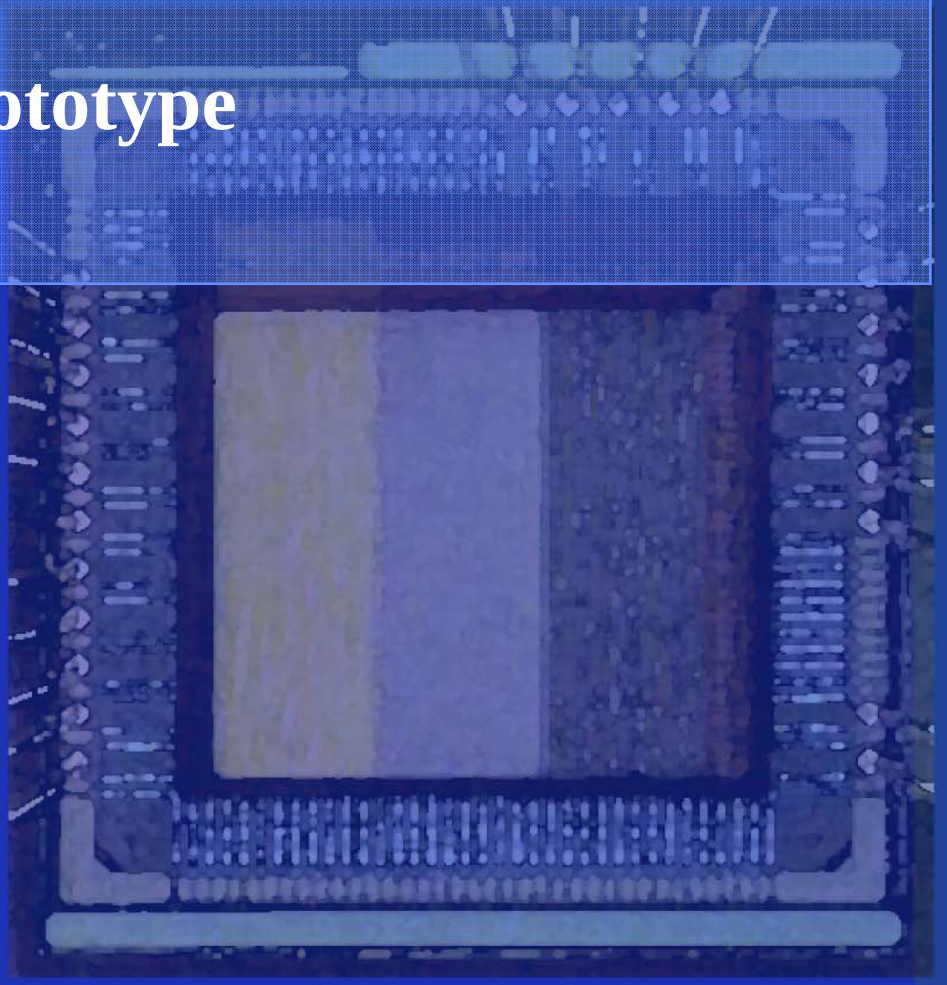


Low density (0.2-0.6 g/cc) high thermal conductivity (40-180 W/m K) foam

Vertex Tracker Design with core-cooled ladders



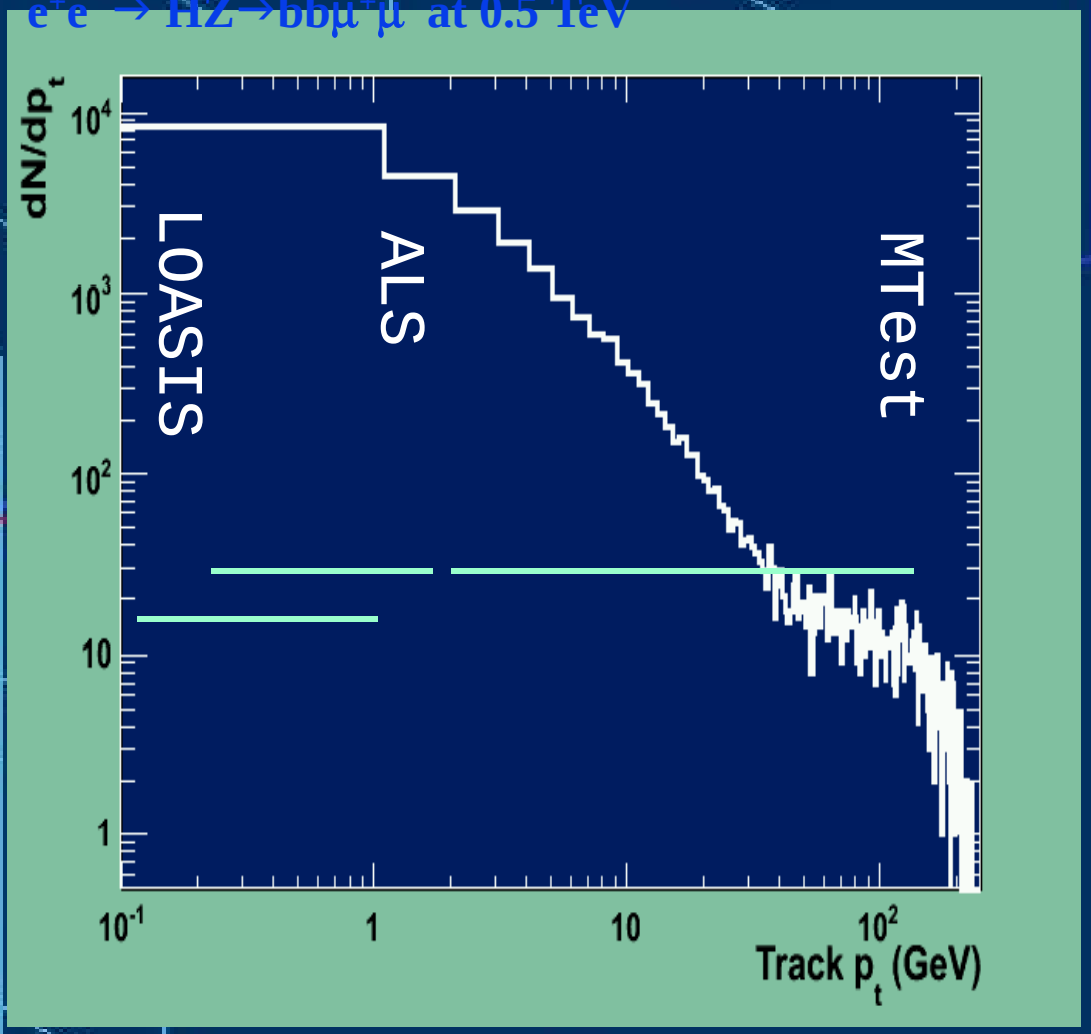
WP-5
Vertex Tracker Prototype



Vertex Tracker Prototype

Study tracking and vertexing over full momentum range relevant to ILC physics with small trackers updated through progress of sensor development and low mass ladder prototyping;

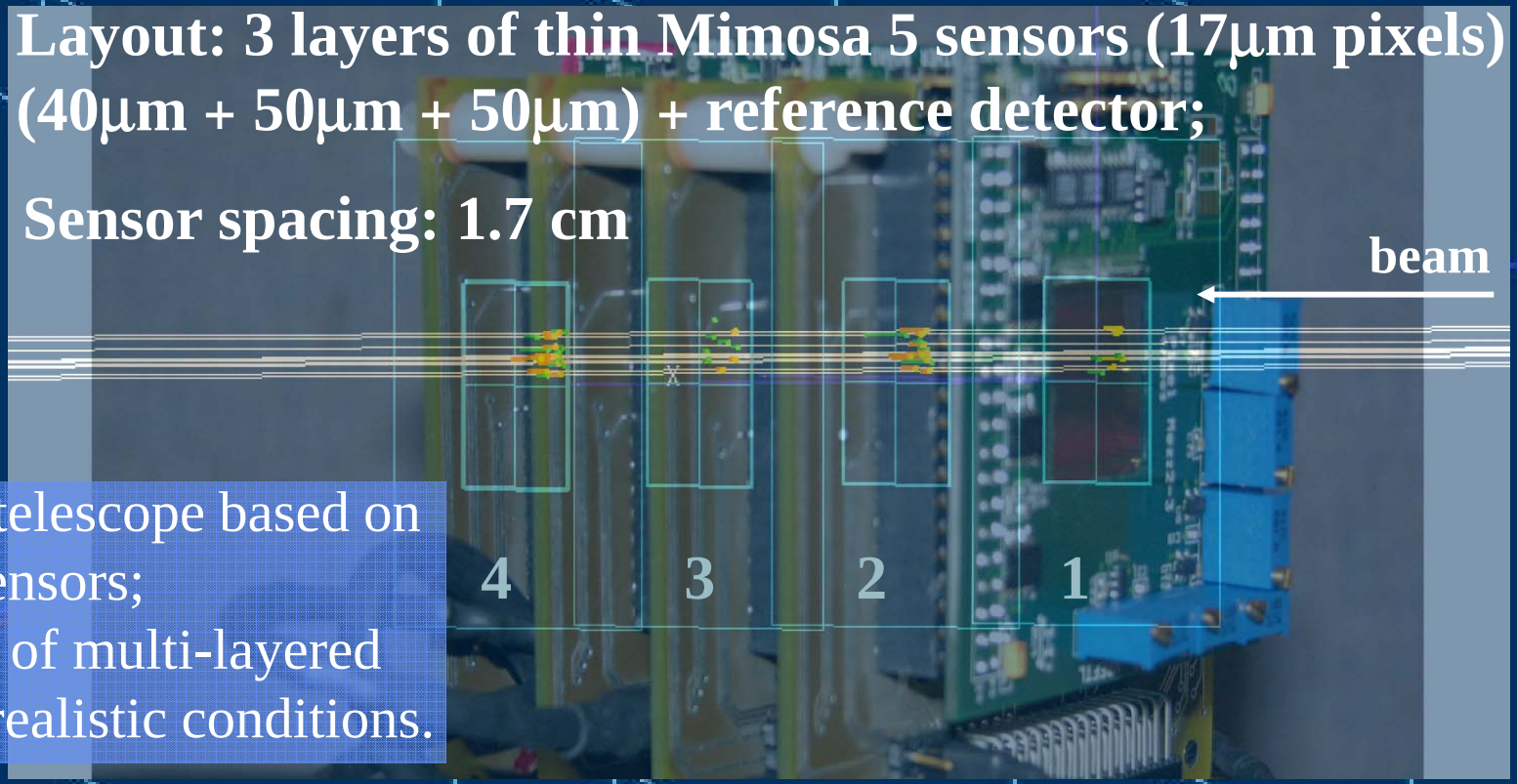
Use combination of accelerators at LBNL and FNAL for beam tests.



Thin Pixel Pilot Telescope

Layout: 3 layers of thin Mimosa 5 sensors (17µm pixels) (40µm + 50µm + 50µm) + reference detector;

Sensor spacing: 1.7 cm



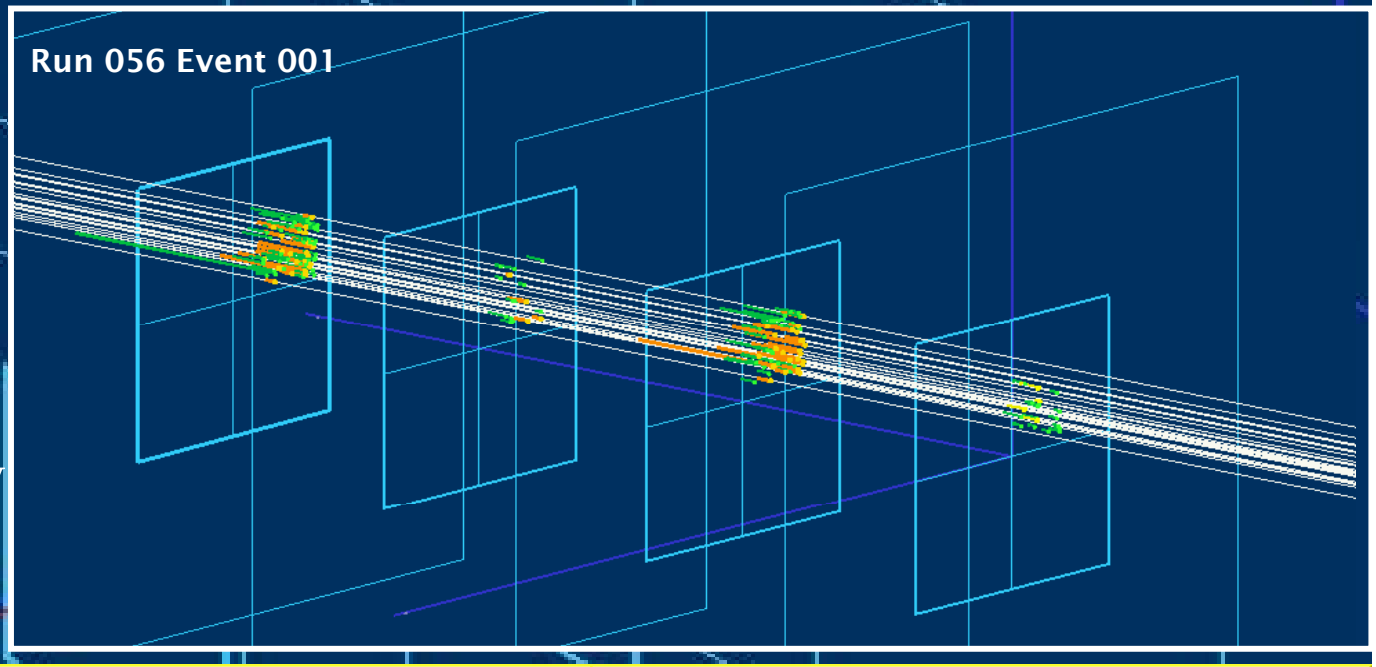
- First beam telescope based on thin pixel sensors;
- System test of multi-layered detector in realistic conditions.

Beam: 1.5 GeV e^- from ALS booster at BTS

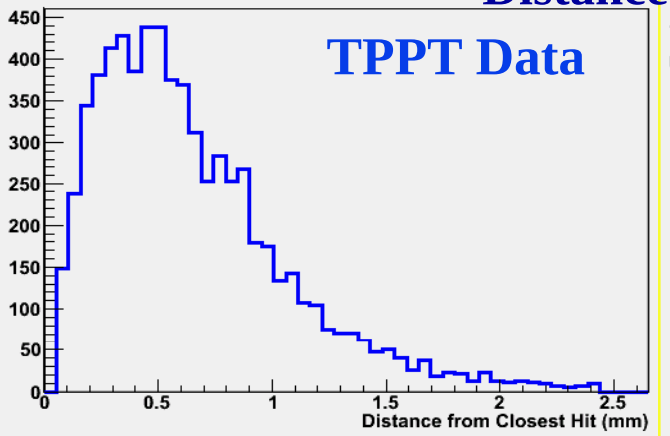
Thin Pixel Pilot Telescope

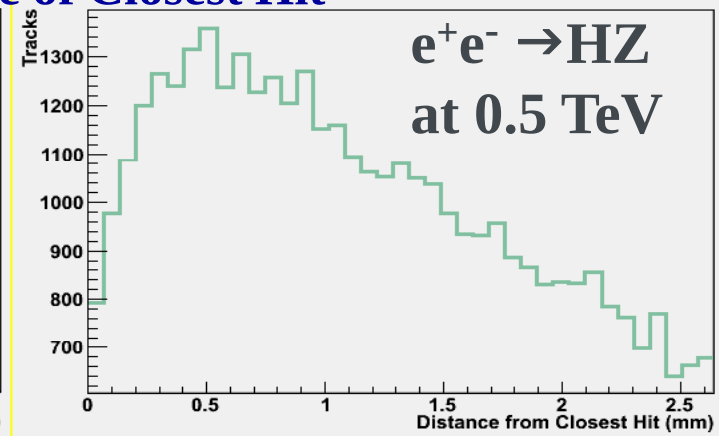
TPPT allows us to perform detailed studies of ILC VTX particle tracking with various, controllable, levels of track density (0.2-10 tracks mm^{-2}) under realistic conditions;

TPPT layout chosen to closely resemble ILC VTX.



Distance of Closest Hit





Thin Pixel Pilot Telescope

Alignment performed using ATLAS optical survey machine and track alignment;

Track Sample	Residual (μm)
2+3 Hits Tracks	9.4
3 Hits Tracks	8.9
High Density	9.5
Low Density	9.2

Extrapolation Resolution on Layer 1: σ = 8.5 μm meets ILC requirements.

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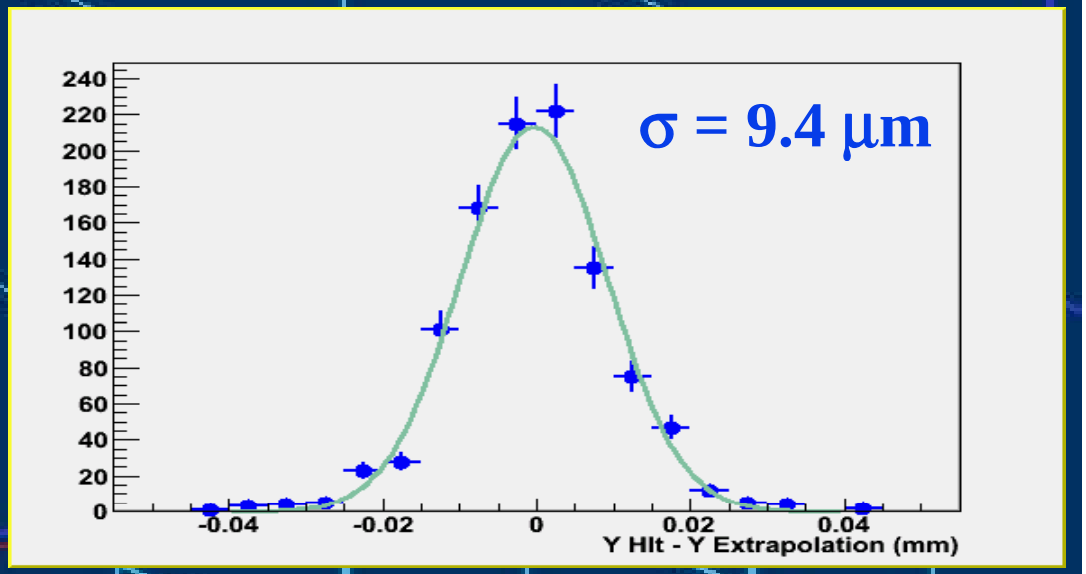
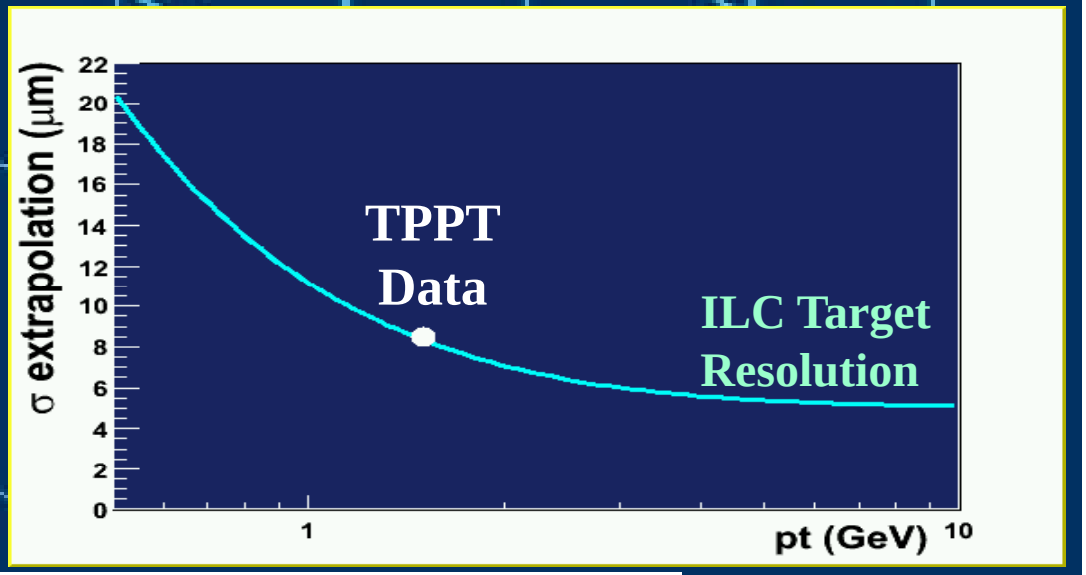


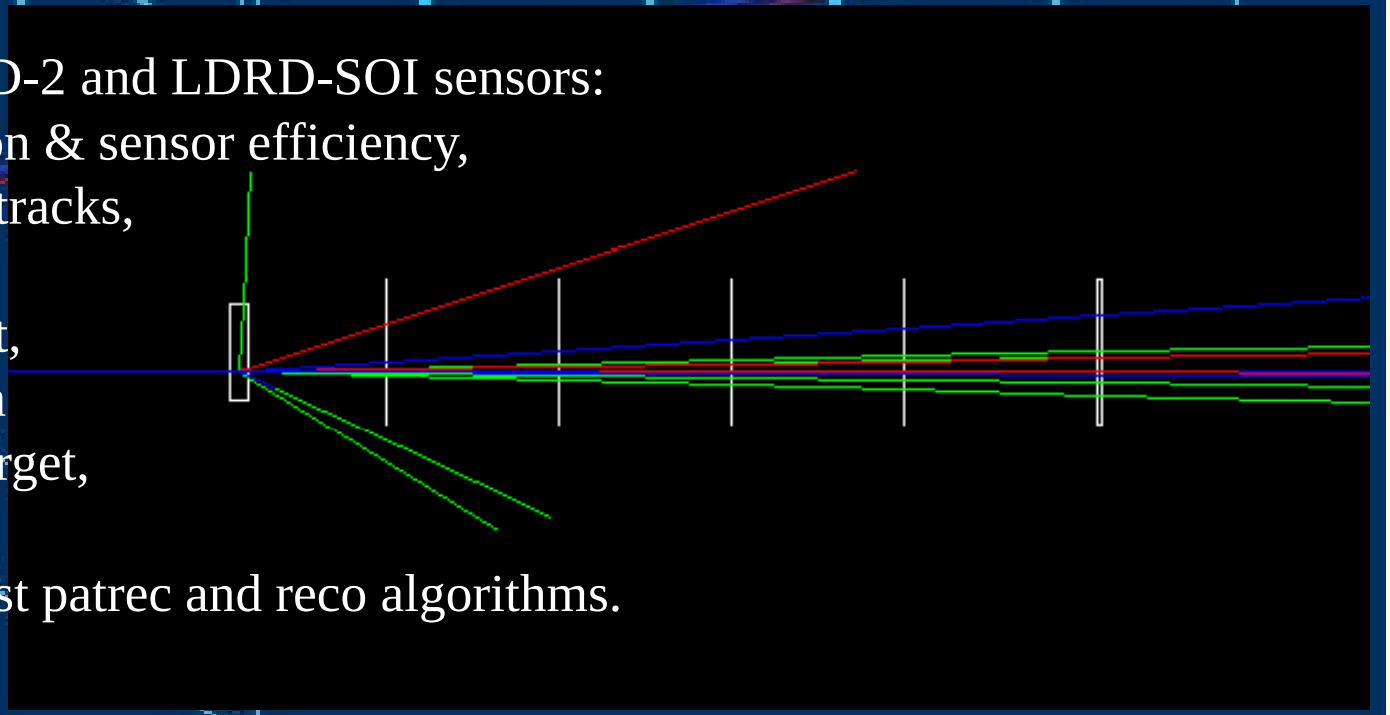


T-966 Beam Test Experiment at Fermilab

Beam Test at FNAL MBTF 120 GeV p beam-line (T-966)
(UC Berkeley + LBNL + INFN, Padova + Purdue U. Collaboration)

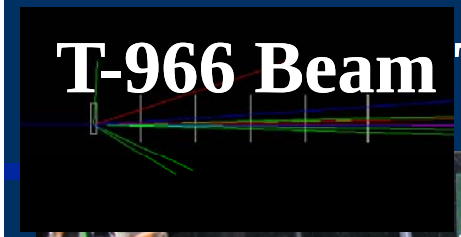
TPPT-2 telescope: 4 layers of 50μm thick MIMOSA-5 sensors,
ILC-like geometry, extrapolation resolution on DUT ~ 2-3 μm

Study LDRD-1, LDRD-2 and LDRD-SOI sensors:
- single point resolution & sensor efficiency,
- response to inclined tracks,
- tracking capabilities in dense environment,
- vertex reconstruction accuracy with thin target,



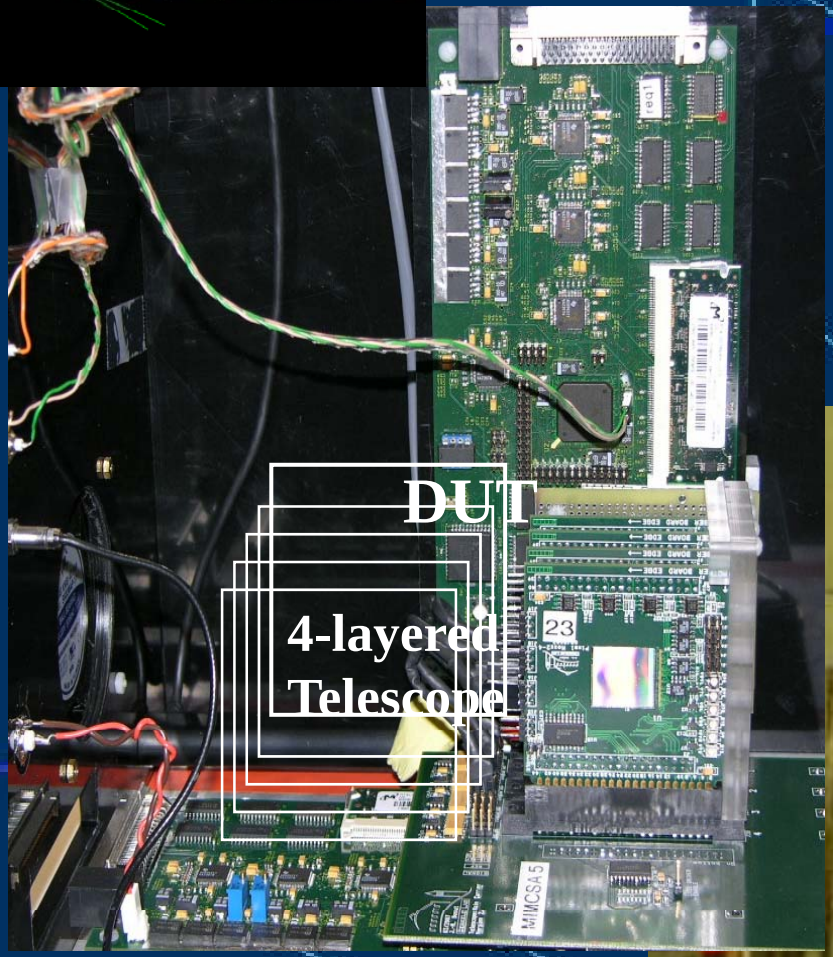
Validate simulation, test patrec and reco algorithms.

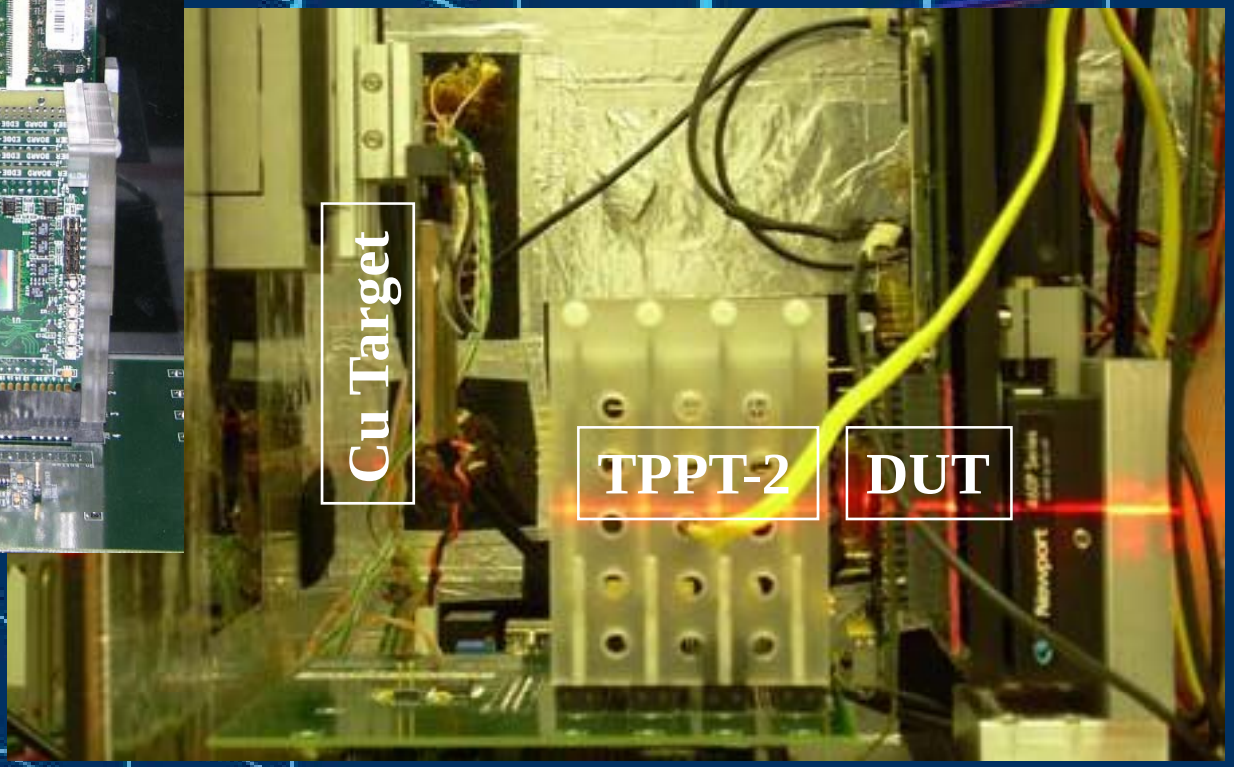
T-966 Beam Test Experiment at Fermilab



Experimental Setup

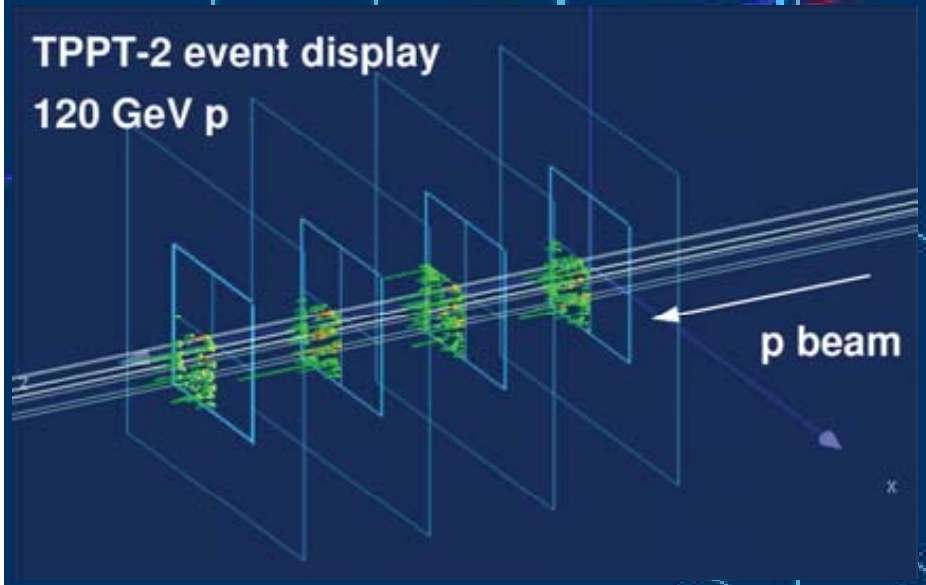
4 layers of 50μm thick MIMOSA-5 chips precisely mounted on PC boards with cut through below chip, DUT on XY stage, finger scintillator coincidence for trigger

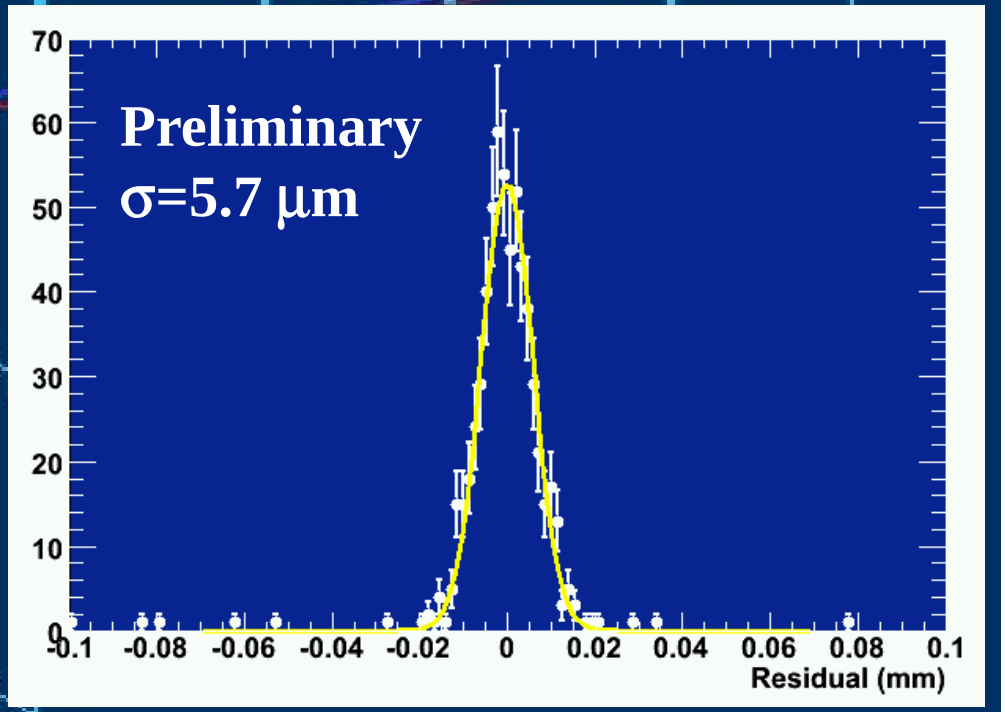




T-966 Beam Test Experiment at Fermilab

First run June-July 2007: collected good statistics in various configurations: TPPT only for alignment & tracking studies, w/ LDRD-2 as DUT, w/ target; Operated at 20ºC through forced cold air cooling, significant day/night temperature effects, need repeat track alignment daily, data analysis in progress, first preliminary results on TPPT performance:



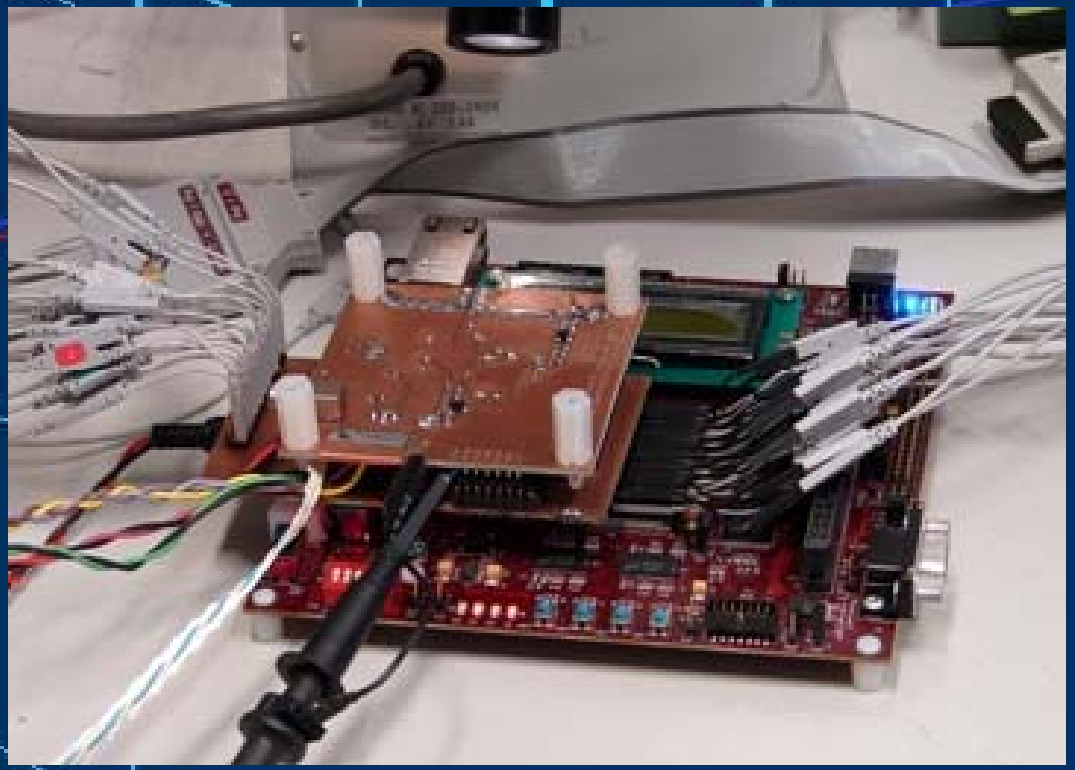


Thin Pixel Pilot Telescope: DAQ

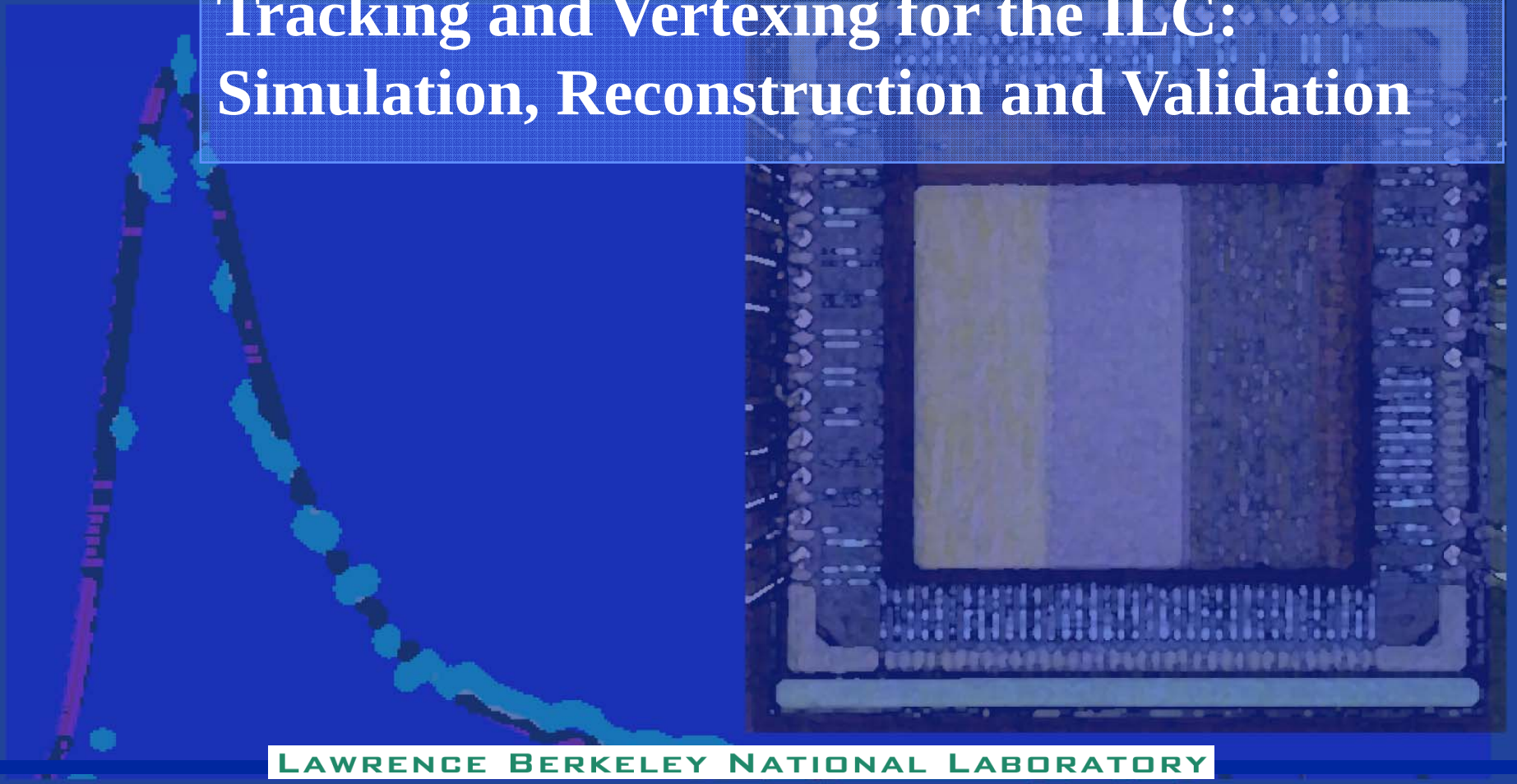
Development of new DAQ system based on commercial Xilinx Virtex-5 development board with Ethernet and USB-2 ports, 64 MB SRAM + custom ADC card with 5 14-bit ADCs 100 MS/s (developed by INFN Padova);

ADC board under test, obtained < 100 μV noise over twisted pairs;

USB driver developed for data bandwidth 50 Mb/s; Firmware under development in collaboration with STAR; Linux/ROOT based online sw.



WP-6
Tracking and Vertexing for the ILC: Simulation, Reconstruction and Validation



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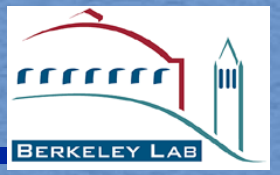
From Sensor Simulation to Physics Analysis



Developing full suite of simulation and recontruction from pixel response to analysis of ILC events at highest energy;

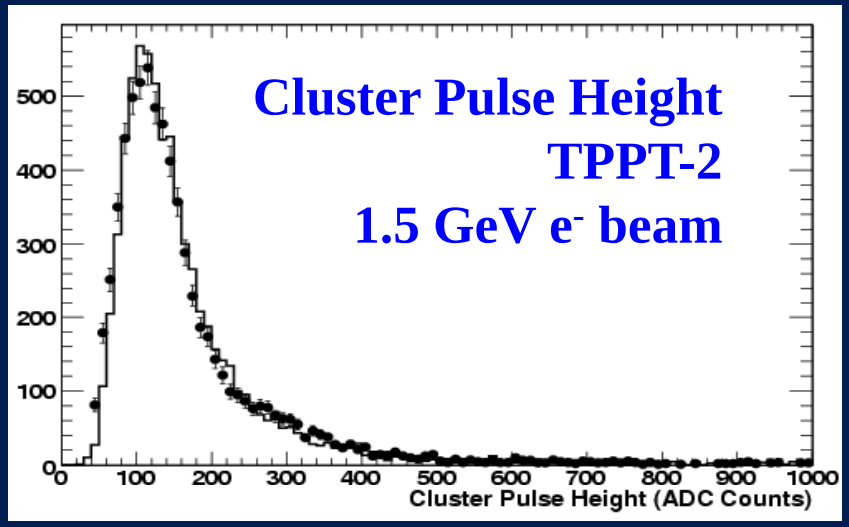
Implemented **sensor simulation** (`PixelSim`) &**cluster analysis** (`PixelAna`) in `Marlin` and interface to `LCIO` for beam test data (`PixelReader`)

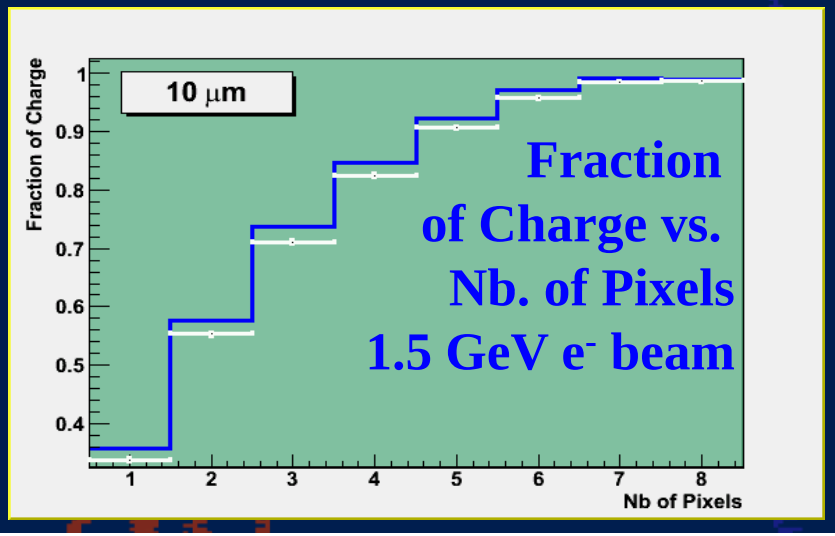
`Marlin` Processors to analyze beam test data and validate simulation response, estimate effect of changes in sensors response and detector geometry and obtain realistic digitized simulation of full physics events and overlayed backgrounds;

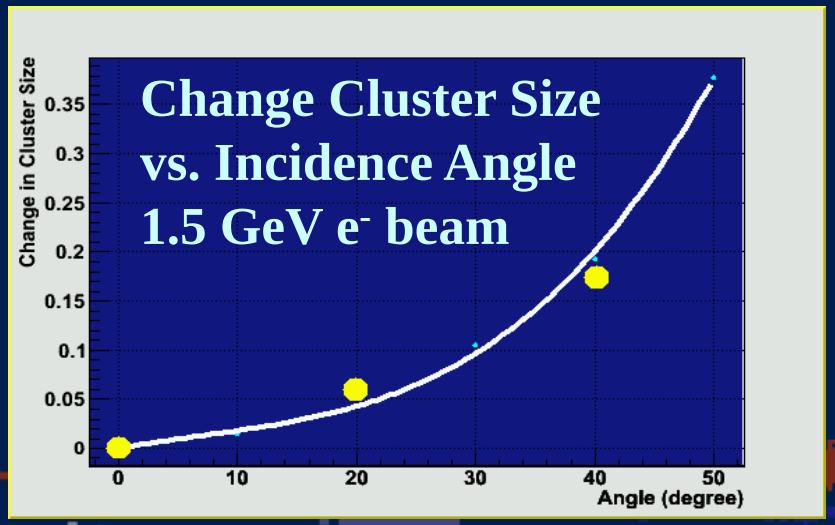
CDF Vertex Fit and b-tagging ported to `Marlin` framework, being tested;

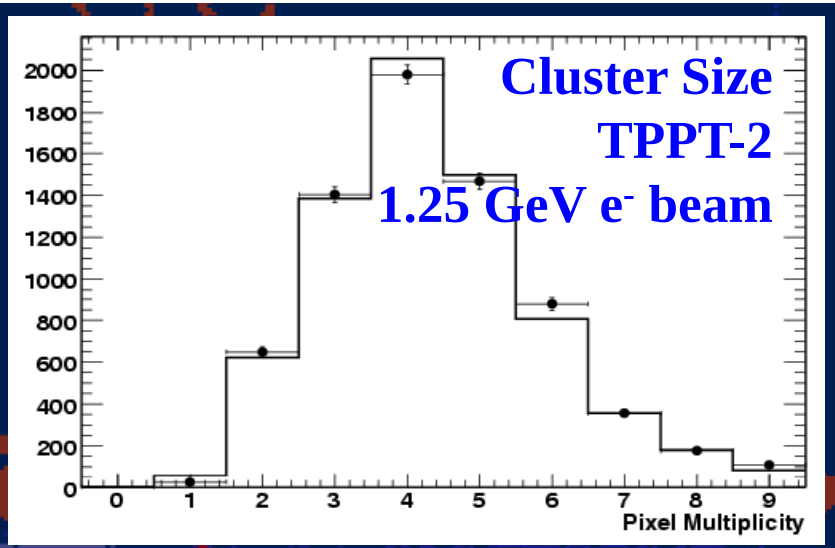
Jet Flavour Tagging and **Physics Analysis** of Dark Matter-motivated SUSY scenarios with fully simulated and digitized VTX currently in progress: physics benchmarking to provide guidance to sensor R&D.

Simulation Validation









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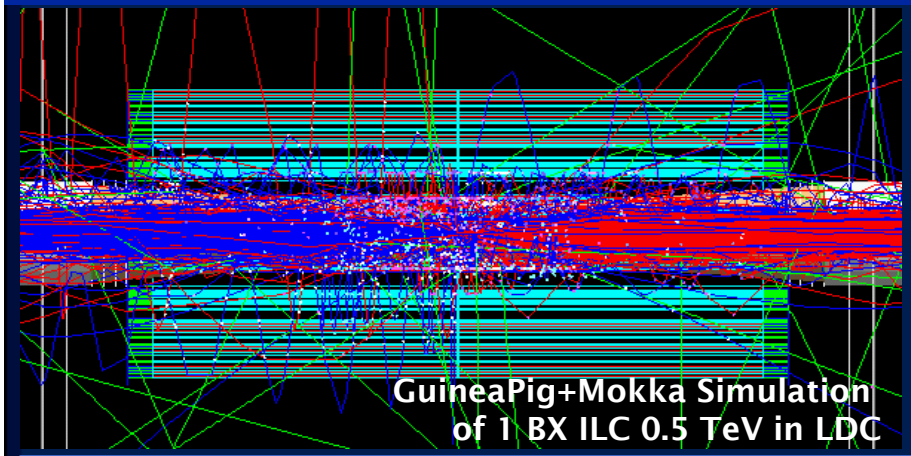
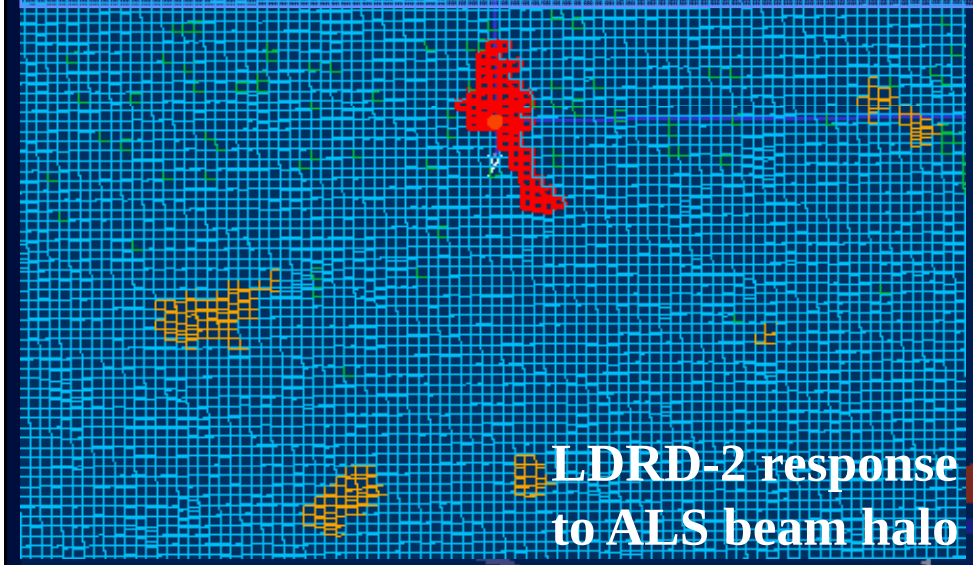
Pair Background Studies at LOASIS



Beam tests using 0.05 - 1.0 GeV e^- beams at **LOASIS** and **ALS** to validate simulation.



Developing design of dedicated user test facility at exit of LOASIS magnetic Spectrometer: dedicated beamline w/ defocusing quad + beam monitor and detector cold box.

Generate library of background pair hits to overlay to hits from physics event and perform detailed simulation of occupancy, rejection and effect on event reconstruction.

Project Funding Sources and Spin-offs

Project Funding

LBNL LDRD Grant: *Advanced Pixel Detectors for the ILC* (FY05-07)
DOE LCRD Grant: *Design of a Monolithic Pixel Detector Ladder* (FY06-07)
PD Core Budget allocated to ILC Project (Sw, Mechanics, CMOS from FY08)
LBNL Strategic Grant: *Detector Test Infrastructures at LOASIS and ALS* (FY08)

External Collaborative Funding

Collaborative effort on SOI and DAQ with INFN Padova, open to other groups

Spin-off Projects

LBNL LDRD Grant: *Advanced Detectors for Beam Monitoring and Imaging at Short Pulse X-Ray and FEL Facilities.* **(FY08-FY10)**

Comparative Study of Performance of LDRD-series CMOS chips and Conventional Film for Electron Microscopy at NCEM (w/ EG, NCEM)