FPCCD Vertex Detector R&D for ILC

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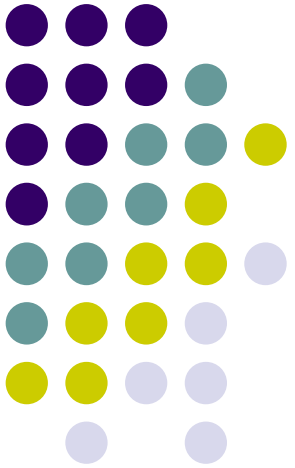
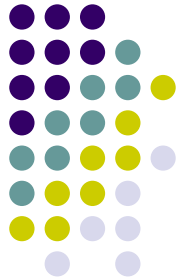
@Vertex Detector Review



Collaboration



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  - A. Miyamoto, K. Nakayoshi, Y. Sugimoto
- JAXA/ISAS
  - H. Ikeda
- Tohoku University
  - T. Nagamine, Y. Takubo, H. Yamamoto
- Tohoku Gakuin University
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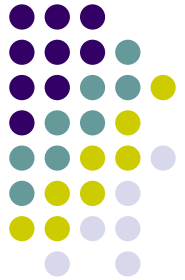
Basic concept (1)

- Pair background at small R
  - ~5000 hits/cm^2/train with B=3T and R=20mm (GLD)
  - Pixel occupancy ~10% for 25μm pixel (several pixels are fired for one track hit) if signal is accumulated for one train
  - In order to keep the occupancy small (<1%),
    - read out 20 times per train (1ms), or
    - 20 times finer pixel ➔ Fine Pixel CCD (FPCCD)

    is necessary

Basic concept (2)



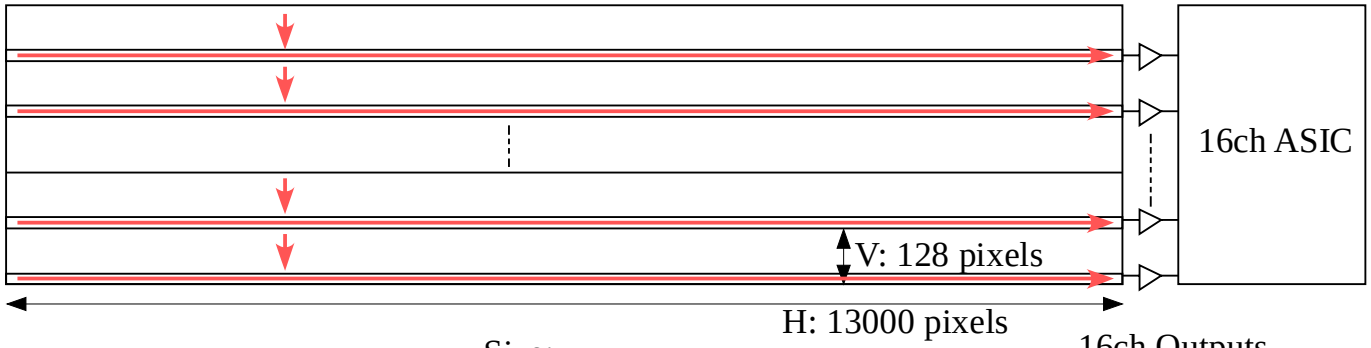
- FPCCD Vertex detector
  - Fine pixel of ~5μm (x20 more pixels than “standard” pixels) to keep low pixel occupancy
  - Fully depleted epitaxial layer to minimize the number of hit pixels due to charge spread by diffusion
  - Accumulate hit signals for one train (2625 BX) and read out between trains (200 ms) → No power cycling
  - Low temperature (~220 K) operation to reduce dark current and to increase radiation tolerance

Advantages of FPCCD VTX

- Completely free from beam-induced RF noise (EMI)
- Excellent spatial resolution of σ_x~1.4μm even with digital readout
- Excellent two-track separation capability because of fine pixels and fully depleted epitaxial layer
- Capability of low-energy pair-background rejection by making use of hit-cluster shape
- Simple structure which enables large wafer size with high yield rate
- No heat source in the image area
- No need for very high readout speed

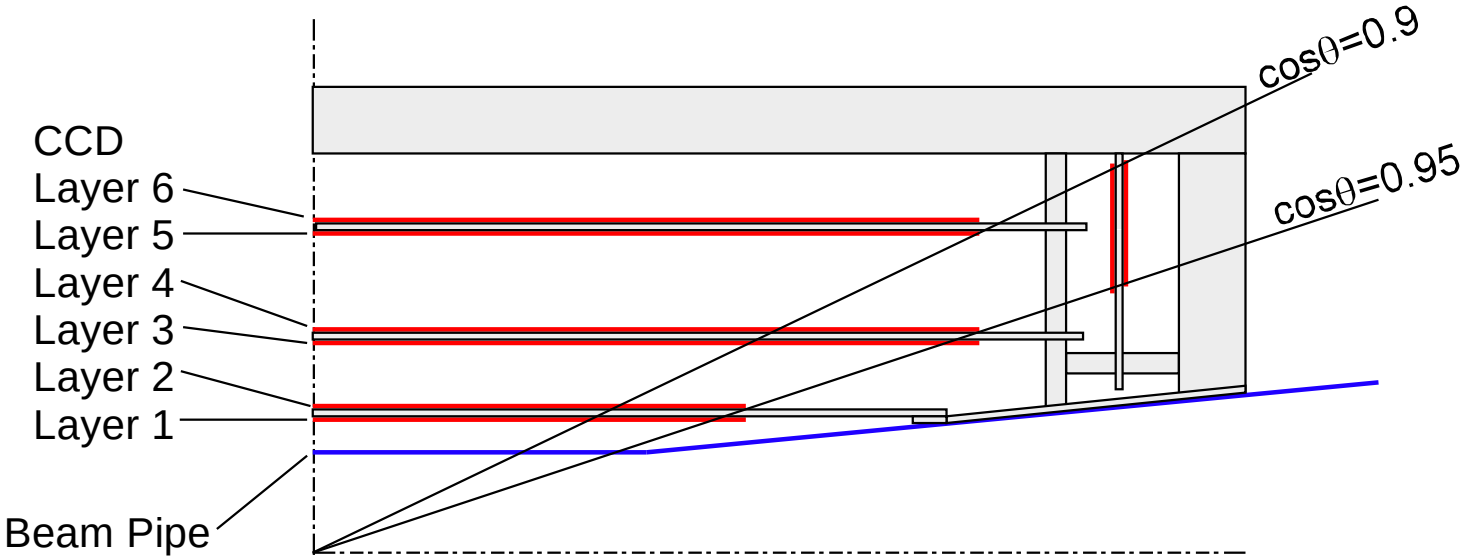
Schematic design (1)

- Sensor and ASIC (for 3T detector – GLD)
  - ~5μm square pixel
  - 128(V)x13000(H) pixels/ch for inner layers
  - 128(V)x20000(H) pixels/ch for outer layers
  - 16ch/wafer for inner layers and 32ch/wafer for outer layers
  - 10x65mm^2 for inner layer and 20x100mm^2 for outer layers
  - 15 – 20 μm thick fully depleted epitaxial layer
  - Readout speed ~ 10Mpixels/s



Schematic design (2)

- Vertex detector
  - Two CCD layers make a ladder
  - 3 ladders make the vertex detector
  - Operation at ~220 K
  - Ladders are confined in a cryostat
  - Angular coverage:
    - $|\cos\theta|<0.9$ with all barrel part
    - $0.9< |\cos\theta|<0.95$ with barrel and forward disk

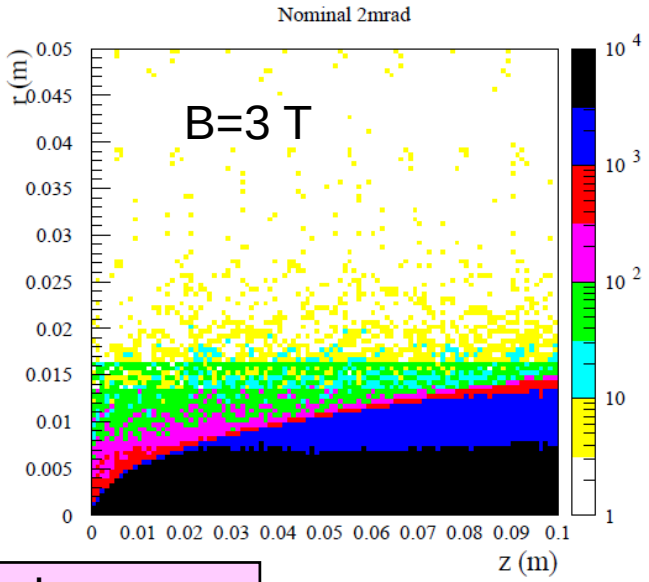


Schematic design (3)

- VTX inner radius
  - Design criteria:

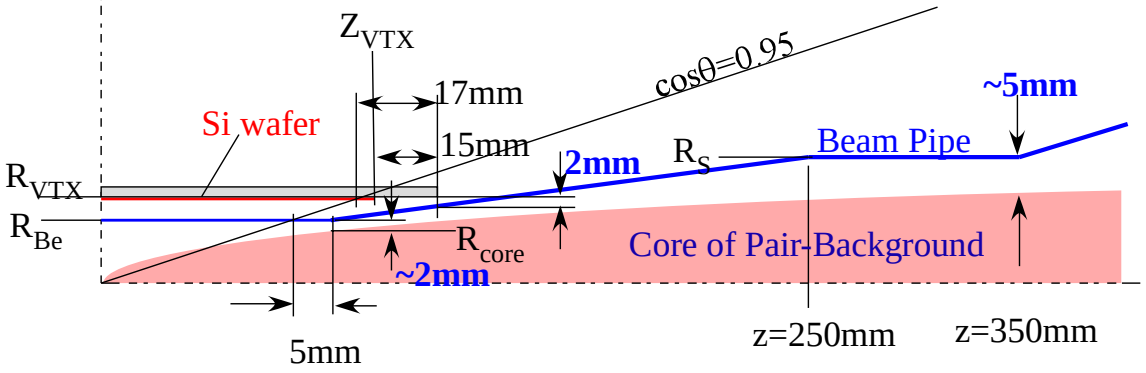
    Beam pipe should not be hit by dense core of the pair background

E_{CM}	Option	R_{bp}	R_{VTX}
500 GeV	Nominal	13 mm	17 mm
1 TeV	High L A1	15 mm	20 mm
500 GeV	High Lum	19 mm	24 mm

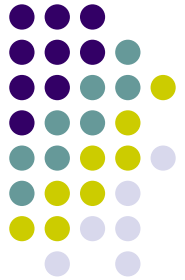


For 3T detector

Strong dependence on machine parameters



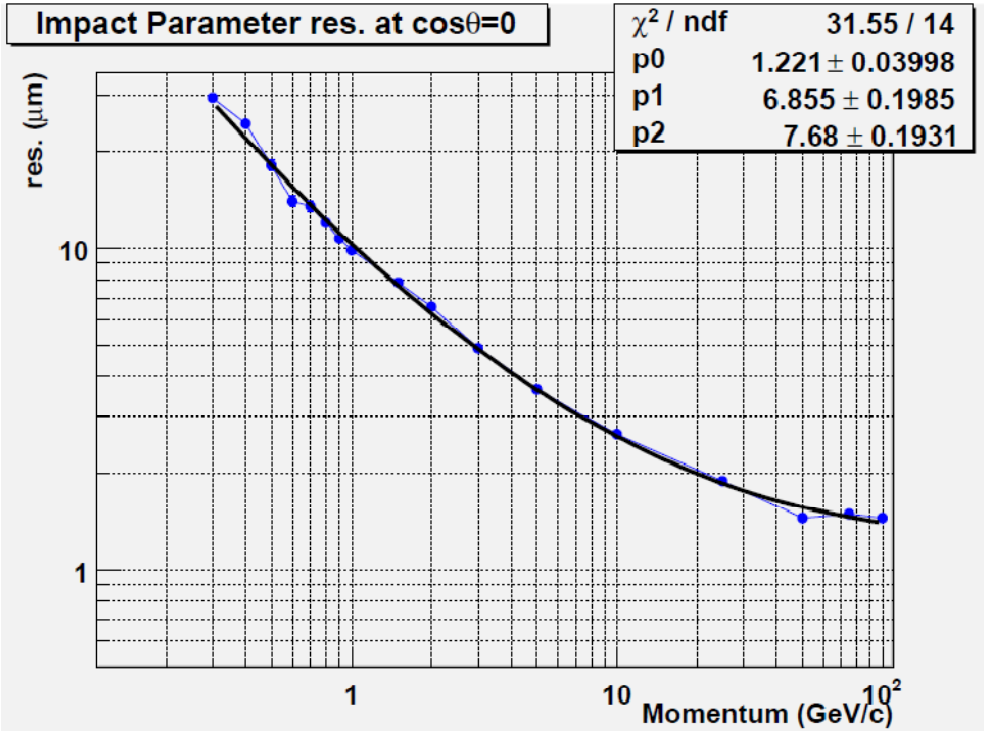
Expected performance (1)



- Simulation model
  - 6 layers of CCD cylinders
    - R=20, 22, 32, 34, 48, 50 mm
    - Beam pipe: R=18mm, t=250μm Be
  - Each layer has 80μm thickness and no ladder material
  - 3T magnetic field
  - GEANT4 based simulator “JUPITER”

Expected performance (2)

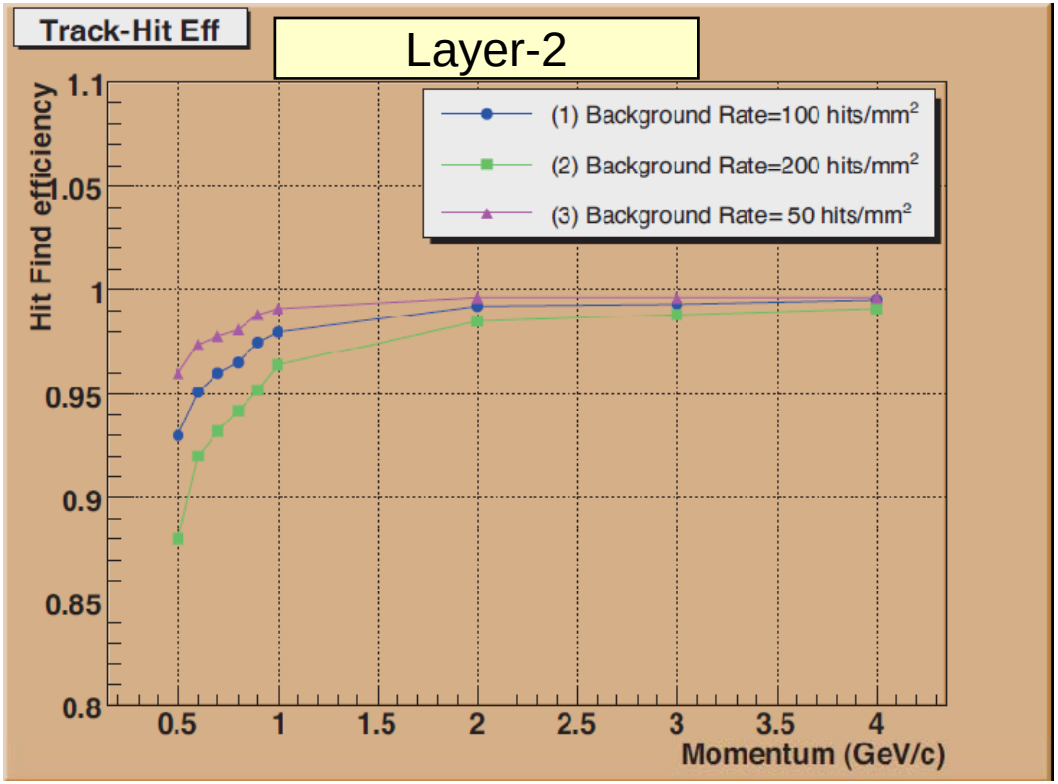
- Impact parameter resolution
  - The result is well fitted with $\sigma = \sigma_0 \oplus \frac{\sigma_1}{p} \oplus \frac{\sigma_2}{p^2}$ rather than $\sigma = \sigma_0 \oplus \frac{\sigma_1}{p}$



Performance goal of $\sigma = 5 \oplus \frac{10}{p}\ \mu\text{m}$ is satisfied

Expected performance (3)

- Track-hit matching efficiency
  - Efficiency of finding the correct hit in the inner layer by extrapolating a track from outer layers in the presence of background hits

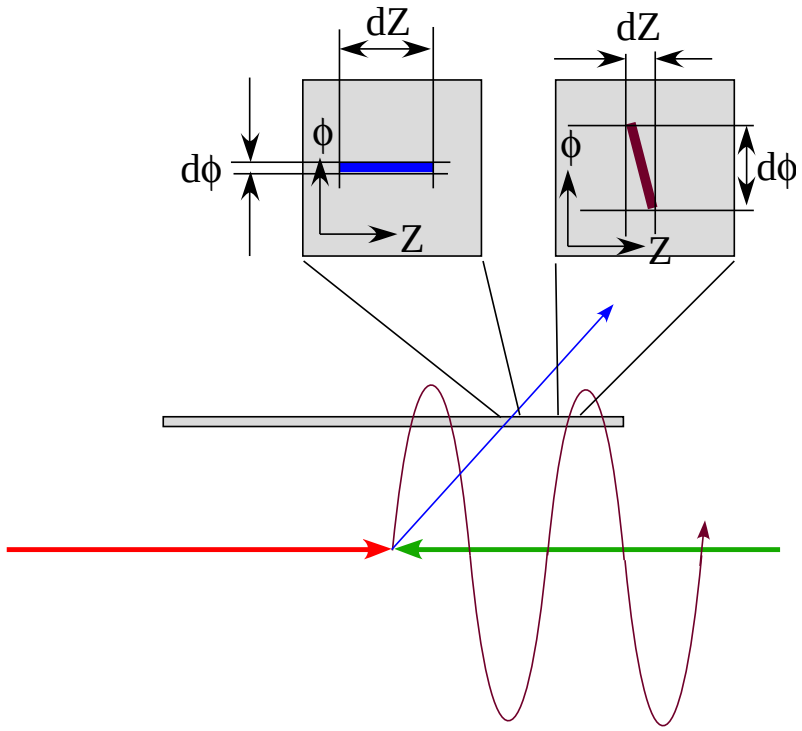


- Improvement is expected by
  - taking correlation of hit points on layer-1 and layer-2 into account (making “mini-vector”)
  - background rejection using hit cluster shape

Further study is necessary

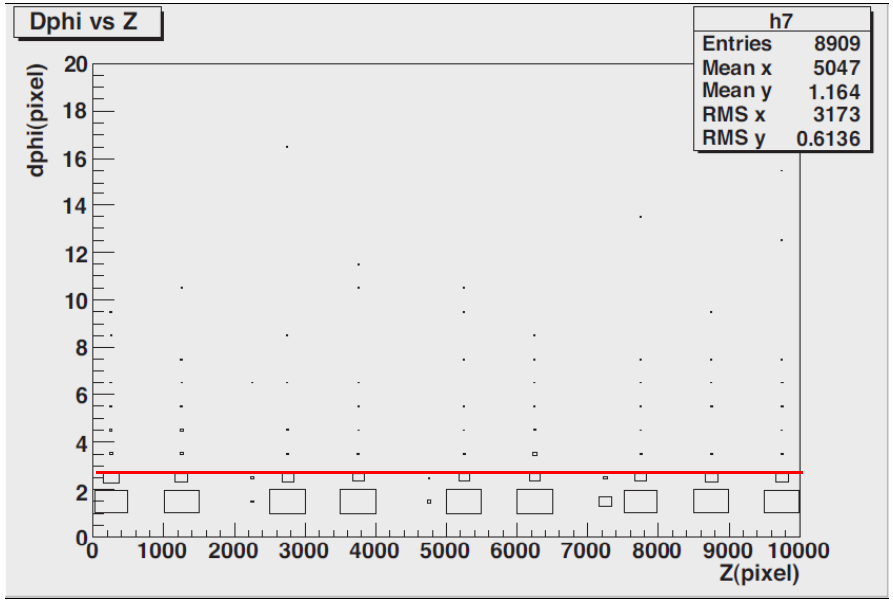
Background rejection

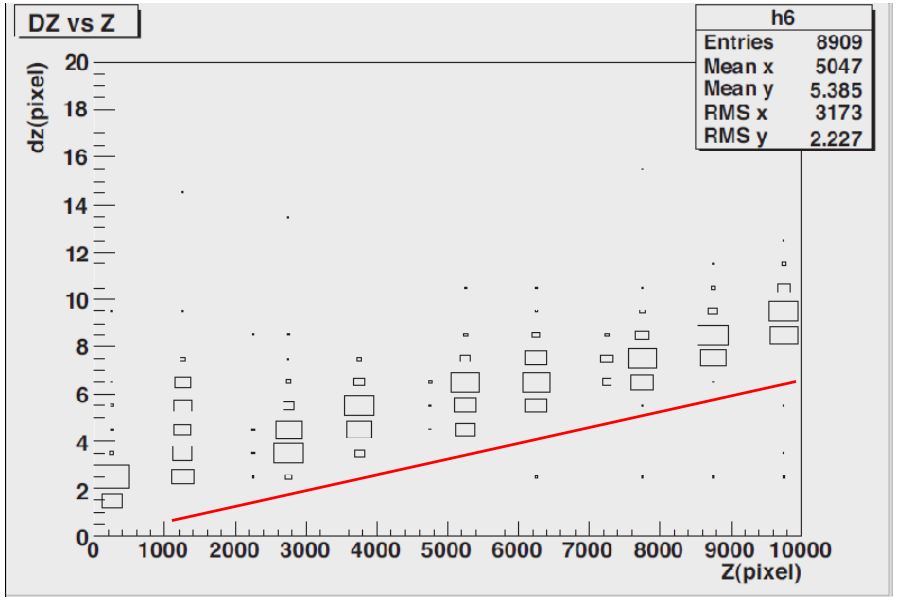
- Background rejection by cluster shape
  - FPCCD has the pixel size smaller than the thickness of the sensitive layer
    ➔ Rough measurement of incident angle can be done with single layer using the cluster shape
  - Pair-background particles have typical momenta of few tens of MeV/c and curvature of few cm, and incident direction is different from that of high p_t particles associated with physics events



Simulation for B.G. rejection(1)

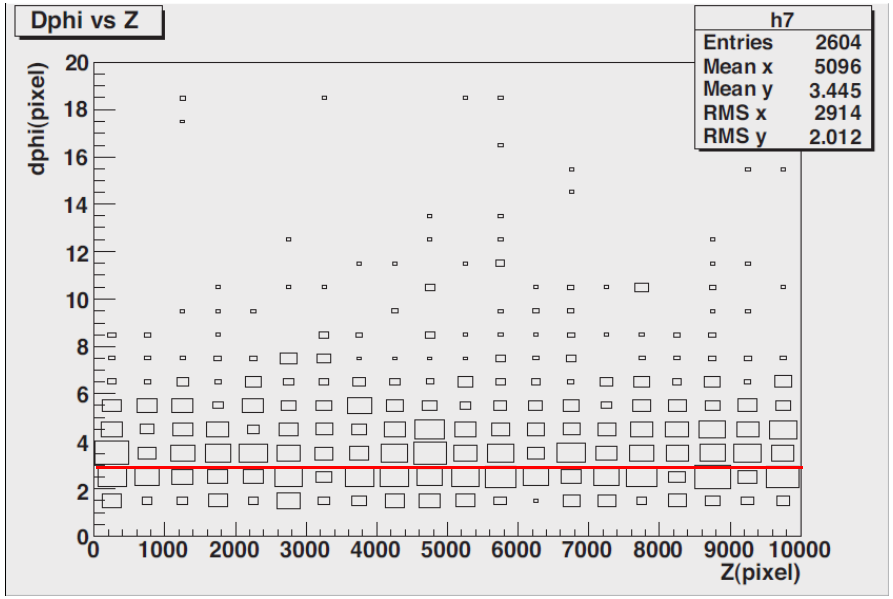
- 1 GeV/c muon

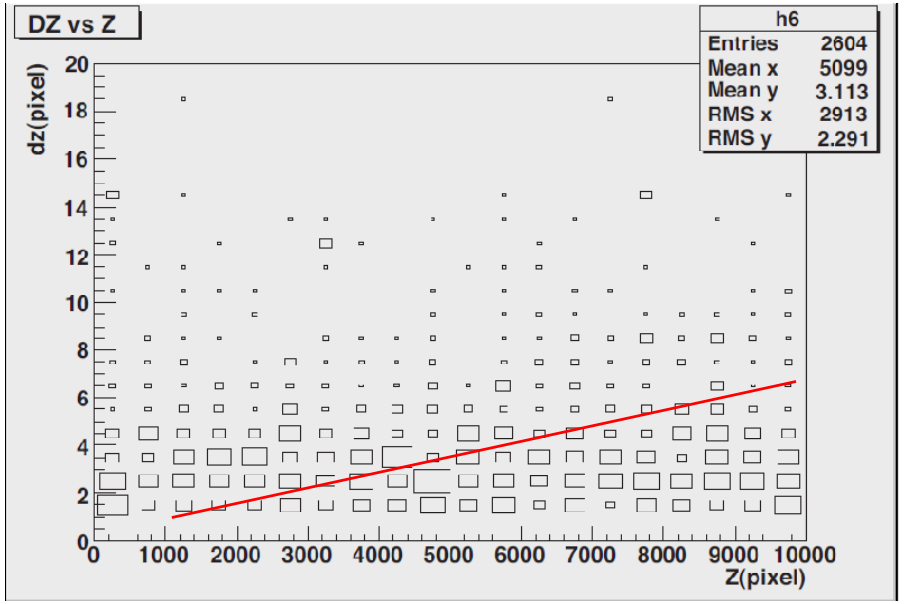




Simulation for B.G. rejection(2)

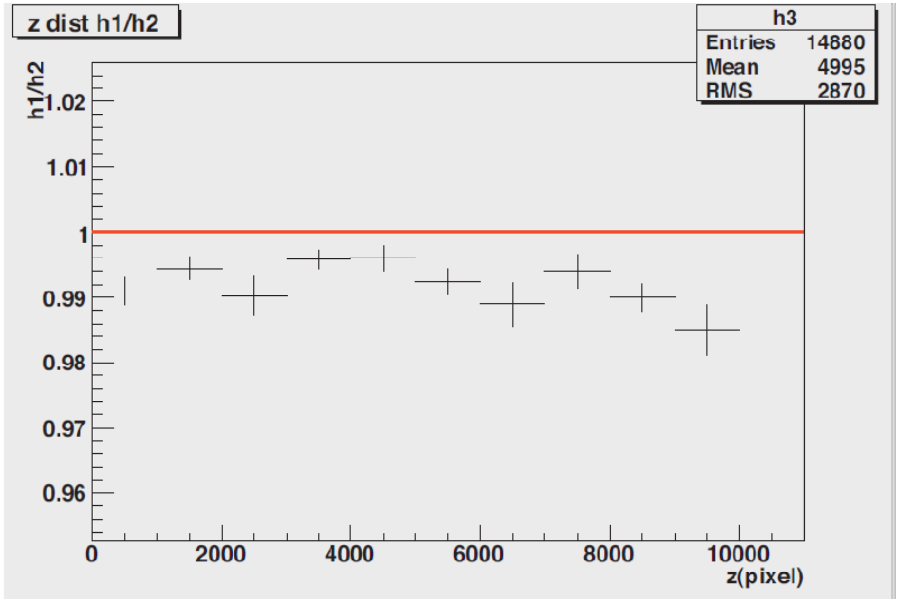
- Pair-background particles



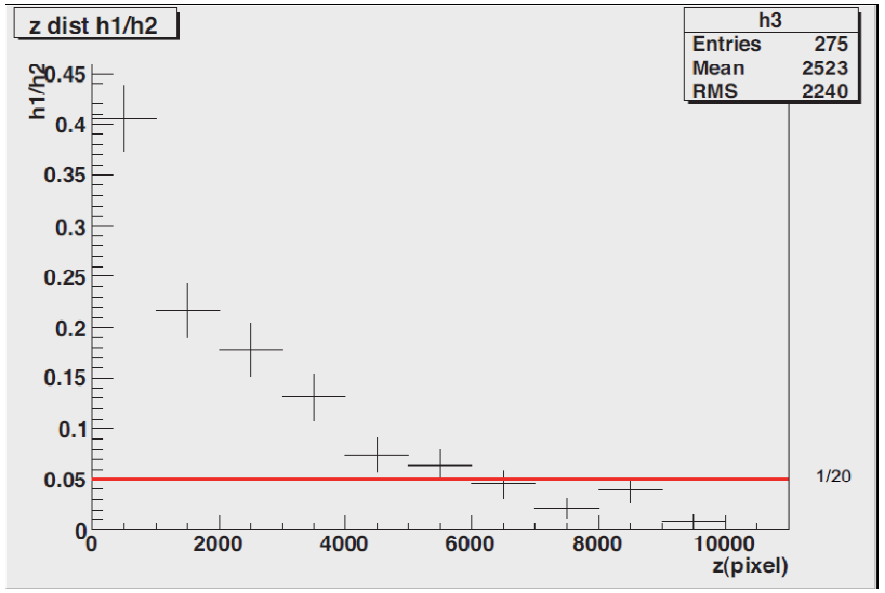


Simulation for B.G. rejection(3)

- Rejection performance

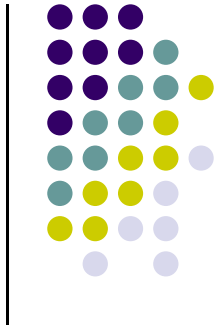


For 1 GeV/c muons



For pair b.g. particles

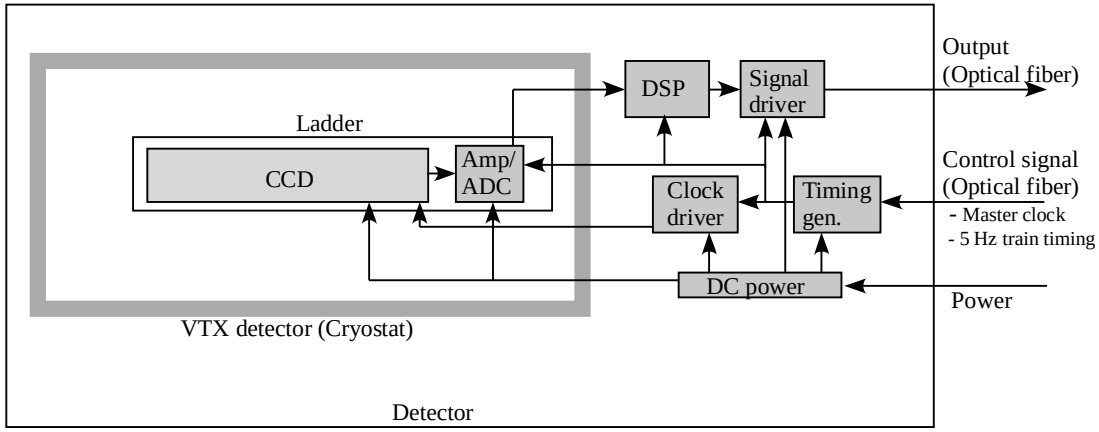
R&D issues (1)

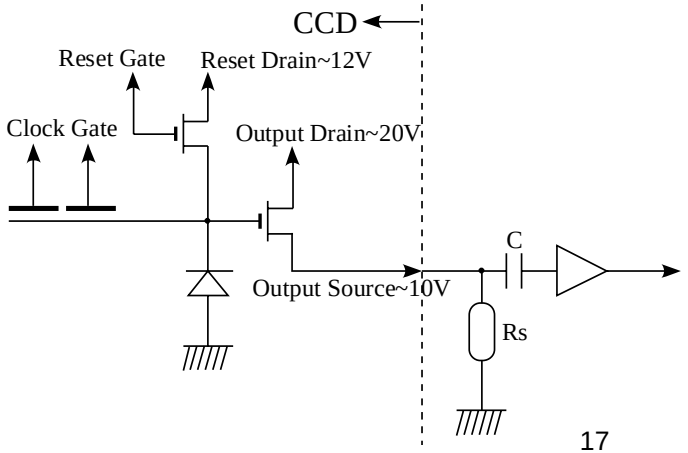


- Sensor R&D
  - Fully depleted CCD
  - Prototype FPCCD
    - Small size (~10mm^2) for proof of principle by 2010
    - Full size (10x65mm^2 and 20x100mm^2) by 2012 – 2013
  - Key issues:
    - Output circuit – Low power consumption, high speed, low noise
    - Radiation tolerance

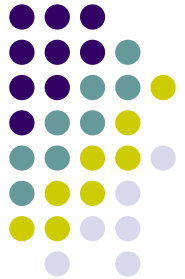
R&D issues (2)

- R&D of readout circuit
  - Front-end ASIC: Amp-LPF-CDS-ADC (-DSP)
  - Peripheral circuits
  - Target performance
    - Power: <100 W inside the cryostat (CCD+ASIC)
    - Speed: ~10 Mpix/s
    - Noise: <50 electrons including CCD noise





R&D issues (3)



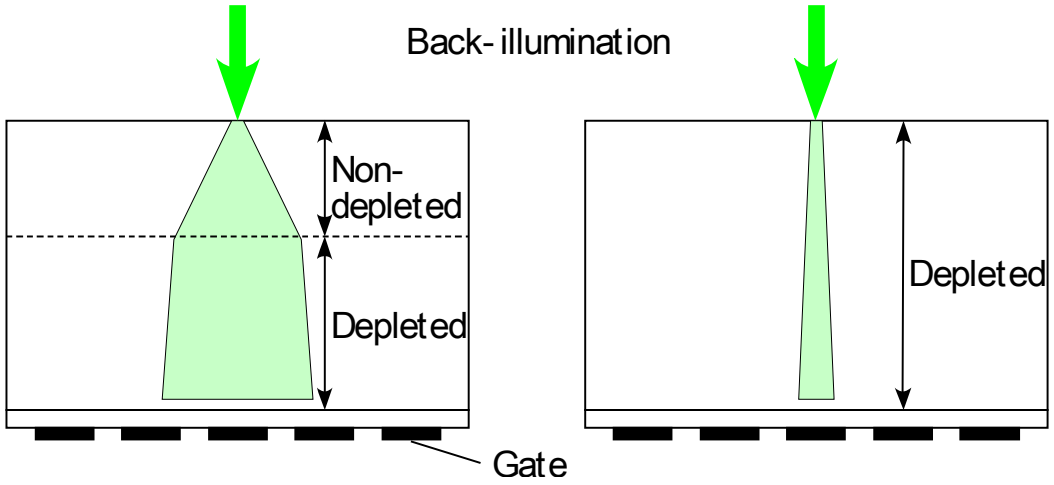
- Engineering issues
  - Low material structure is extremely important
    - Wafer thinning
    - Design of ladders
    - Design of support structure of ladders
    - Cryostat and cooling system
  - Other issues
    - Integration to detector system
    - Alignment
  - Timeline
    - Design of FPCCD vertex detector by 2010
    - Full-scale engineering prototype by 2012 – 2013 for the construction-ready EDR

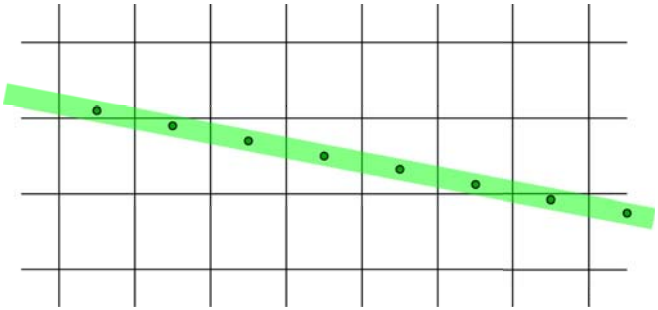
R&D status

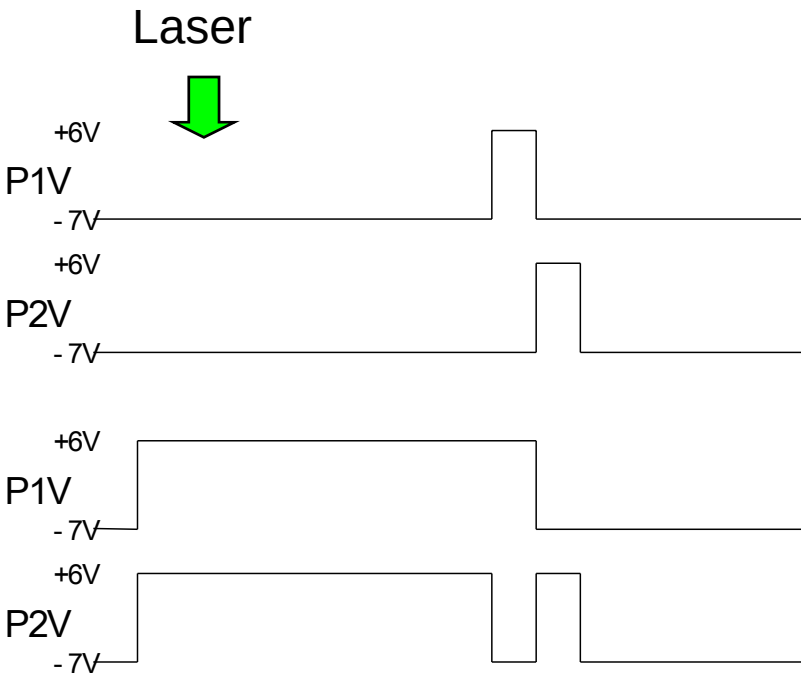
- Development of fully depleted CCDs
- Design of the first prototype of FPCCD
- Design of readout ASIC

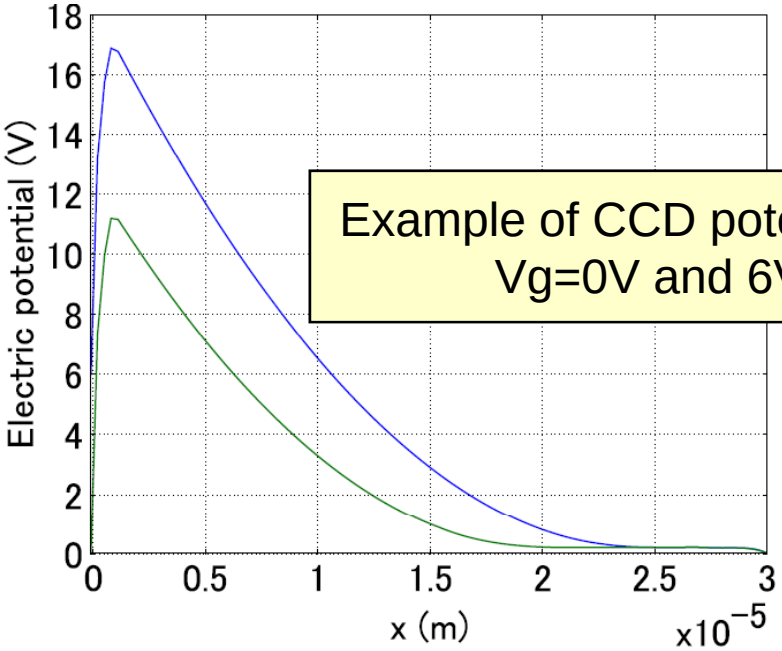
Fully depleted CCD (1)

- Several samples are obtained from Hamamatsu
- Confirmation of full-depletion by measurement of charge spread
  - LASER light (532nm) focused to a thin (<pixel size) line was illuminated to back-illuminating CCDs slightly inclined w.r.t. CCD pixel grid ➔Effectively scan inside a pixel
  - Compare signal distribution between V_{gate}=-7V and V_{gate}=+6V during LASER illumination
  - If distributions are same, the CCD is fully depleted in both cases





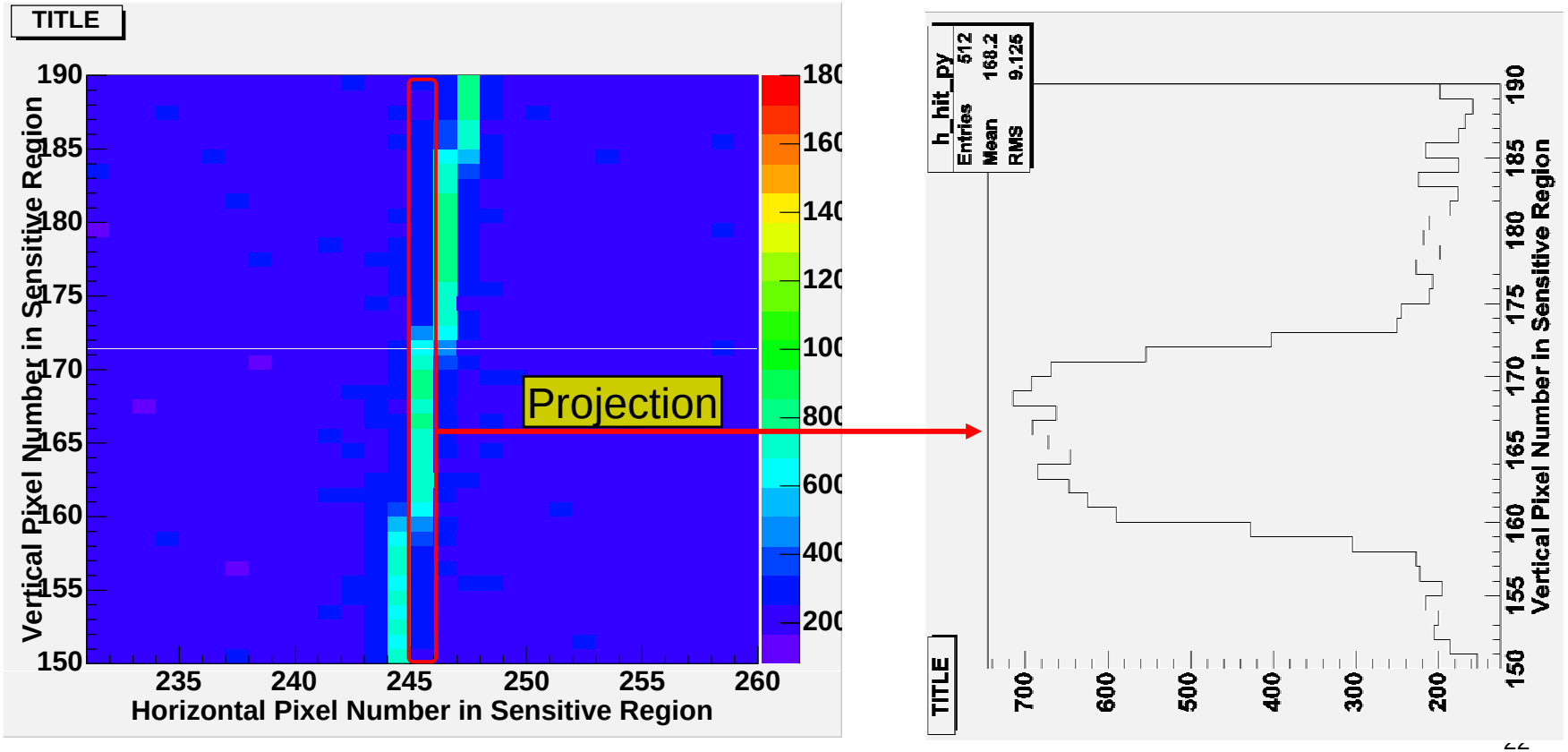




Example of CCD potential for Vg=0V and 6V

Fully depleted CCD (2)

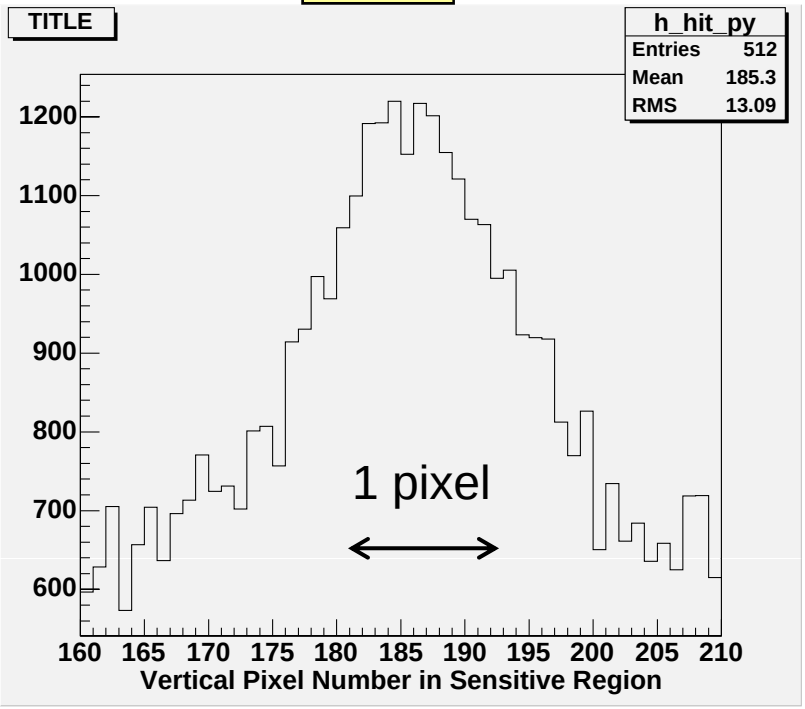
- Results of experiments



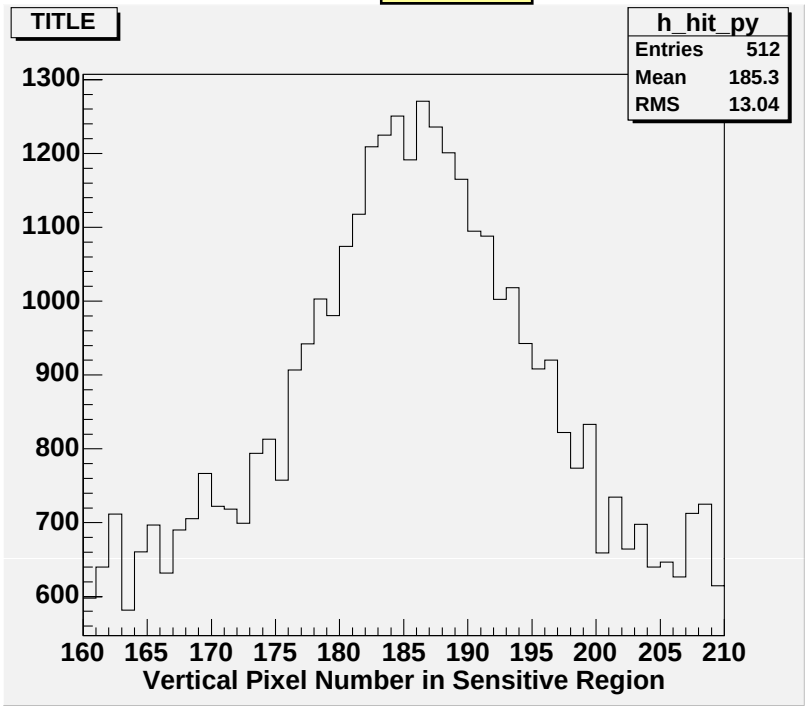
Fully depleted CCD (3)

- S7170 Standard
  - Low resistivity epitaxial layer → thin depletion layer

-7V



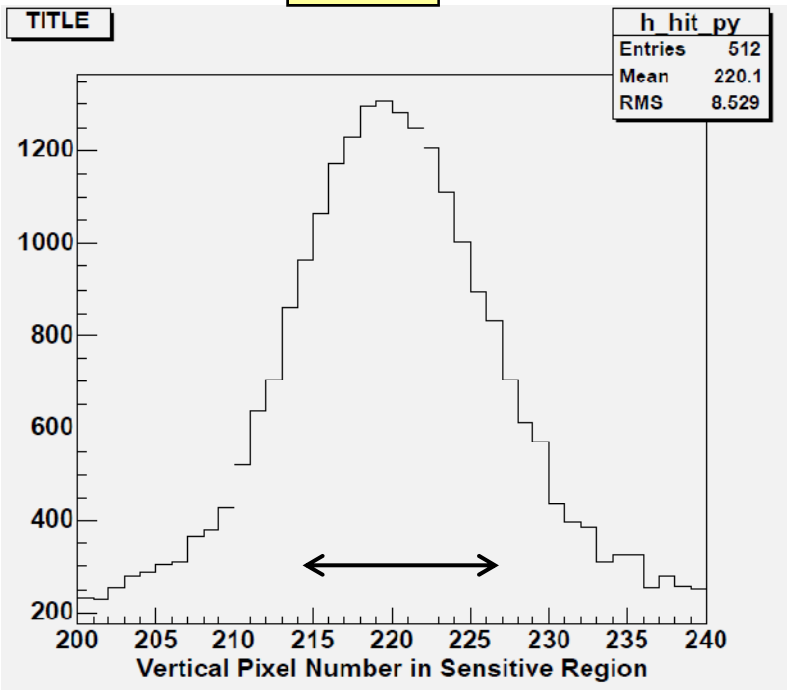
+6V



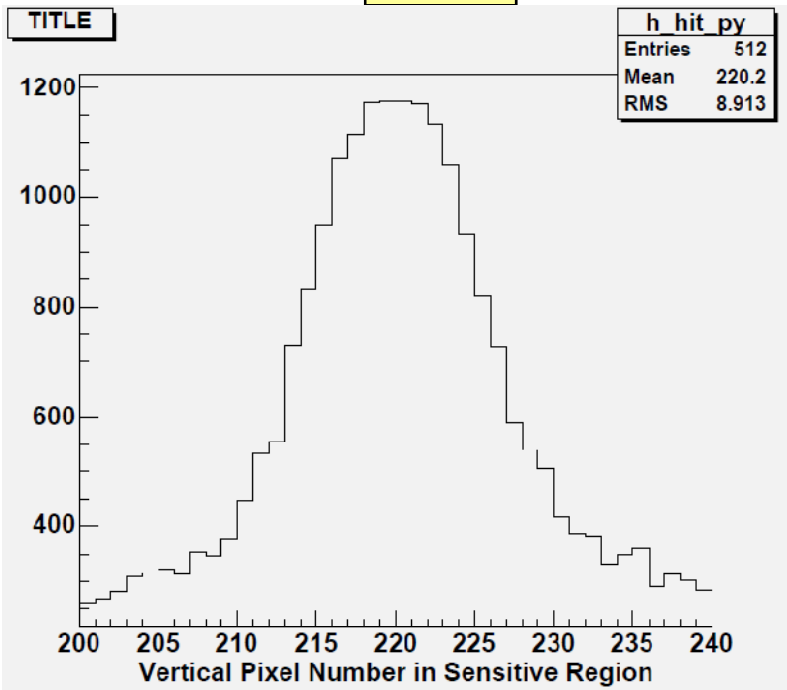
Fully depleted CCD (4)

- S7170 Deep2
  - Higher resistivity 30μm thick epitaxial layer

-7V

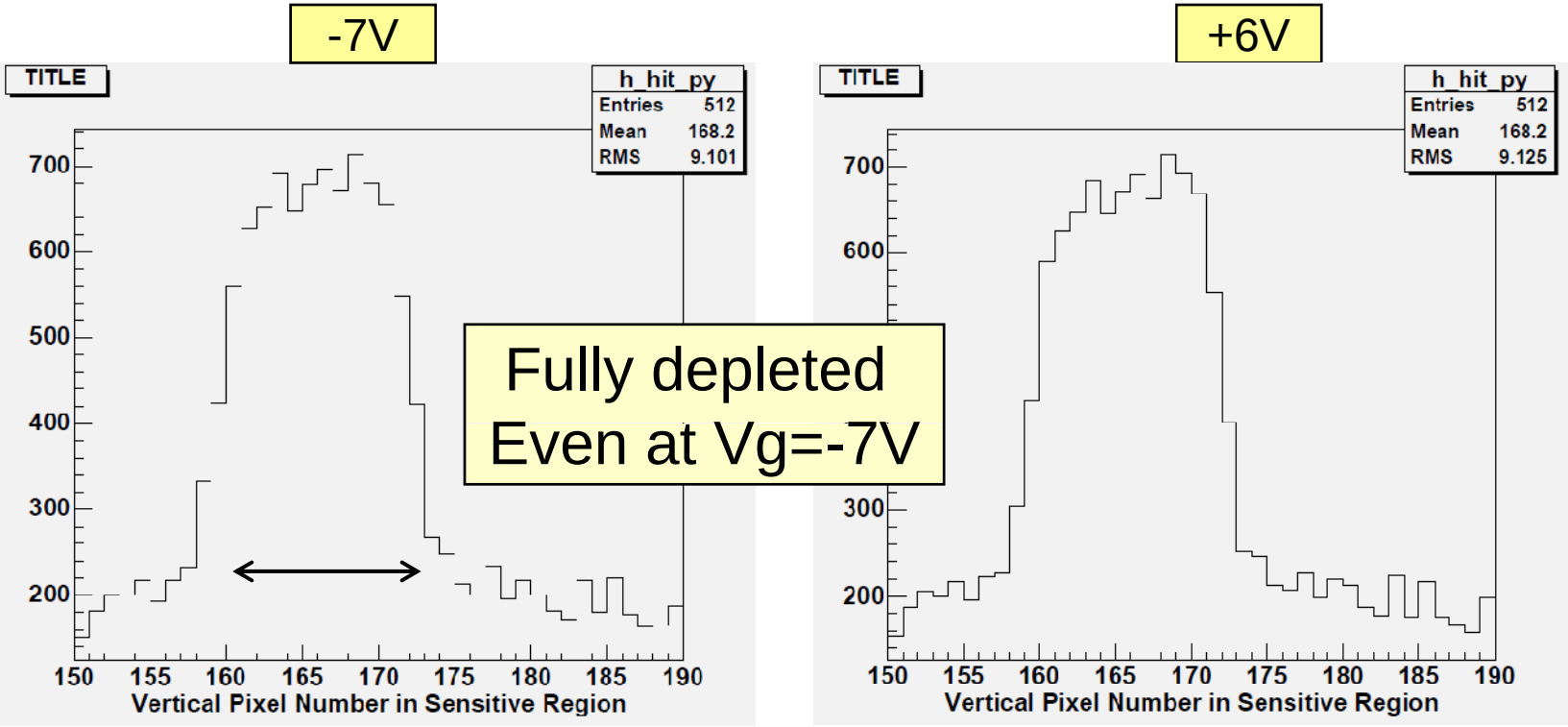


+6V



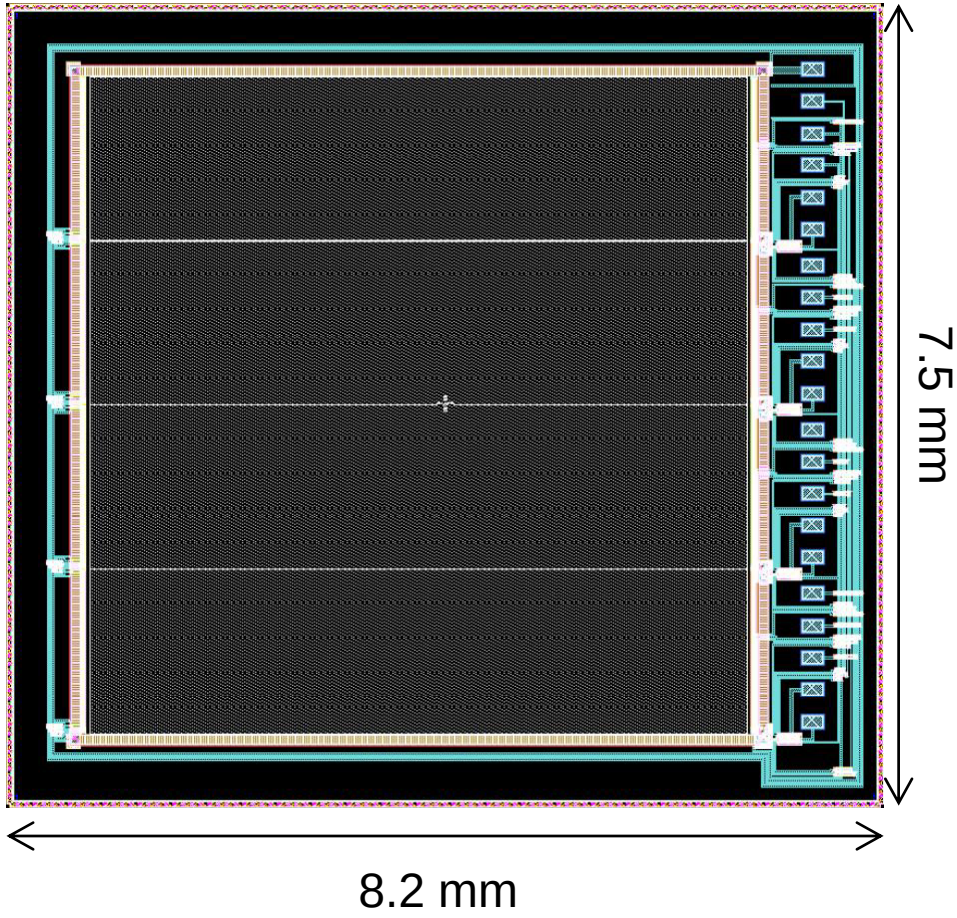
Fully depleted CCD (5)

- S7170 SPL24mm
  - Highest resistivity 24μm thick epi-layer



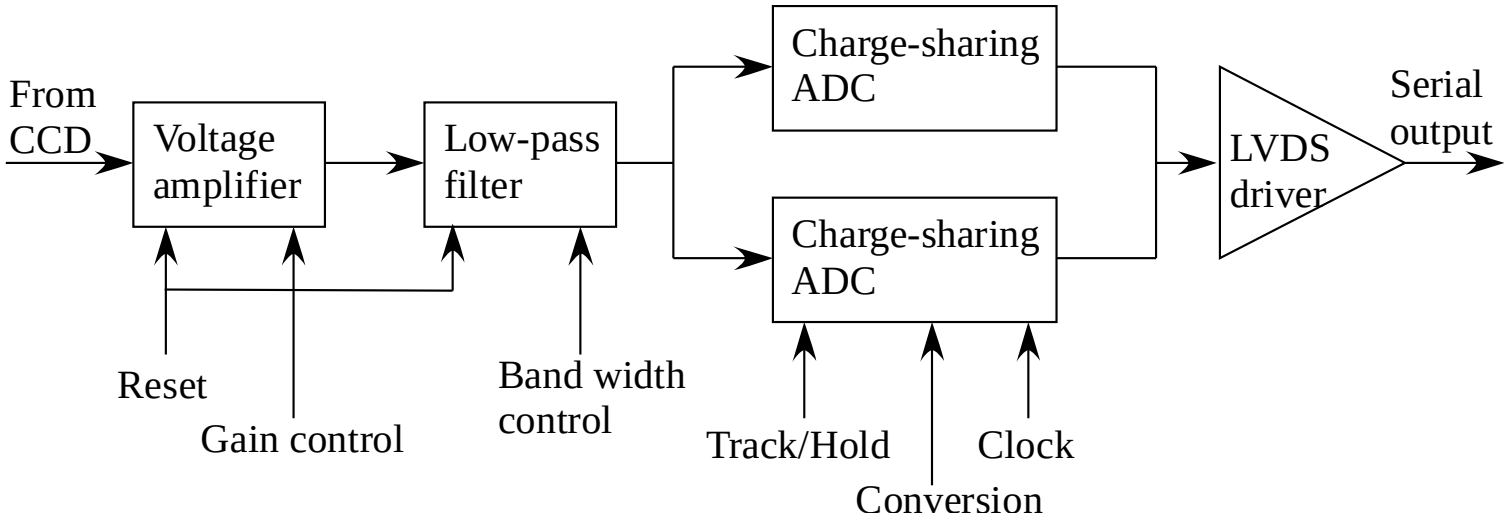
Design of prototype FPCCD

- 12μm pixel size
- 24μm epitaxial layer
- 512x512 pixels
- 6.1mm^2 image area
- 4ch /chip
- 128(V)x512(H) pixels for each channel
- 4 different design of output amp
- To be delivered at the end of 2007

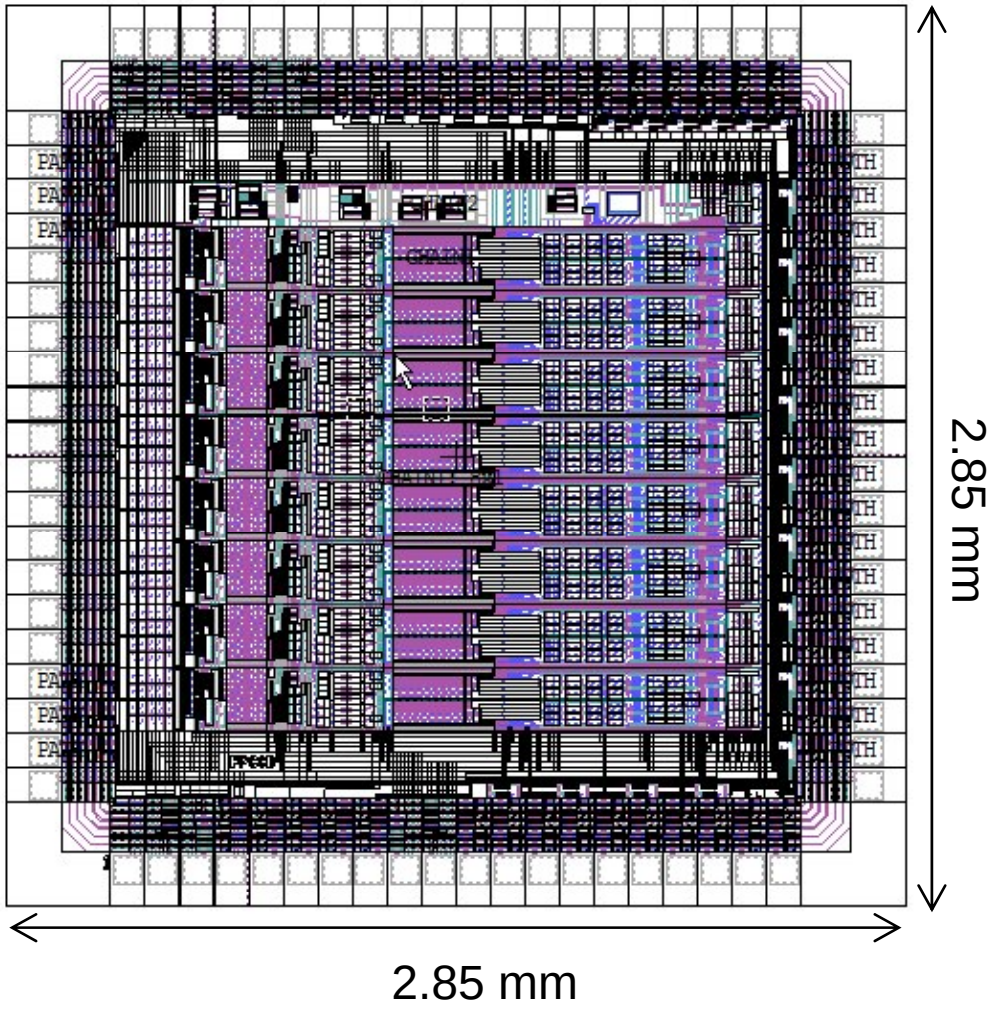


Design of readout ASIC (1)

- Amp, LPF, CDS, ADC, and LVDS driver
- 8 ch/chip
- Two ADCs/ch work alternatively to achieve fast readout
- Max sampling rate ~ 10 Msample/s
- Charge sharing SAR ADC → Low power
- 0.35μm CMOS
- To be delivered at the end of 2007



Design of readout ASIC (2)



Summary and outlook (1)

- R&D for FPCCD vertex detector has just begun in 2006 supported by JSPS funding
- So far, we have made simulation studies and obtained promising results on
  - Impact parameter resolution
  - Background rejection using hit-cluster shape
- Concerning the sensor R&D, we have developed fully depleted CCDs in collaboration with HPK, and started design of a prototype FPCCD
- A prototype of front-end ASIC is designed and submitted to a foundry
- In order to make a construction-ready design of the FPCCD vertex detector, we think we need
  - At least 6 times iteration of production-characterization cycle of FPCCD and front-end ASIC
  - R&D of peripheral circuits and DAQ system
  - Engineering study including full-scale prototype
- But, established support is far below the need to complete these tasks

Summary and outlook (2)

- If we succeed to obtain necessary support in future, we plan to
  - Demonstrate the feasibility of FPCCD vertex detector by making small prototype of FPCCD and front-end ASIC by 2010
  - Study on key technologies of engineering issue such as wafer thinning, ladder design, and cooling system
  - Carry out beam tests of small prototype in ~2010
  - Develop full-size prototype sensors, total readout system, and full-size engineering prototype detector for construction-ready EDR by 2012 – 2013