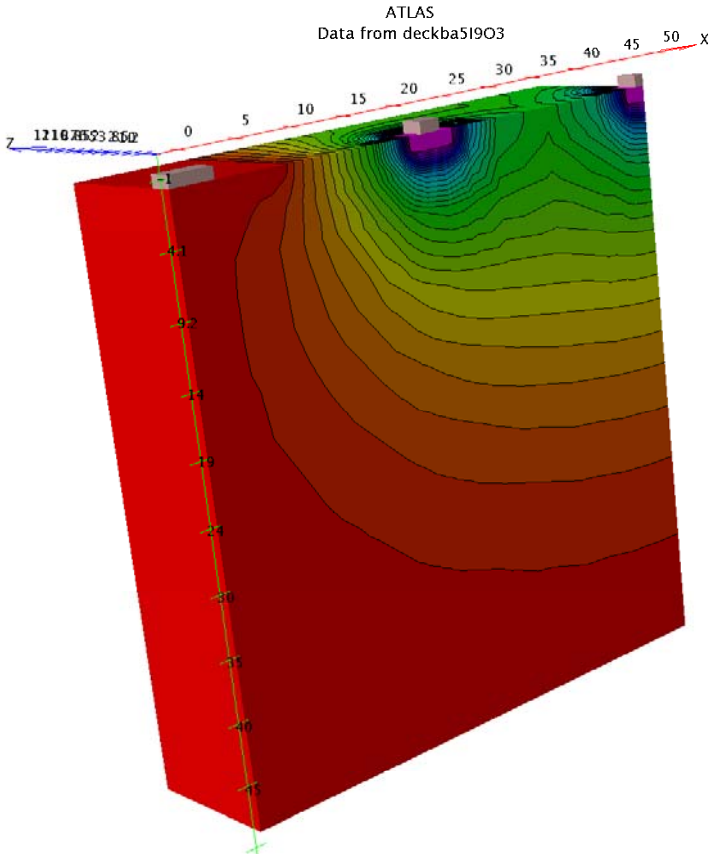
3D and SOI Sensors and Electronics

- ILC inner layer challenge
- 3D and SOI
- Thinned sensor R&D
- Laser Annealing
- SOI Technology
  - OKI Process/Mambo Chip
  - Back gate effects
  - American Semiconductor process
  - Device simulation
- 3D Technology
  - VIP Chip
- Power distribution
- Conclusions



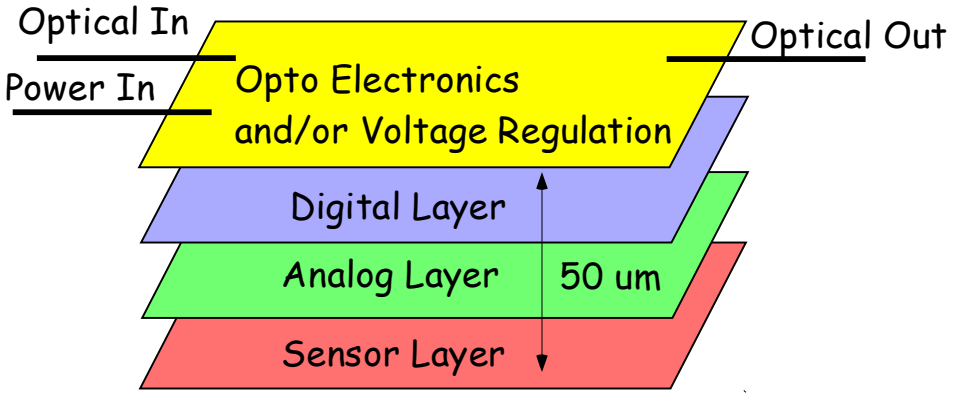
Cornell, Fermilab, Purdue U., U. Washington

The Challenge

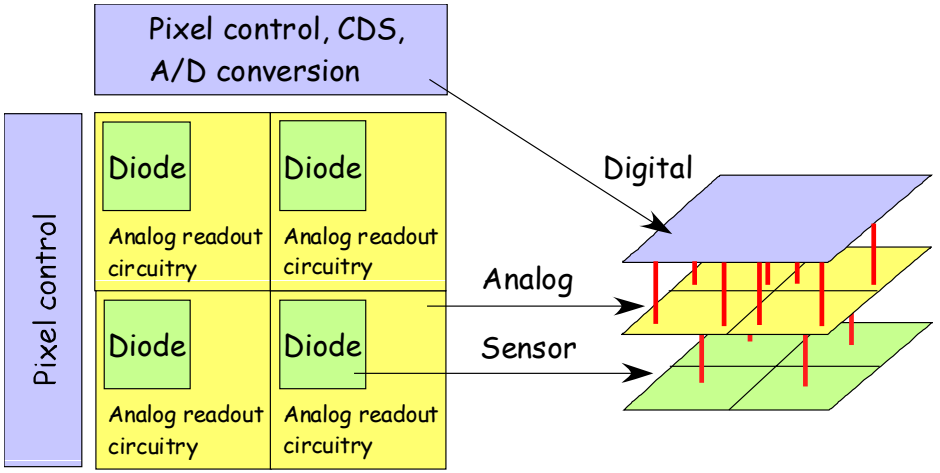
- Combination of small pixels, short integration time, low power required for ILC is difficult to achieve
  - Small pixels tend to limit the amount of circuitry that can be integrated in a pixel - forces examination of each pixel (CCD, rolling shutter …) this, in turn forces high clock speeds
  - Small pixels also mean that the power/pixel must be kept low
- The low occupancy/pixel/train (~0.5%) means that a sparse scan architecture would be appealing if:
  - Signal/noise is high
  - Enough electronics can be integrated on a pixel
- We feel that the best prospects for an optimal vertex detector are the emerging vertical integration (3D) and related SOI technologies. These offer the prospect of thin, densely integrated, devices with excellent signal/noise and low power. 3D also offers prospects for integration of power management into the pixel structure.
- Ultimate vertex detector will likely use a mix of technologies - R&D will define the options for a future optimal design.

3D Concept

- A 3D chip is generally referred to as a chip comprised of 2 or more layers of active semiconductor devices that have been thinned, bonded and interconnected to form a “monolithic” circuit.
- Often the layers (sometimes called tiers) are fabricated in different processes.
- Industry is moving toward 3D to improve circuit performance.
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power and crosstalk
- Utilizes technology developed for Silicon-on-Insulator devices
- This is a major direction for the semiconductor industry.



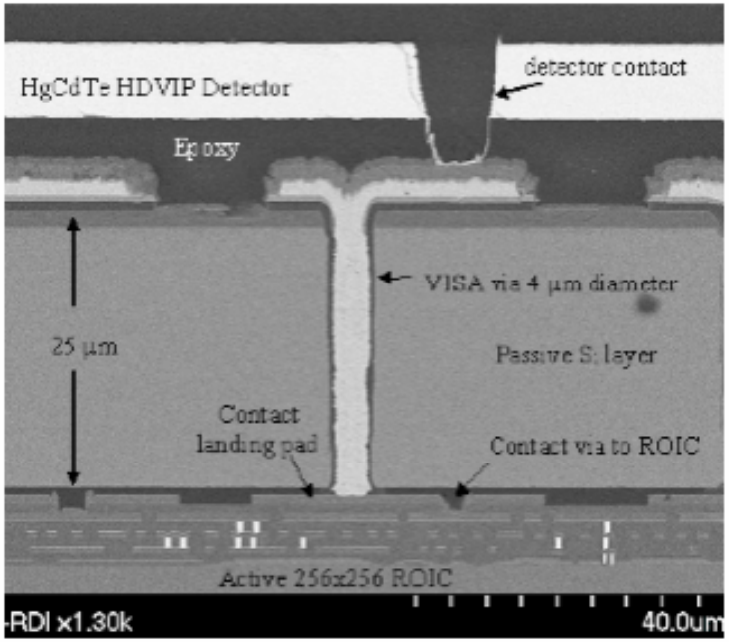
Physicist’s Dream



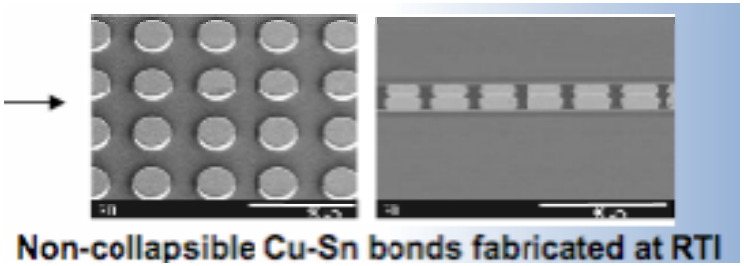
Conventional MAPS 4 Pixel Layout

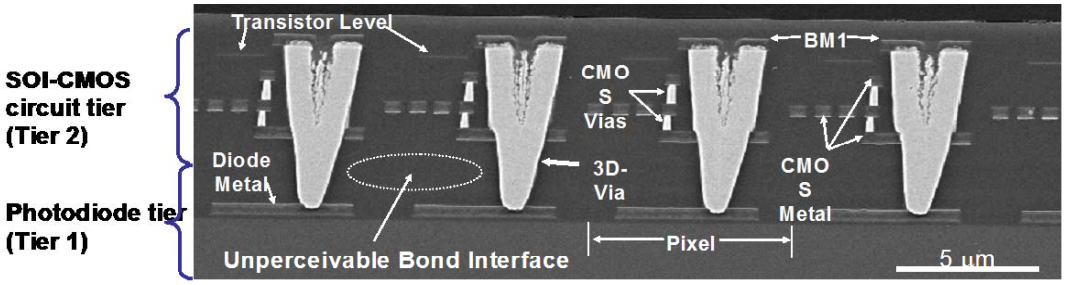
3D 4 Pixel Layout

3D Sensor Integration

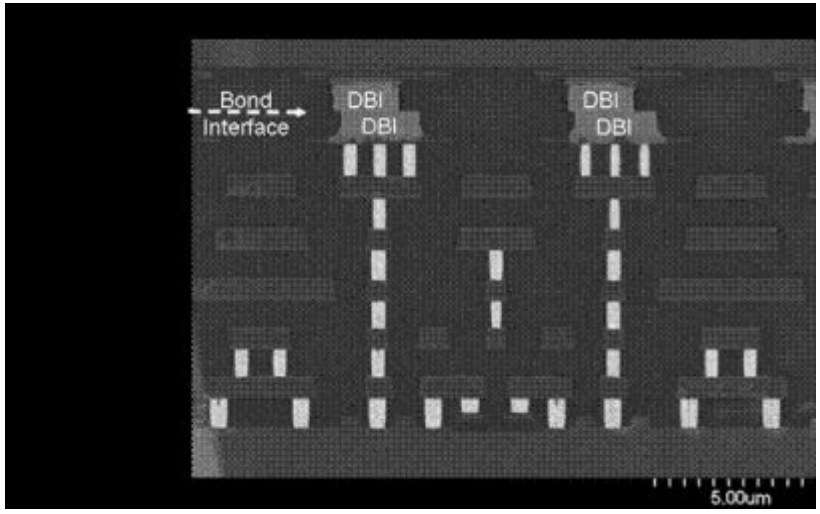


Epoxy bonded 3D connected imager (RTI/DRS)





8 micron pitch, 50 micron thick oxide bonded imager (Lincoln Labs)

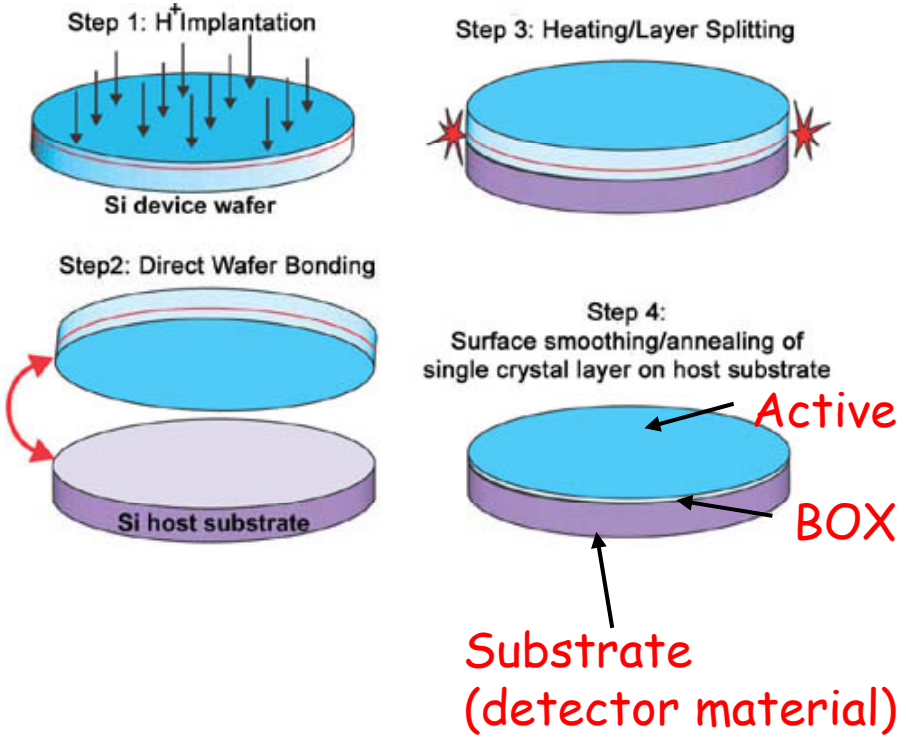


8 micron pitch DBI (oxide-metal) bonded PIN imager (Ziptronix)

Silicon on Insulator

- SOI is based on a thin active circuit layer on an insulating substrate. Modern technology utilizes ~200 nm of silicon on a “buried” oxide (BOX) which is carried on a “handle” wafer.
- The handle wafer can be high quality, detector grade silicon, which opens the possibility of integration of electronics and fully depleted detectors in a single wafer with very fine pitch and little additional processing.
- Diode can be formed by implantation through the BOX
- Used for high speed, circuits, immune to SEU
- Important for 3D integration

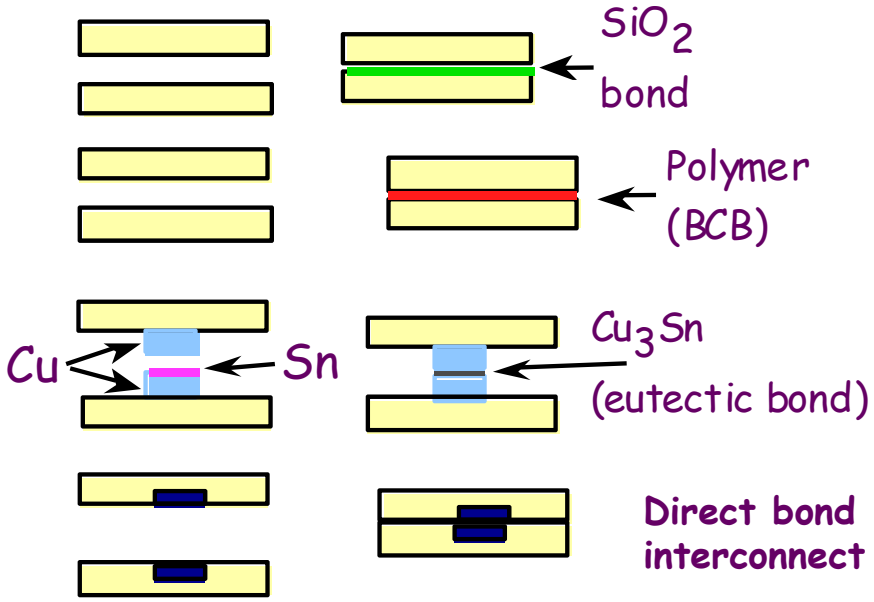
(Soitech illustration)



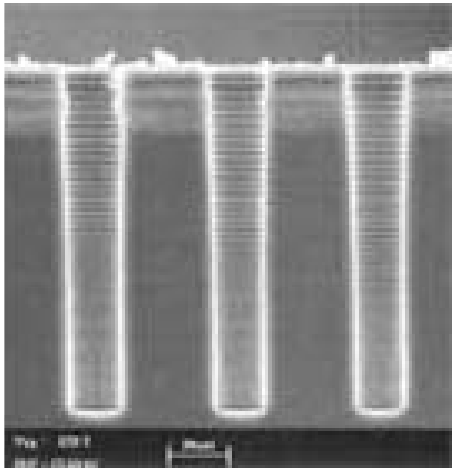
Steps for SOI wafer formation

Key Technologies for SOI/3D

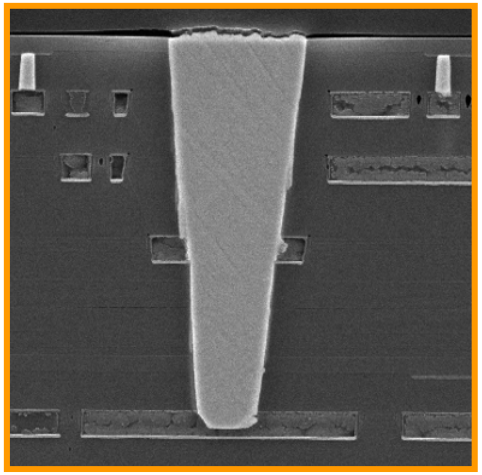
1) Bonding between layers
   - Oxide to oxide fusion
   - Copper/tin bonding
   - Polymer/adhesive bonding
2) Wafer thinning
   - Grinding, lapping, etching, CMP
3) Through wafer via formation and metalization
   - With isolation
   - Without isolation
4) High precision alignment



SEM of 3 vias using Bosch process



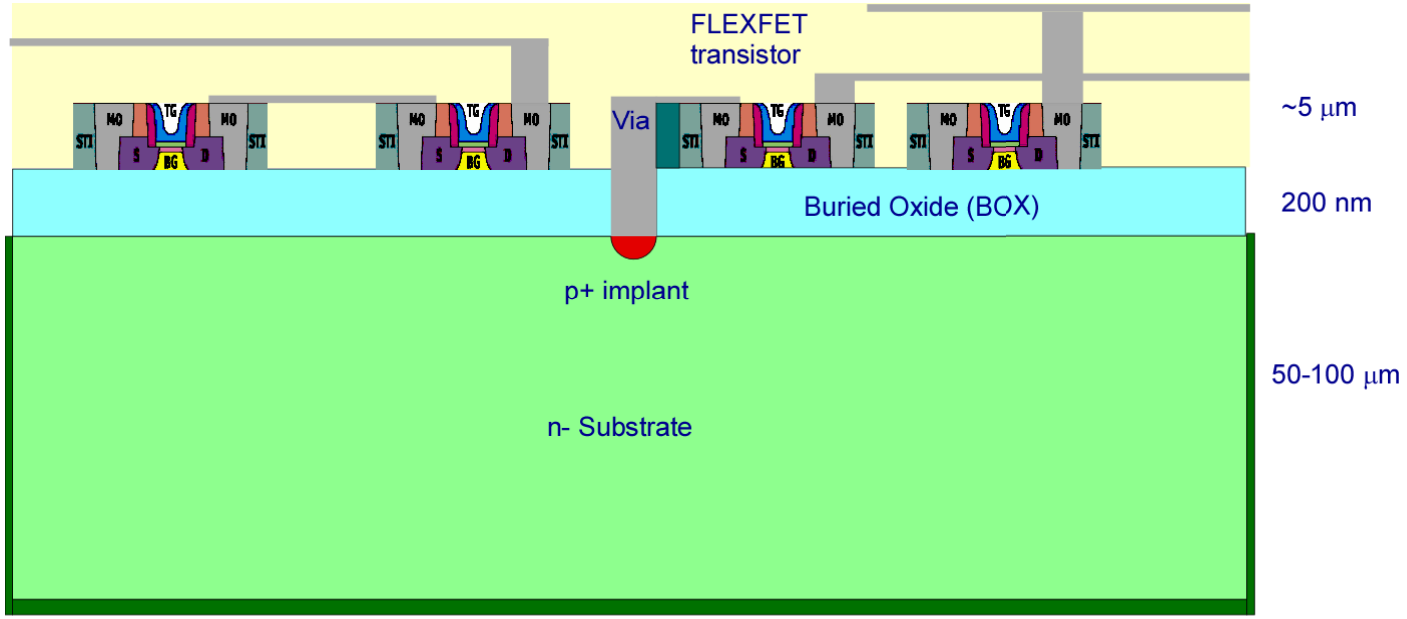
Via using oxide etch process (Lincoln Labs)



SOI Concept for HEP

not to scale

Minimal interconnects,
low node capacitance



High resistivity
Silicon wafer,
Thinned to 50-
100 microns

Active edge
processing

Backside implanted after thinning
Before frontside wafer processing
Or laser annealed after processing

Advantages of SOI/3D

- Advantages of SOI/3D
  - High resistivity substrate available for fully depleted diodes - large signal
  - No limitation on PMOS transistor usage as in CMOS MAPs
    - Full low power CMOS, integration of digital and analog in pixel
    - No parasitic charge collection
  - Sense nodes can have very low capacitance – important for low power signal/noise
  - Moderately Radiation hard, low SEU sensitivity
  - SOI is a low power technology
  - Sensor thinning to 50 microns has been demonstrated
  - Minimum charge spreading with fully depleted substrate
    - Can be engineered
  - No bump bonds
  - 100% diode fill factor

Integrated Sensor R&D Issues

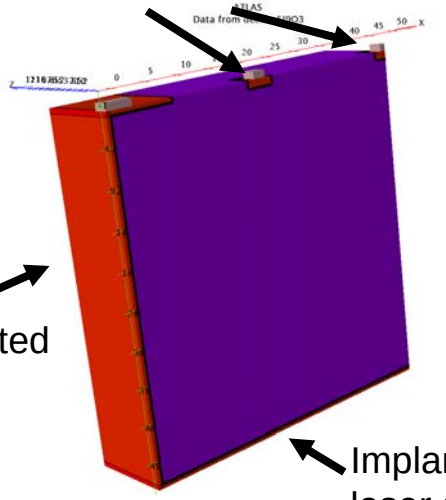
- Explore SOI processes which include processing of the handle wafer as part of the fabrication process
  - *OKI, American Semiconductor, MIT-LL*
- What is the optimal process for forming the detector diodes?
  - *Model charge collection, shielding, pinning layers*
- After thinning a backside contact must be formed. This is usually done by implantation and high temperature furnace annealing - which will destroy the front side CMOS SOI circuitry. An alternative is laser annealing of the backside implantation, which limits the frontside temperature.
  - *Laser anneal R&D*
- Can we retain good, low leakage current, detector performance through the CMOS topside processing?
  - *SOI diode test structures*
- How does the charge in the BOX due to radiation and potential of the handle wafer affect the operation of the top circuitry?
  - *Radiation studies*
  - *Test structures*
- How does topside digital circuitry affect the pixel amplifier?
  - *Simulation and test structures*
- Understand and qualify thinning processes for fully depleted devices

Edgeless Thinned Detector Concept

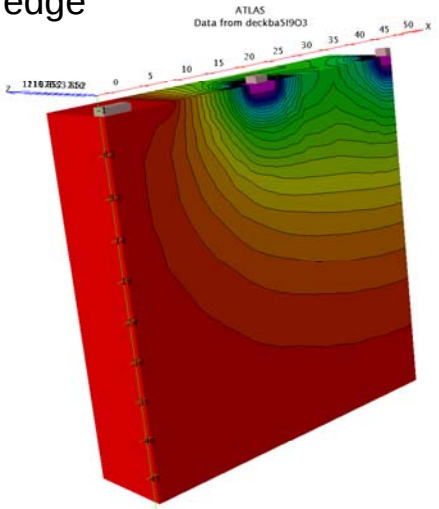
We are producing a set of thinned, "edgeless" sensors at MIT-LL

- Produce a set of detectors thinned to 50-100 microns for beam and probe tests.
- Validate and develop thinning process
- Understand performance
- Explore and validate the technologies which provide detectors sensitive to the edge
- Measure the actual dead region in a test beam
- Parts available for prototype vertex structures
- Also study radiation effects for SLHC

Status - Wafer processing complete - initial VI looks good. Now thinning prototype trenched wafer



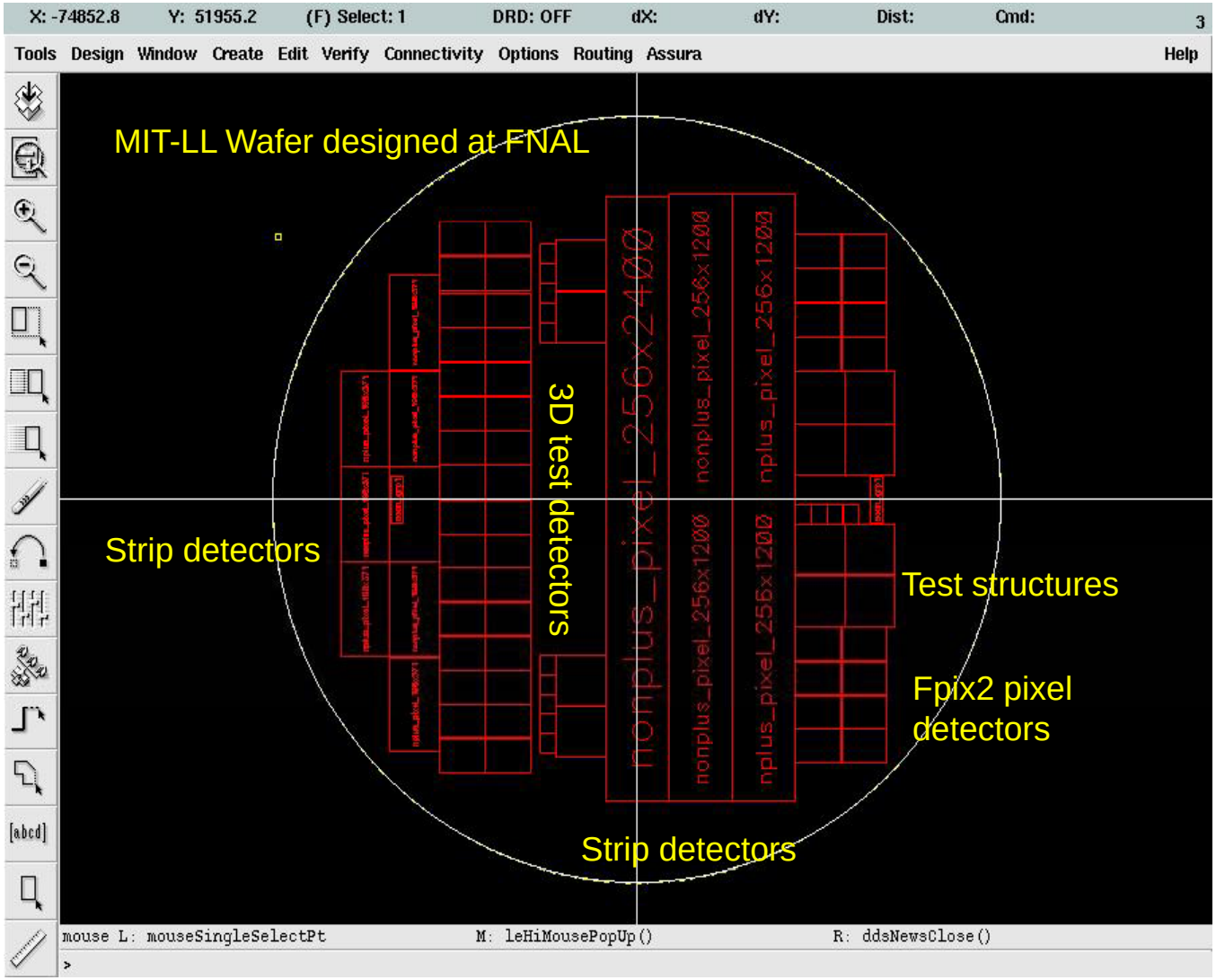
Detector Cross section near one detector edge



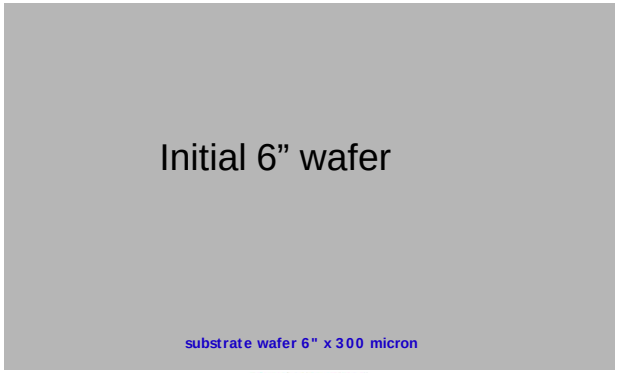
Equipotential lines in detector near one detector edge

Mask Design

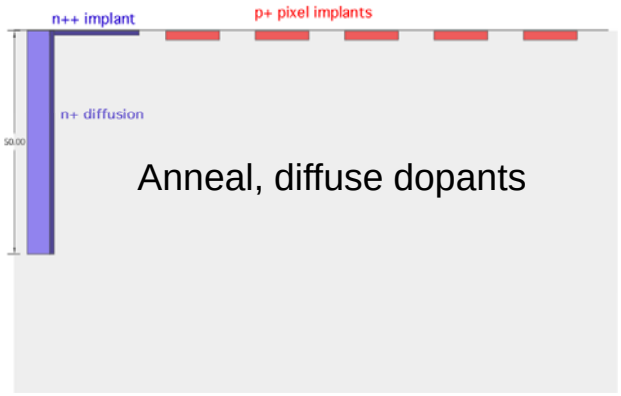
- Masks designed at FNAL
  - Test structures
  - Strip detectors (12.5 cm and ~2 cm)
  - FPiX2 pixel detectors (beam tests)
  - Detectors to mate to 3D chip



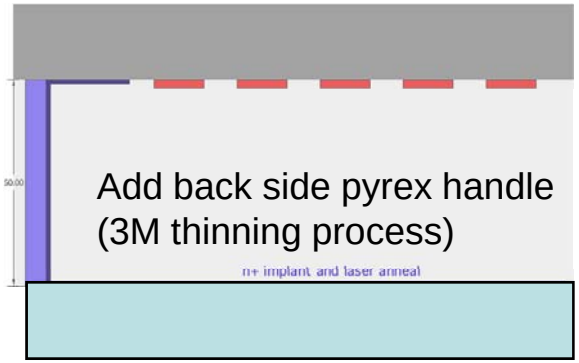
Detector Process



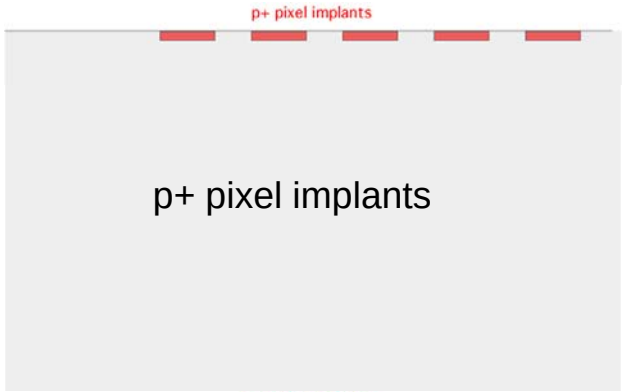
Initial 6” wafer



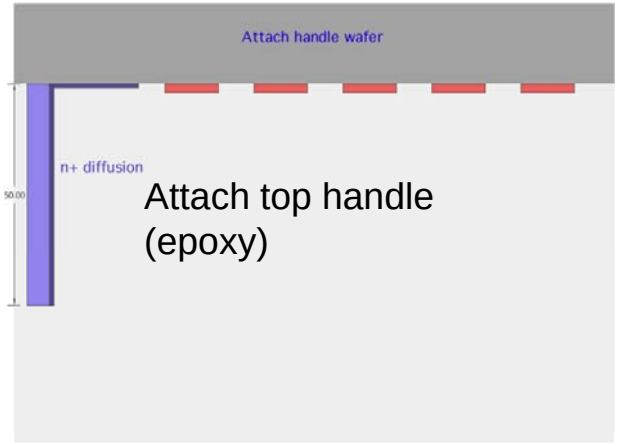
Anneal, diffuse dopants



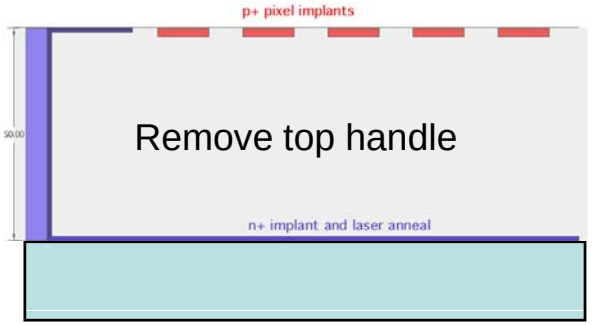
Add back side pyrex handle (3M thinning process)



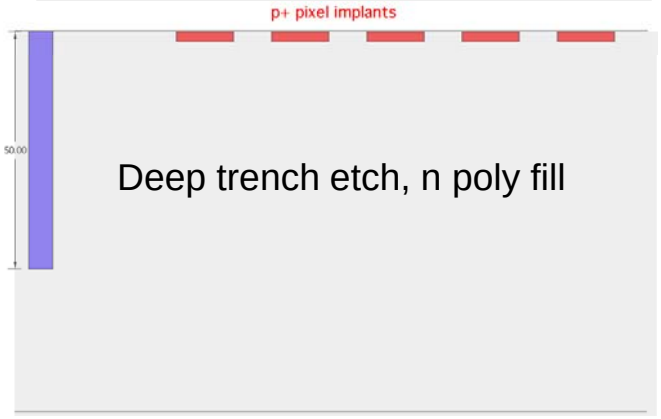
p+ pixel implants



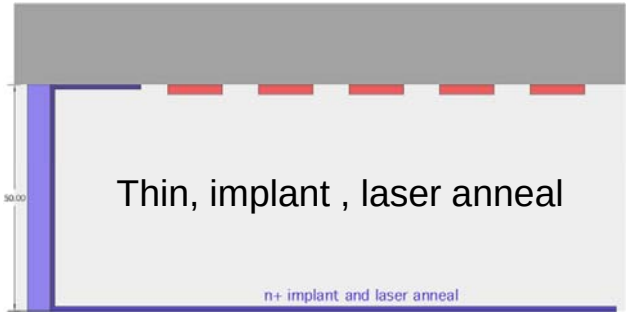
Attach top handle (epoxy)



Remove top handle



Deep trench etch, n poly fill



Thin, implant , laser anneal

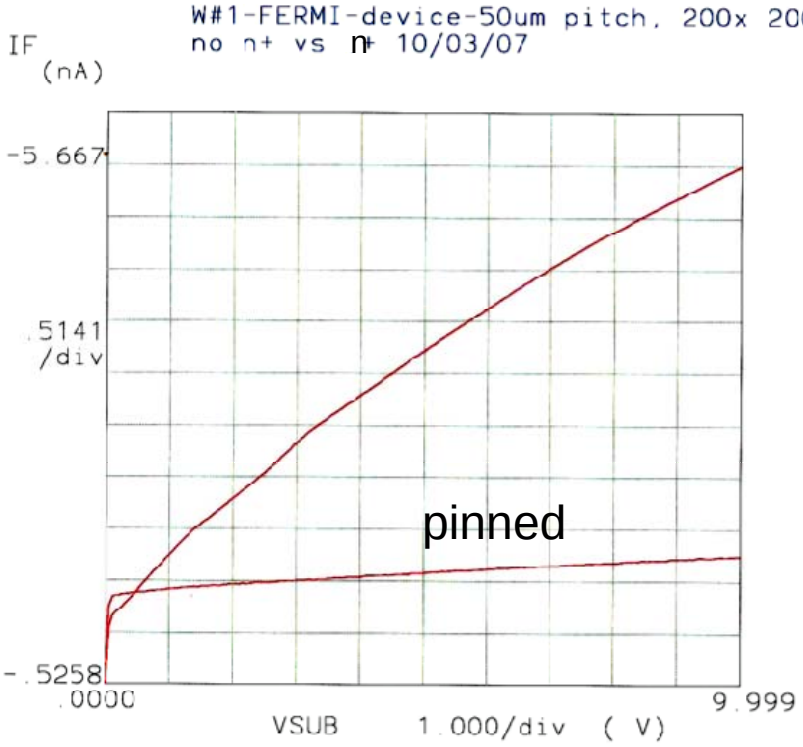
Remove bottom handle

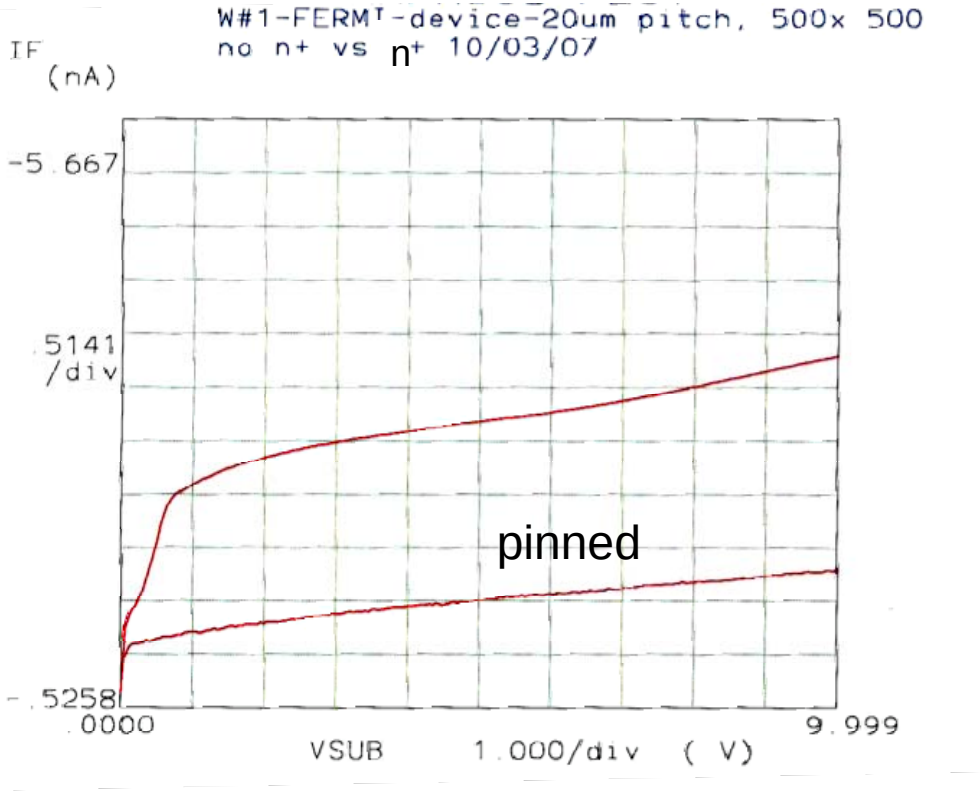
Initial Measurements (Unthinned)

Measurements at MIT-LL - n+ reduces dark current as expected

These are biased only from the trench - just an initial test

Vdep should be about 10 V



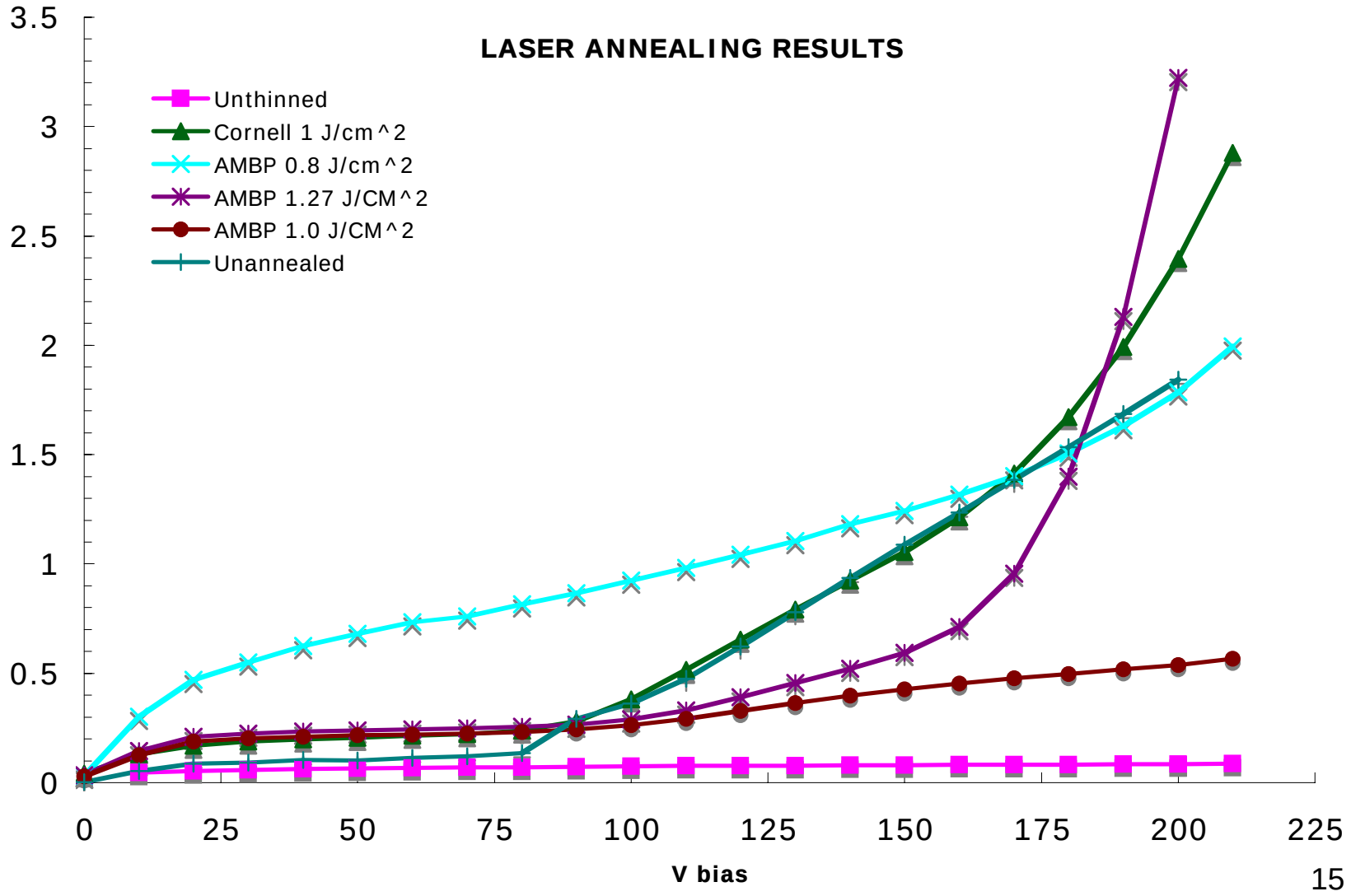


Laser Annealing

Problem: provide a backside ohmic contact to a thinned wafer while keeping topside below ~500 deg C to protect topside circuit

- Use a raster scanned eximer laser to melt the silicon locally – this activates the ohmic implant and repairs the implantation damage by recrystallizing the silicon
- We are developing a laser annealing capability which does not seem to be easily available commercially.
- To study and qualify this process we took a sample of Run2b HPK, low leakage 4x10 cm, strip detectors and reprocessed them
  - Backgrind by ~50 microns to remove back implant and aluminization, polish
  - Re-implant detector using 10 KeV phosphorus at 0.5 and $1.0x10^{15}/cm^2$
  - Laser anneal and measure CV and IV characteristics
    - AMBP - 0.8, 1.0, 1.2 J/cm^2, 248 nm laser
    - Cornell - 1.0 J/cm^2 305 nm laser

Preliminary Results (Cornell)

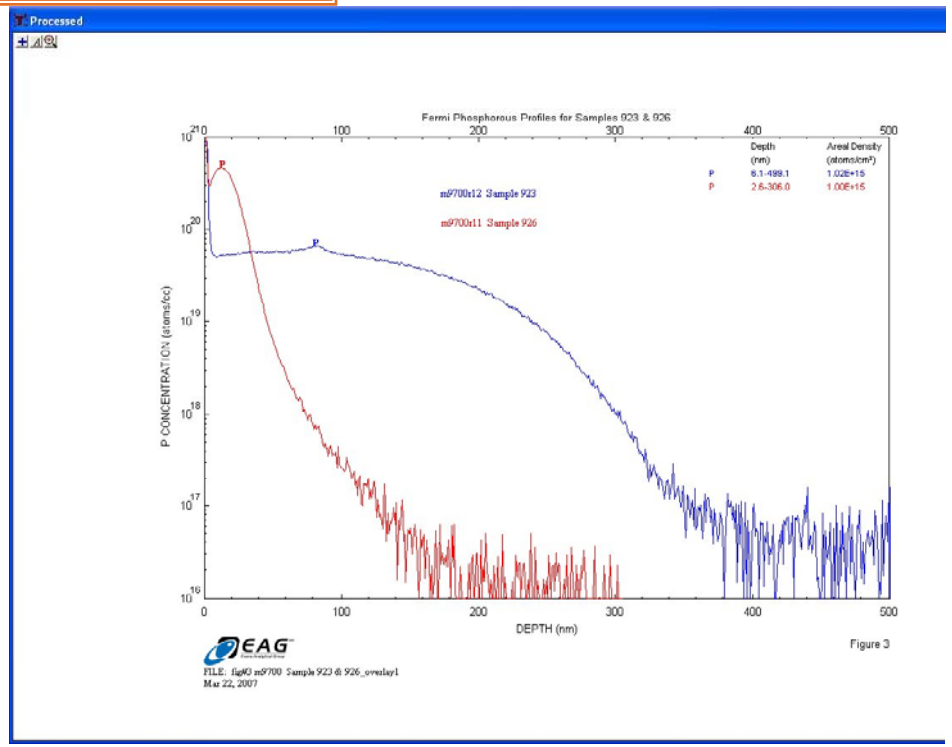


SIMS Measurements

Secondary Ion Mass Spectroscopy provides implant depth profiles by analysis of ions ejected from the surface upon ion bombardment:

- Two samples, before and after 1.2 J/cm^2 248 nm laser anneal
- Goal was ~>2x10^{19} concentration
- Melt depth ~300 nm

- Laser melt depth, phosphorus concentration is close to expectation
- Additional sintering at 400 deg should improve leakage



Program underway to explore optimal parameters with diodes fabricated and annealed at Cornell.

Plan to certify the full thinning (3M) and annealing (Cornell) process with 6" sensor wafers, then thin to 50 microns and anneal OKI SOI wafer.

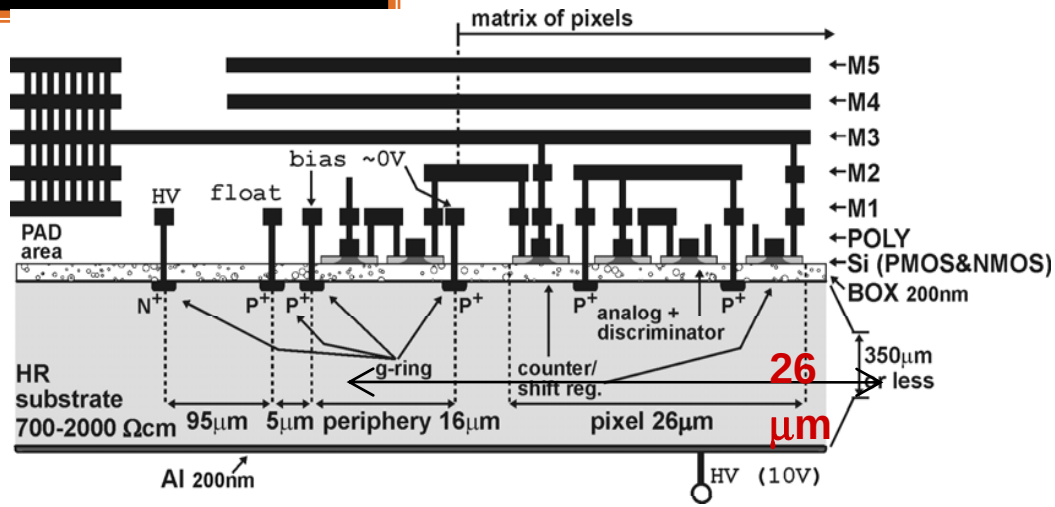
Fermilab SOI Detector Activities

SOI detector development is being pursued by Fermilab at three different foundries:OKI in Japan (via KEK), and American Semiconductor Inc. (ASI) and MIT Lincoln Labs in the US.

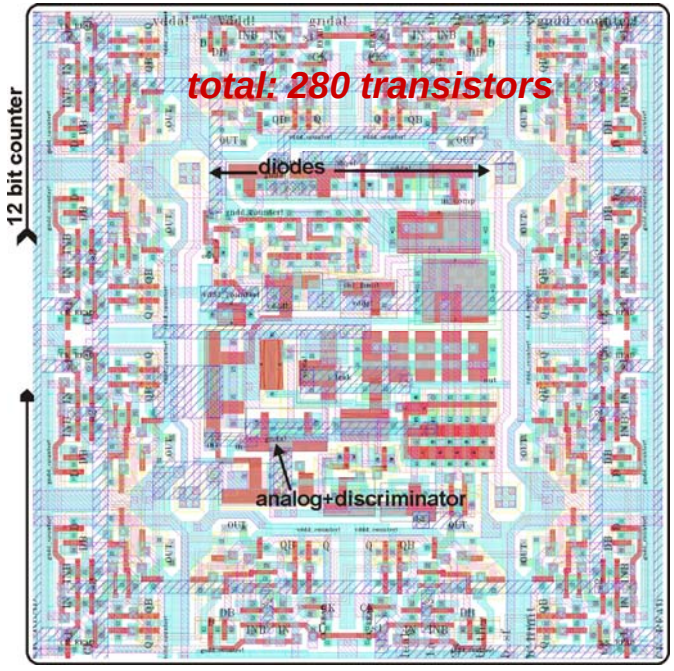
	OKI	MIT-LL	ASI
Feature size (μm)	0.15 0.2	0.18 0.15	0.18
Wafer Diameter	150mm	150mm	200mm
Transistor type	Fully depleted	Fully depleted	Partially depleted dual gate
Buried Oxide	200 nm	400 nm	200 nm
Work underway	Test Structures Mambo chip Laser anneal Mambo II	Test Structures 3D chip 3D RunII 3D Dedicated	SBIR design Simulation Test Structures Sensor SBIR

MAMBO - Monolithic Active pixel Matrix with Binary cOunters in SOI Technology OKI 0.15µm

- Submitted to the KEK sponsored multiproject run at OKI. The chip incorporates a 64 x 64 26 micron pitch 12 bit counter array for a high dynamic range x-ray or electron microscope imaging. (G. Deptuch)

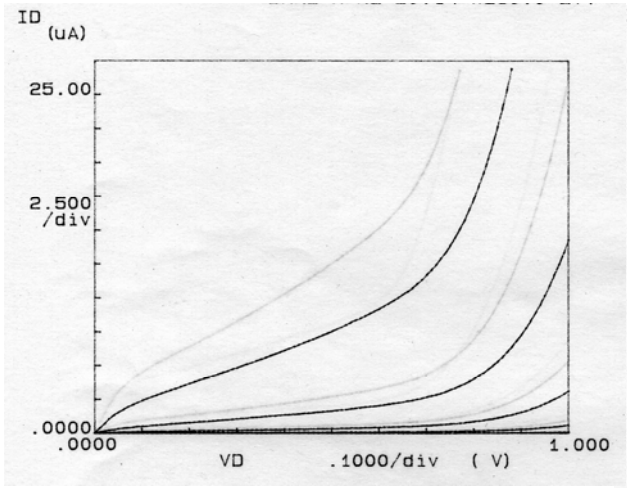


Counting pixel detector plus readout circuit
- Maximum counting rate ~ 1 MHz
- Each pixel: CSA, CR-RC2 shaper, discriminator + 12 bit binary counter
- Reconfigurable counter/shift register
- Peripheral circuitry limited to digital drivers (RO clock distribution, I/O signals, configuration switch) and bias generator
- 350 micron detector thickness
- Max 13 m implant pitch (4/pixel) is determined by the “back gate” effect where the topside transistors thresholds are shifted by handle potential

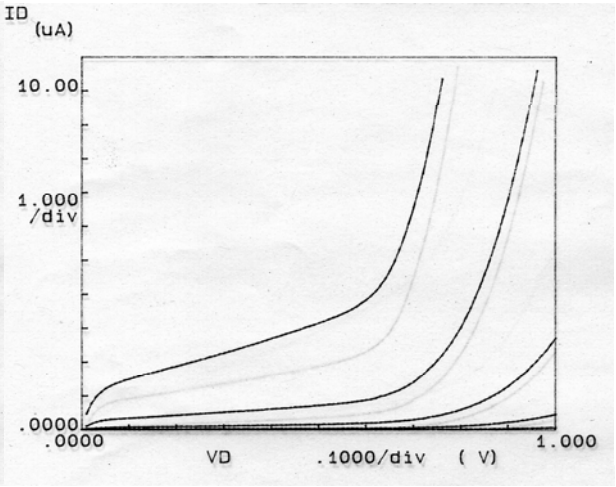


SOI Transistor Characteristics

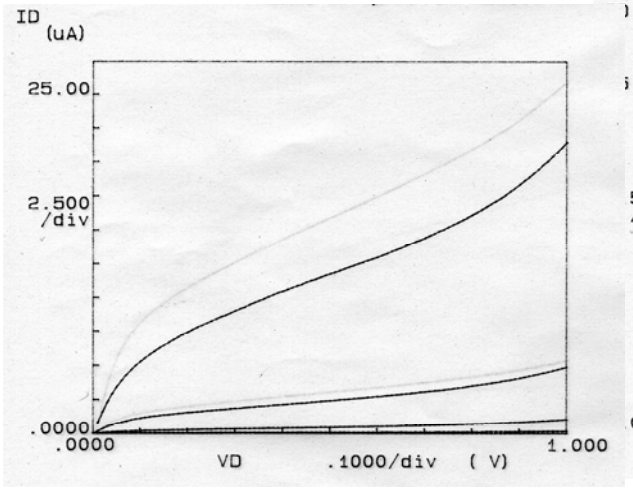
- There is mutual interaction between transistors and the substrate (used as detector)
- In fully depleted (FD) SOI, substrate plays role of a second gate with gate oxide thickness equal to the thickness of buried oxide (200nm)



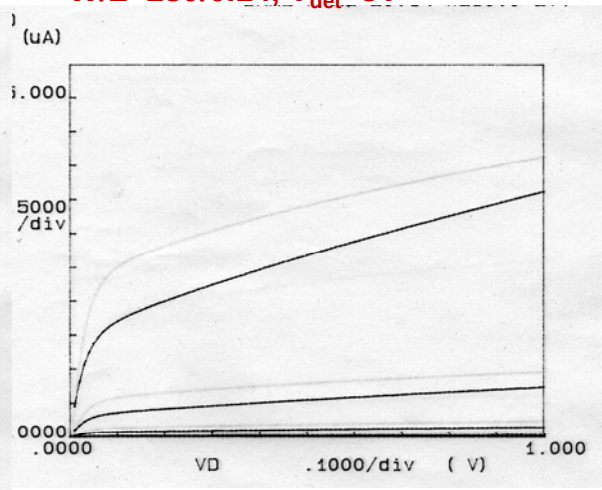
• NMOS; floating body, W/L=280/0.14, V_{det}=0V



• NMOS; floating body, W/L=280/0.14, V_{det}=5V



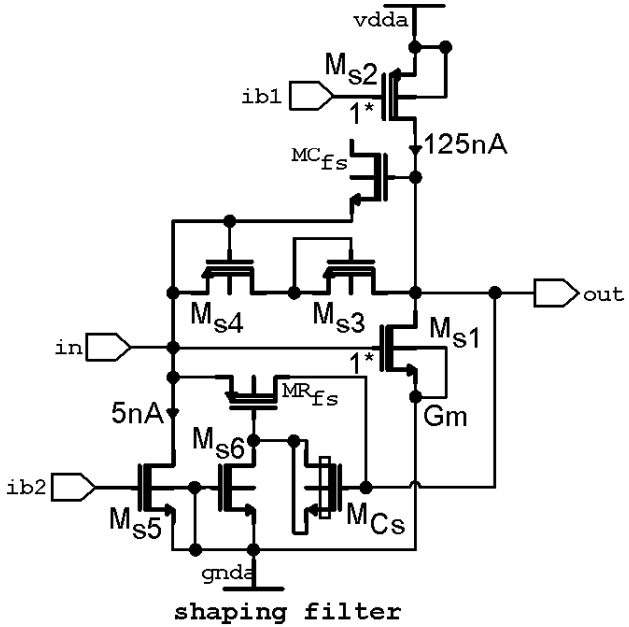
• NMOS; tied body, W/L=280/0.14, V_{det}=0V

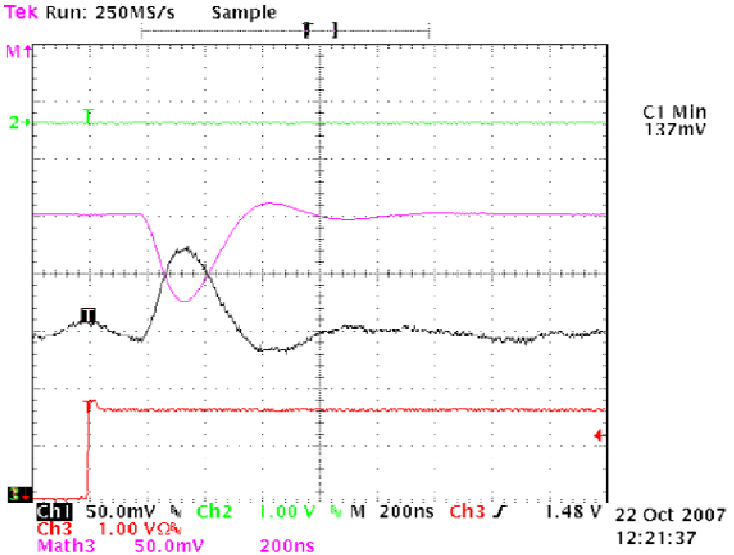


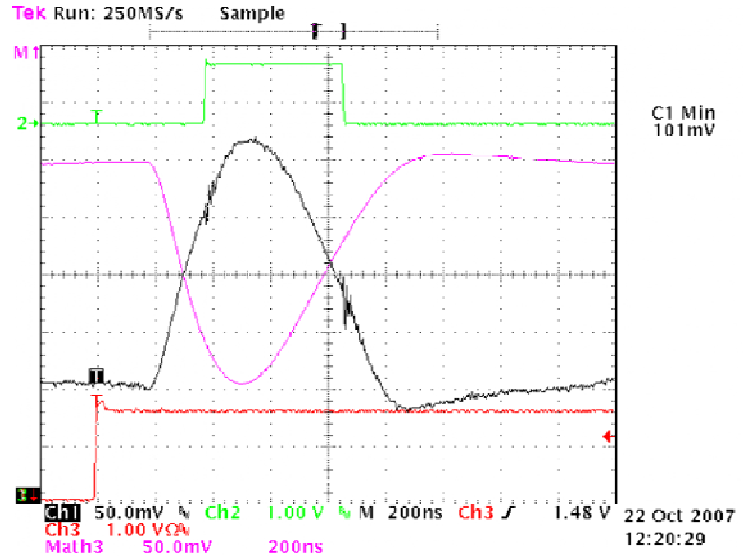
• NMOS; tied body, W/L=280/0.14, V_{det}=5V

Analog Performance

- Original specs almost recovered with good shaping time and very almost correct gain when applying -0.07V bias on feedback resistance (transistor) in the shaper (Vdet=5V):
- input charge ~1250 e-,
- 80e-<ENC<100e-

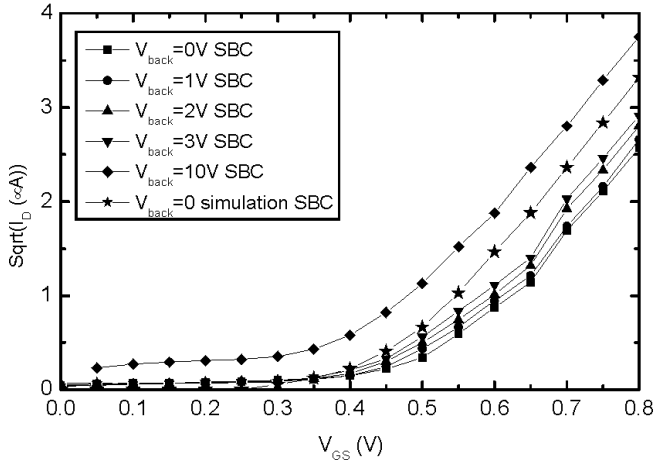




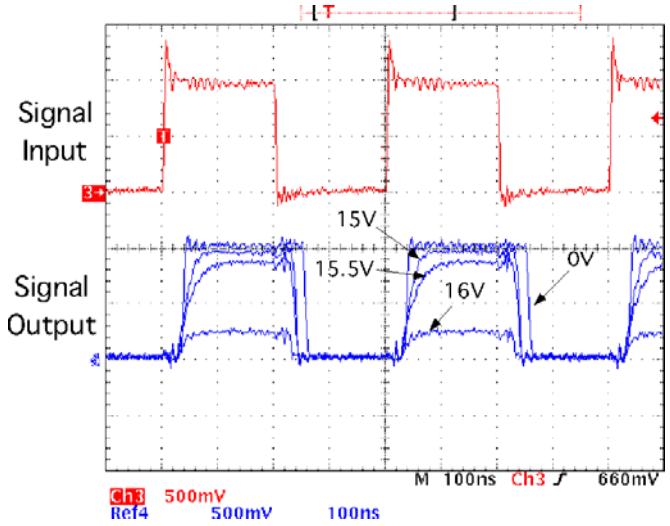


Testing Results

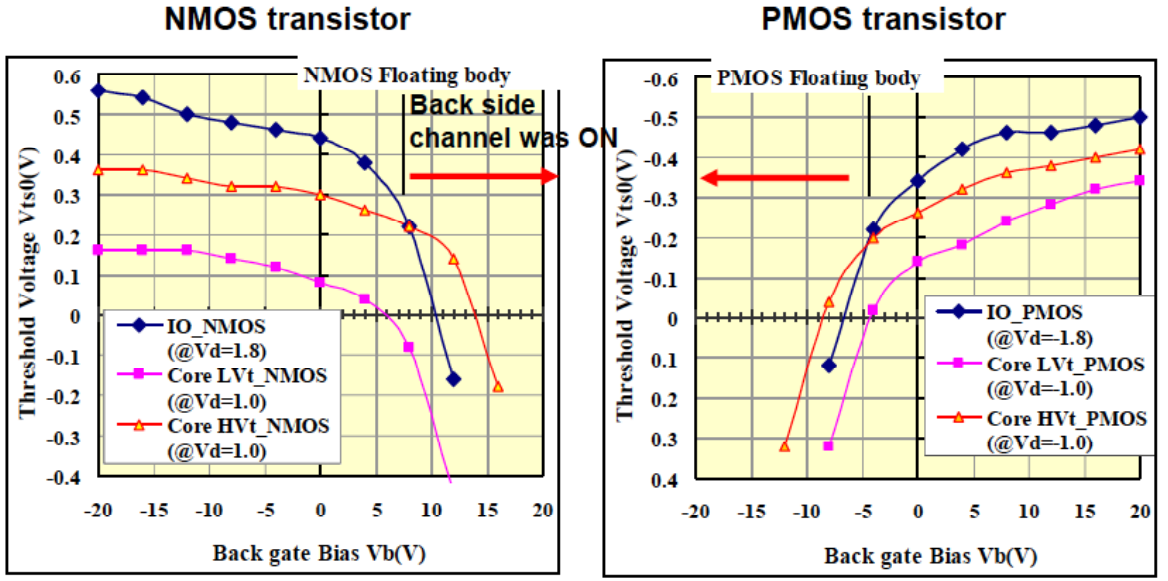
- Analog channel with charge injection by pulse generator OK
- Counter/shift register OK, (proper operation requires back-gate voltage above certain level ~5V due to conflicting leakage of NMOS and PMOS transistors in OFF state)
- Discriminator OK
  - There are substantial back gate effects on transistor operation
  - Full image readout was not achieved
- Problems understood as due to inaccuracy of transistor models and back gate effects
  - OKI process models good to 50%
- Process and limits now understood
- Need to design more conservatively for next run (December 0.2 micron process)



Back Gate in SOI (KEK)



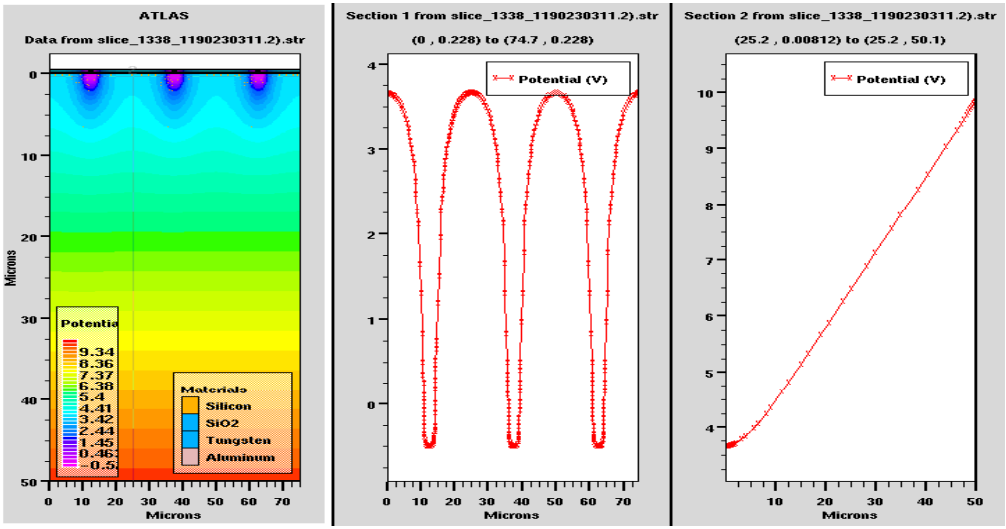
Signal diappears at Vb~16V



Substrate voltage acts as a back gate bias and changes the transistor threshold - like another gate

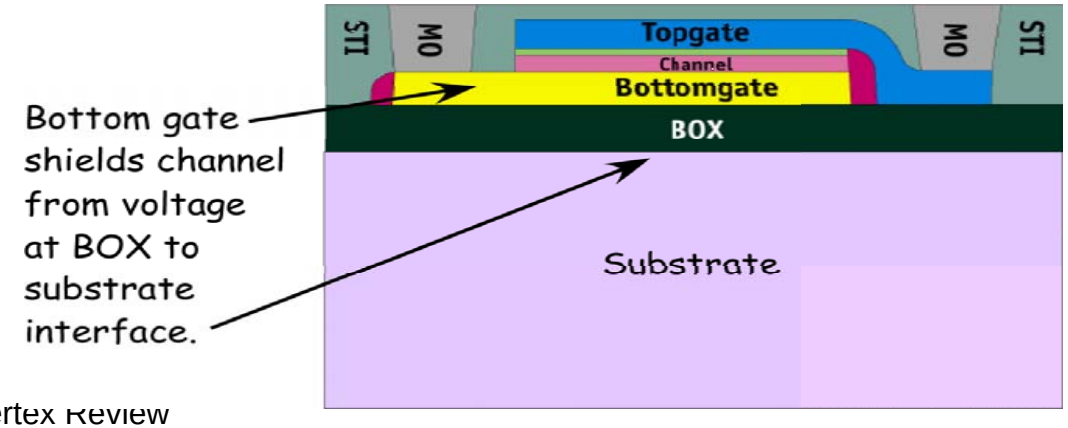
- Requires minimum ~15 micron diode spacing to control surface potential

(from Y. Arai (KEK))



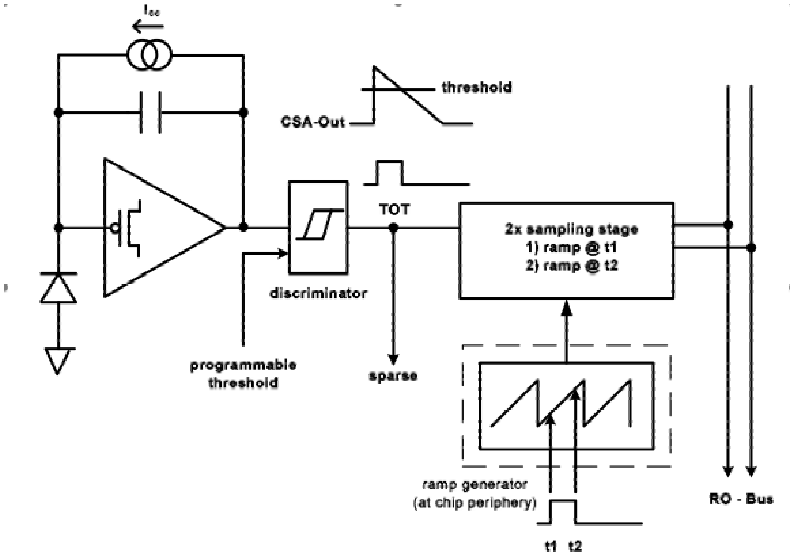
Avoiding the Back Gate

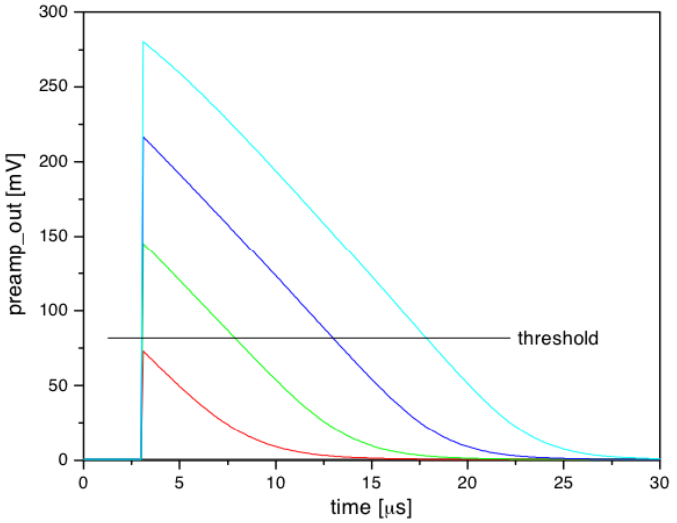
- Use thicker BOX (400 micron in MIT-LL)
- Decrease diode pitch (uses space)
- Use ASI process based on dual gate transistor called a Flexfet.
  - Flexfet has a top and bottom gate.
  - Bottom gate shields the transistor channel from charge build up in the BOX caused by radiation.
  - Bottom gate also shields the transistor channel from voltage on the substrate and thus removes the back gate voltage problem.
  - The process can include a “pinning layer” which can be used to shield the analog pixel from digital activity

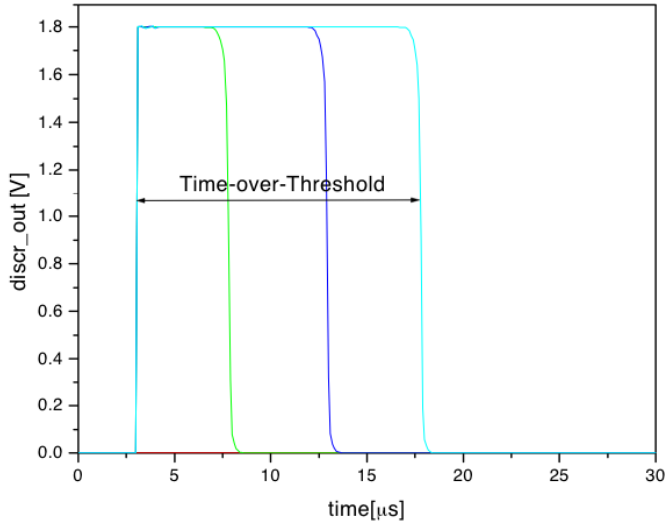


ASI Simulations

- As part of a phase I SBIR with ASI FNAL designed ans simulated a demonstration SOI Pixel cell
  - Voltage ramp for time marker
  - Sample 1 - crossing time
  - Sample 2 - time over threshold for analog pulse height information
  - Additional 3-5 bit counter for coarse



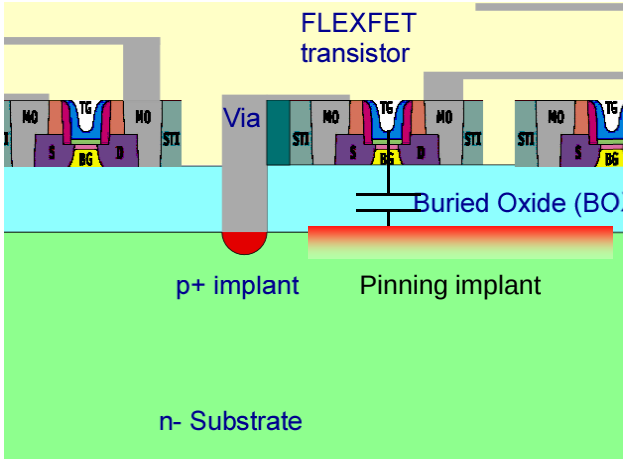


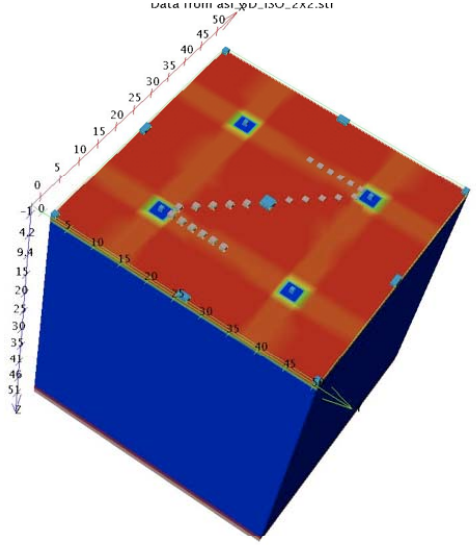


Analog/Digital Coupling

- SOI is sensitive to capacitive coupling of digital signals to pixel
  - Add a “pinning” layer at the surface of the substrate between pixels tied to a fixed potential
  - Layer must be designed to limit back to pinning current (punchthrough)
- Available in ASI, MIT-LL Process
- Simulate 1.8V digital coupling to pixel
- 2D / 3D Silvaco device simulations confirm effectiveness of pinning layer
- But - pinning layer can also increase capacitance, make depletion harder, and trap charge

Condition	Q injected (e)
Unipolar, no pinning	2300
Bipolar, no pinning	~1/3
Unipolar pinned	23
Bipolar, pinned	~0



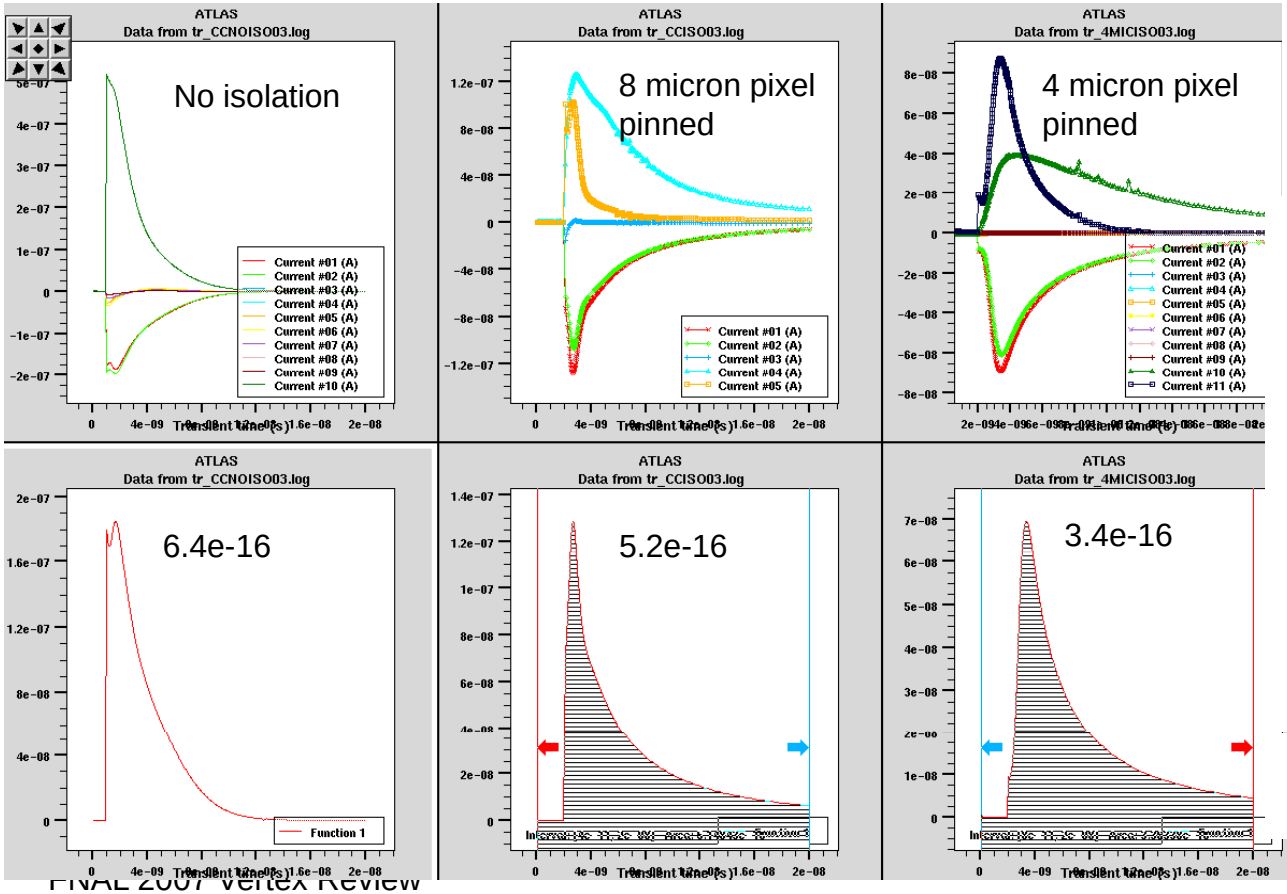


3D model of SOI pixel with injection electrodes

Device Simulation

- Study charge collection, coupling, and diffusion as a function of pixel implant and pinning layer dimensions. Keep bias at 10 V to limit back gate effects. (Silvaco 3D TCAD simulations)

QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.

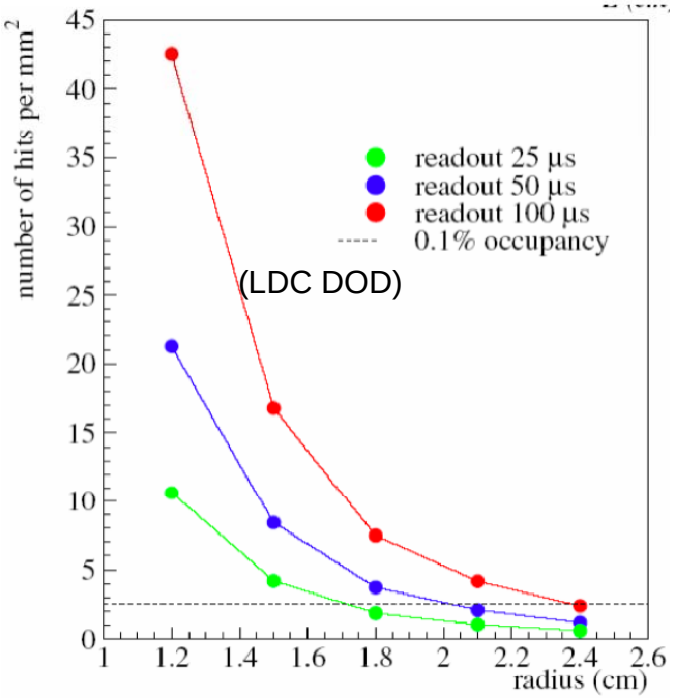


No pinning 10V Bias
8 micron pixels

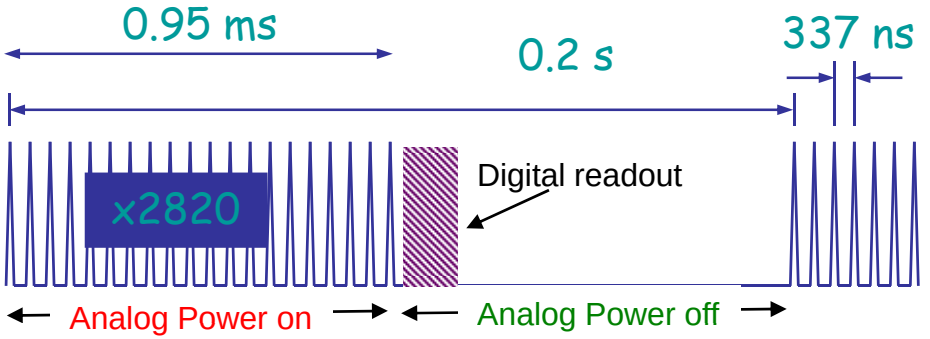
QuickTime™ and a
TIFF (LZW) decompressor
are needed to see this picture.

n+ pinning 10V Bias
8 micron pixels

Time Resolution and Occupancy



- ~200 hits/mm^2/train
  - Considerable uncertainty in projections
  - <1% hit probability per 20 micron pixel
- Sparse scan readout between trains makes sense
  - Need time stamp
  - Single buffer?
- In-pixel sparse scan implementation limited by amount of circuitry which can be integrated in a small pixel
  - Signal/noise
- For frame level readout:
  - 50µs/10^6 pixels ~ 20 GHz clk full RO
  - 50µs/10^3 pixels ~ 20 MHz clk Column Parallel
- 3D/SOI allows high circuit density, full CMOS and a large signal enabling sparse scan and accurate time stamping.



Noise and Power

For pixel amplifier-based devices the FE amplifier usually dominates power consumption:

- Series white noise:

$$ENC^2 = (C_{\det} + C_{gate})^2 \frac{a_1 \gamma 2kT}{g_m t_s}$$

- Noise scales as C and 1/sqrt[transductance (g_m)]
- Pixel front end transistors will operate in weak inversion - where g_m is independent of device geometry and ~(I_d/nV_T).
- Assume 130 μW/mm^2 , 20 micron pixel, duty factor ~ 100
  - 5.2 μW/pixel
  - 3.5 μA @ 1.5 V
- Acceptable low current operation (<1 μA) requires long shaping and/or low node capacitance
  - For t_s = 100ns, I_d=1 μA C_d ~ 100 ff noise ~ 35-50 e
  - ~10 ff should be achievable in SOI devices
- 3D chip designed for ~500 na

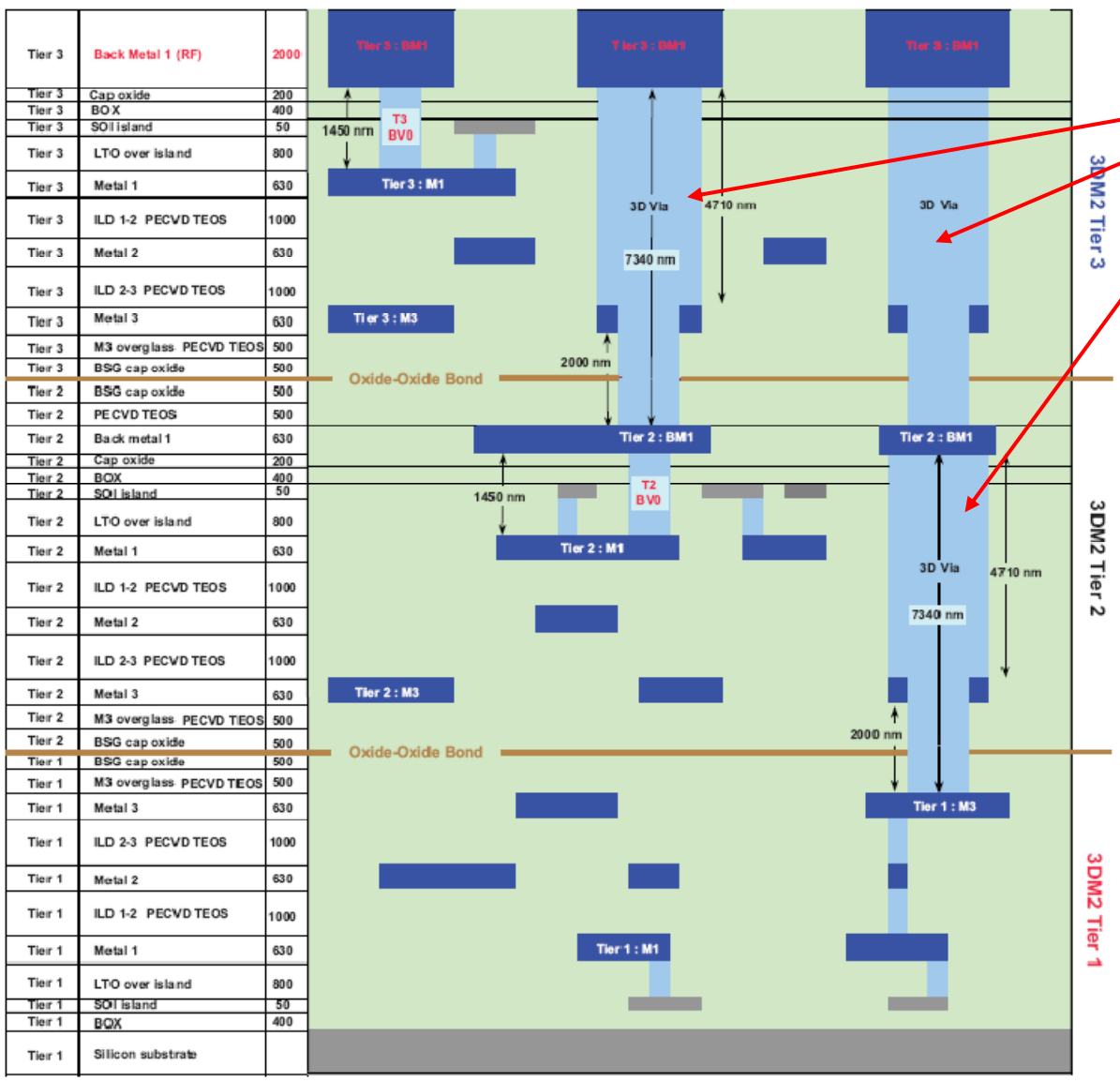
3D Pixel Design for ILC Vertex

Goal - demonstrate ability to implement a complex pixel design with all required ILC properties in a 20 micron square pixel

Previous technologies limited to very simple circuitry or large pixels

- 3D chip design in MIT Lincoln Labs 0.18 um SOI process.
- 3D density allows analog pulse height, sparse readout, high resolution time stamp in a 20 micron pitch pixel.
  - Time stamping and sparse readout occur in the pixel, Hit address found on array perimeter.
  - 64 x 64 pixel demonstrator version of 1k x 1K array.
  - Submitted to 3 tier DARPA multi project run. Sensor to be added later.
- Low power front end 1875 $\mu W/mm^2$ x DF

MIT-LL 3D Multiproject Run Chip Cross Section



Tier 3	Back Metal 1 (RF)	2000
Tier 3	Cap oxide	200
Tier 3	BOX	400
Tier 3	SOI island	50
Tier 3	LTO over island	800
Tier 3	Metal 1	630
Tier 3	ILD 1-2 PECVD TEOS	1000
Tier 3	Metal 2	630
Tier 3	ILD 2-3 PECVD TEOS	1000
Tier 3	Metal 3	630
Tier 3	M3 overglass PECVD TEOS	500
Tier 3	BSG cap oxide	500
Tier 2	BSG cap oxide	500
Tier 2	PECVD TEOS	500
Tier 2	Back metal 1	630
Tier 2	Cap oxide	200
Tier 2	BOX	400
Tier 2	SOI island	50
Tier 2	LTO over island	800
Tier 2	Metal 1	630
Tier 2	ILD 1-2 PECVD TEOS	1000
Tier 2	Metal 2	630
Tier 2	ILD 2-3 PECVD TEOS	1000
Tier 2	Metal 3	630
Tier 2	M3 overglass PECVD TEOS	500
Tier 2	BSG cap oxide	500
Tier 1	BSG cap oxide	500
Tier 1	M3 overglass PECVD TEOS	500
Tier 1	Metal 3	630
Tier 1	ILD 2-3 PECVD TEOS	1000
Tier 1	Metal 2	630
Tier 1	ILD 1-2 PECVD TEOS	1000
Tier 1	Metal 1	630
Tier 1	LTO over island	800
Tier 1	SOI island	50
Tier 1	BOX	400
Tier 1	Silicon substrate	

3D vias

8.2 μm

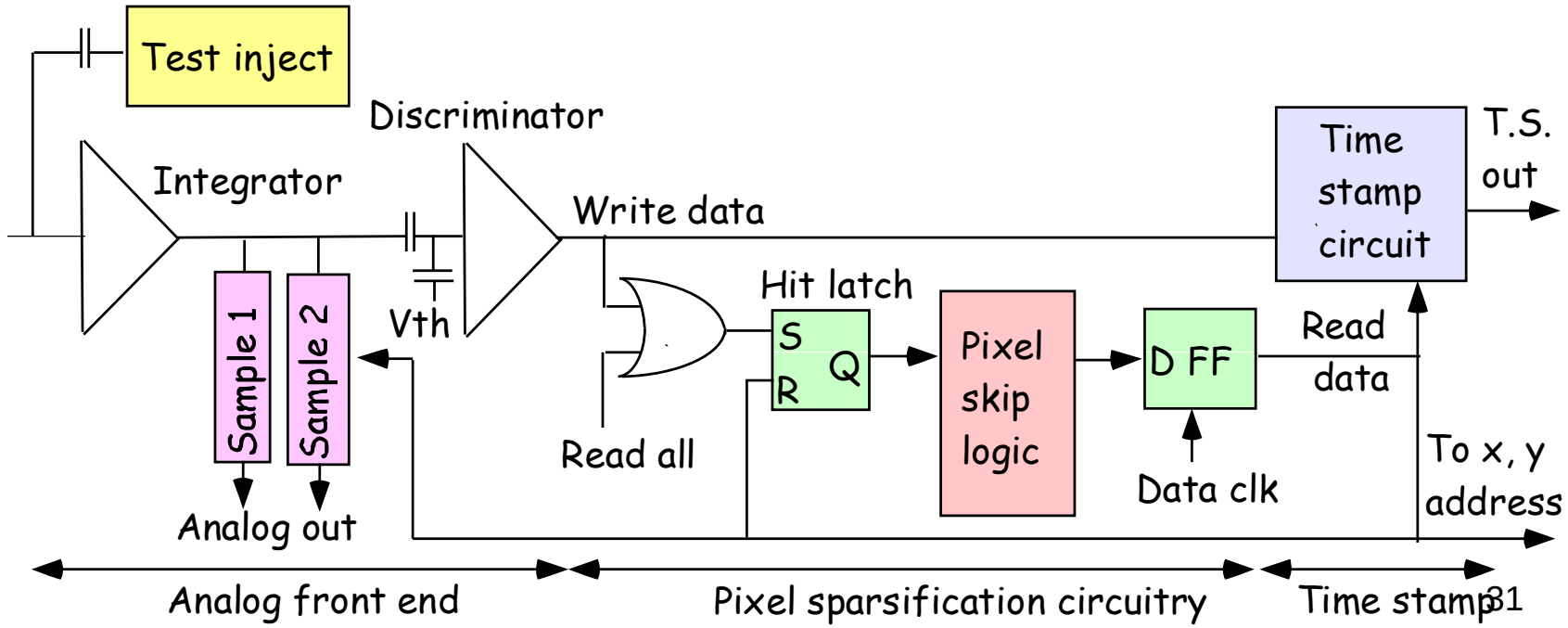
7.8 μm

6.0 μm

Three levels of transistors, 11 levels of metal in a total vertical height of only 22 um.

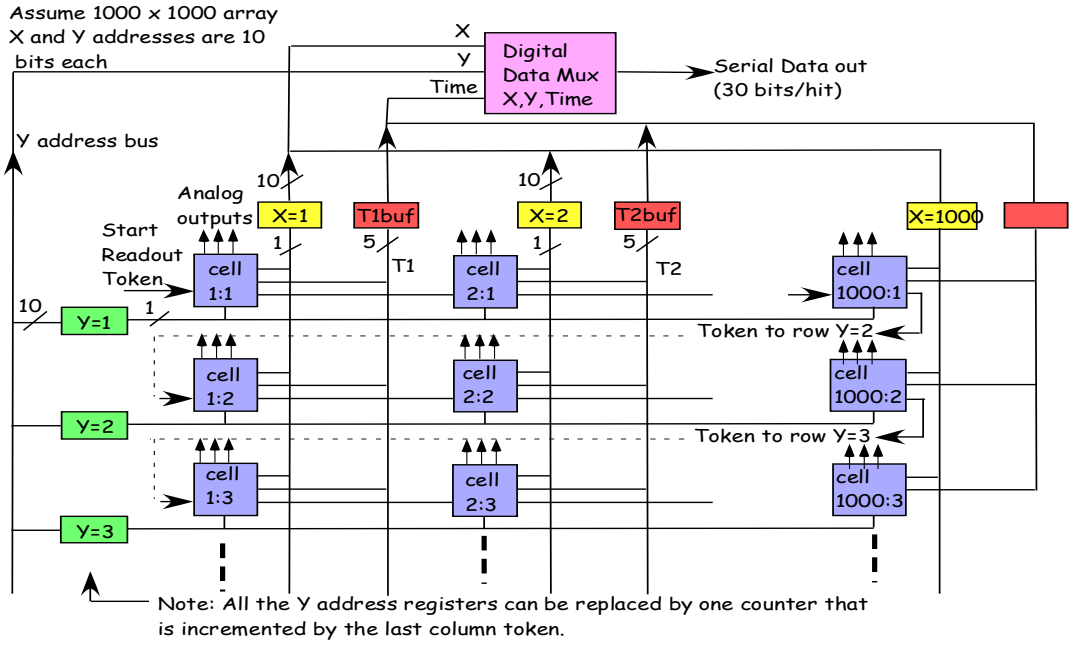
Simplified Pixel Cell Block Diagram

- Baseline is stored before train in sample 1. When a hit occurs, the hit pixel stores samples 1 & 2 and the time stamps, and sets the hit latch in sparse readout circuit.



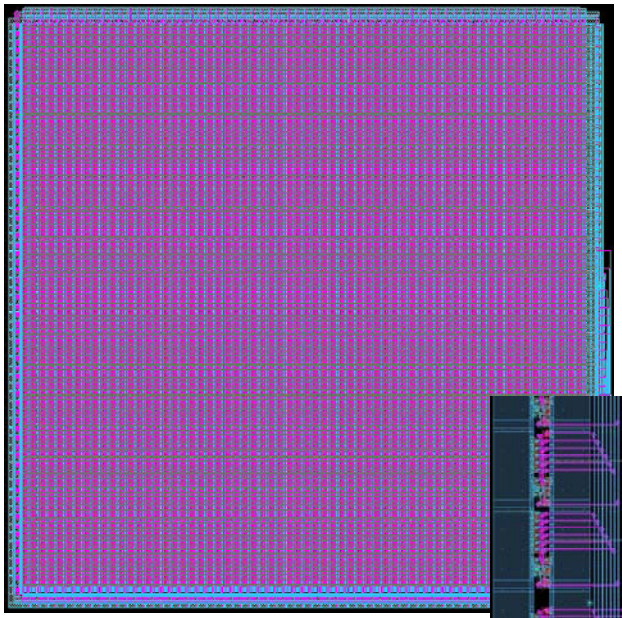
Readout Timing

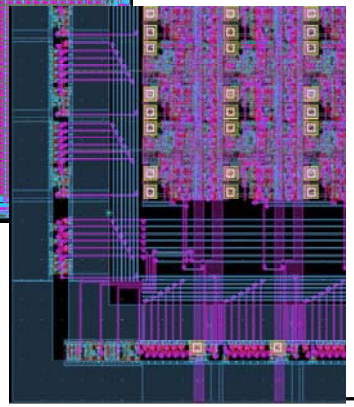
- During data acquisition, hit sets a latch.
- Sparse readout row by row.
- To start readout, all hit pixels are disabled except the first hit pixel in the readout scan.
- The pixel being read points to the X address and Y address stored on the perimeter and at the same time outputs the Time Stamp and analog information from the pixel.
- While reading out a pixel, a token scans ahead looking for next pixel to readout.



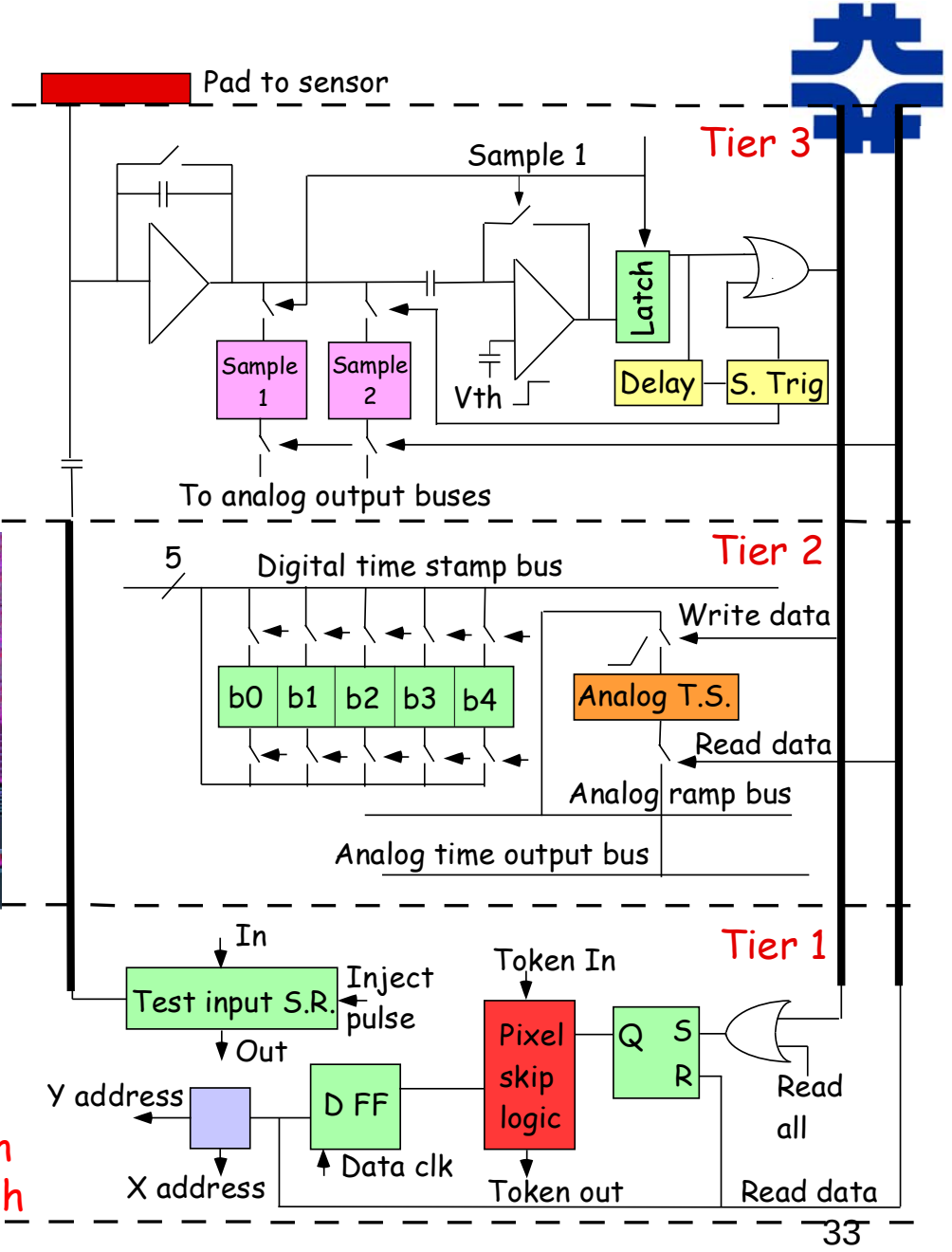
- Chip set to always readout at least one pixel per row in the array.
- Assume 1000 x 1000 array (1000 pixels/row)
  - Time to scan 1 row = .200 ns x 1000 = 200 ns (simulated)
  - Time to readout cell = 30 bits x 20 ns/bit = 600 ns
- Max hits/chip = 250 hits/mm^2 x 225 mm^2 = 56250 hits/chip.
- For 50 MHz readout clock and 30 bits/hit, readout time = 57250 hits x 30 bits/hit x 20 ns/bit = 34 msec

3D Geometry

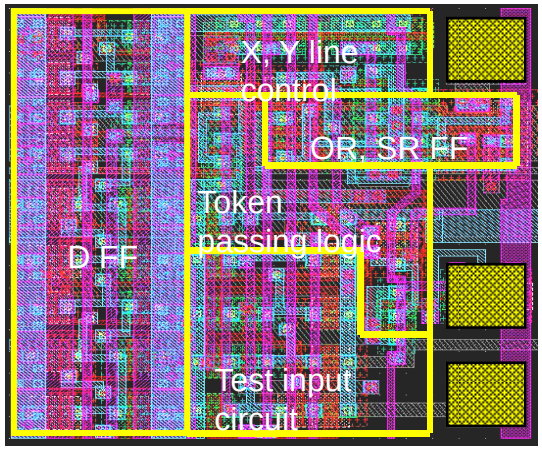


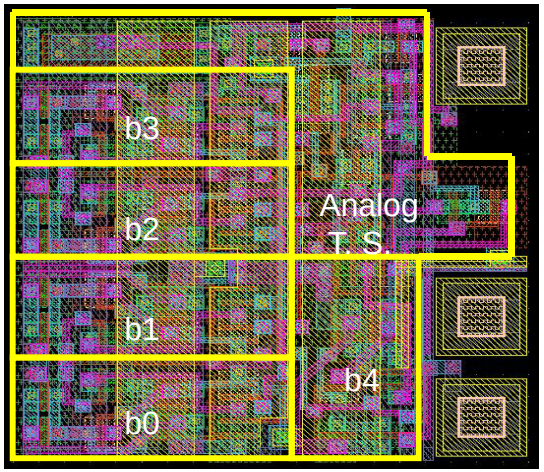


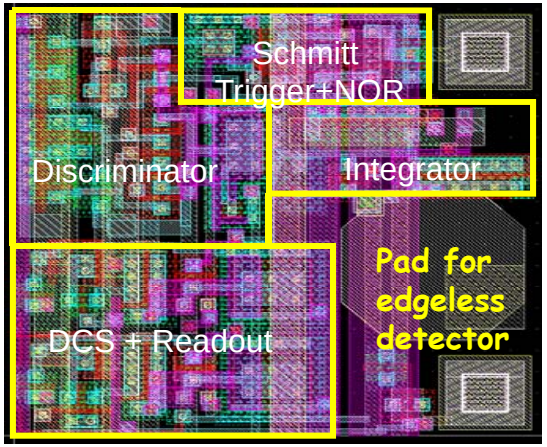
Chip designers:
Tom Zimmerman
Gregory Deptuch
Jim Hoff



- Tier 1
  - OR for READ ALL cells
  - Hit latch (SR FF)
  - Pixel skip logic for token passing
  - D flip flop (static), conservative design
  - X, Y line pull down
  - Register for programmable test input.
  - Could probably add disable pixel feature with little extra space
  - 65 transistors
  - 3 via pads
- Tier 2
  - 5 bit digital time stamp
  - Analog time stamp – resolution to be determined by analog offsets and off chip ADC
  - Gray code counter on periphery
  - 72 transistors
  - 3 vias
- Tier 3
  - Integrator
  - Double correlated sample plus readout
  - Discriminator
  - Chip scale programmable threshold input
  - Capacitive test input
  - 38 transistors
  - 2 vias 1.5 µm dia by 7.3 µm long

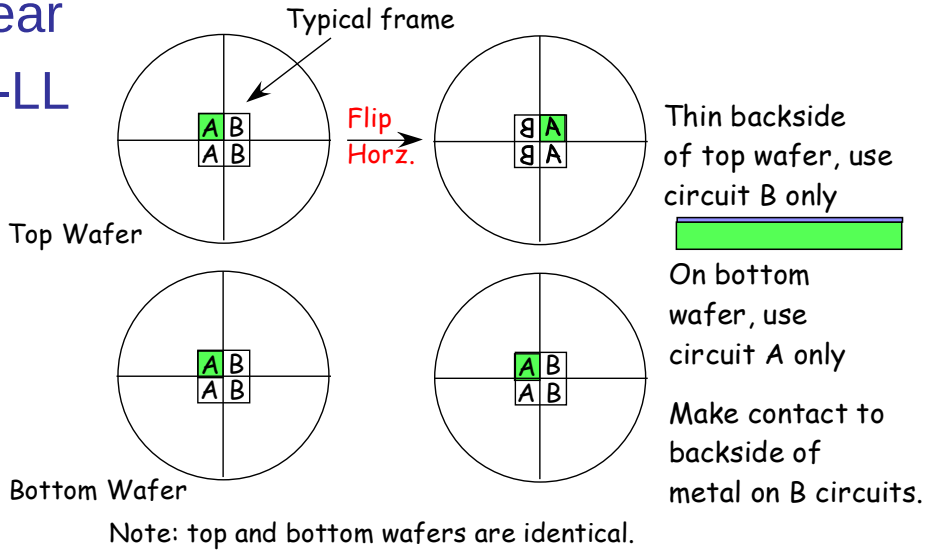






Future 3D Work

- 3rd DARPA run expected next year
- Considering dedicated HEP MIT-LL multiproject run
  - Exploring interest, funding and technical options
- Reduce costs for R&D
  - Two circuit tiers
  - Sensor on SOI handle
  - Use results from 2 DARPA runs and test structure measurements
- CuSn structures with RTI
- Collaboration with other groups beginning 3D work



Power Distribution

- Peak and average power are both crucial issues for the vertex detector
- Power pulsing for FE chips - just turn power on during 0.95/200 ms
  - Maximum duty factor ~200, assume ~100 may be practical 2000 W=> 20 W (average)
  - But I_{peak} is still the same - 2000A if we saturate the 20W limit
- Similar problems for most other technologies
- High peak currents => more conductor to limit IR drop => Mass
- Serial powering or DC-DC conversion can lower instantaneous current
  - Peak currents reduced by number of modules per string
  - Local regulation relaxes the IR constraints
  - Conductor volume set by IR drop is reduced
  - Forces due to BxI reduced
- Most work on serial power to date has been done by ATLAS for sLHC,ATLAS power loss in cables 2-3x detector power
- We believe that this and power cycling will be an increasingly important component of ILC vertex R&D

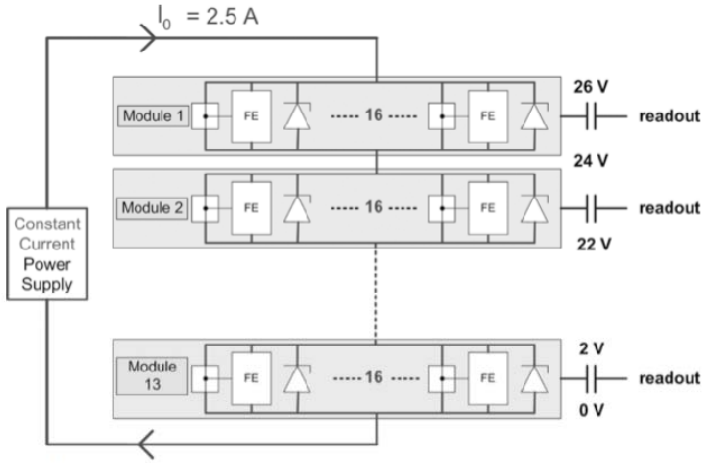
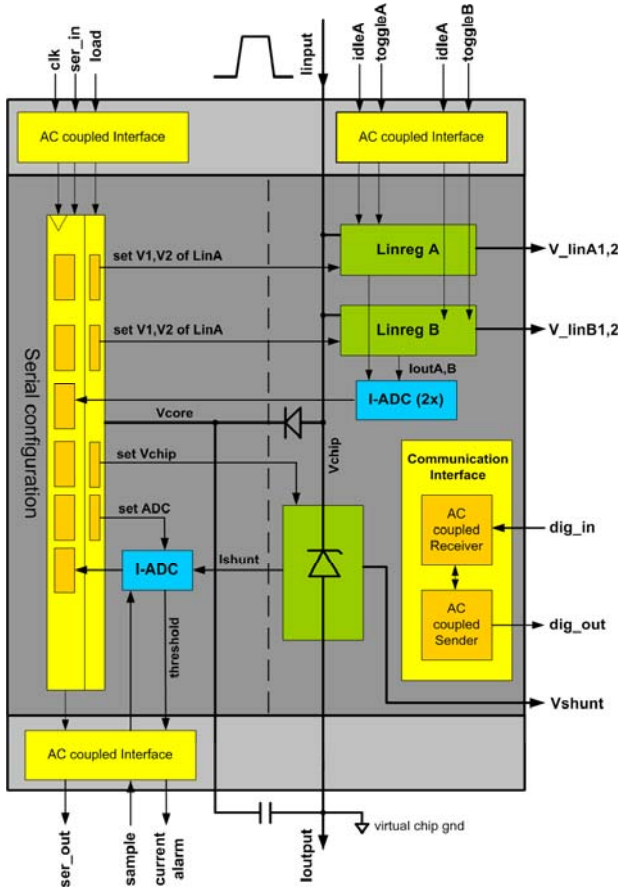


Fig 1. Basic scheme of serial powering. A power supply provides a constant current which is fed into a chain of modules. In each module a shunt generates a constant voltage from the constant current. Additional linear regulators are used if more than one supply voltage is needed.

Atlas SLHC design

Serial Power

- Fermilab is designing a serial powering chip in collaboration with Penn/RAL
  - Design of a shunt regulator being capable of regulating up to 1A @ 2.5V
  - 2 linear regulator (analog and digital) with up to 1A, idle feature, switchable between two downloadable voltages (power pulsing)
  - Core voltage for chip control (1.5 to 2.5V)
  - ADCs read back shunt and Linreg current
  - Current alarm (programmable threshold)
  - AC coupled interface
  - TSMC 0.25 micron (radtolerent design)
- Concerns:
  - Increased vulnerability to failures in the string
  - Increased coherent noise sensitivity due to lack of ability to interconnect local grounds with low impedance (ok in initial ATLAS tests)
  - Increased interconnect complexity, bias distribution
  - AC isolation to readout (optical)
  - Current balance and torques



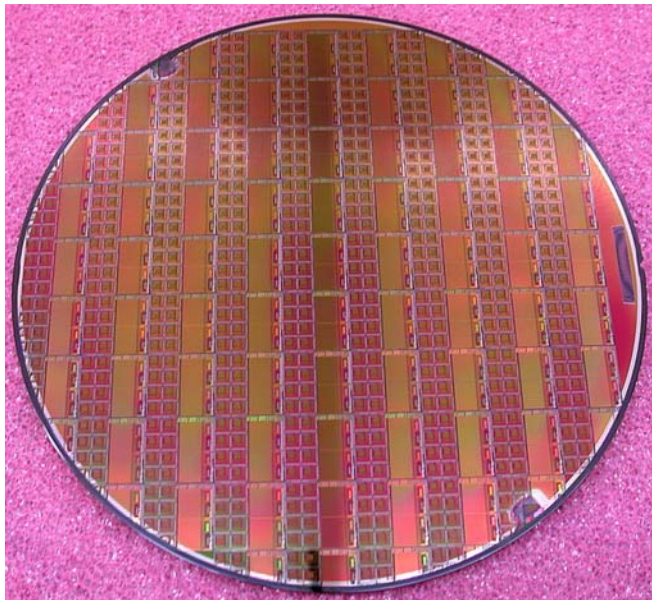
FNAL serial powering chip concept

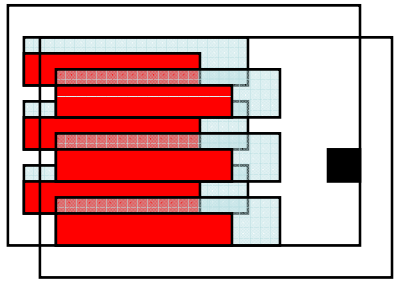
(M. Trimpl)

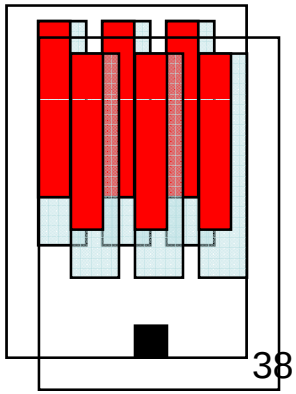
Test Beam Telescope

- Fermilab 120 GeV test beam

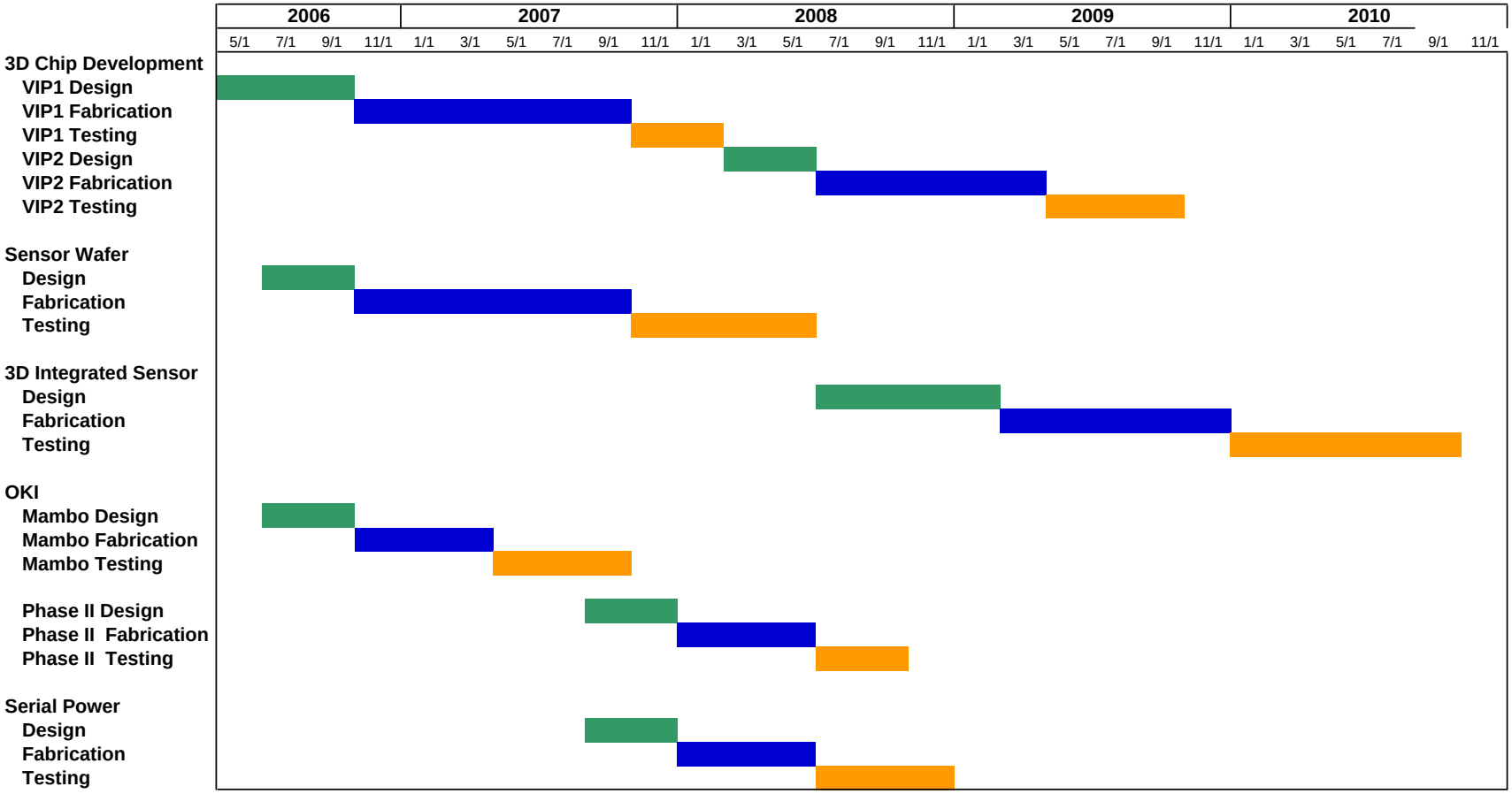
- FPIX (BTeV) pixel telescope under construction
- Hybrid pixel telescope will measure every beam particle with good timing and moderate precision (5-10 μm).
  - Station = two half-planes offset by active area of sensor read out by 1 FPGA
  - 2 stations upstream of DUT & 2-4 downstream (precision x & precision y)
- Anticipate the addition of one station with very high precision (& probably much less good time resolution), such as MAPS







Electronics R&D Schedule



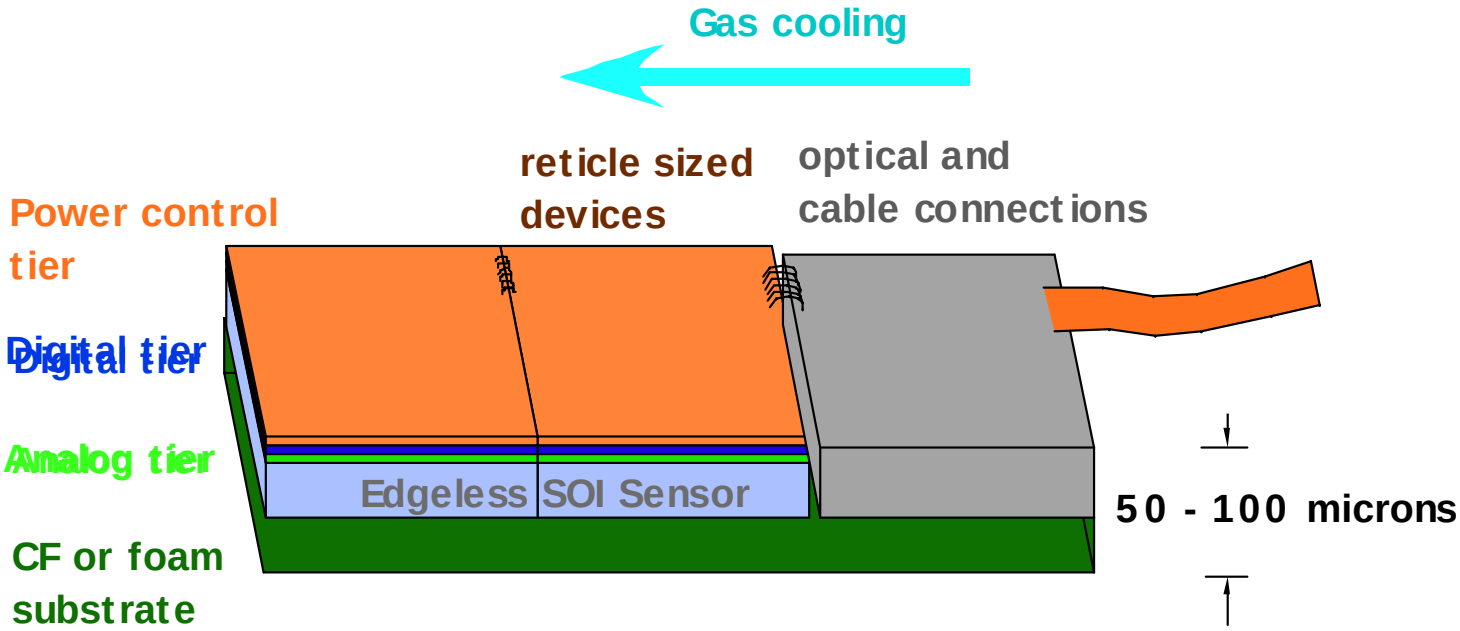
Collaboration

- This work, although focused on ILC has other (perhaps shorter term) applications
  - Synchrotron radiation x-ray detectors
  - Electron microscopes
  - Medical
  - LHC
    - Thinned detectors for radiation hardness
    - Serial powering
    - SOI
  - RHIC
- The collaboration is focused on developing technology for a variety of applications - the only way to keep ILC R&D healthy in an indeterminate time scale.

Summary of Work

- SOI
  - Tests of Mambo (FNAL)
  - MIT-LL test structures (Bergamo, FNAL, Purdue)
  - OKI test structure irradiation (Purdue)
  - ASI sensor SBIR (FNAL,Purdue,Cornell)
  - OKI wafer thinning and laser anneal (FNAL, Cornell, Purdue, U. Chicago)
  - Mambo II (FNAL)
- 3D
  - FPIX thinning studies (FNAL, RTI, IZM)
  - VIP1 chip testing (FNAL)
  - Cu-sn bonding (FNAL,RTI)
  - VIP2 design
  - 3D dedicated multiproject run
- Sensor
  - MIT-LL device testing (FNAL, Brown, Syracuse, Boston U.)
- Power
  - Serial power chip (FNAL, Penn, RAL)
  - Serial and pulsed power tests (FNAL(CMS)…)
- Test Beam

3D Ladder



- Detector goal
  - Edgeless or stitched 50μ thick fully depleted reticle-sized sensors
  - 3D integration of analog, digital and power control tiers
  - Optical signal coupling
  - Smart pulsed serial powering