LCTPC
“Advanced Endplate”
(Discussion)

LC TPC Meeting at ALCGP07

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LC TPC

After the Large Prototype-I test,
some of the important issues may still remain:

- Methods and their demonstrations of the precision correction for the ion disks of “high density” (with any other distortion).
- **Endplate flip-chip mounted with LC TPC readout electronics chips.**
- Engineering design.

- Decisions on the technologies.

Advanced Endplate: LC TPC Electronics

We had the presentations of readout electronics by Luciano and his company and Eric at the LC TPC meeting in Paris (Oct. 11)

- **The "General purpose charge readout chip" (Luciano) is in progress. The 10 bit pipeline ADC is tricky, but the design is available in market if necessary. This is a solution of straight forward.**

- **When a zero suppression mechanism is implemented to minimize the size of analog memories, the "AFTER" approach (Eric) may be another option.**

Please see their slides in:
http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2260

Programmable Charge Amplifier

Programmable Charge Amplifier submitted in May

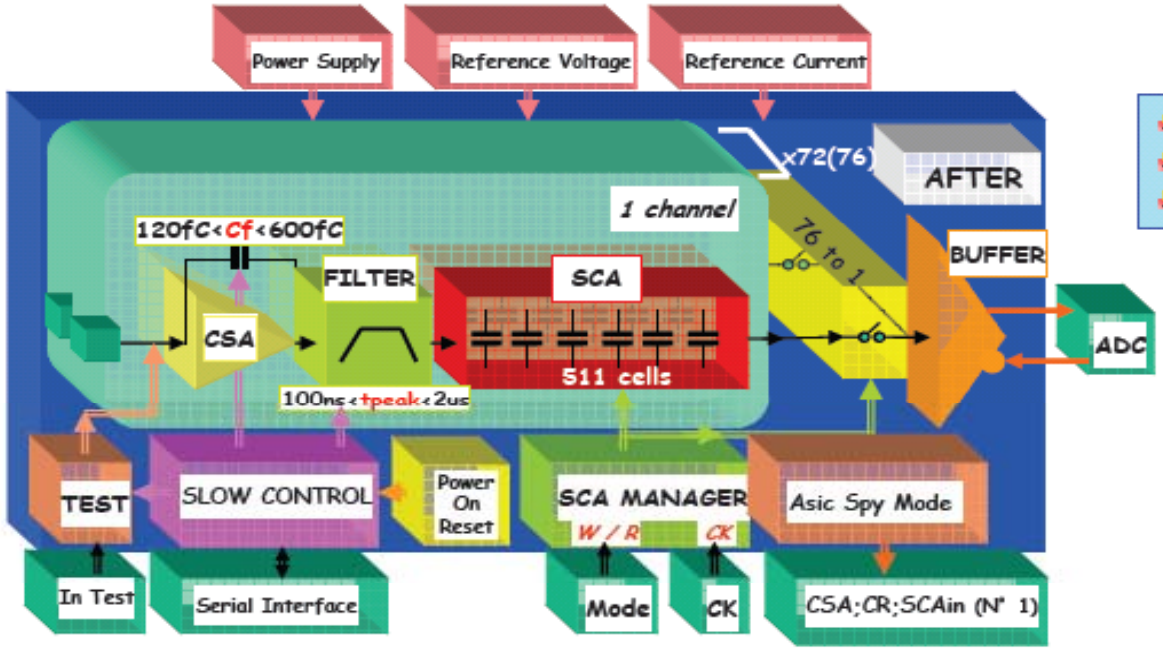
- 1.5 V Supply, power consumption < 8 mW / channel
- 16 channel charge amplifier + anti-aliasing filter
- Single ended preamplifier
- Fully differential output amplifier
- Both signal polarities
- Power down mode (wake-up time = 1 ms)
- Programmable peaking time (30 ns – 120 ns) – 3rd order semi Gaussian pulse shape
- Programmable gain in 4 steps (12 – 27 mV/fC)
- Preamp_out mode
- Tunable time constant of the preamplifier
- Submitted in May
- Silicon back in September
- Delivery of packaged chips in October

AFTER Main Features

dapnia SEDI

cea

saclay



- No zero suppress.
- No auto triggering.
- No selective readout.

Main features:

- **Input Current Polarity:** positive **or** negative
- **72** Analog Channels
- **4** Gains: 120fC, 240fC, 360fC & 600fC
- **16** Peaking Time values: (100ns to 2µs)
- **511 analog memory cells / Channel:**
  Fwrite: 1MHz-50MHz; Fread: 20MHz

- **Slow Control**
- **Power on reset**
- **Test mode:**
  calibration or test **[channel/channel]**
  functional **[72 channels in one step]**
- **Spy mode on channel 1:**
  CSA, CR or filter out

Advanced Endplate: LC TPC Electronics

The IC area (die size) is small enough for the direct mounting on the endplate (Luciano) .
(the General purpose charge readout chip)

Considerations on readout plane

IC Area (die size)

- 1-2 mm^2 /channel
  - Shaping amplifier 0.2 mm^2
  - ADC 0.6 mm^2 (estimate)
  - Digital processor 0.6 mm^2 (estimate)
- in the following we consider the case of 1.5mm^2 / channel
- 64 ch / chip ➡ ~ 100 mm^2

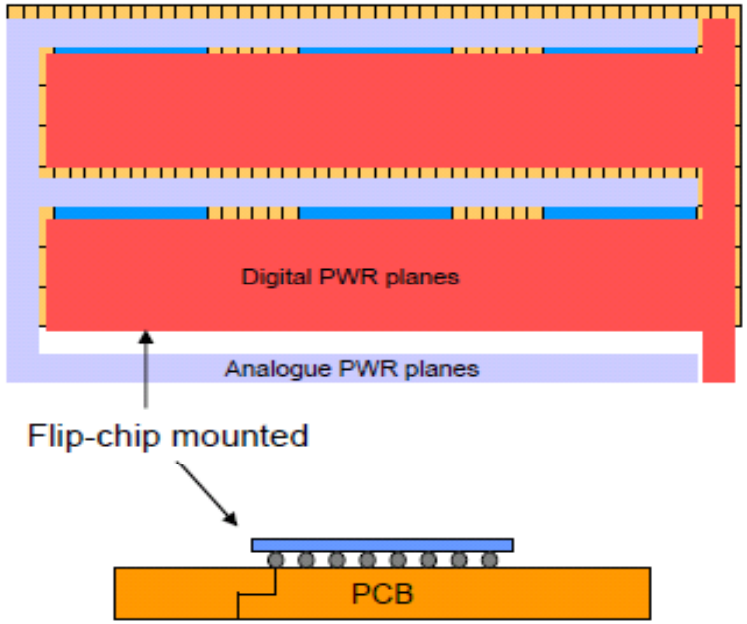
Area of the chip on the PCB: 14 x 14 mm^2 / chip ⇨ ~ 3 mm^2 / pad

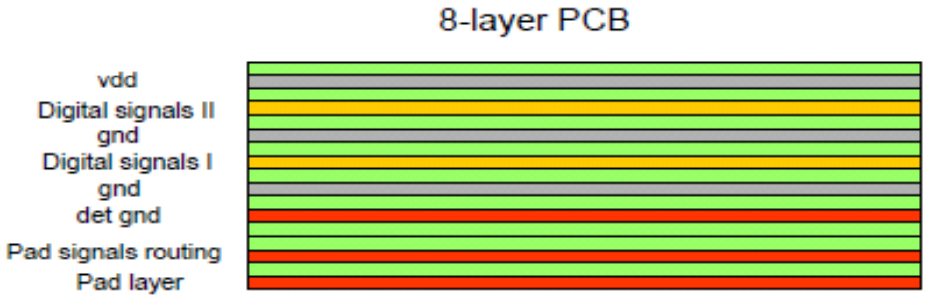
PCB dimensions < 40 x 40 cm^2 ⇨ ~53000 pads, ~800 FE chips / board

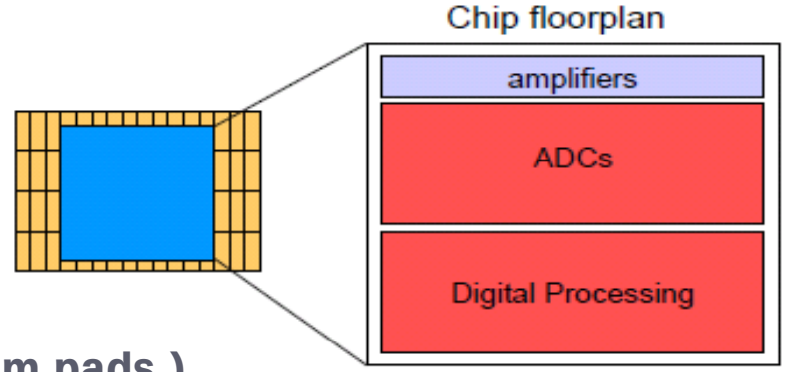
Advanced Endplate: Endplate

Considerations on readout plane

PCB topology and layer stack-up







(This is an extreme case with 1 mm x 3 mm pads.)

Advanced Endplate: Electronics

To get complete LC TPC readout schemes:

- **The signal processing on board (the endplate or in TPC) has to be defined, and**
- **The data link between the chips and the optical link from TPC have to be integrated in the designs.**

  -> Need also some space on the endplate, or we may have another idea (3D chip) (Luciano). The power of the fast optical link may be an issue.

  -> There are the recent progresses of the high speed data links such as Space Wires, GBT(CERN/LHC), PCI Express and also the high density interconnects such as the 3D system integration which may be beneficial to us.

Advanced Endplate: Electronics

Considerations on readout plane

Power consumption

- amplifier 8 mW / channel
- ADC 30 mW / channel
- Digital Proc 4 mW / channel
- Power regulation and links 10 mW / channel
- duty cycle: 1%

← power switching / power delivery

- average power / channel ~ 0.5 mW / channel
- average power / m^2 167 W

← cooling

- **The power delivery network with capacitors** has to be examined to avoid the large transient spikes to destroy the front-end electronics (See the slides by Luciano).
- **The cooling**: Is air enough? May need special structures of the PCB board to prevent the heat goes into the TPC gas volume via bumps? In the case of accidents (Failure of the power cycling, latch up etc?

Advanced Endplate

My conclusion and proposals

A systematic R&D of the PCB pad plane with flip-chips electronics is urgent.

A basic design of the whole readout electronics including data transfer.

A design of the pad PCB plane with the flip-chip assembly.
Simulations of power delivery, cooling and thermo mechanical features, and
Tests of pad PCB plane models mounted with dummy chips.

We need a group of electronics/mechanics experts together with some LC TPC physicists to work on the R&D systematically. (Luciano seems to be too busy to lead this task by himself, which is unfortunate for us) (*)

(*) The CDC group have one such volunteer, Dr. Takahiro Fusayasu, an electronics person at NIAS, probably helped by Drs. H. Ikeda and Y. Arai inside Japan. We may cooperate with some space companies if we get fund for it.

Some information

Some institutes (you know probably) and some space companies should be knowledgeable about the light structures and cooling, though they may be expensive:

http://www.ihi.co.jp/ia/
http://www.ntspace.jp/
http://www.mhi.co.jp/nasw/index.html

http://www.alenia-aeronautica.it/ (EUSO)

(More companies probably in Europe and US.)

Inter-chip data links and 3D chip (Sorry, the selection is not systematic):

Space wires:
http://www.spacewire.esa.int/content/Home/HomeIntro.php
GBT and 3D integration etc:
http://indico.cern.ch/conferenceTimeTable.py?confId=11994
3D chip: http://indico.in2p3.fr/conferenceDisplay.py?confId=400