Special requirements for ILC TPC Electronics

LCTPC meeting

ALCPG007 Workshop

Fermilab, Oct 21, 2007

J.P. Martin, University of Montreal

R&D program,history and future

1999

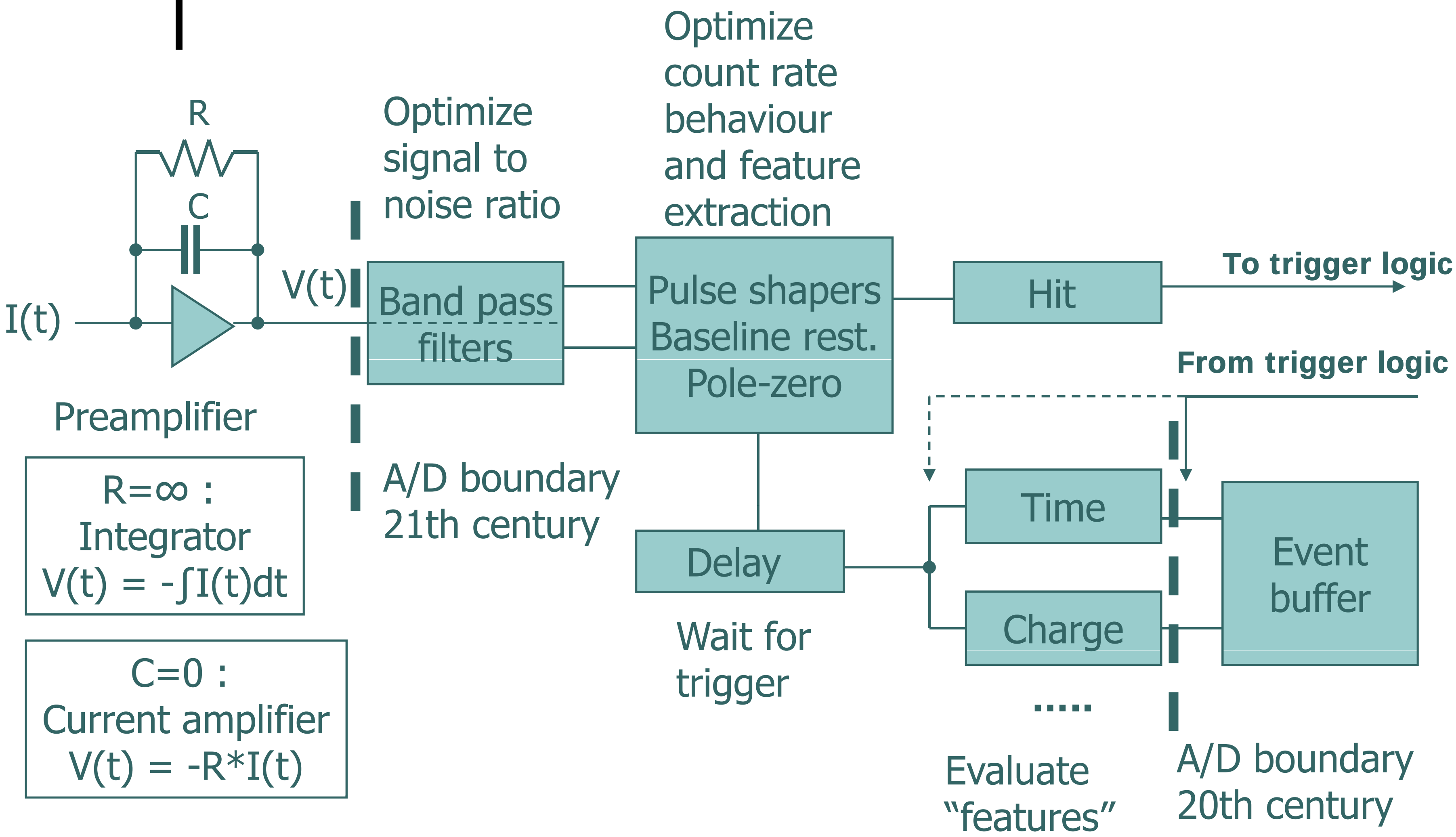
2007

2010

2017

Detector	Electronics
Prototype TPCs (Carleton-Victoria) - Gas studies - Pad design studies - MPGDs - Resistive film	**Designed for R&D requirements** - 200 MHz VME FADCs - Adapt legacy material (ALEPH,STAR) - High density 48 channel cards (65 MHz VF48)
« LC TPC » -Anode pad modules Gem + small pad MicroMgas + resistive film	**Objective: Produce a Realistic model for electronics** using existing ASICS and off the shelf components - Optimize for detector requirements - Address heat management
Final detector	**Objective: Integrated electronics** - ASIC

Typical tracking detector readout elements



Preamplifier requirements

The density of collected electrons is inhomogeneous (effect of the finite number of primary clusters)
-The time structure is different in adjacent pads for the same track
- There is an statistical error dependent on 1/SQRT(Number of clusters) over the pad

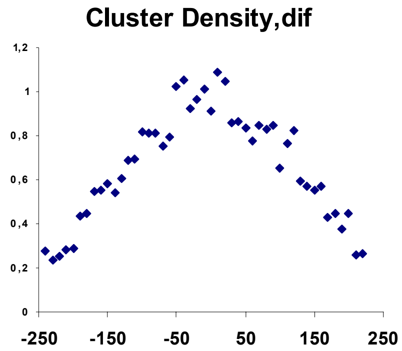
→ Account for every cluster without bias, irrespective of their time of arrival
Make the charge evaluation independernt of the time structure

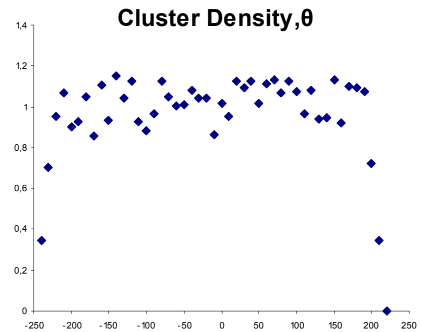
- There is an additional uncorrelated error due to the electronic noise

→ The GEMs or MicroMegas are operated at low gain to reduce the positive ion backflow. Low noise preamplifiers are mandatory

Time structure of the pad signals in a large TPC

- Case 1: Track almost parallel to the pad plane =>
  The electrons drift for a long distance (meters) =>
  Longitudinal diffusion (200 – 500 ns, gaussian)
- Case 2: The track passes close to the pad =>
  It has a large θ angle =>
  Spread in arrival times (>500 ns, uniform)





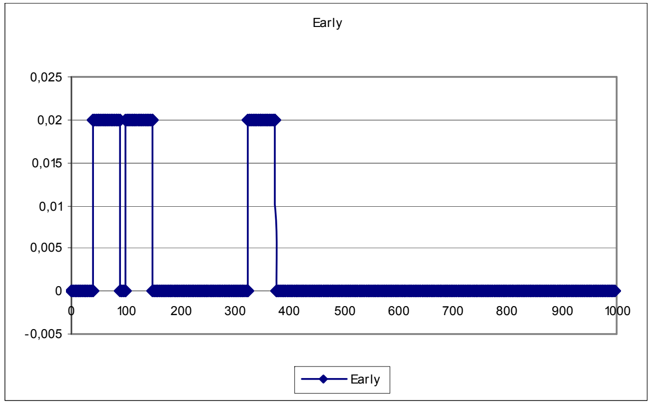
- All cases: Transit time of electrons in the induction gap : adds 50-100 ns for GEM)

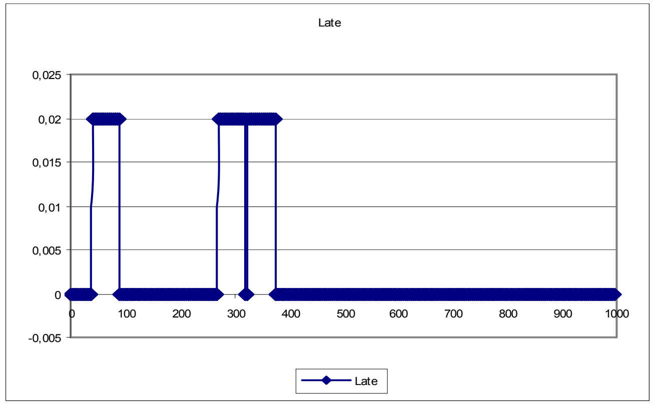
Bottom line: - The charge collection process at the pads is long
- It varies significantly from track to track

Charge collection time structure artefacts

Exemple: collection of 3 unit charge clusters with a different time structure on 2 adjacent pads

Pad current, 50 ns gap, diffusion in gap neglected.

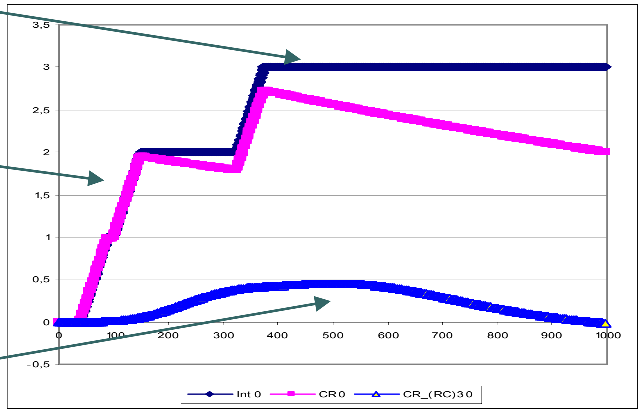


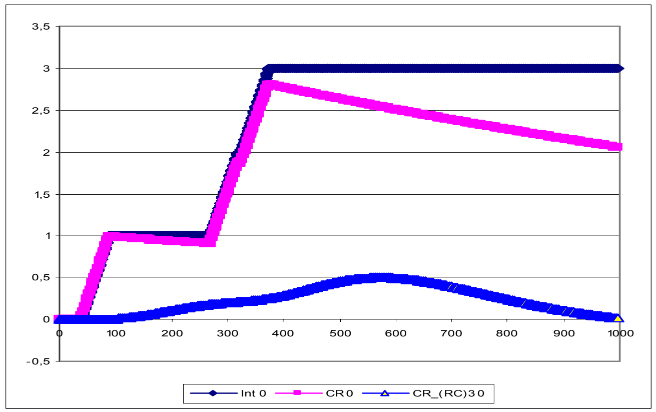


Current integral

Preamp decay: 2µs

CR-(RC)³ shaper peaking time: 300 ns

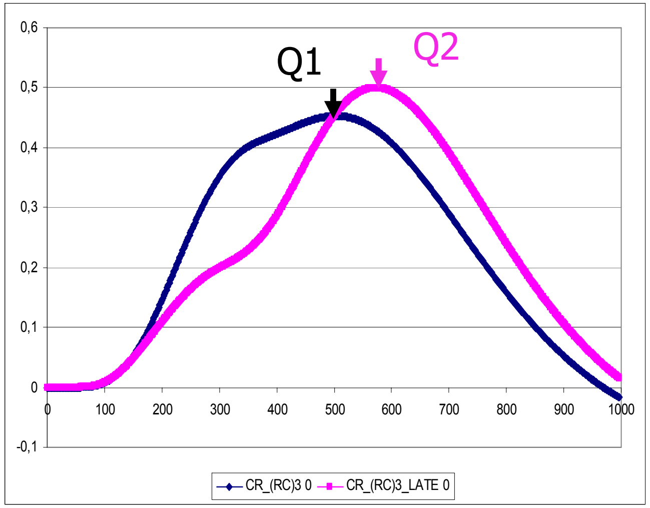


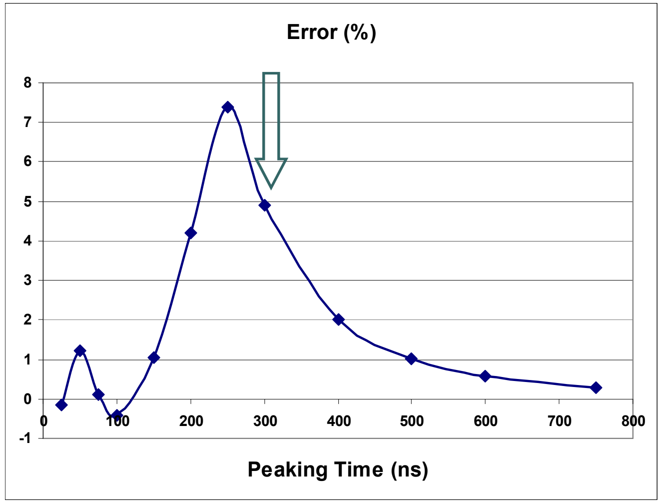


Signal at shaper output

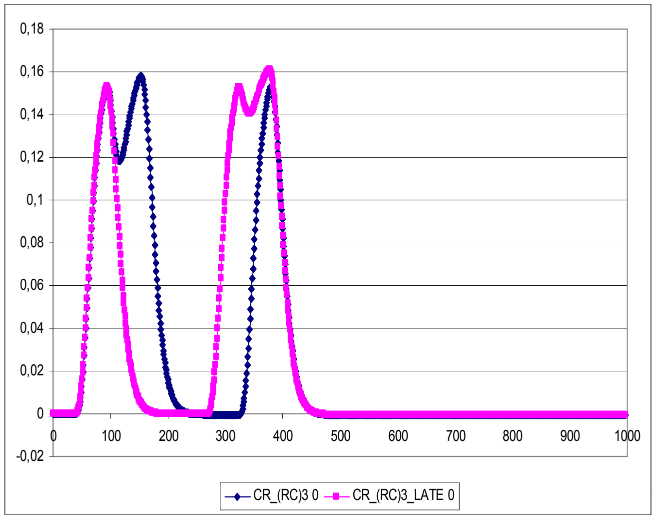
Err% = 100*(Q2-Q1)/(Q2+Q1)

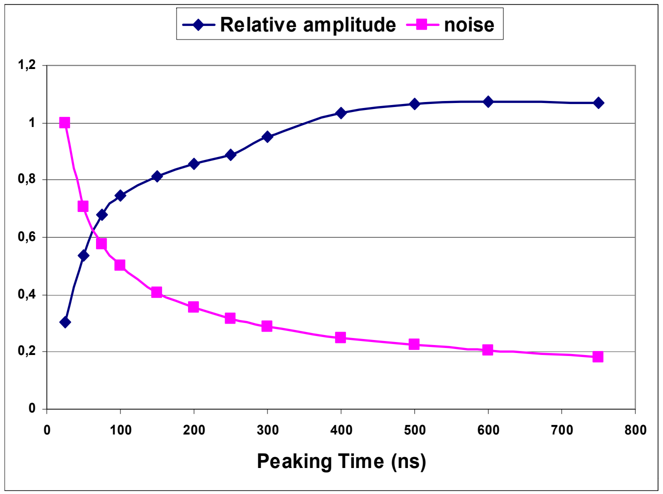
Shaper Peaking time: 300 ns





Shaper Peaking time: 25 ns





Typical digital signal processing

« Moving window deconvolution » FIR transform:

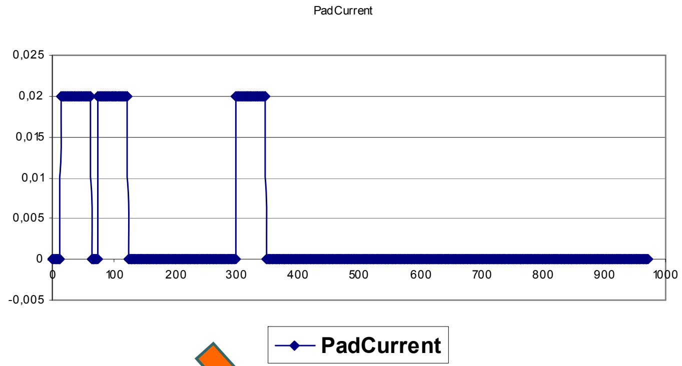
$$N_k = A_k - A_{(k-w)} + (1/TauPreamp)*\sum_{i=1,w} A_{(k-i)}$$

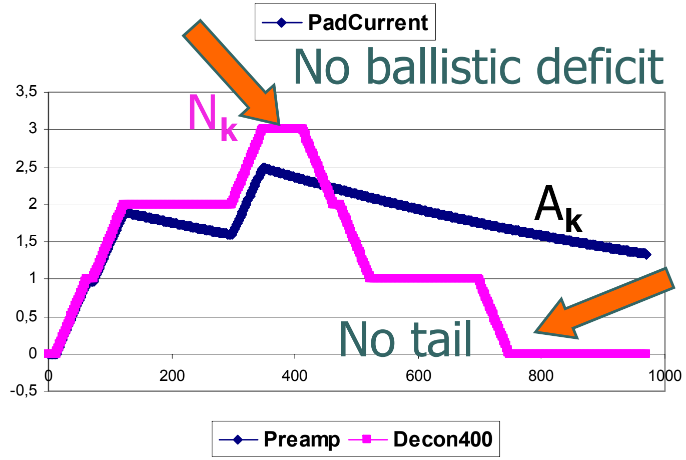
Conditions:
Window width (w) = 400 ns
Preamp decay = 1000 ns

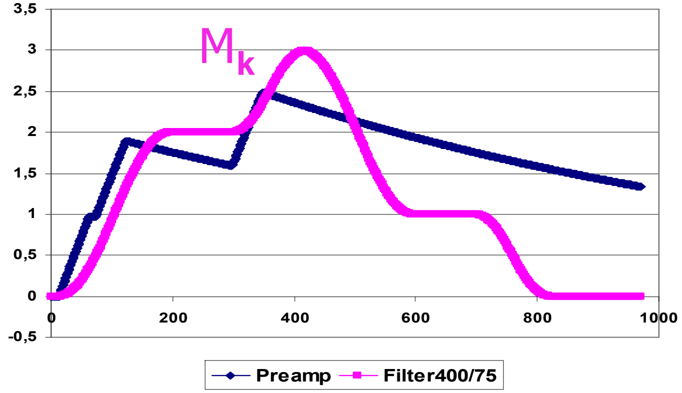
« Boxcar » low-pass filter, T samples:

$$M_k = \left(\sum_{i=0,T-1} N_{(k-i)} \right) / T$$

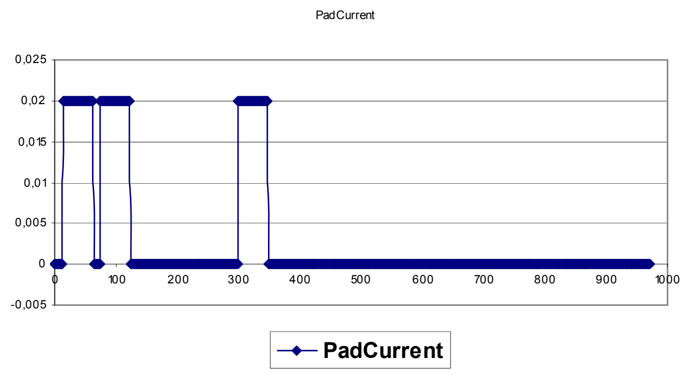
Conditions: T = 75



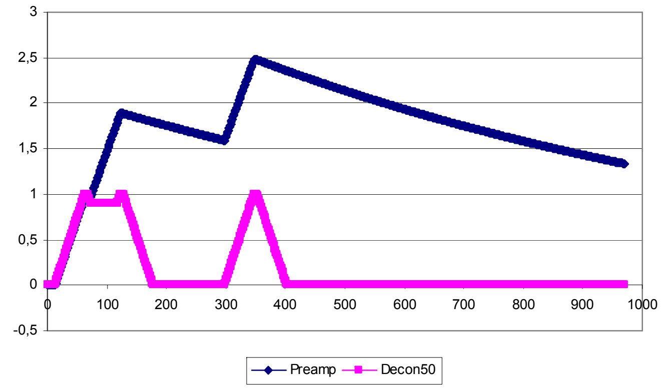




Example with fast digital shaping



Conditions:
Window width (w) = **25 ns**
Preamp decay = 1000 ns



Note: Fast timing is useful for the timing or trigger channel

Carleton – Montreal short term R&D plans

Prototype card built and tested in 2007:

High density card built with off the shelf components
FPGA based: platform to test firmware signal processing algorithms

2008:

Include the new preamp ASIC
Include compatibility with power pulsing

Prototype card built and tested in 2007

- 16 channels (2 octal 50 MS/sec FADCs with LVDS serial outputs)
- Cyclone III FPGA (Low cost, low power)
- USB 2 interface (for test systems)

Presently:

- No power pulsing
- Preamp not on board

2008 => to be transformed into a compact 128 channel card with preamp ASIC and power pulsing capability

Develop electronics compatible with power pulsing

- Based on the KOPIO design (OTS components)
- Use latest serial output (LVDS) FADCs and FPGA
- Total area of FADCs + FPGA smaller than the altro chip
- Design to match the TPC pad pitch
- Include power pulsing capability
- Validate on existing test TPCs
- BUT: Not cost effective for large production

  (> 100K channels)

  (Will need ASIC in due time)

Power pulsing principle

- Power supplies designed for average power rather than peak power
- Distributed charge storage capacitors close to the switchable loads supply the peak current. Allow ~ 1 volt drop during power on cycle
- Local « Low dropout » voltage regulators keep voltage stable on the electronics

- Properly controlled constant current sources recharge the capacitors between cycles