Detector Interface (DIF) Status

Mathias Reinecke

DIF environment – DAQ scheme

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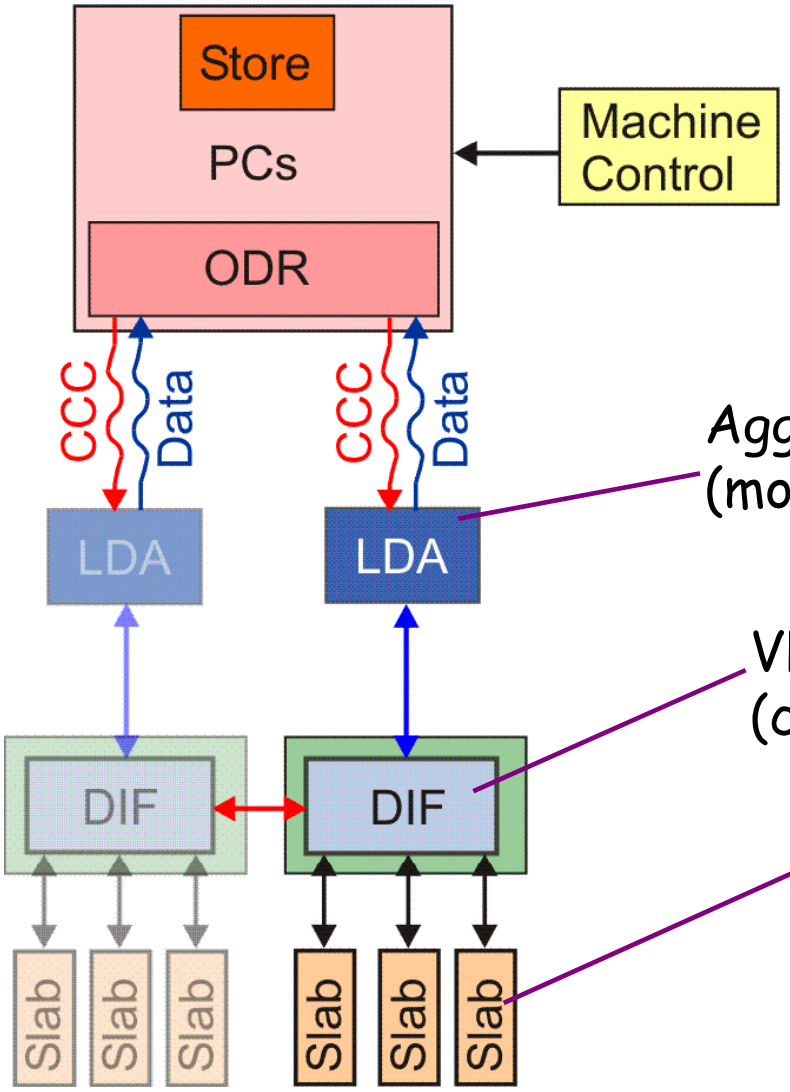

ODR: Off-Detector Receiver
LDA: Link/Data Aggregator
DIF: Detector (specific) Interface
CCC: Clock/Control/Config

Aggregator
(mostly common for all detectors)

VFE Interface Electronics
(common + detector specific parts)

ECAL, DHCAL or AHCAL
(VFE ASICs and detectors)

From M. Wing et al.

LDA Data Flow

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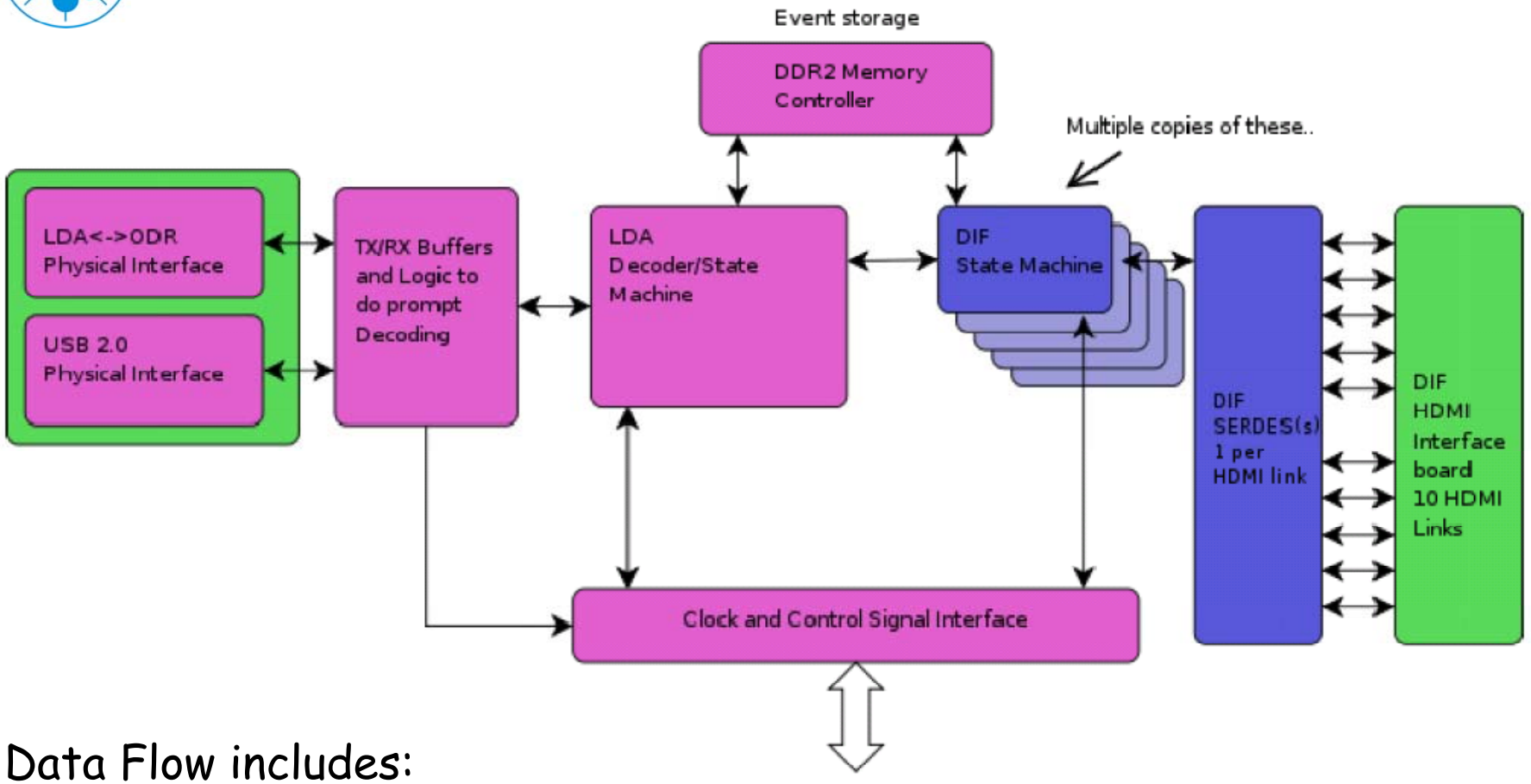

Data Flow includes:

- Control and Configuration Path
- Event Readout Path
- Fast Access (timing related)

From M. Kelly et al.

LDA Prototype Design

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Commercial Spartan3 FPGA Board

Add-on boards for:
-ODR-LDA interface (Ethn)
-LDA-DIF interface (HDMI)
-First prototypes expected soon (Manchester).

From M. Kelly et al.

LDA - DIF protocol ideas

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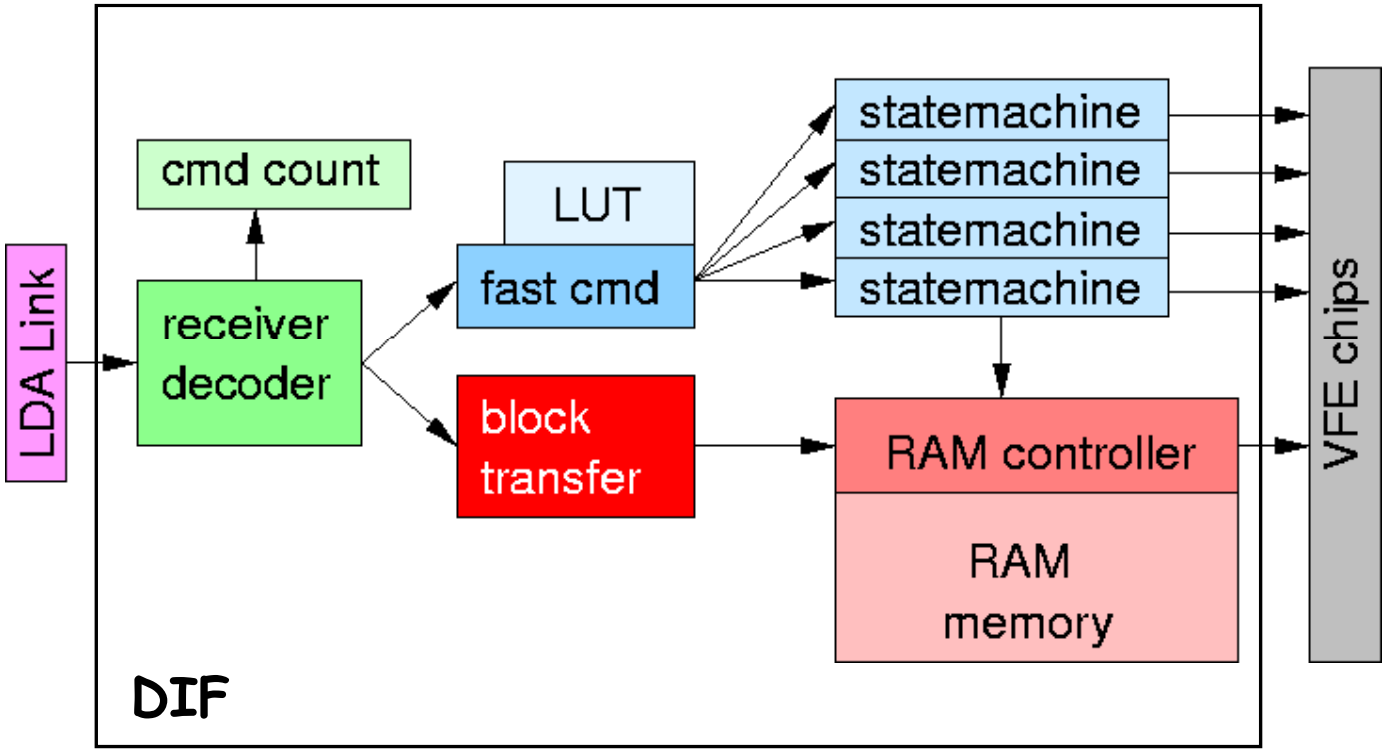

Upstream example:

-enables fast (8-bit) commands

-block transfer for large amounts of data (e.g. configuration data)

-acknowledge to LDA (link robustness)

From B. Hommels
and M. Goodrick et al.

DIF common blocks

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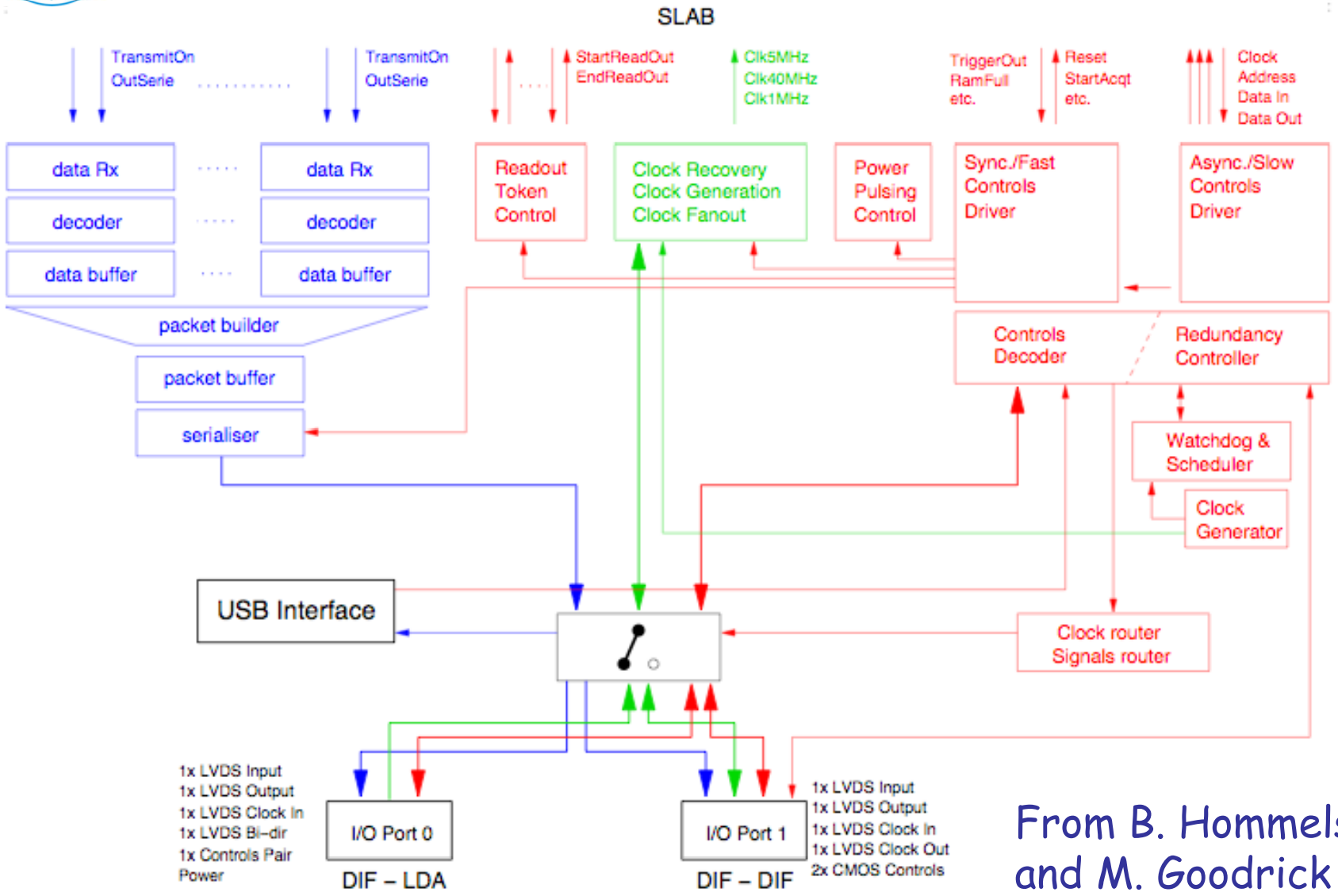

From B. Hommels and M. Goodrick et al.

DIF working group

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A „DIF Task Force" has been established in order to exploit the synergies of the detector- and DAQ designs.

- Bart Hommels (Cambridge) for the DAQ
- Remy Cornat (Clermont) for the ECAL
- Julie Prast (Annecy) for the DHCAL
- Mathias Reinecke (DESY) for the AHCAL

-Signal interface DIF – Slab has been defined (ASIC prototypes).

-VHDL programming in progress (DIF, test prototypes)

-Website with common VHDL blocks in preparation (J. Prast et al.)

-Current status and upcoming questions => report

DIF – Slab Common Signal List

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	Signal	Function	I/O for slab	Valid on	ECAL (SKIROC)	DHCAL (HARDROC)	AHCAL (SPIROC)
Power							
	Vdda	Analog supply +3.5V	I	-	power	power	power
	Vddd	Digital Supply +3.5 V	I	-	power	power	power
	GND	Common ground 0V (GND)	I	-	power	power	power
	HV	High Voltage (SiPM)+/-xxxV	I	-			power
		DAC/Analog +5.0V	I	-			power
	Vref	Reference voltage +x.xV	I	-			power
slow control							
	clk_sc	slow-control shift-reg. clock	I	rising	LVCMOS	LVCMOS	LVCMOS
	srin_sc	slow-control shift-reg. input	I	high	LVCMOS	LVCMOS	LVCMOS
							LVCMOS
							LVCMOS
							LVCMOS
readout							
						OS	LVCMOS
						OS	LVCMOS
						S	LVDS
						S	LVDS
						ector	open collector
						ector	open collector
							open collector
						ector	
controls							
	start_acqt	start data acquisition	I	high	LVCMOS	LVCMOS	LVCMOS
	start_conv_DAQb	start ADC conversion	I	low			LVCMOS
	no_trig/RazChn	Suppr. Int. trig. / rearm trig.	I	high	LVDS	LVDS	LVDS
	Val_Evt	event valid	I	high	LVDS	LVDS	LVDS
	trig_ext	external trigger	I	high	LVCMOS	LVCMOS	LVCMOS
	resetb_BID	reset event counter	I	low	LVCMOS	LVCMOS	LVCMOS
	resetb	global reset	I	low	LVCMOS	LVCMOS	LVCMOS
Power Controls							
	pwr_analog	analog power on	I	high	LVCMOS	LVCMOS	LVCMOS
	pwr_adc	ADC power on	I	high	LVCMOS	___	LVCMOS
	pwr_dac	DAC power on	I	high	LVCMOS	LVCMOS	LVCMOS
	pwr_ss	Slow shaper power on	I	high	____	LVCMOS	____
	pwr_sca	SCA power on	I	high	LVCMOS	____	LVCMOS
	pwr_digital	digital power on	I	high	LVCMOS	LVCMOS	LVCMOS
Calibration							
	CTest	*charge injection (pulse)*	*I*	-	*analogue*	*analogue*	analogue

List for ASIC's prototypes operation.

Additional functionalities (e.g. failsafe) for next version under investigation.

Power Cycling (e.g. SPIROCs)

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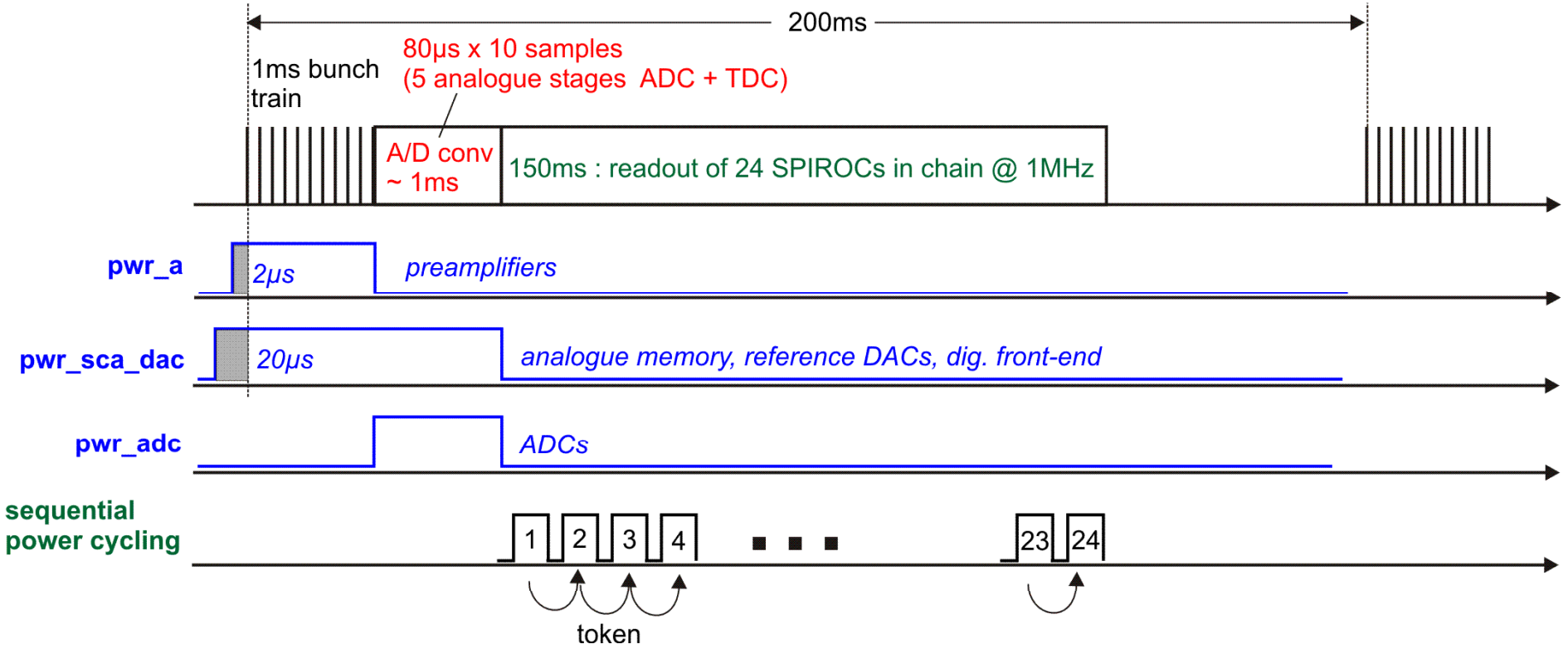

Sequential power cycling of digital part during readout, controlled by readout token.

(in this example: SPIROC with 5 analogue stages : individual channel trigger, SIPM noise above threshold rate ≈ 300Hz).

DIF – AHCAL specific part

AHCAL Half Sector - Reminder

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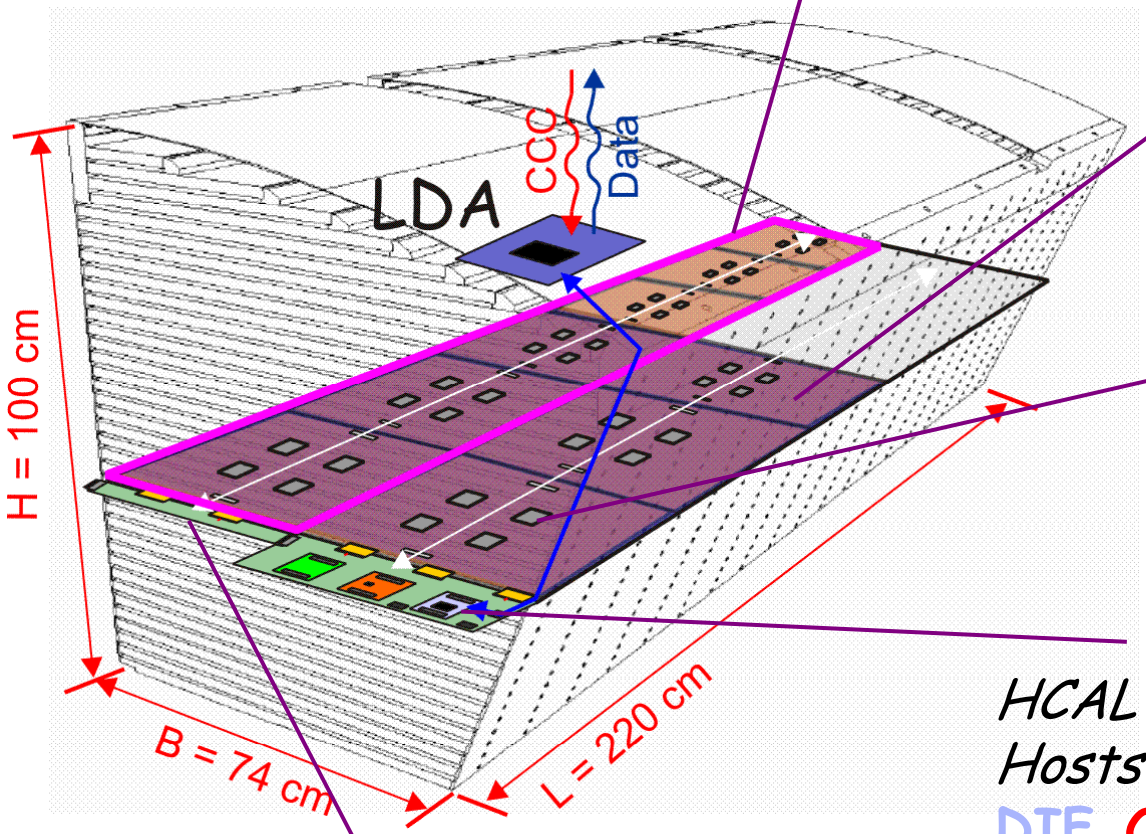
AHCAL Slab

6 HBUs in a row



HBU

HCAL Base Unit

typ. 12 x 12 tiles

SPIROC

typ. 4 on a HBU

HEB

HCAL Endcap Board

Hosts mezzanine modules:

DIF, **CALIB** and **POWER**

HLD

HCAL Layer Distributor

AHCAL: Unit CALIB

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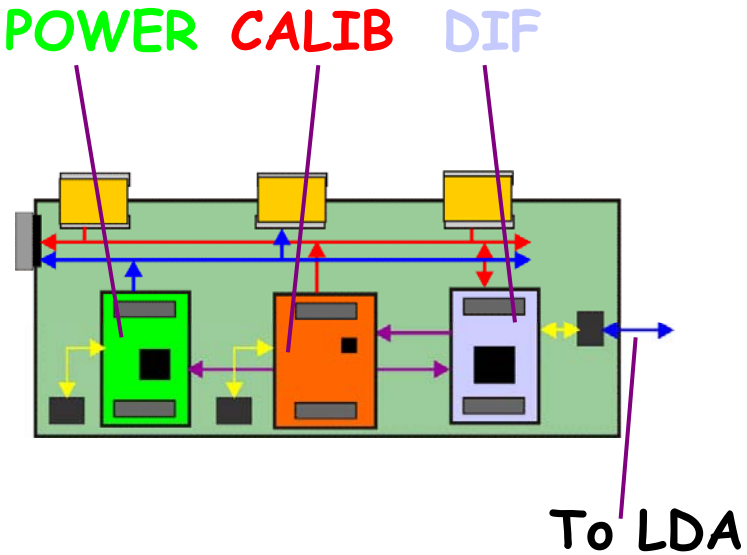
Gain calibration, -monitoring and operational tests by controlling the:

-Charge injection circuits (SPIROC's charge inj. inputs)

-Light calibration (LED) system

-External trigger (without or in combination with LCS)

-Power cycling for electronics inside detector layer



Unit CALIB is fully controlled by the DIF (slave operation).

AHCAL: Unit POWER+Monitoring

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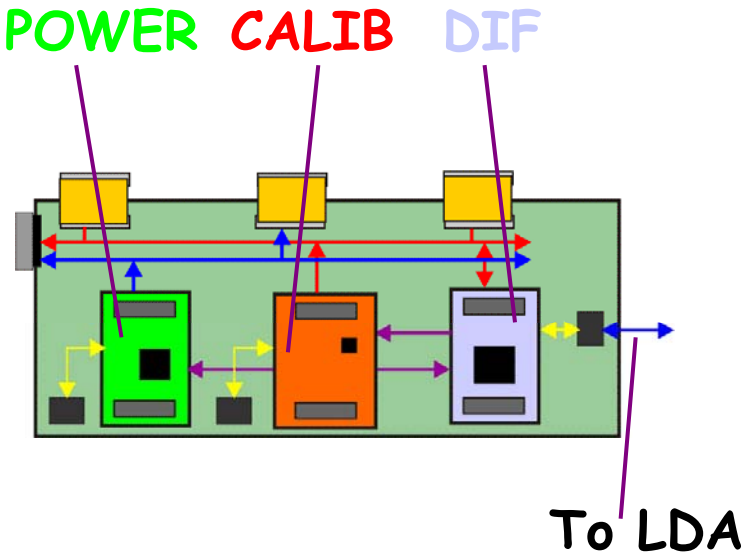
Power supply for the HBUs, monitoring of temperature and supply voltages

-Provide +3.5V, +5V and SiPM bias voltages (+GND) to the HBUs

-Read temperature monitors from HBUs (inside gap)

-Read voltage/current monitors of supply voltages (outside gap).

-Power cycling for electronics inside detector layer



Unit POWER is fully controlled by the DIF (slave operation).

DIF: AHCAL specific part

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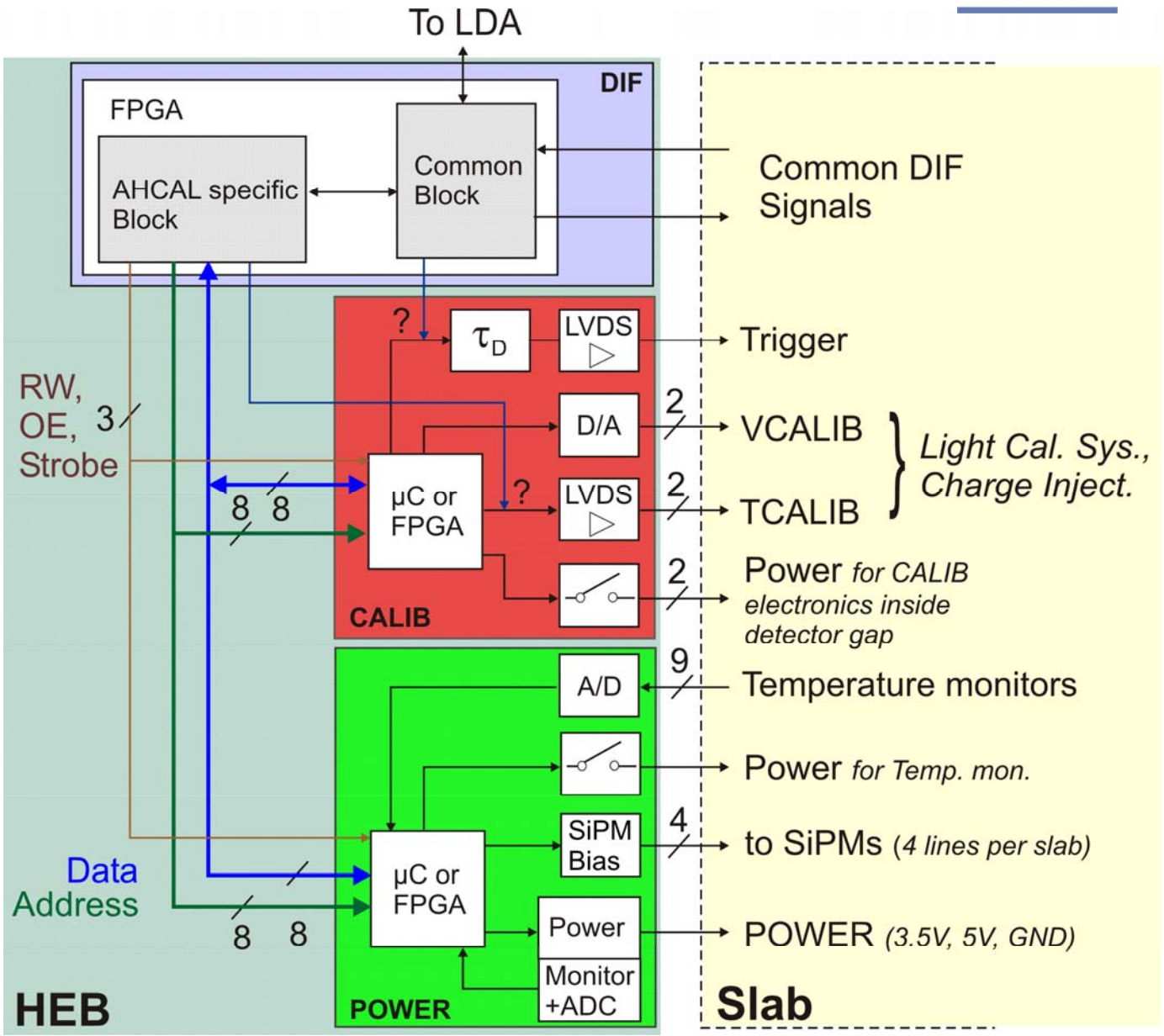
Very first idea about a possible setup.



DIF - AHCAL Interconnection

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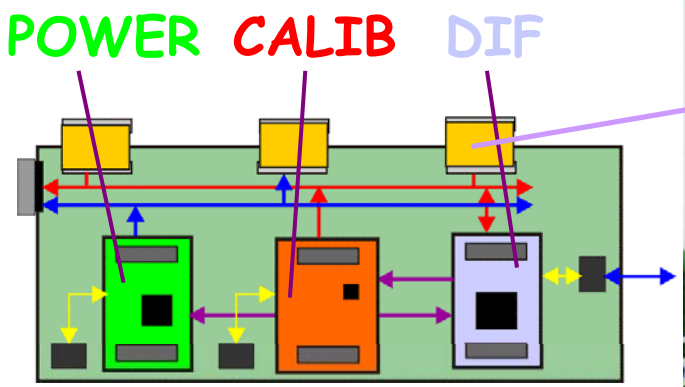
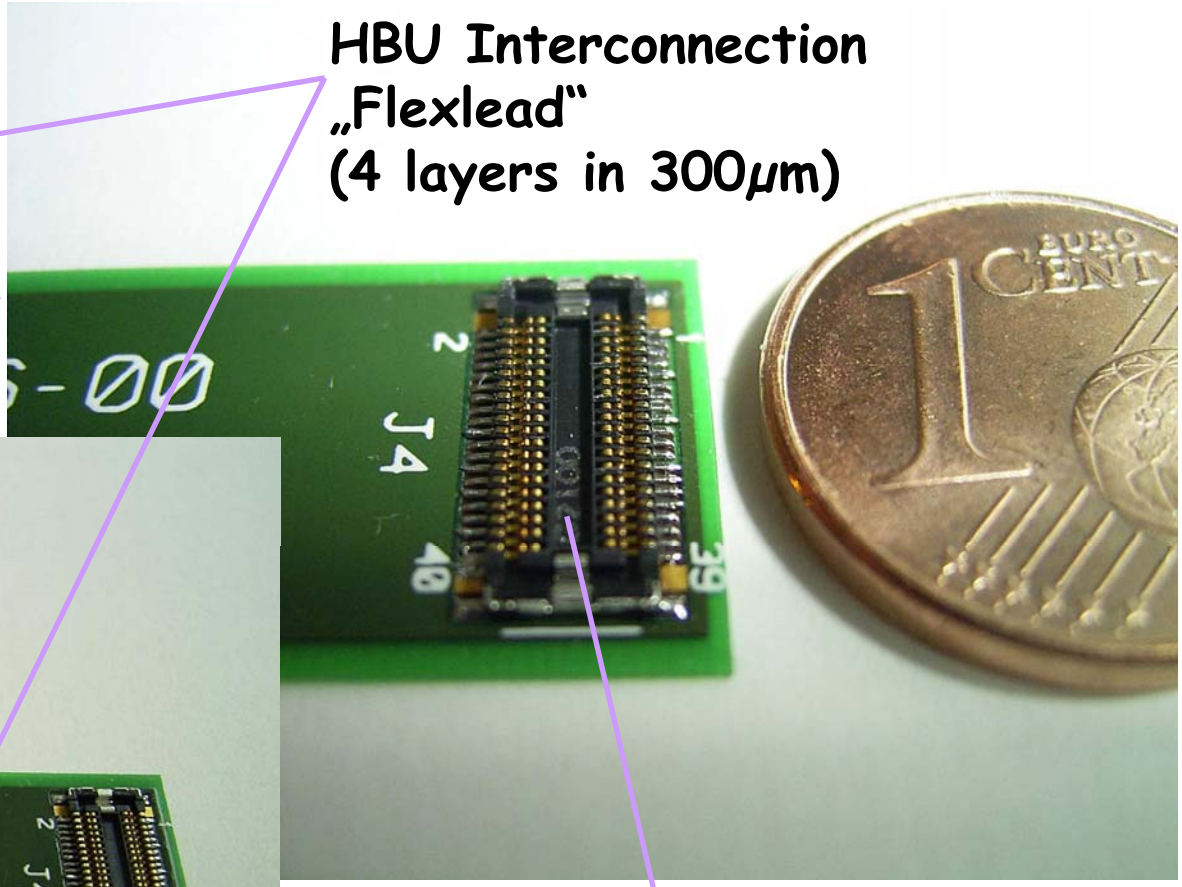
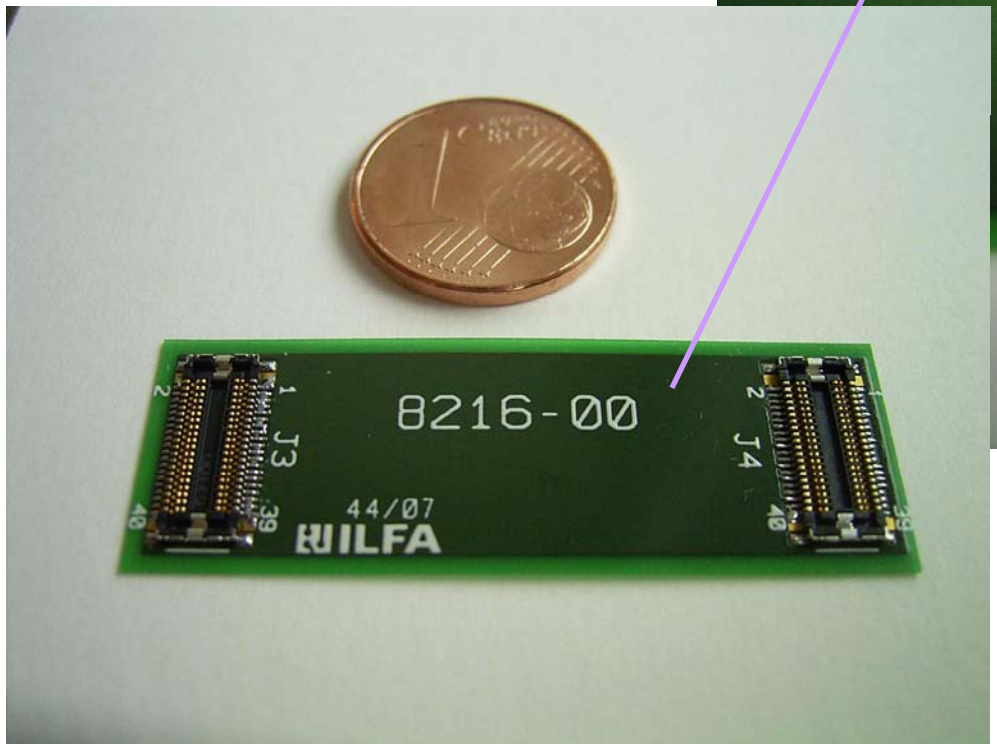


HBU Interconnection
„Flexlead"
(4 layers in 300µm)





Connector stacking height
(both parts): 800µm