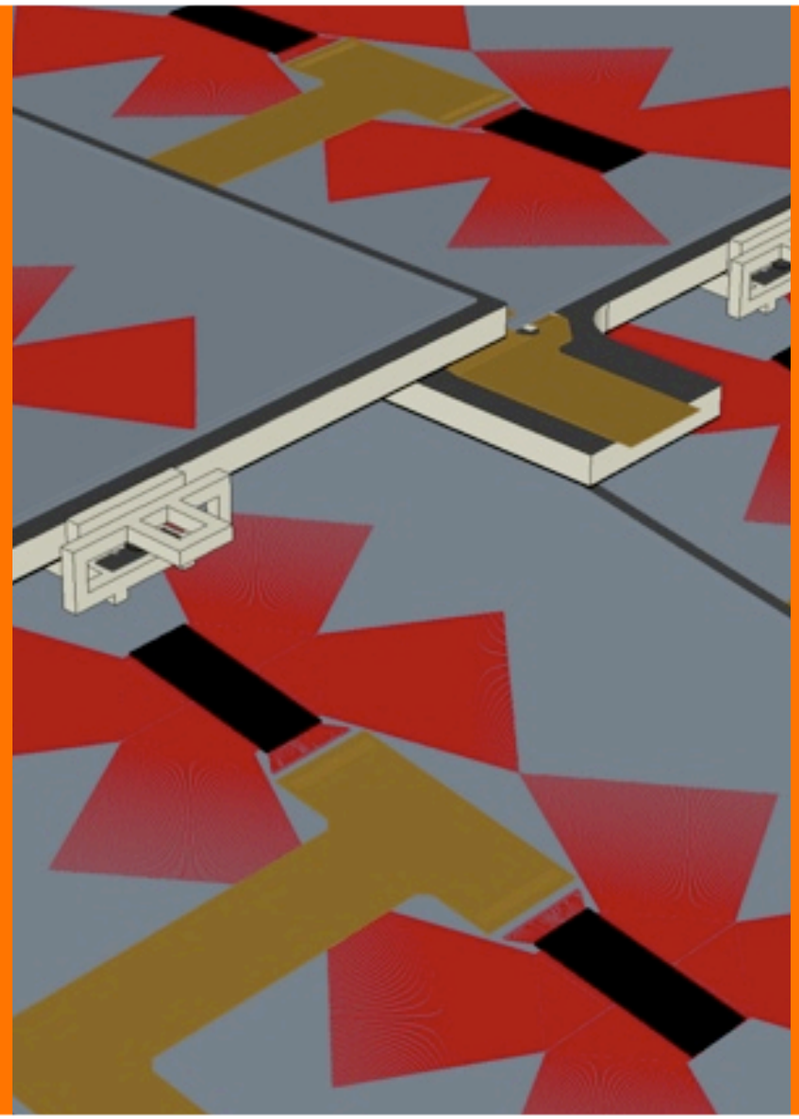


Tracker R&D Status

Tim Nelson - SLAC

*Si*D Collaboration Meeting

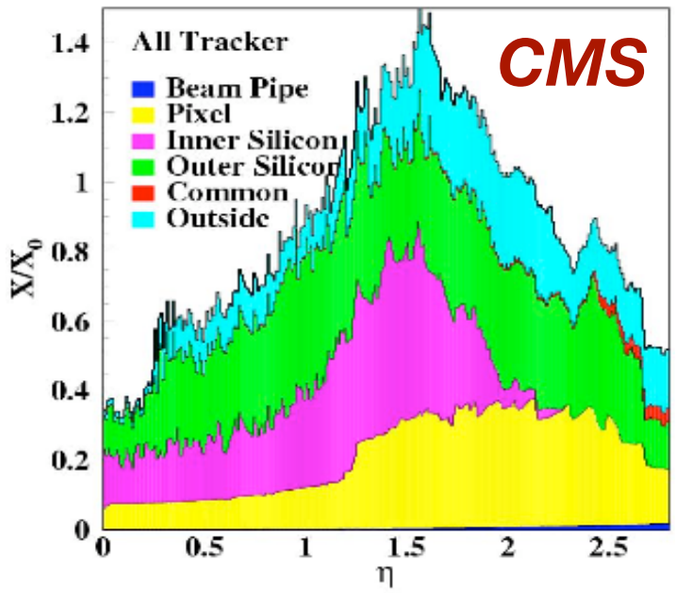
SLAC - January 29, 2008

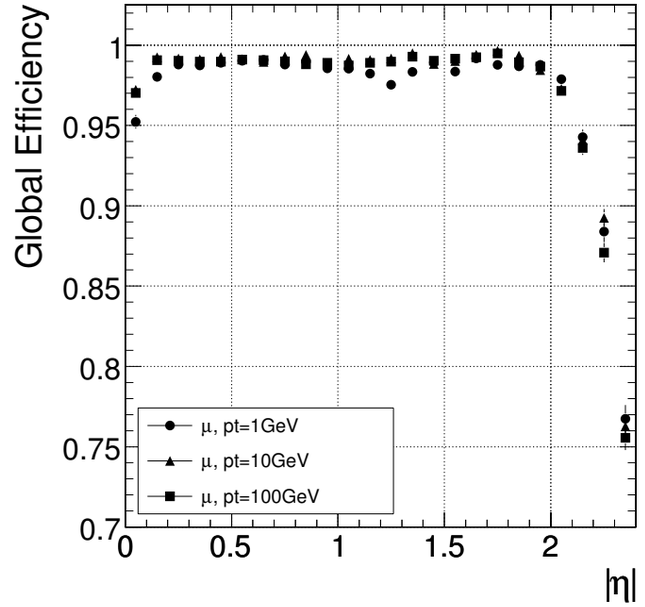
Key R&D Drivers

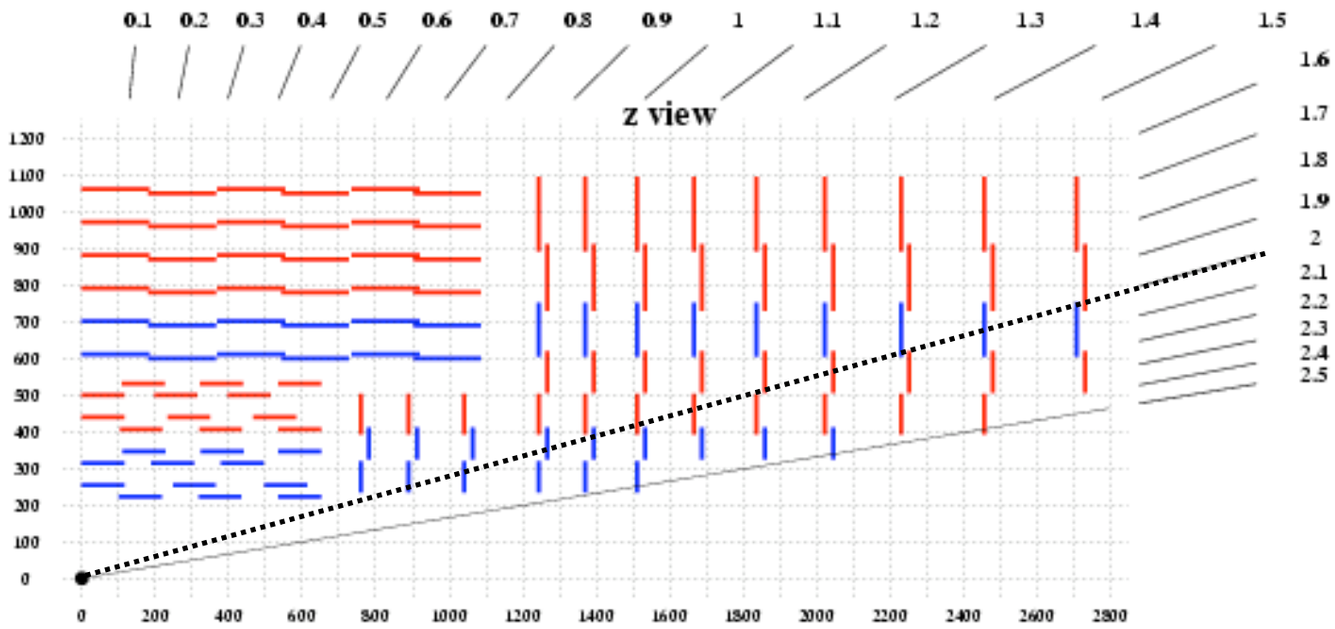
Where is the R&D challenge?

- Large silicon trackers (ATLAS, CMS) have been too massive
- Excellent forward tracking has eluded previous efforts
- Some tracks (e.g. non-prompt) can pose difficulties

These are the key issues to be resolved by the R&D program

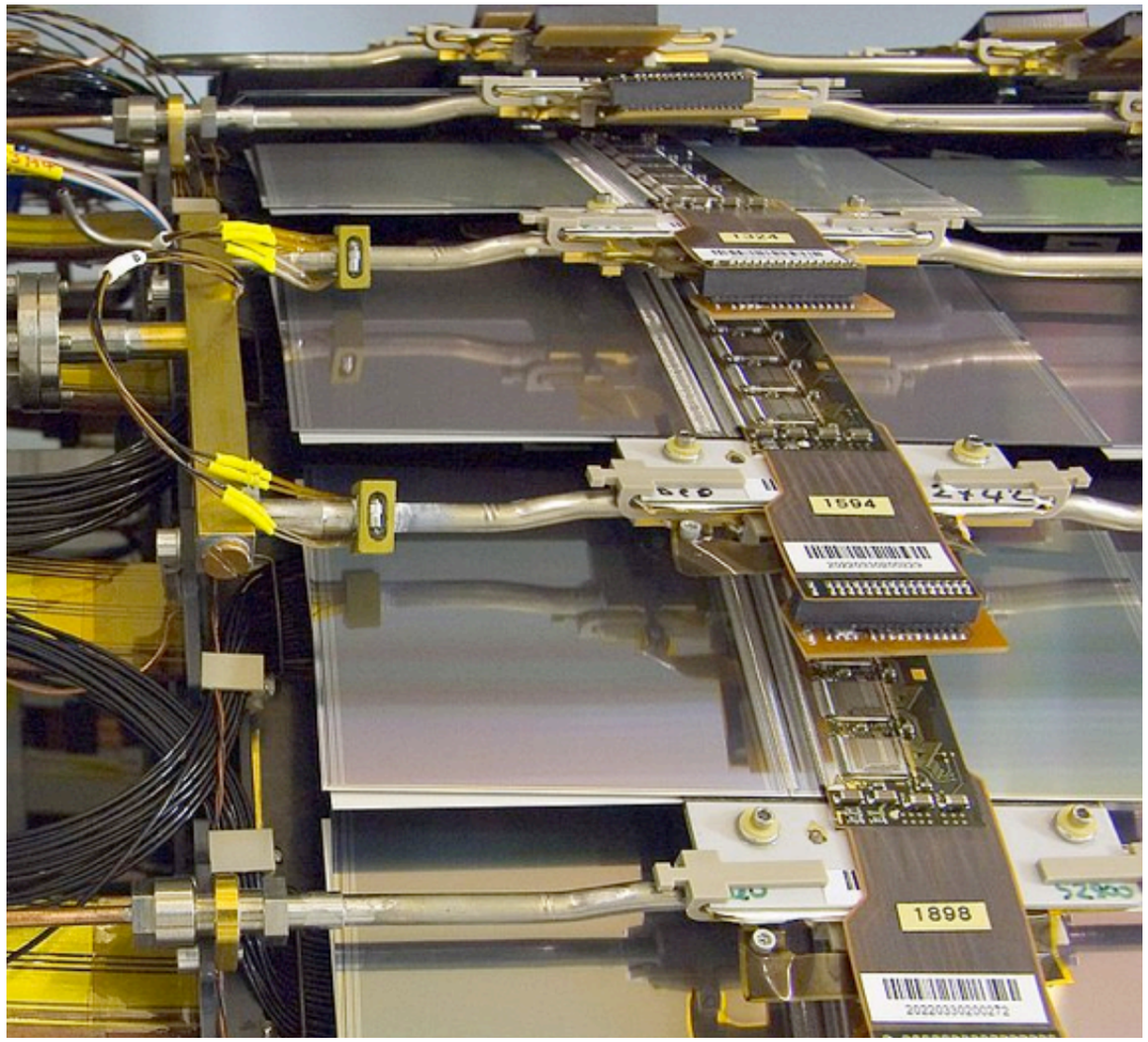






It's The Material, Stupid!

- Cooling: eliminate
- Readout / Power: reduce
  - Chips
  - Hybrid circuit boards
  - Cables
- Support: minimize
- Sensor: thin?



Eliminate Liquid Cooling

- Pulsed operation of front end results in ~100X reduction in power
- Tracker designs under consideration can be gas cooled

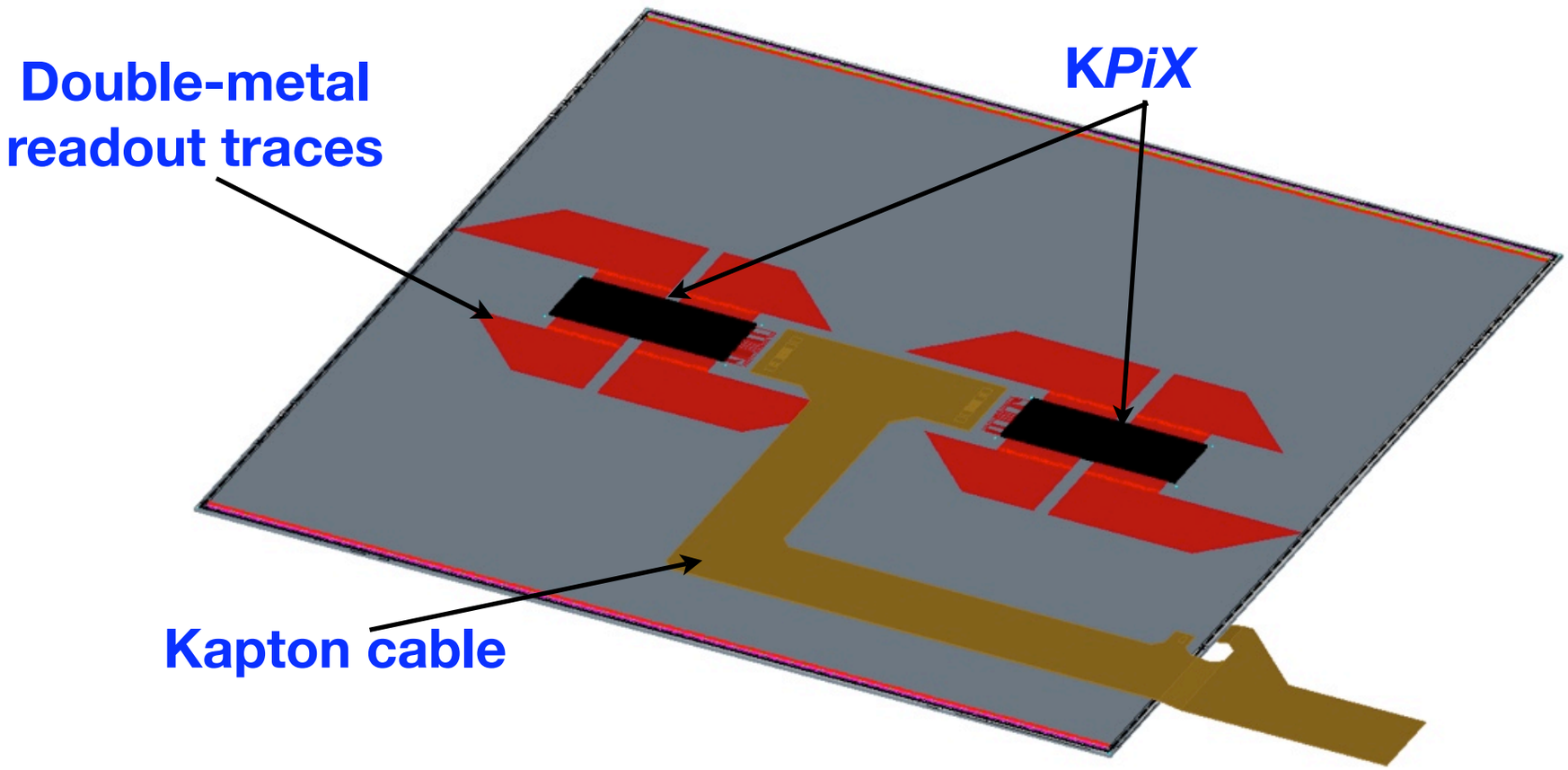
Pulsed power is a common element of ILC readout efforts, in particular:

- K*PiX* (also Si-W ECal) - *BNL, UC Davis, Oregon, SLAC* ***(SiD Baseline)***
- Long Shaping Time Front End (LSTFE) - *SCIPP/UCSC*
- SiTR - *LPNHE/LAPP* (SiLC Collaboration)

These efforts differ primarily in approach to reducing readout material

Baseline *Si*D Design

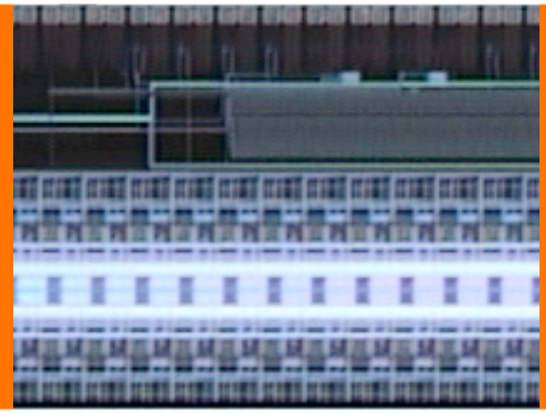
Relatively aggressive approach to material reduction: double-metal readout



Proof-of-principle requires full prototype, planned for this year

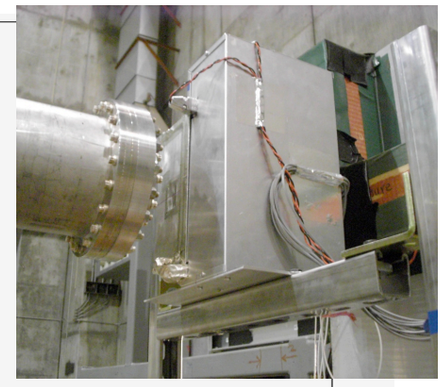
KPiX

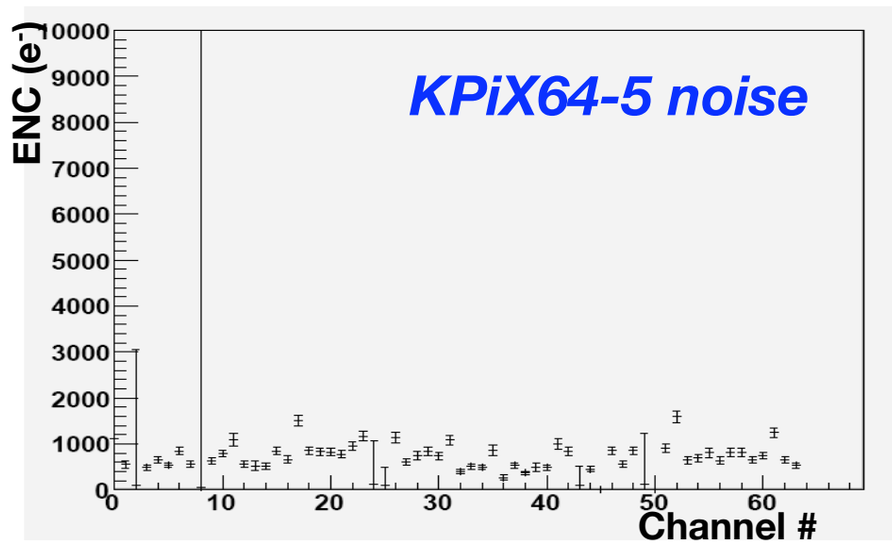
BNL, UC Davis, Oregon, SLAC



Store signals in 4 analog buffers, digitize/read out between trains: quiet operation during acquisition

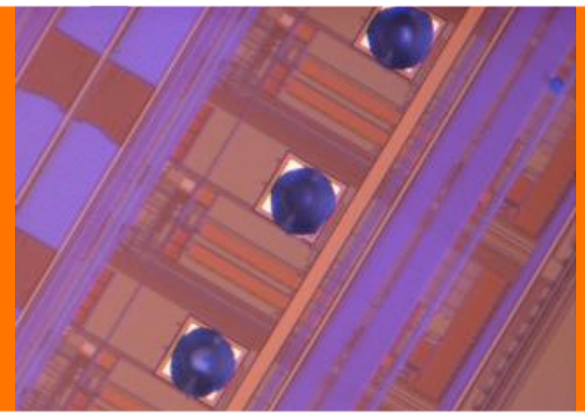
- SLAC ESA test beam with K*PiX*64-4 last fall
- K*PiX*64-5 and K*PiX*64-6 are major improvements
- K*PiX*64-5 achieves expected noise in the trigger branch, much better threshold and gain uniformity
- Digital crosstalk problems necessitate low-DVDD operation: problem understood, easily resolved
- Noise from ADC still nearly 2000 electrons: by far the largest problem not yet understood
- Plan a K*PiX*64-7 to resolve these issues





K*PiX* Bump Bonding

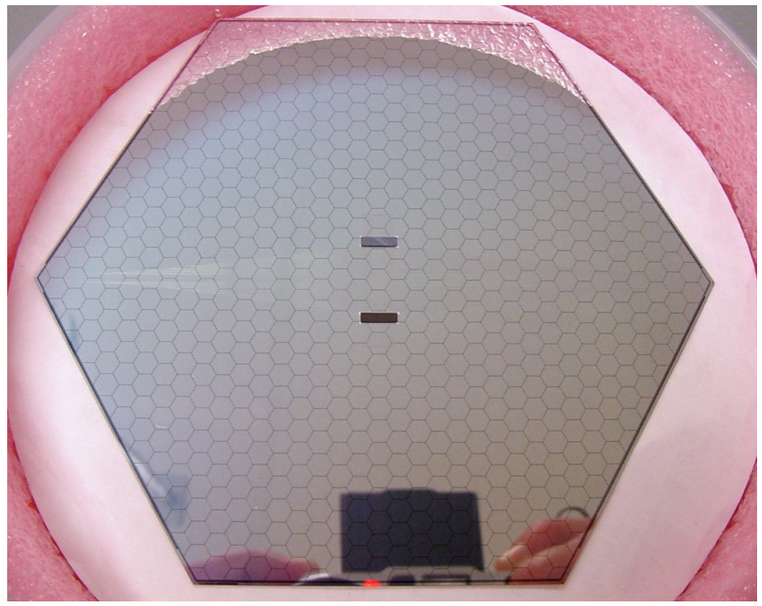
UC Davis

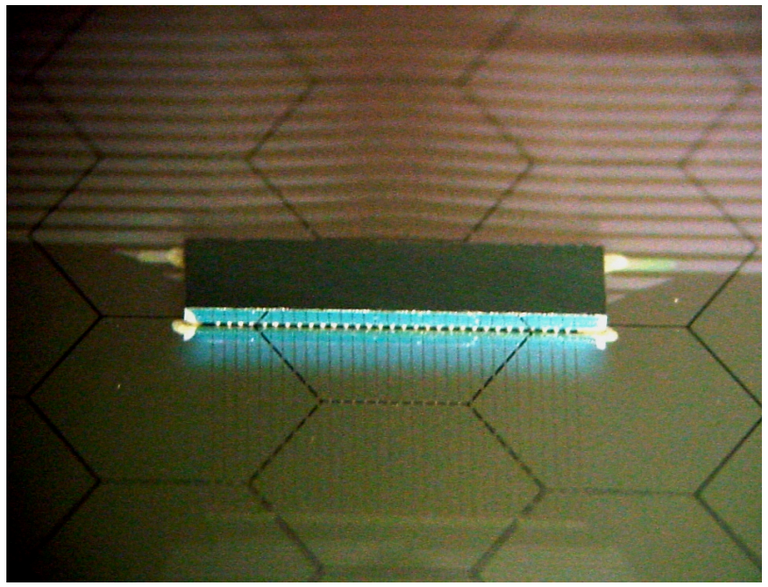


Bump-bonding is a critical process for this design

- At these pitches, gold-stud bumping becomes feasible, especially attractive for small-run R&D
- First attempts at gold-stud bump bonding by Palomar Technologies on KPiX-5 and ECal prototype sensors
- Initial testing on first part shows one open of 24 bonds on first part, testing is ongoing

Encouraging progress for an unfamiliar technique: anticipate using this process for prototype modules



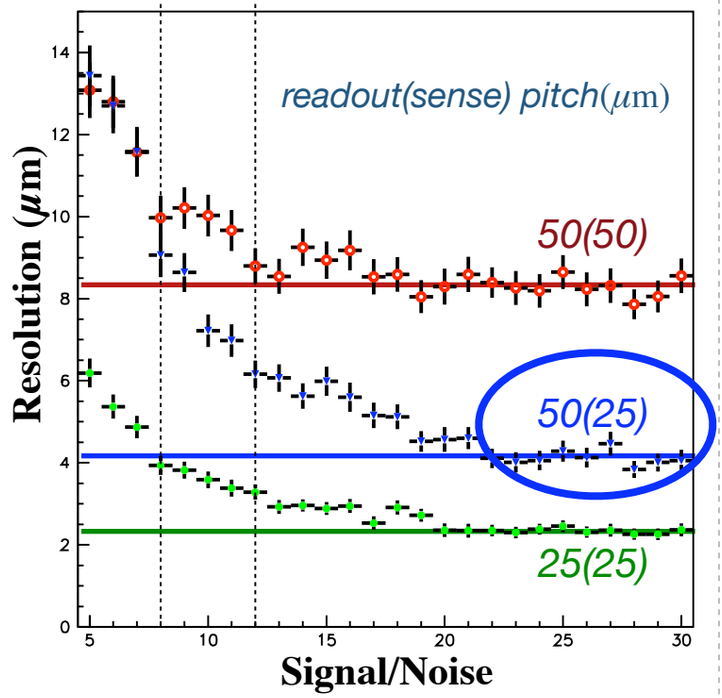


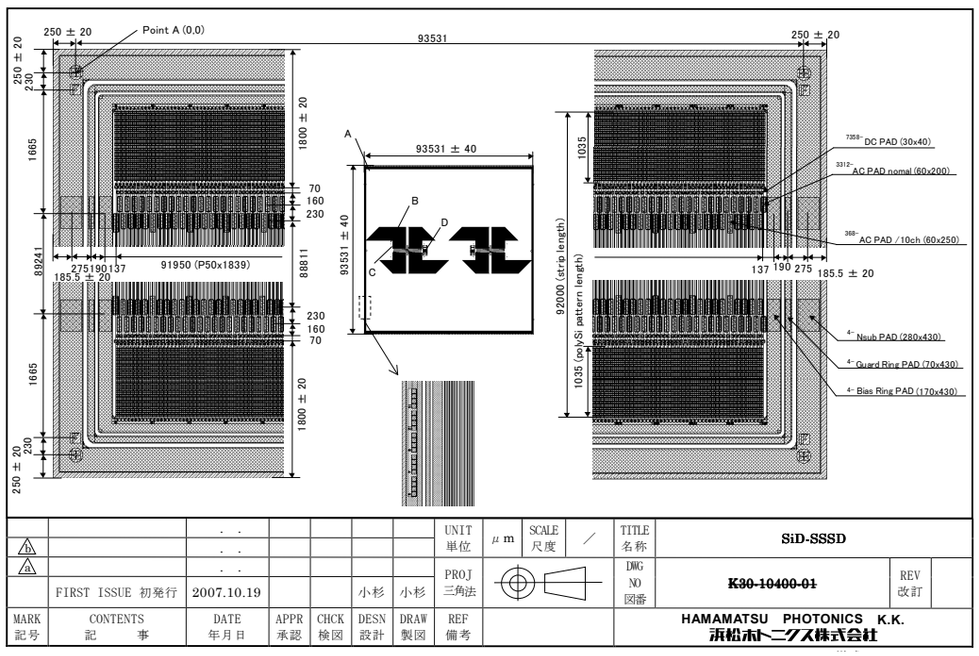
Barrel Sensors

FNAL, SLAC

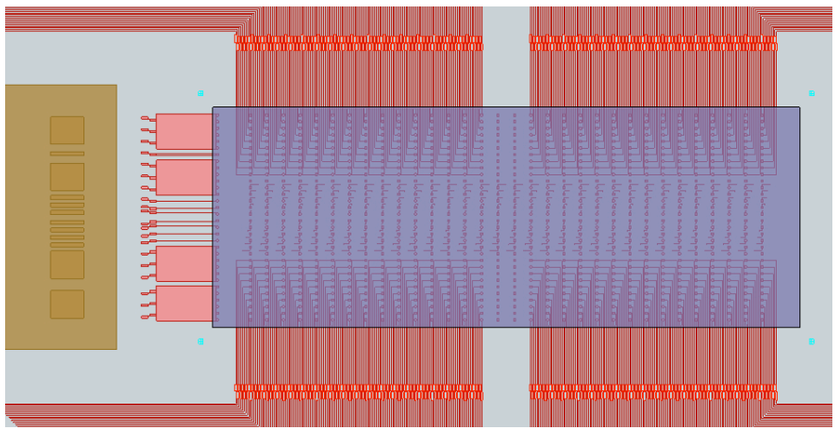
Double-metal prototype sensors submitted to HPK

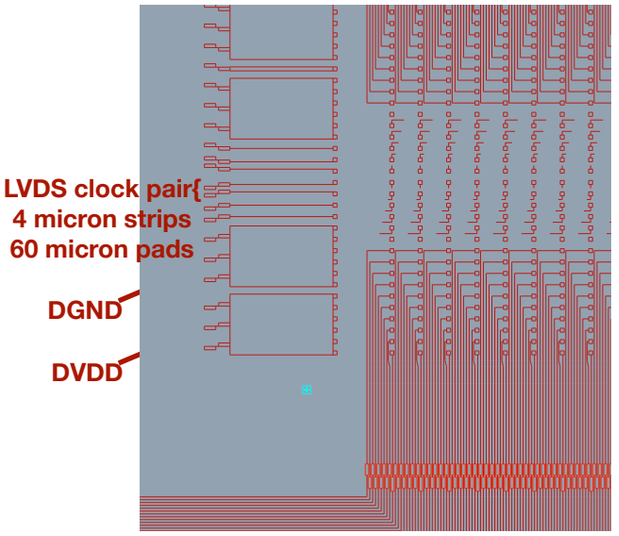
- Should achieve 5μm resolution for short modules
- Configured for both bump-bonding and wirebonding
- *Purdue* group is successfully thinning similar sensors
  - New submission with Sintef planned
  - 200 μm silicon should not compromise resolution





May 2008 delivery



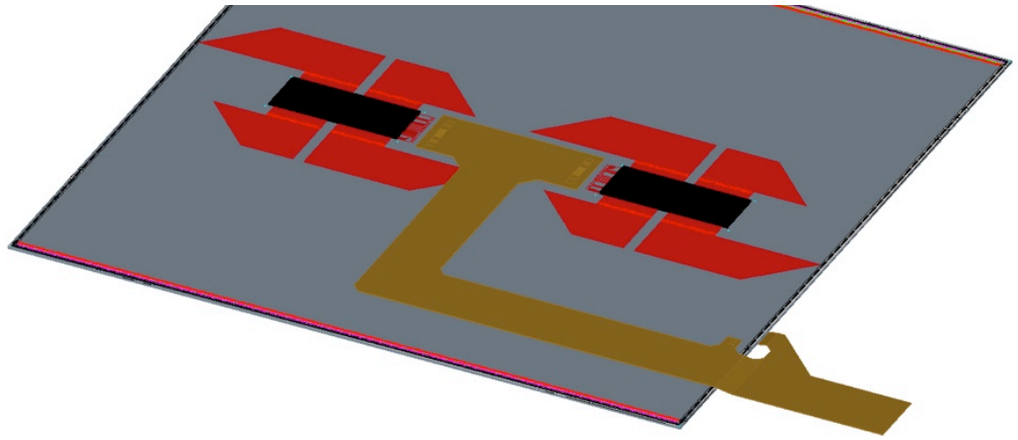


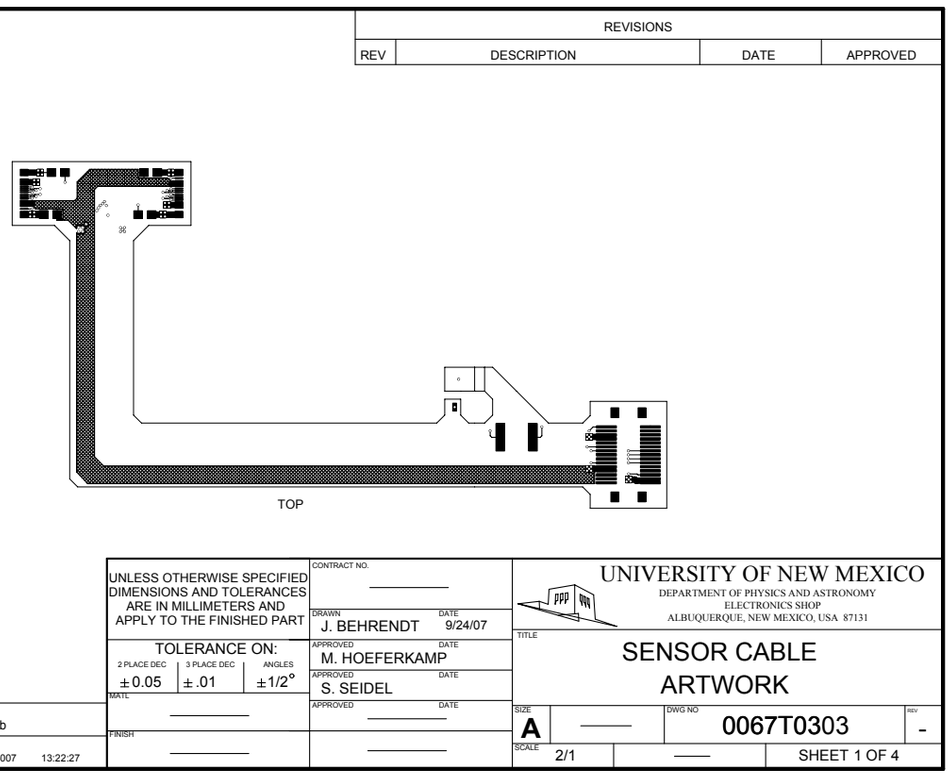
Pigtail Cable

UNM

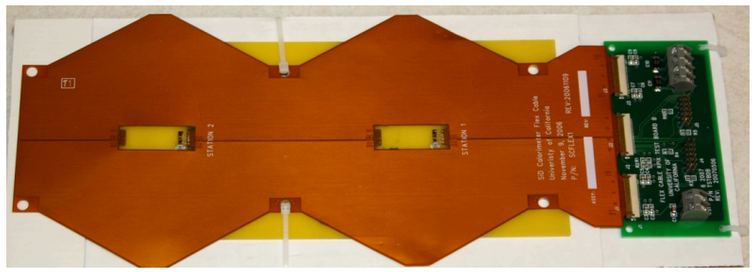
Design for pigtail prototype completed

- ¼-ounce copper on 50μm Kapton
  - 2 power+ground pairs <0.5Ω/trace
  - 8 narrow control/readout lines
  - HV pair for sensor bias
  - ➡ cable width 8mm
- evaluating design: material budget?
- deliverable on same timescale as prototype sensors





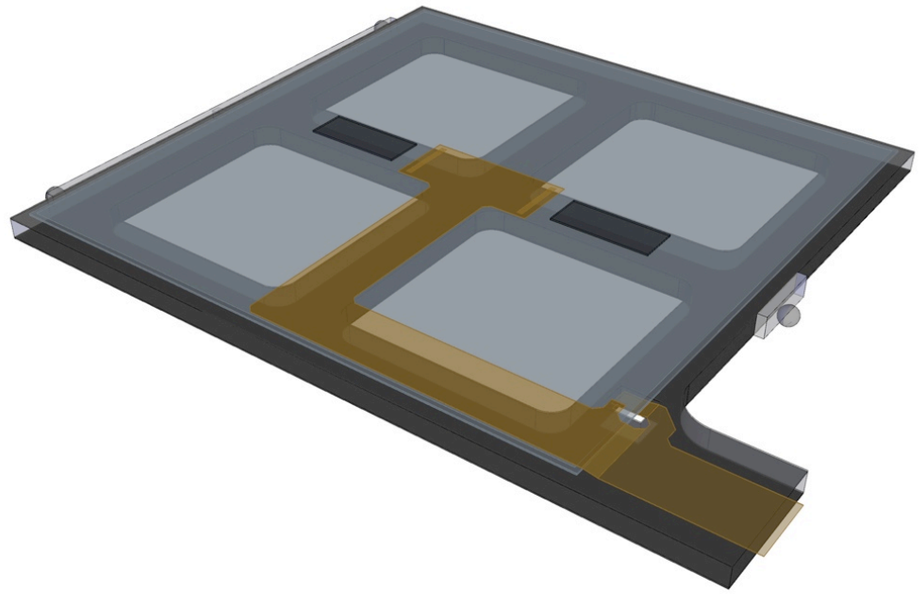
ECal K*PiX* cable (UC Davis)

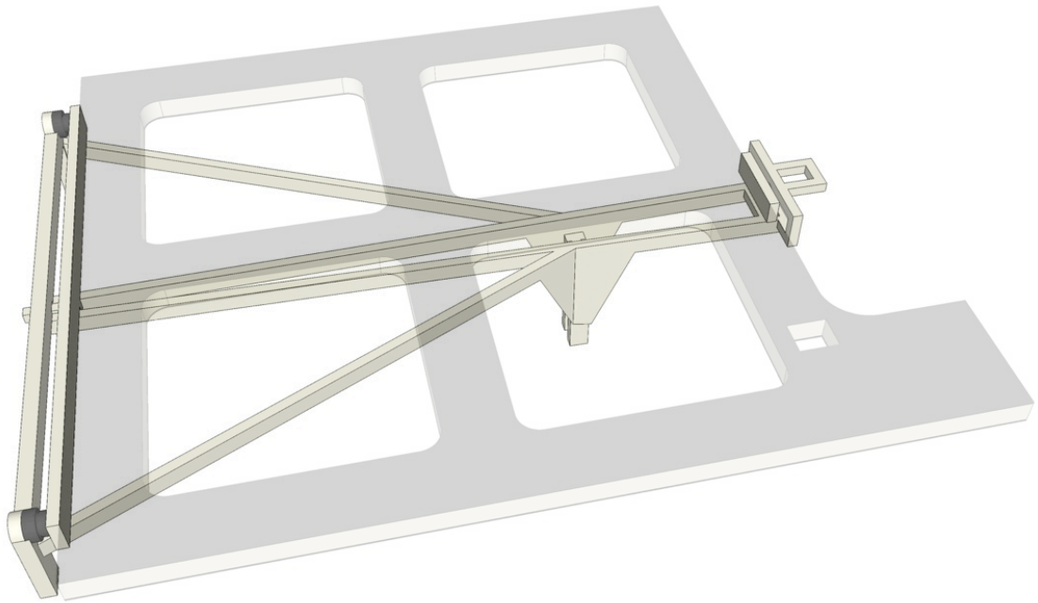


*Si*D Barrel Module Design

FNAL, SLAC

- Support frame is minimal: holds silicon flat and provides precision mount
  - CF-Rohacell-Torlon frame w/ ceramic mounts
  - CF-Torlon clips glue to large-scale supports
- Designed for mass-producibility, ease of assembly, handling, installation/replacement
- Can be made double-sided (stereo) with addition of same silicon on back side
- Now have engineering support at SLAC and new RP machine to fabricate and test rapid prototypes and perform FEA studies



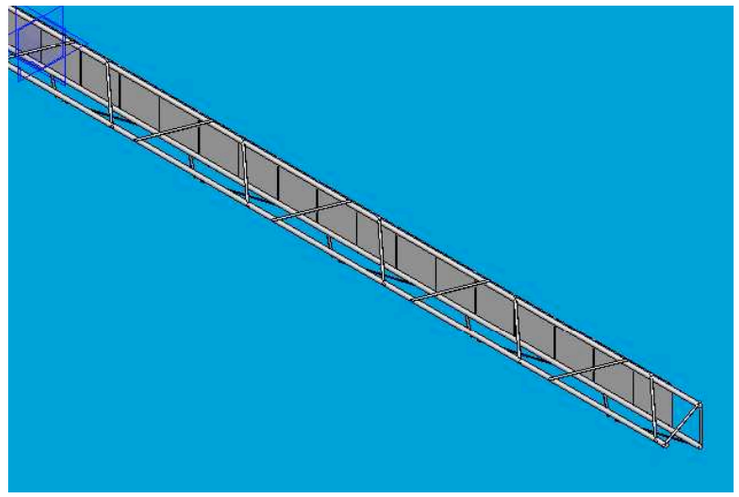


LSTFE

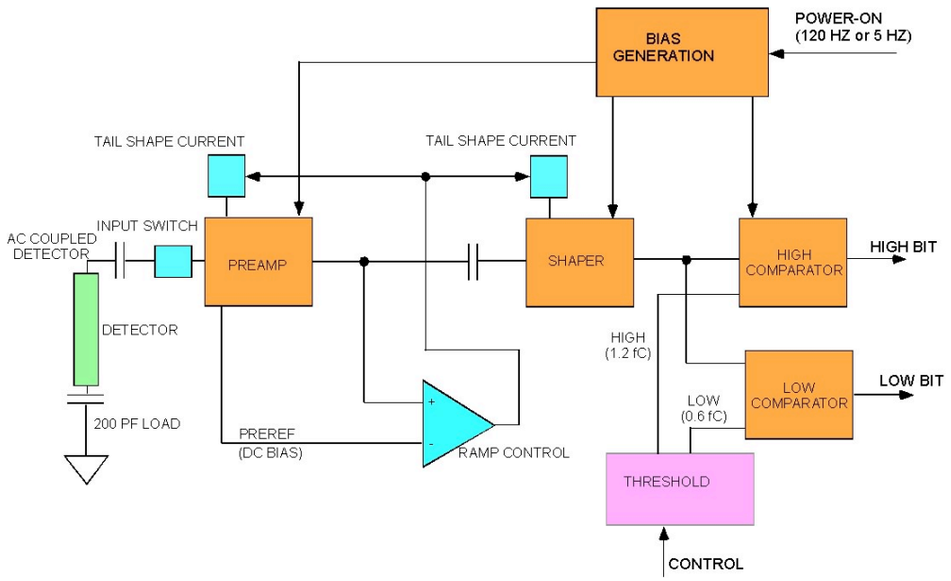
SCIPP/UCSC

Simpler approach: dilution of readout material

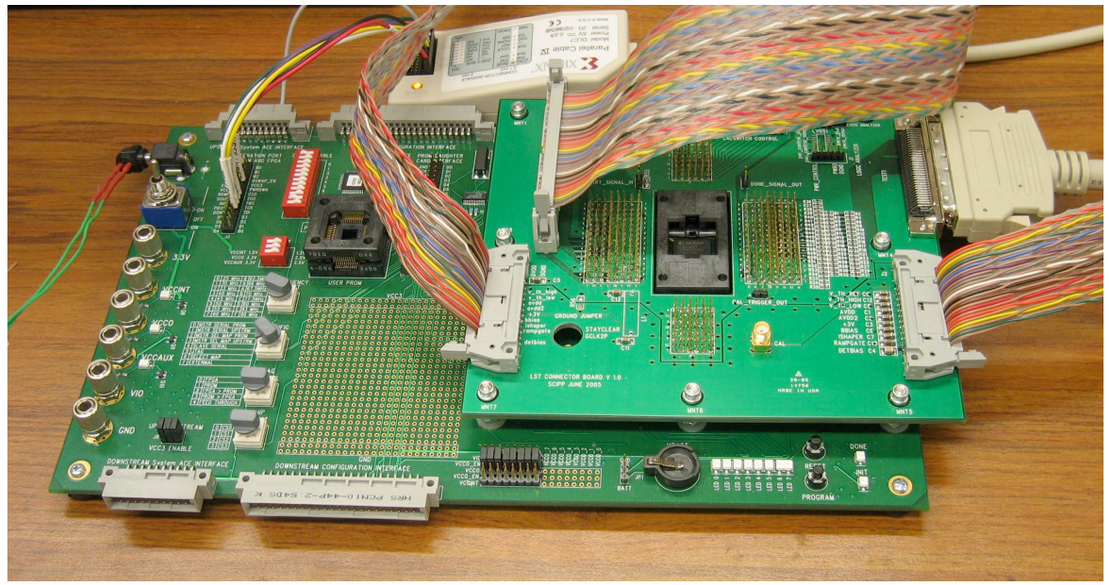
- Design tracker with long daisy-chained strips
- Goal: ladders 1/4 length of SiD barrels (~80 cm)
- Requires carefully designed front end, optimized for low noise in this regime: Long Shaping Time Front End



LSTFE architecture



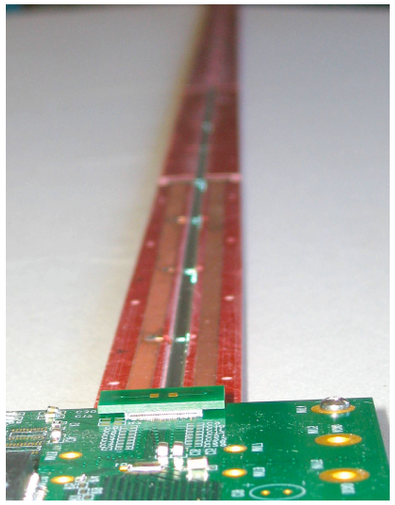
FPGA-based digital section

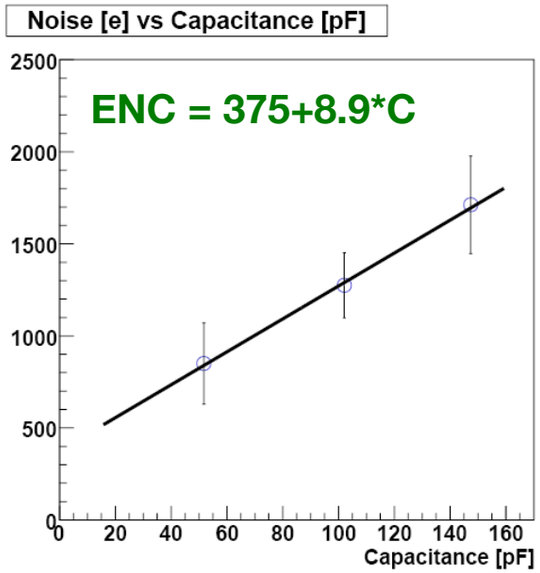


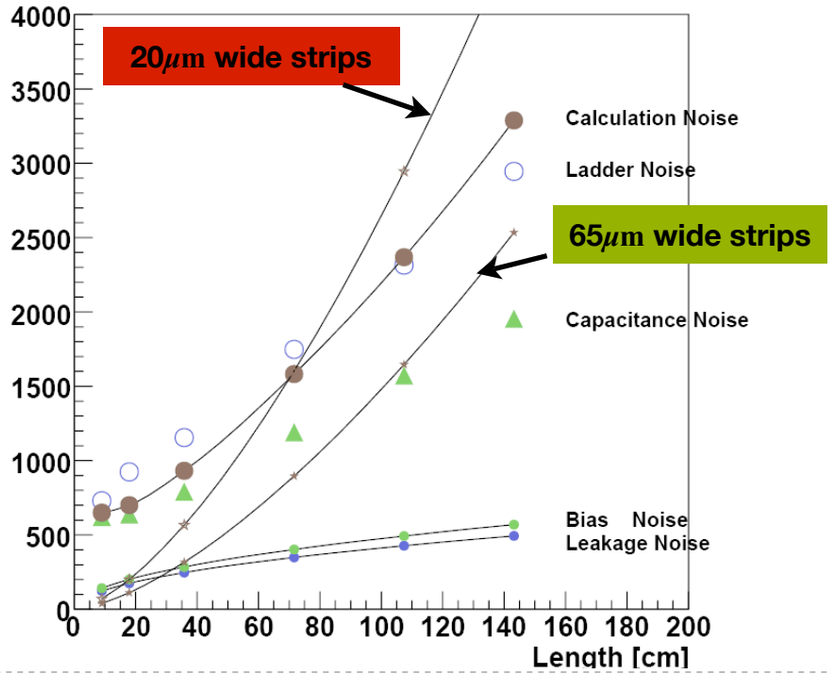
LSTFE

SCIPP/UCSC

- Noise performance of front end is excellent
- Series resistance of narrow strips a concern
  - Narrow-strip test ladders being built using CDF L00 sensors (8μm strip width)
- Submission of 128-channel LSTFE-2 in 2008
  - Improved power cycling
  - Increased dynamic range (≥ 50 × min ionizing)
  - Improved time-over-threshold precision
  - Multiplexed to 8 outputs, digital still on FPGA
- Planning work to integrate digital logic on chip: progress will be limited by resources this year





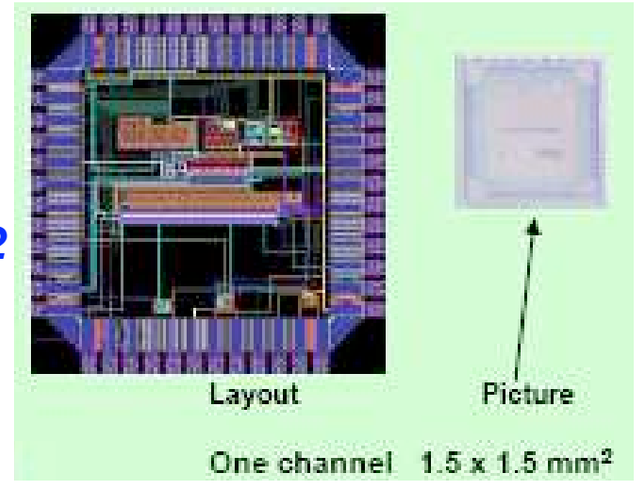


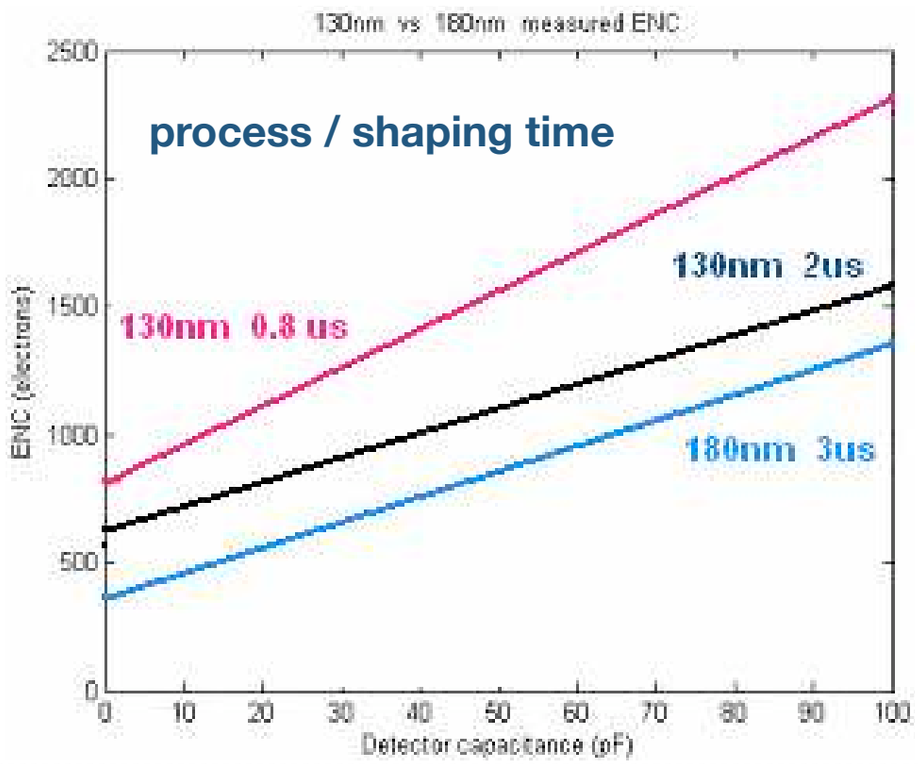
SiTR

LPNHE, LAPP (SiLC)

- Also optimized for long ladders
  - preamp/shaper w/ 2.5μs shaping time
  - “analog” charge measurement (instead of TOT)
- Pushing to smaller process sizes
  - Currently 130 nm: noise appears manageable
- Significant function currently integrated on-chip
  - trigger/sparsifier, buffering, digitization, calib.
  - no power cycling yet
- Next chip Q1 2008: 128 channels, power cycling

SiTR-130_v2

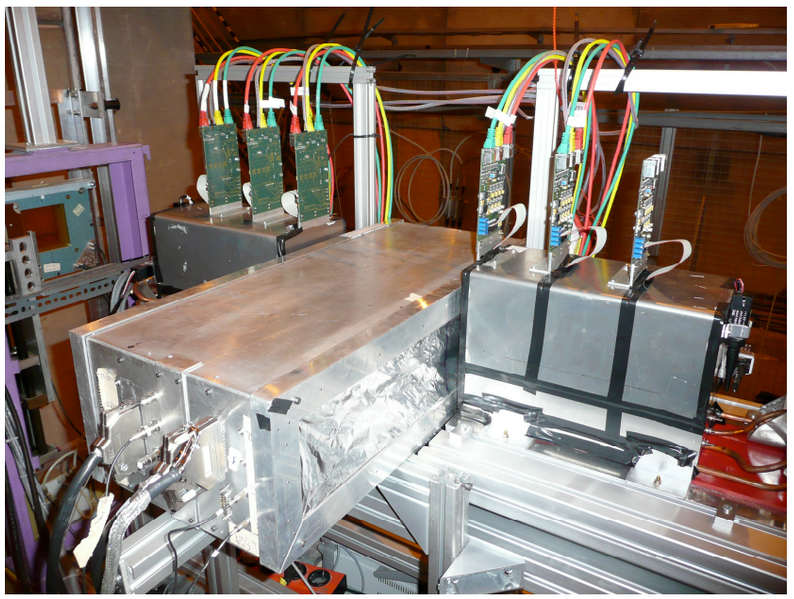




SiLC Sensors and Modules

HEPHY, LPNHE, Liverpool (SiLC)

- Prototype HPK sensors, some with IR-transparent laser-alignment windows
- Also studying sensors on thinned wafers
- Investigating various “traditional” ladder concepts: CERN test-beam with EUDET pixel telescope
  - CMS sensor / VA1 chips
  - CMS sensor / SiTr-130
  - Prototype HPK sensor / SiTr-130
- Developing planar/3D sensors (nearly edgeless)
- Developing sensors with flip-chip readout
- Investigating sensors from 8” or 12” wafers

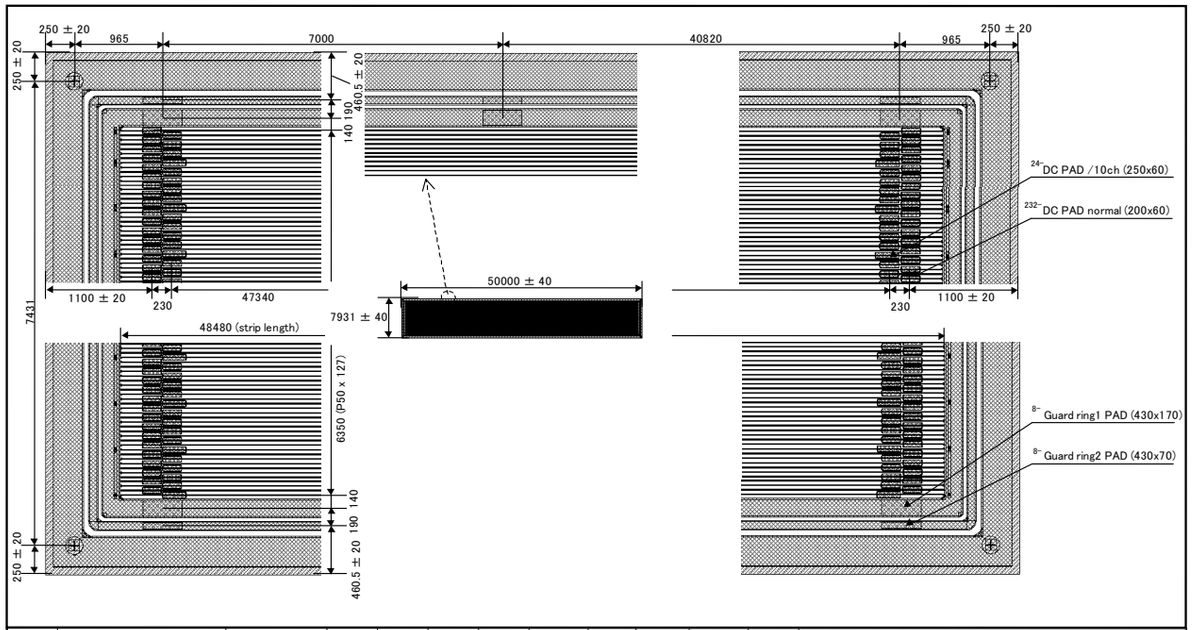


Charge Division Readout

Brown, SCIPP/UCSC

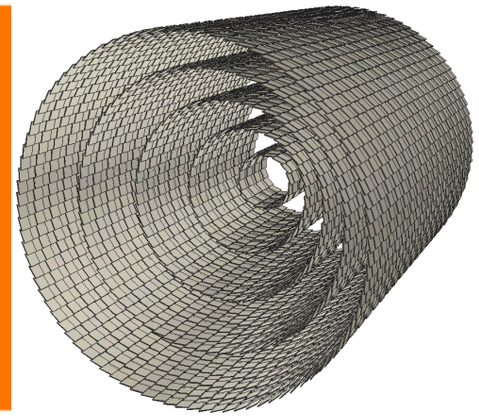
Obtain 3-d measurement by instrumenting both ends of strip

- Like double-sided modules, could be used forward, barrels if necessary
  - Single sensor: less material, cost
  - Somewhat less precision: theoretical limit is ~5mm
- Test sensor included with double-metal sensor submission
- Design studies for prototype readout chip are encouraging

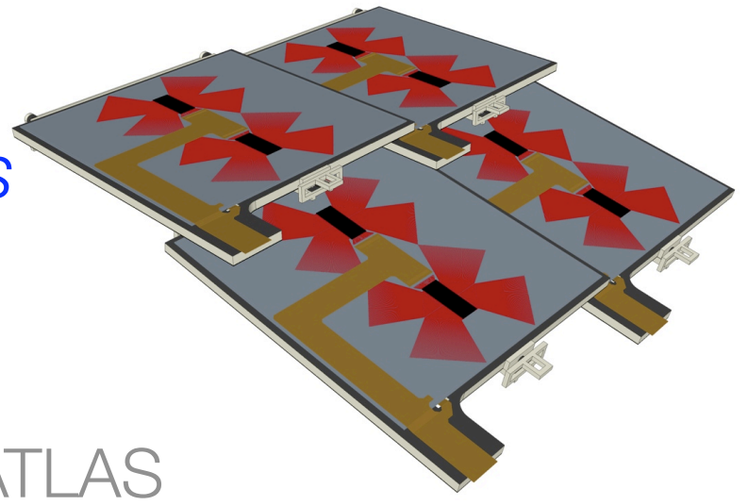


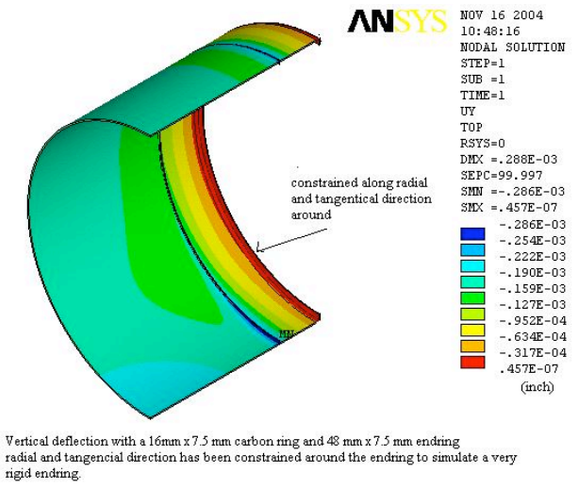
*Si*D Barrel Tracker Design

FNAL, SLAC



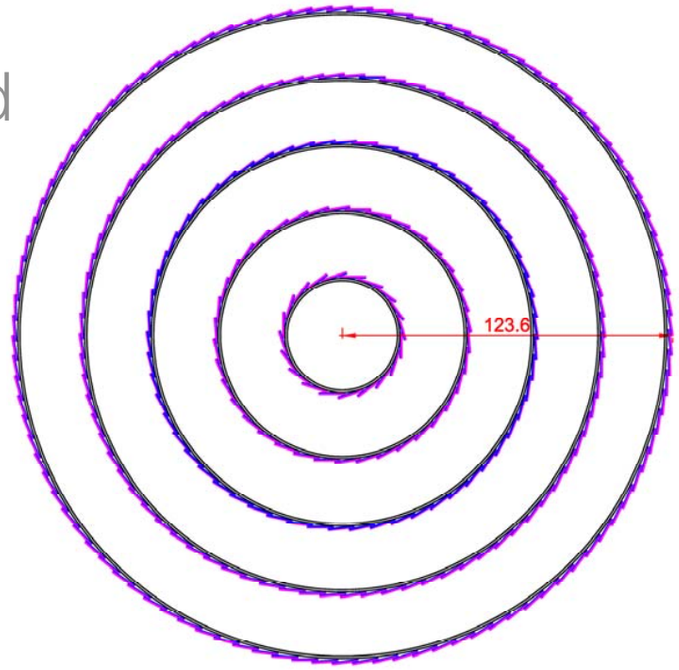
Modules tile CF-Rohacell cylinders



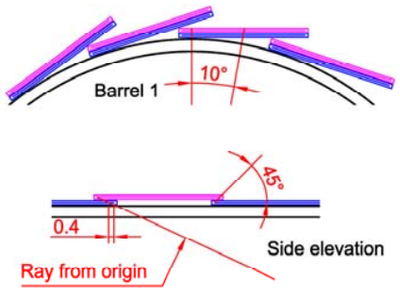


Vertical deflection with a 16mm x 7.5 mm carbon ring and 48 mm x 7.5 mm endring
radial and tangencial direction has been constrained around the endring to simulate a very rigid endring.

- Module tilt corrects for Lorentz drift
- Similar cylinders fabricated for D0, ATLAS
  - FEA results: 7um deflection fully loaded
  - 0.3% X_0 for solid cylinders: could be made up to 50% void
- More engineering ultimately required, but not critical for proof-of-concept (LOI)



Sensors:
Cut dim's: 9.35 cm x 9.35 cm
Active dim's: 9.20 cm x 9.20 cm
Modules:
Outer dim's: 9.65 cm x 9.65 cm x 0.3 cm
Support cylinders:
OR: 21.5, 46.5, 71.5, 96.5, 121.5 cm
Number of phis: 20, 38, 58, 80, 102
Tilt angles: 6.6 to 10 degrees
Radii normal to silicon (mm):
Barrel 1: 2.175, 2.215 cm
Barrel 2: 4.675, 4.715 cm
Barrel 3: 7.175, 7.215 cm
Barrel 4: 9.675, 9.715 cm
Barrel 5: 12.175, 12.215 cm
Blue and magenta sensors are at different Z's to provide longitudinal overlap.
Within a given barrel, cyan sensors overlap in phi, as do magenta sensors.



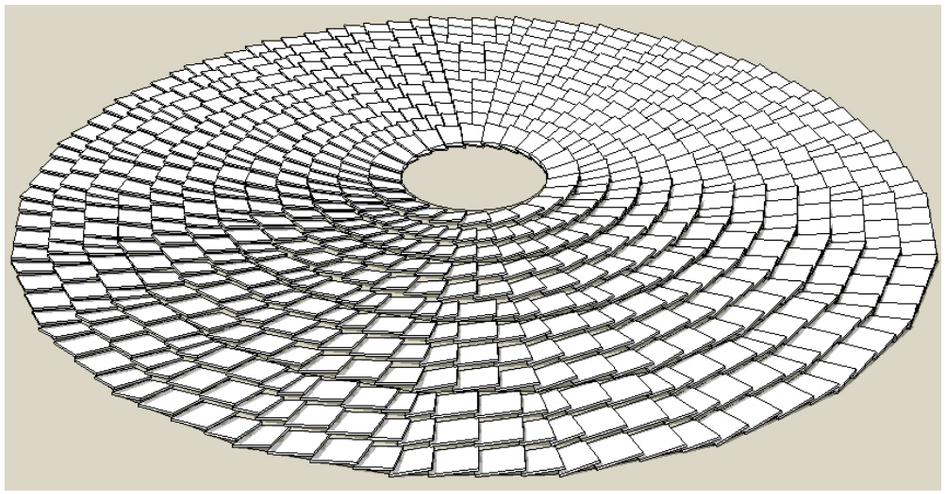
*Si*D Forward Tracker Design

SLAC

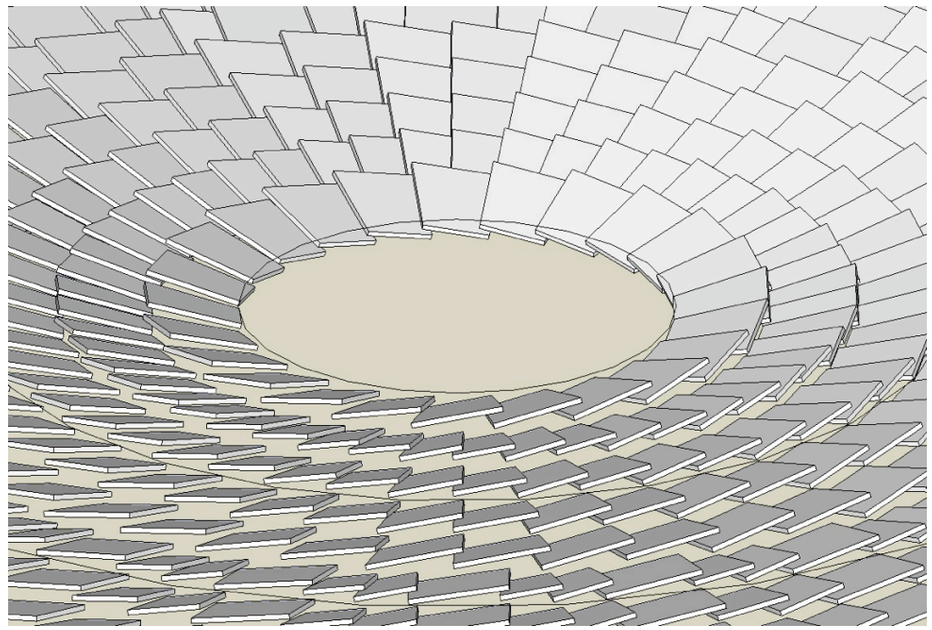
Barrel cylinders closed by forward disks

- Straw man mechanical layout for wedges : squares, hexagons also being considered
- Issues demanding module R&D largely independent of shape
  - Short module accommodates many choices: designed with double-sided modules in mind
  - Long-module mechanics may exclude some tiling options

Simulation must inform these decisions



10 sensor designs



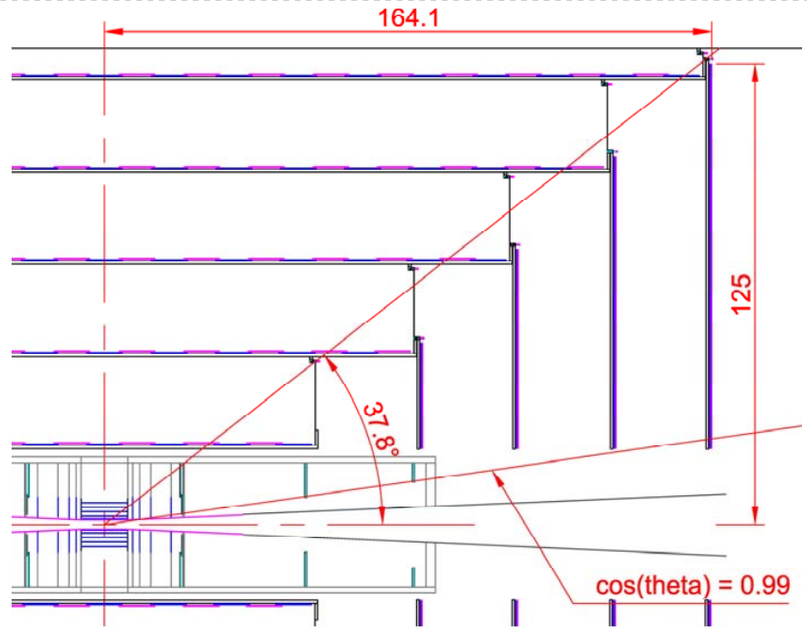
SiD Tracker Design

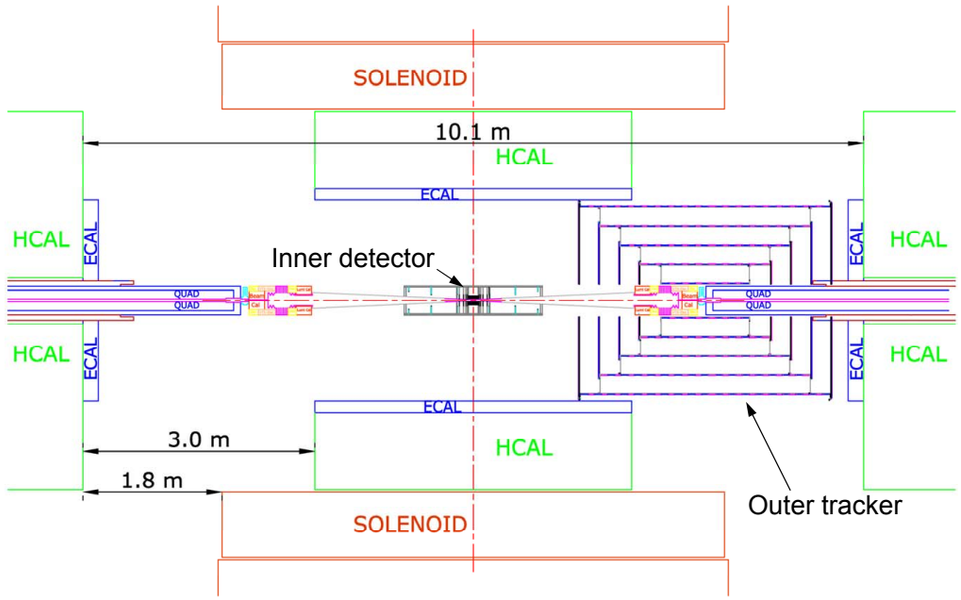
FNAL, SLAC

Nested cylinders supported by annular rings

- Inner portion of disks supported with VTX to allow servicing
- Support rings also host power distribution and data concentrators: existing optical transceivers can easily meet requirements
- DC/DC conversion or serial powering assumed to reduce cable plant
  - Peak current for tracker is 5000 amps
  - Lorentz forces could be problematic

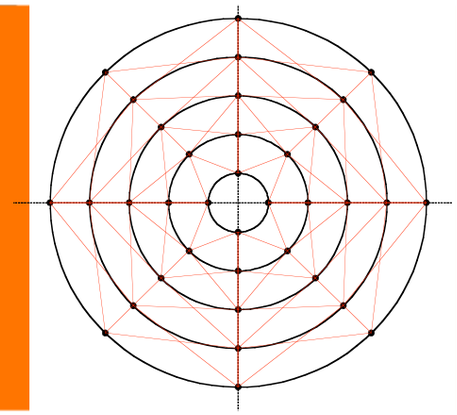
This is an area of generic detector R&D where more effort is still needed





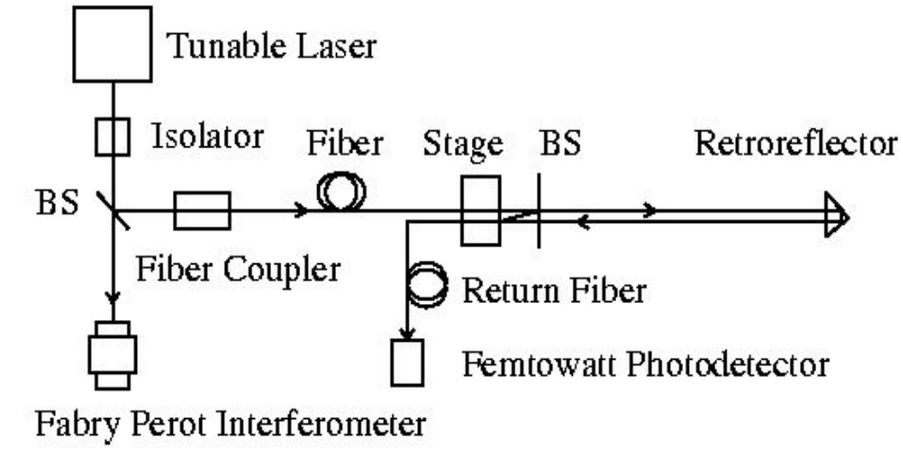
Dual Laser FSI

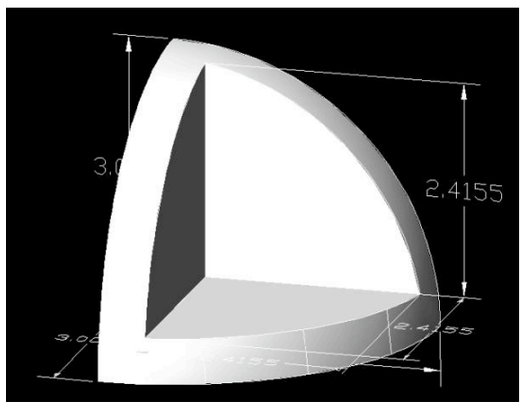
U. Michigan

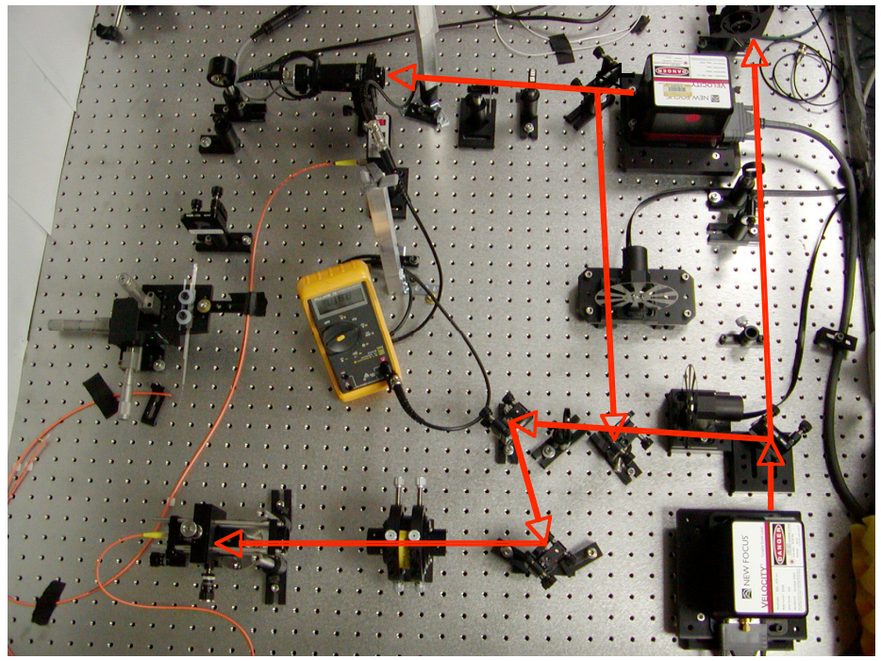


Aggressive material trimming, pulsed-power and push-pull may create need for alignment monitoring

- Absolute distances measured to ~200nm in real-world conditions with commercial optics
- Working on miniaturization: initial testing achieved 70nm precision with corner cube array
- Simulations of resolution degradation due to tracker distortions continuing





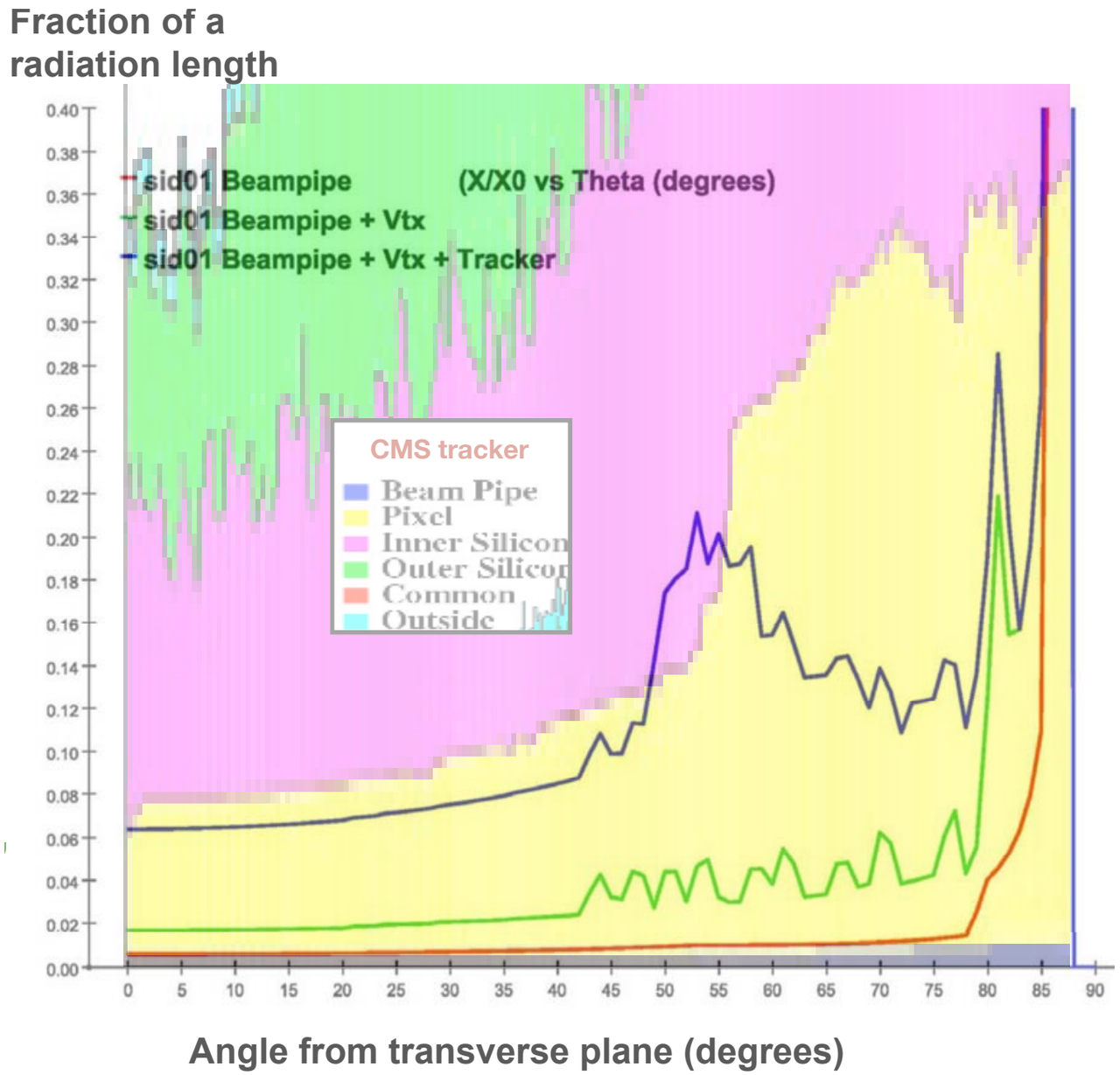


*Si*D Material Estimates

Scrupulous attempt to account for material

- Included in GEANT: sensors, chips, cables, connectors, bypassing, glue, module supports, module mounts, overlaps, power distribution boards, DAQ for baseline design
- Not included: alignment monitoring, mounting to ECAL, voids in large scale support structures
- Goal 0.8%/layer, currently 0.92%/layer

Good enough? Simulation required.



Summary: Towards an LOI?

- *Hardware:*
  - Develop concept for lightweight silicon tracker that passes “laugh test”
  - Demonstrate that proposed technical approaches meet our requirements
- *Simulation:*
  - Demonstrate that concept is light enough
  - Demonstrate that concept provides efficient tracking (w/ VXD, CAL)
  - Demonstrate that concept performs well in forward region

Good progress... some hardware R&D still needed for LOI

*Simulation, physics studies are **critical** to complete the picture for an LOI*