SiD KPiX Electronics

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- Electronics requirements
- KPiX concept
- Performance
- Plans

Si-W work – personnel and responsibilities

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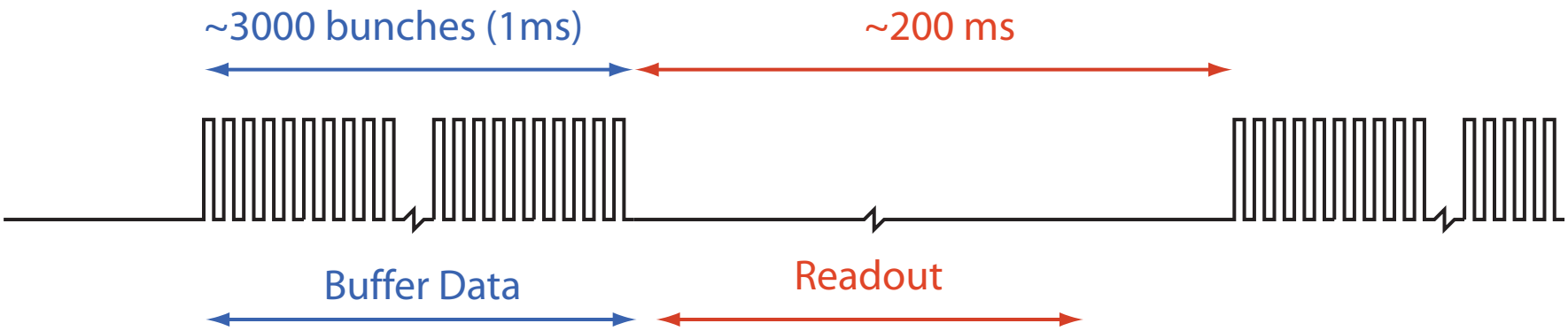
Mechanics	**Electronics**	**Bump Bonding** **Cabling** Mechanics	**Si Detectors** Mechanics Simulation	**Electronics** Mechanics **Simulation**

Bunch Structure at the ILC



- Duty cycle of bunches is low, $\sim 1/200$

$\Rightarrow$ Only provide high current to front end during bunch train

Reduces power

- In the high granular SiD concept, occupancy is low

$\Rightarrow$ Buffer data during the bunch train

Potential to minimize digital interference to analog signals

How many buffers are needed?

Study* with Luminosity $= 3 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$, 2820 bunches/train

The following processes were simulated:

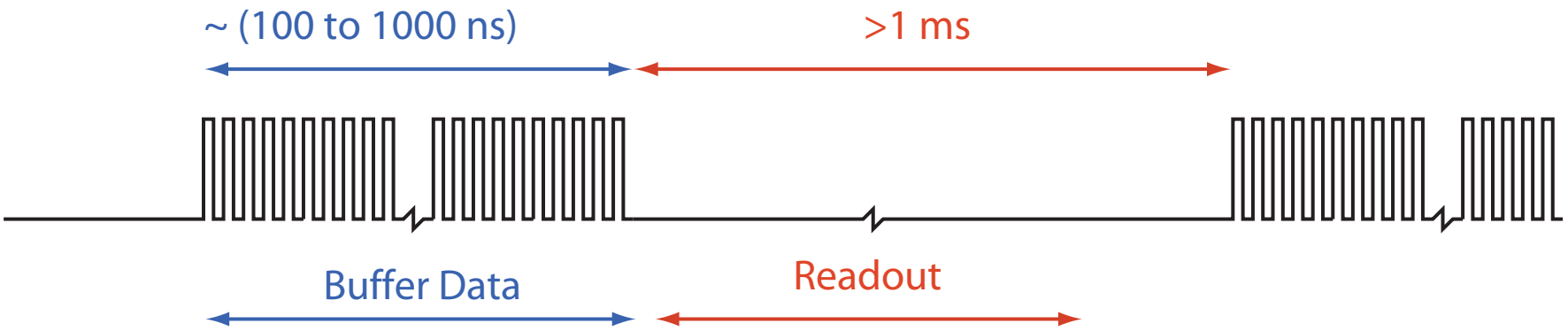
- $e^+e^- \rightarrow hadrons\ e^+e^-$
- $e^+e^- \rightarrow \mu^+\mu^- e^+e^-$
- $e^+e^- \rightarrow e^+e^- e^+e^-$
- Bhabhas
- Radiative bhabhas

showed that with 4 buffers, we have less than 1% dead time, everywhere in the ECAL (down to $\theta = 120\,mrad$).

HCAL occupancy should be lower.

* Ron Cassel, SiD LCWS mini-workshop 17 March 2005.

Bunch structure in warm machines



- Requires faster power pulsing for electronics:

$\Rightarrow$ 10μs possible in simulation (but not yet demonstrated)

$\Rightarrow$ 100μs would give $<$ 1.25% duty cycle

- Faster clock needed for better timing resolution

- At 50 MHz clock rate, could transfer 400kbits/train in 8msec

$\Rightarrow$ Need $\sim$ 25kbits/train for one buffer

$\Rightarrow$ Zero suppression possible – could readout in less than 1ms

Dynamic range

- Electromagnetic Calorimeter (300 μm silicon sensors)
  - smallest signals 1MIP (1MIP = 24,000 electrons = 3.8 fC)
  - largest signals 2000 MIPs (8.0 pC) at 1 TeV

- GEM based HCAL
  - typical signals 5 to 30 fC (depends on gain used)

- RPCs
  - typical signals $\sim$ 0.2 to 10pC avalanche mode

(more than 100 pC for streamers, depending on gas)

- Tracker requires noise less than 1000 electrons

$\Rightarrow$ Design electronics for $\sim$ 0.16 fC to $\sim$ 10 pC

Power requirement – Can we get the heat out?

Back of the envelope calculation
of Δ temperature in ECAL

Thermal Conductivity:
- W alloy 120W/(K-m)
- Cu 400W/(K-m)

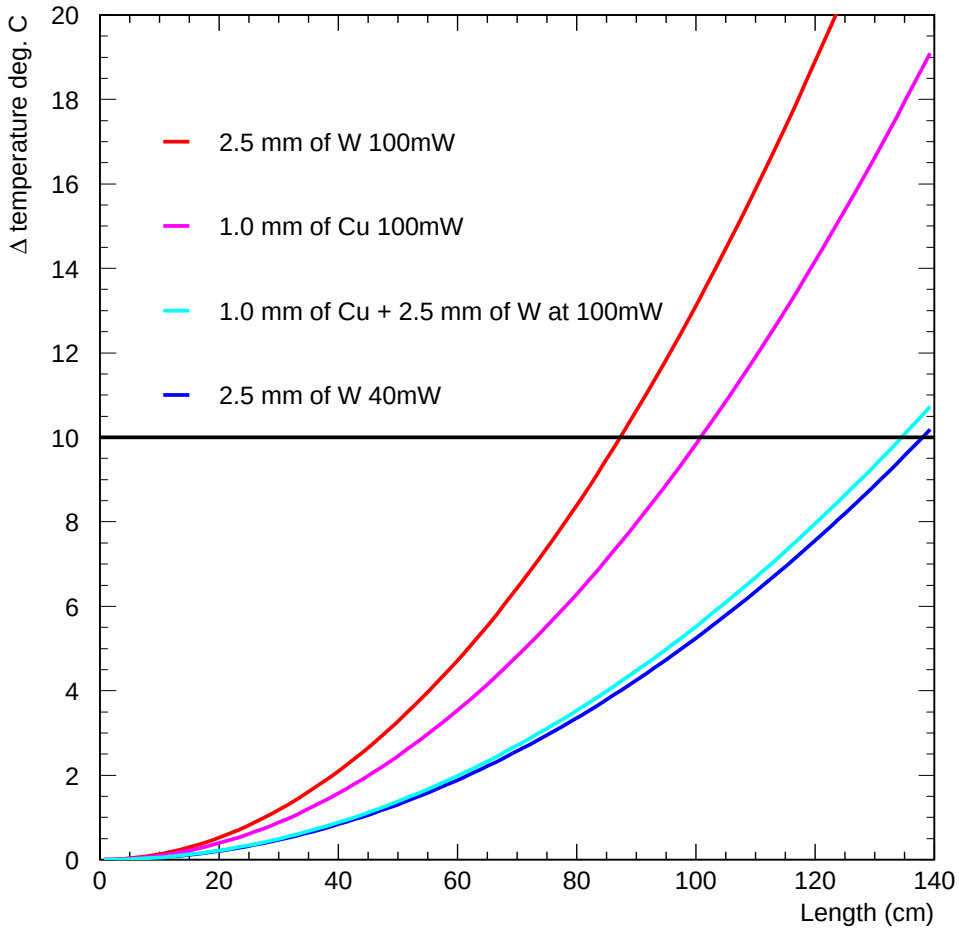
Need to reduce heat to below 100mW/wafer ($\sim$ 1mW/cm^2).

- HCAL will be easier

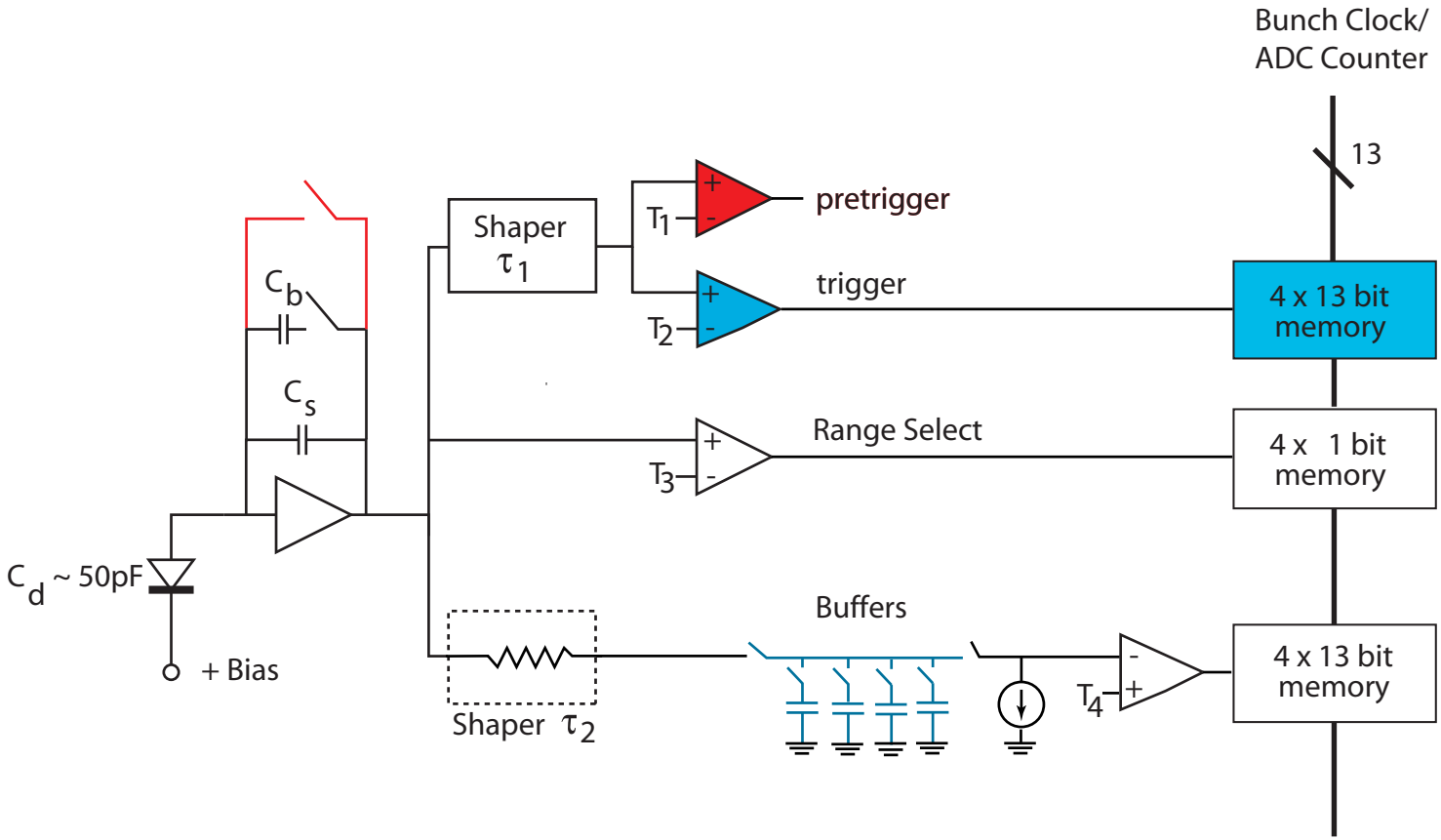
$\Rightarrow$ lower channel density

$\Rightarrow$ thicker absorber

Present design $\sim$ 20 mW
Consistent with prototype measurements

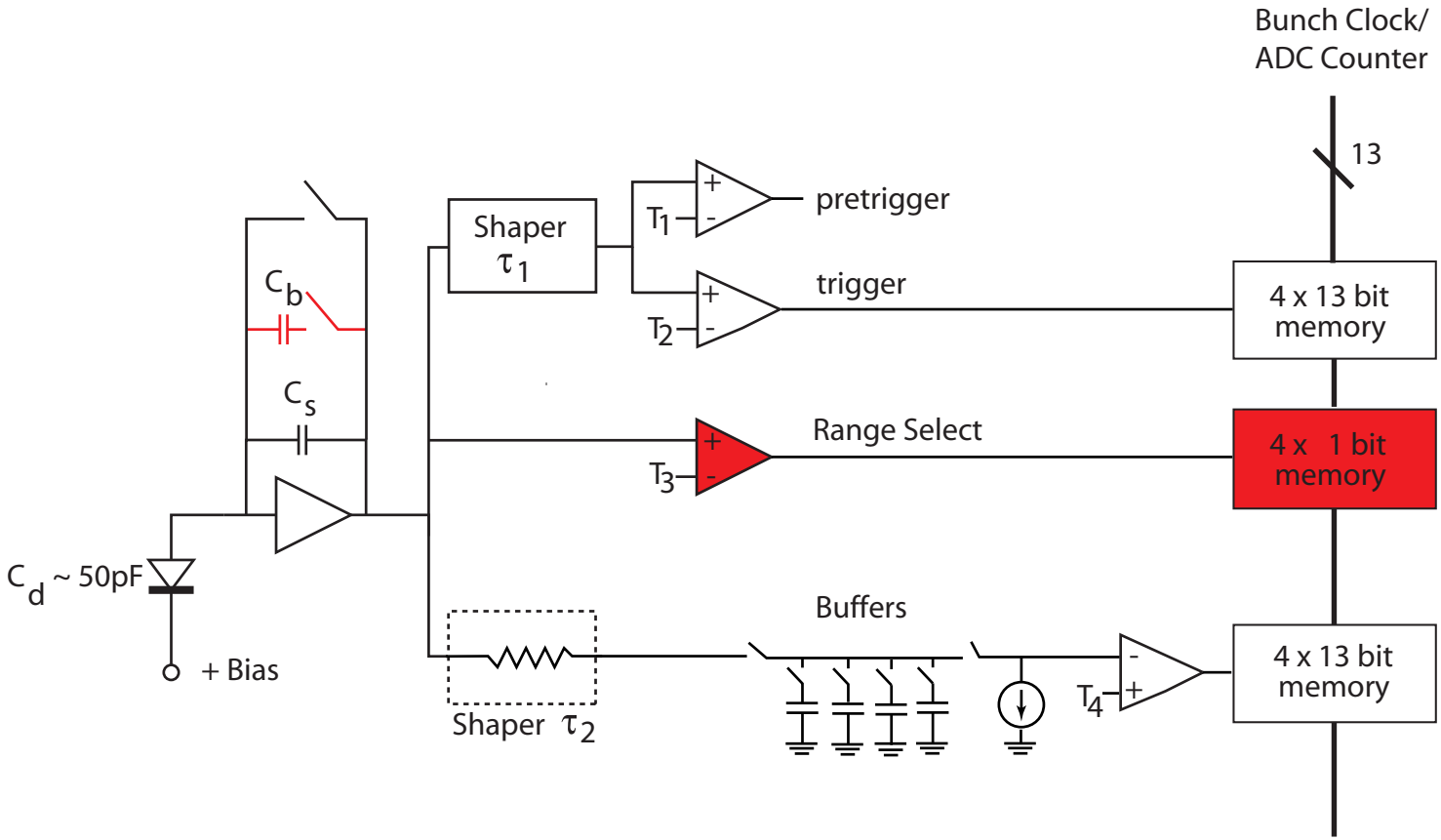


KPiX Concept – saves up to 4 samples from each train



- Threshold T_1 is used to inhibit resets (set at 2 $\times$ noise)
- Threshold T_2 is used to enable data storage (set at 4 $\times$ noise)
- Bunch clock (time) is stored in SRAM (13 bit precision)
- Analog charge is stored on capacitors (13 bit precision)

Range Switching



- Dynamic range switching (driven by threshold T_3) selects C_s or $C_b||C_s$

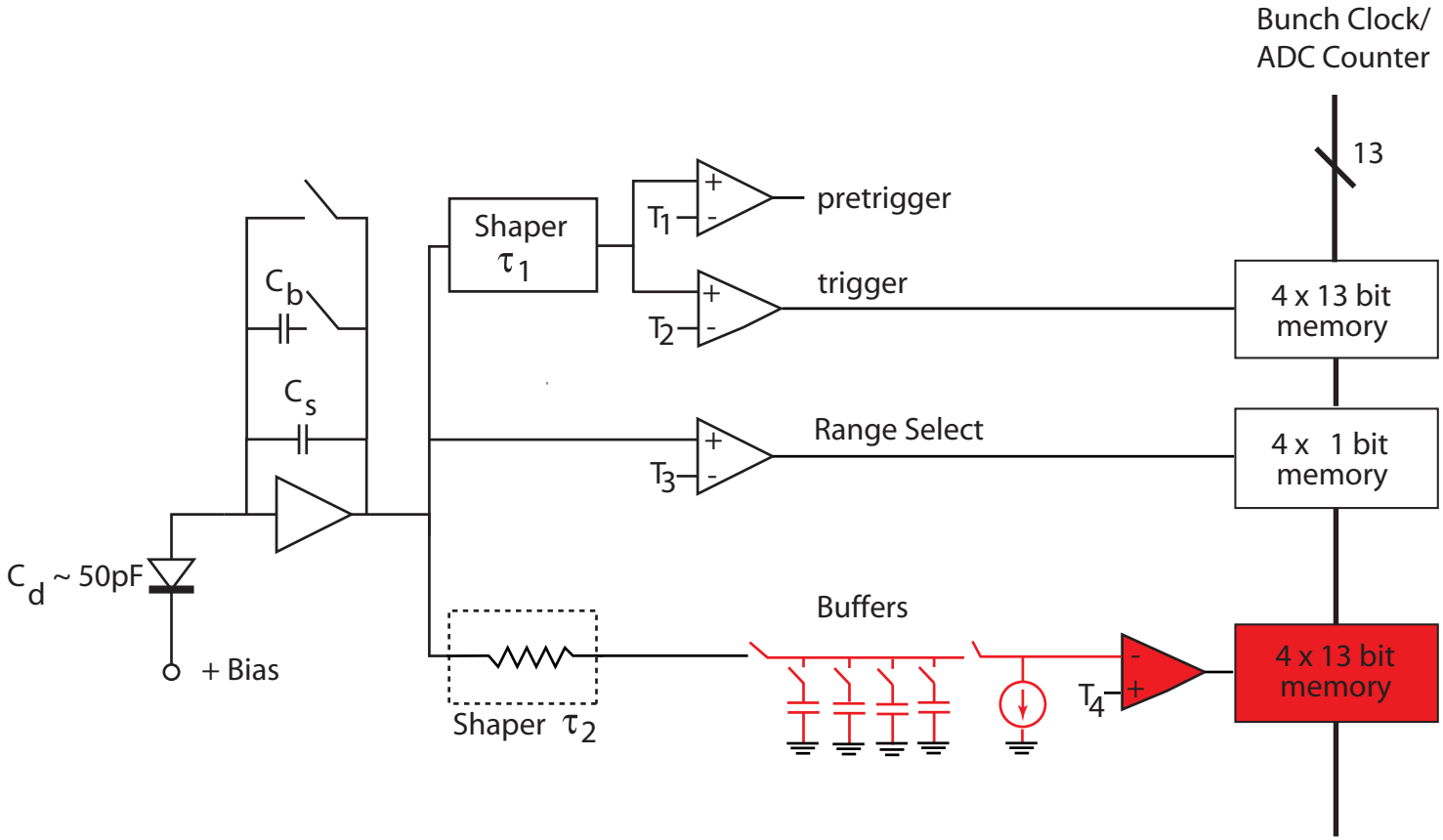
$\Rightarrow$ Feedback capacitor $C_b = 10\,\text{pF}$ stores up to 10 pC

$\Rightarrow$ Feedback capacitor $C_s = 400\,\text{fF}$ (0.3 fC gives 0.7 mV)

$\Rightarrow$ Feedback capacitor $C_s = 200\,\text{fF}$ for tracker (0.16fC gives 0.8 mV)

N.B. Switches to capacitors closed for several RC times so signals settle

Charge Digitization (between bunch crossings)



- Time needed to discharge each capacitor stored in 13 bit memory
- Time is combined with range bit to correct amplitude

Additional features not shown in simple schematic:

- Built-in calibration system with 2 calibration ranges and up to 4 injections per bunch train
- Choice of two values for pretrigger and trigger thresholds
- Bias current servo system for DC coupled detectors

Additional features added in prototype versions 3 or 4:

- Polarity selection (mainly for GEMs)
- External trigger for test beam
- Nearest neighbor trigger logic
- Staticly selectable feedback capacitor for tracker

All these features are tested and working

Chip Size

- Chip is implemented in TSMC 0.25μm CMOS
- Single analog channels comfortably fits into 200μm by 500μm cell
- Overall chip size (1024 channels) approximately:

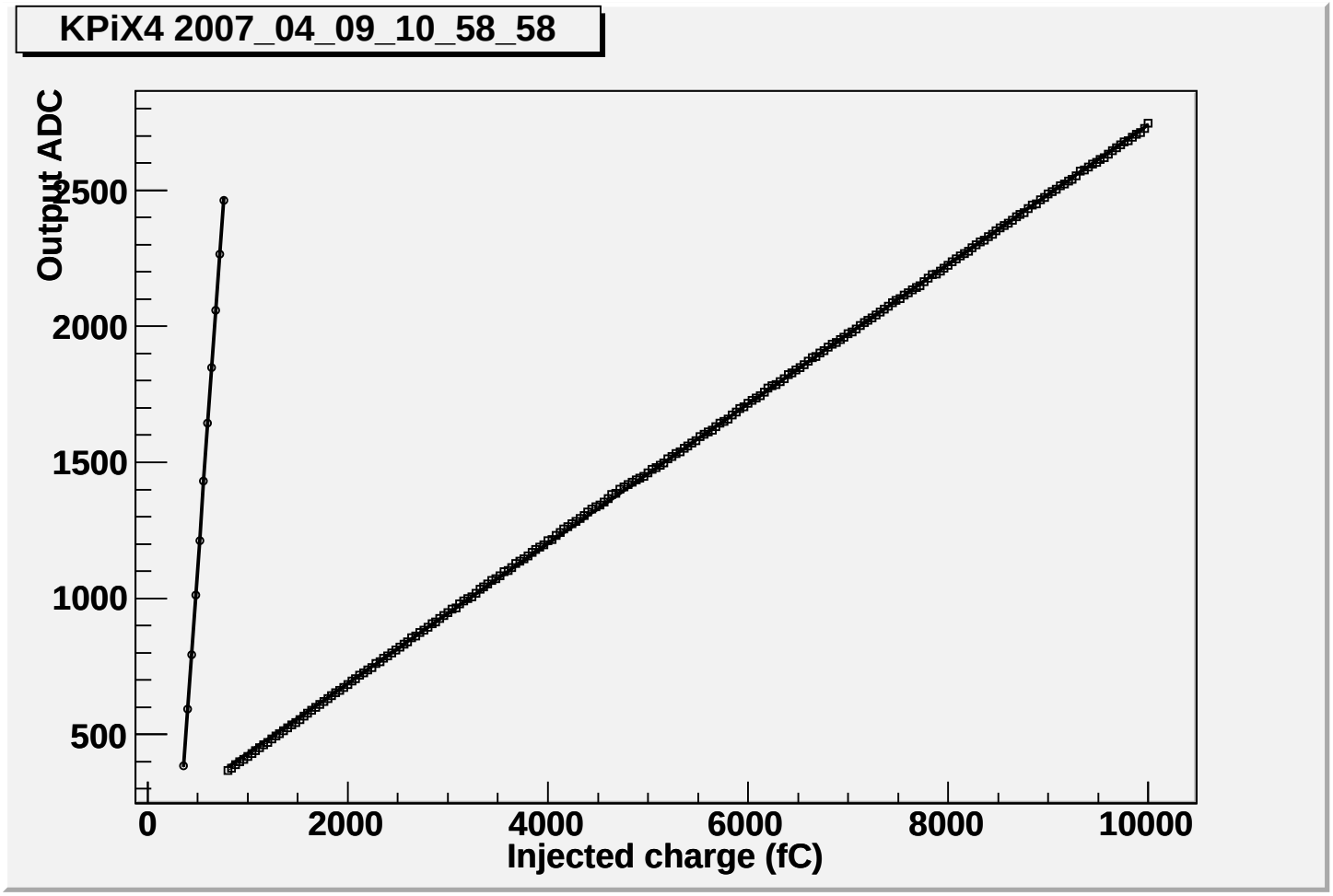
$$18\,\mathrm{mm} \times 6.5\,\mathrm{mm} \sim 1.2\,\mathrm{cm}^2$$

- Aspect ratio helps in routing traces on silicon sensors
- Could not reduce chip size without making bump bounding more difficult

Overall chip size close to optimal

Performance – 64 channel prototype

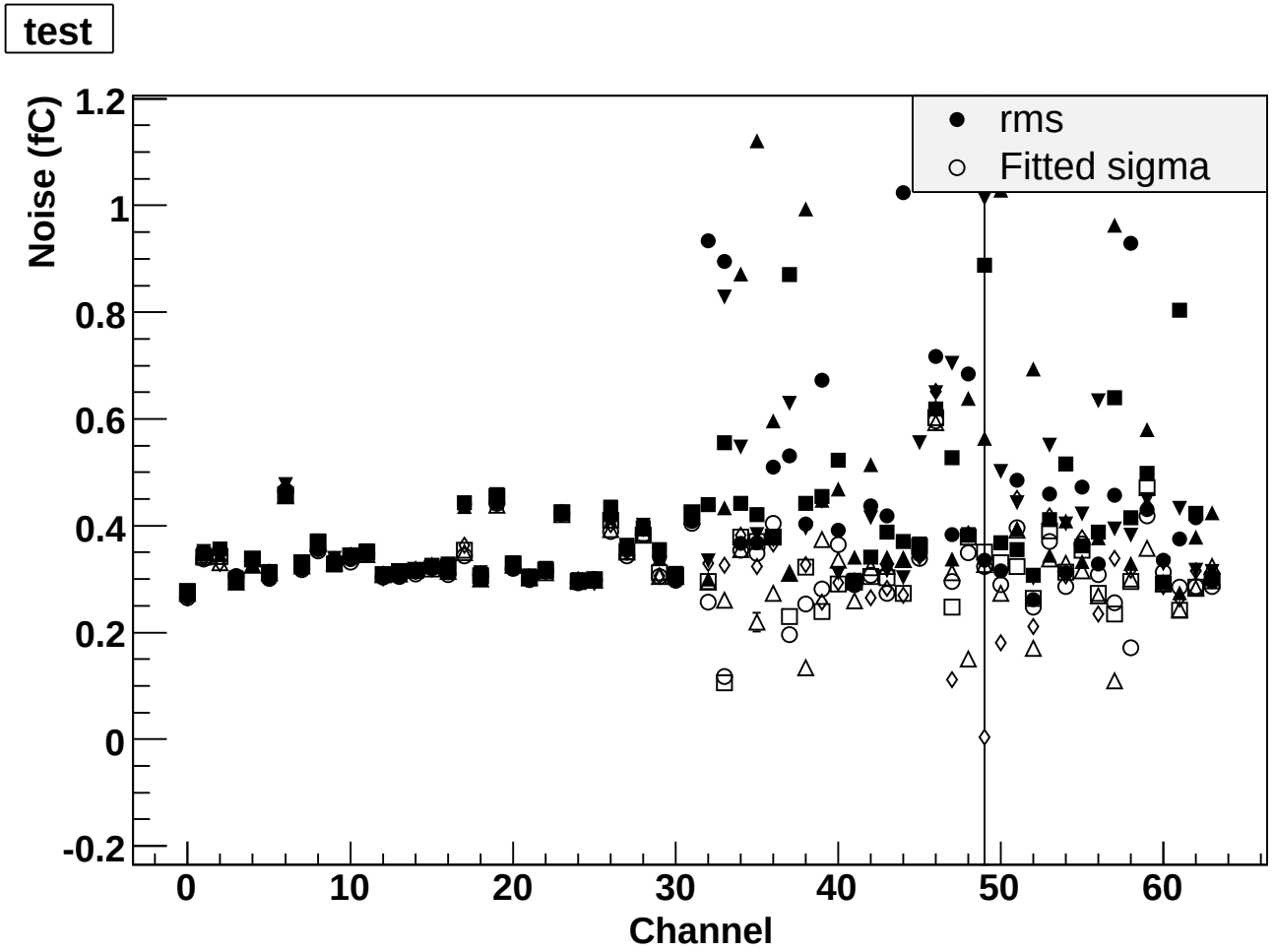
Range switching feature works as designed



Linear behavior extends beyond 10 pC

(Nonlinear behavior extends range by 50% or more)

KPiX 6 noise in the digitized charge value similar to 5 and 4.



Bit errors observed in KPiX5 and 6 in upper 32 channels.

Different symbols correspond to the four buffers on each channel

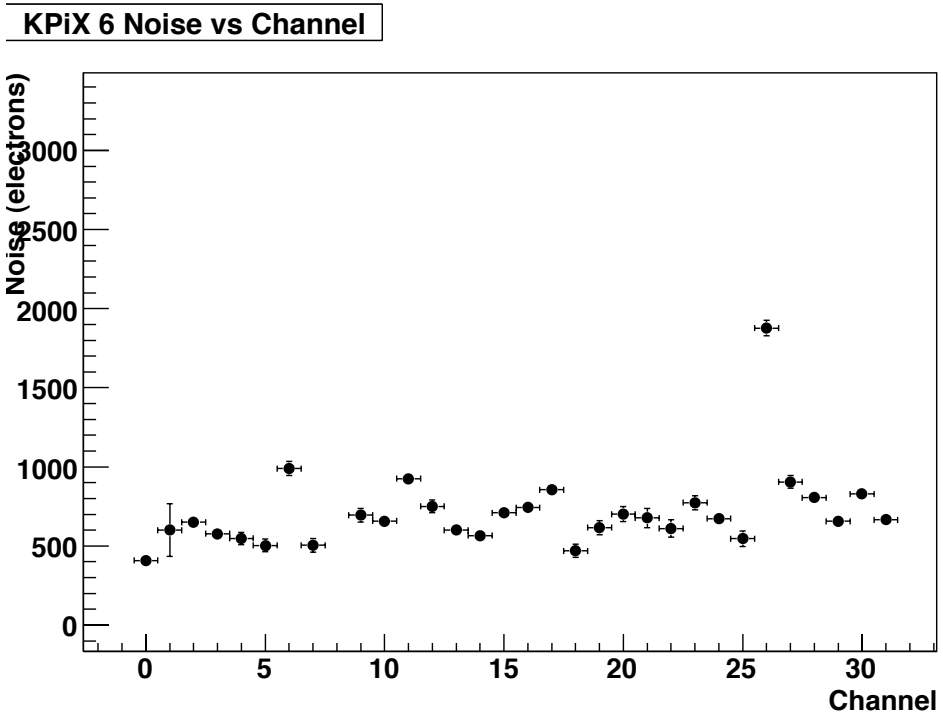
- Meets spec of signal noise 8:1 for MIPs in ECAL, but not yet at full capacitive load
- Tracker would like signal to noise of 20:1

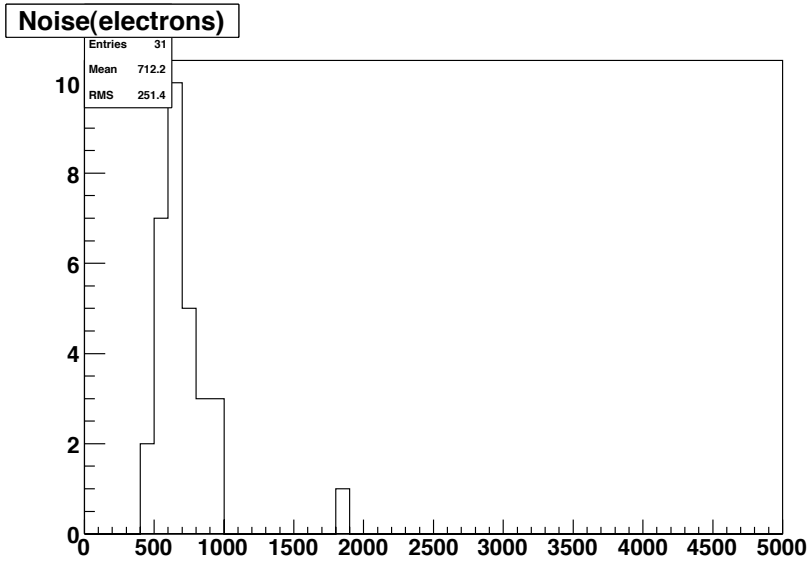
Performance adequate for externally triggered ECAL test beam

Improvements in KPiX 5 and 6

- Many layout changes to reduce coupling
- Improved isolation of digital and analog sections
- Improved current mirrors for equalization of gains
- Improved shaper in trigger branch – disconnect when threshold is reached
- Improved threshold in trigger branch

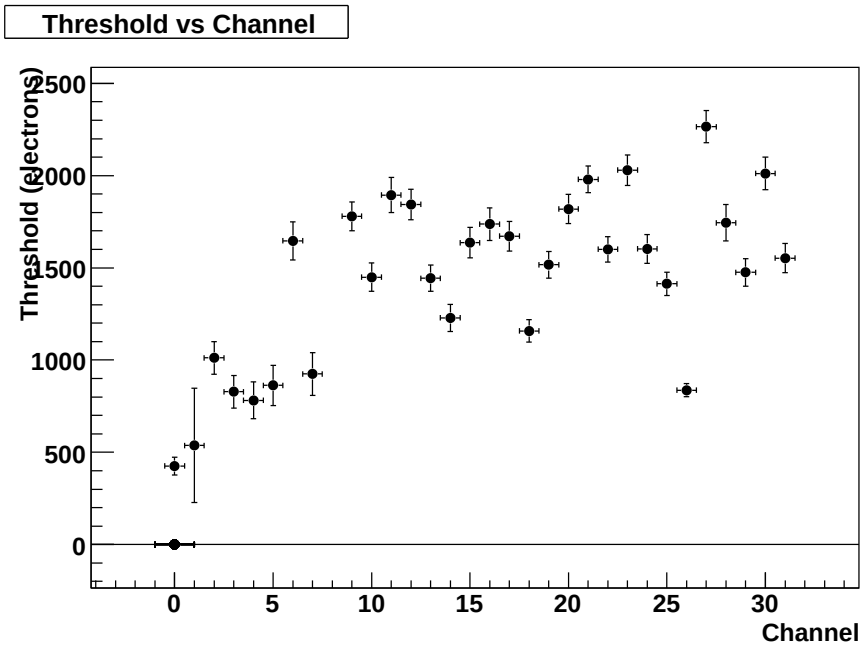
Noise in trigger branch is now very reasonable in KPiX 6.

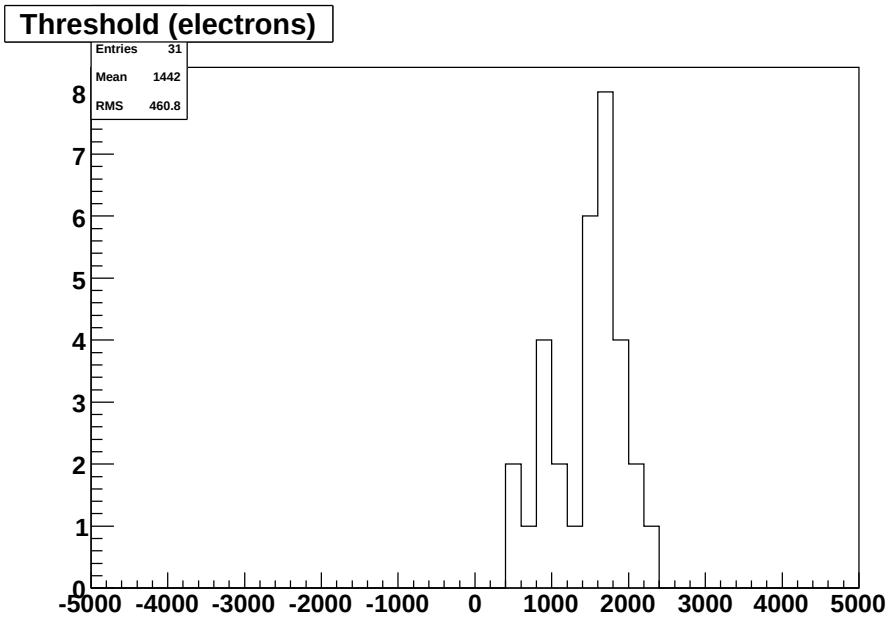




- First 32 channels only, second 32 have possible bit errors in KPiX 5&6 – should be fixed in next version
- ADC noise is similar to KPiX4
- Noise versus capacitance is still under investigation

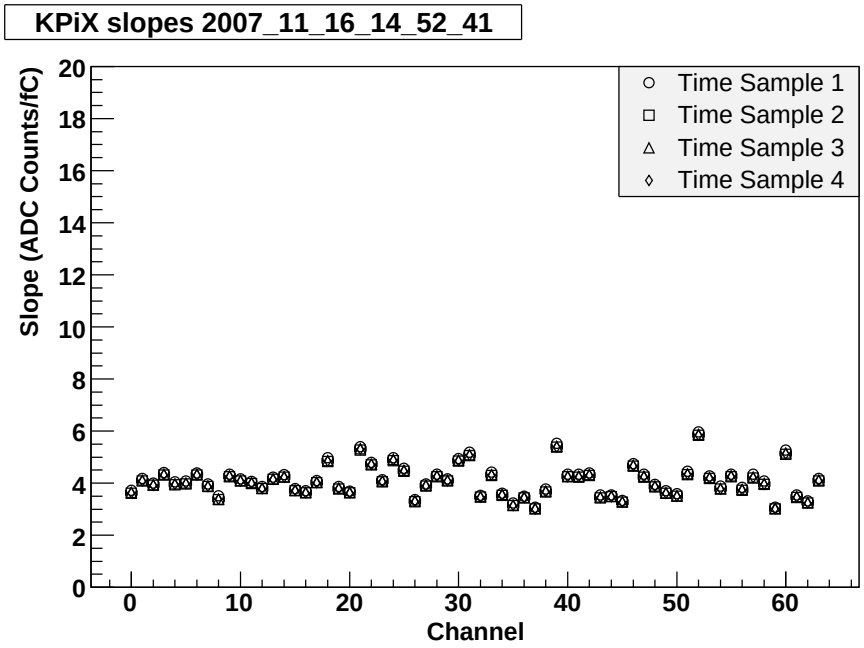
Trigger Threshold are very consistent for channels

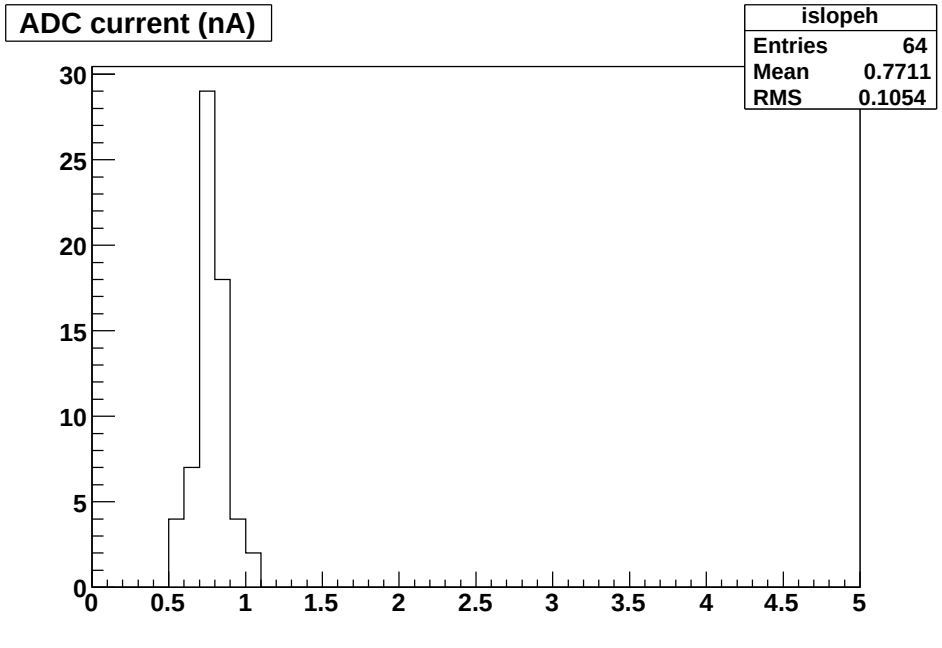




- RMS is only 460 electrons!
- **We will need to control and understand the thresholds at the level of 5% of MIP (1200 electrons) or better to keep the constant term in the calorimeter energy resolution below 1%.**

ADC gain is more equal

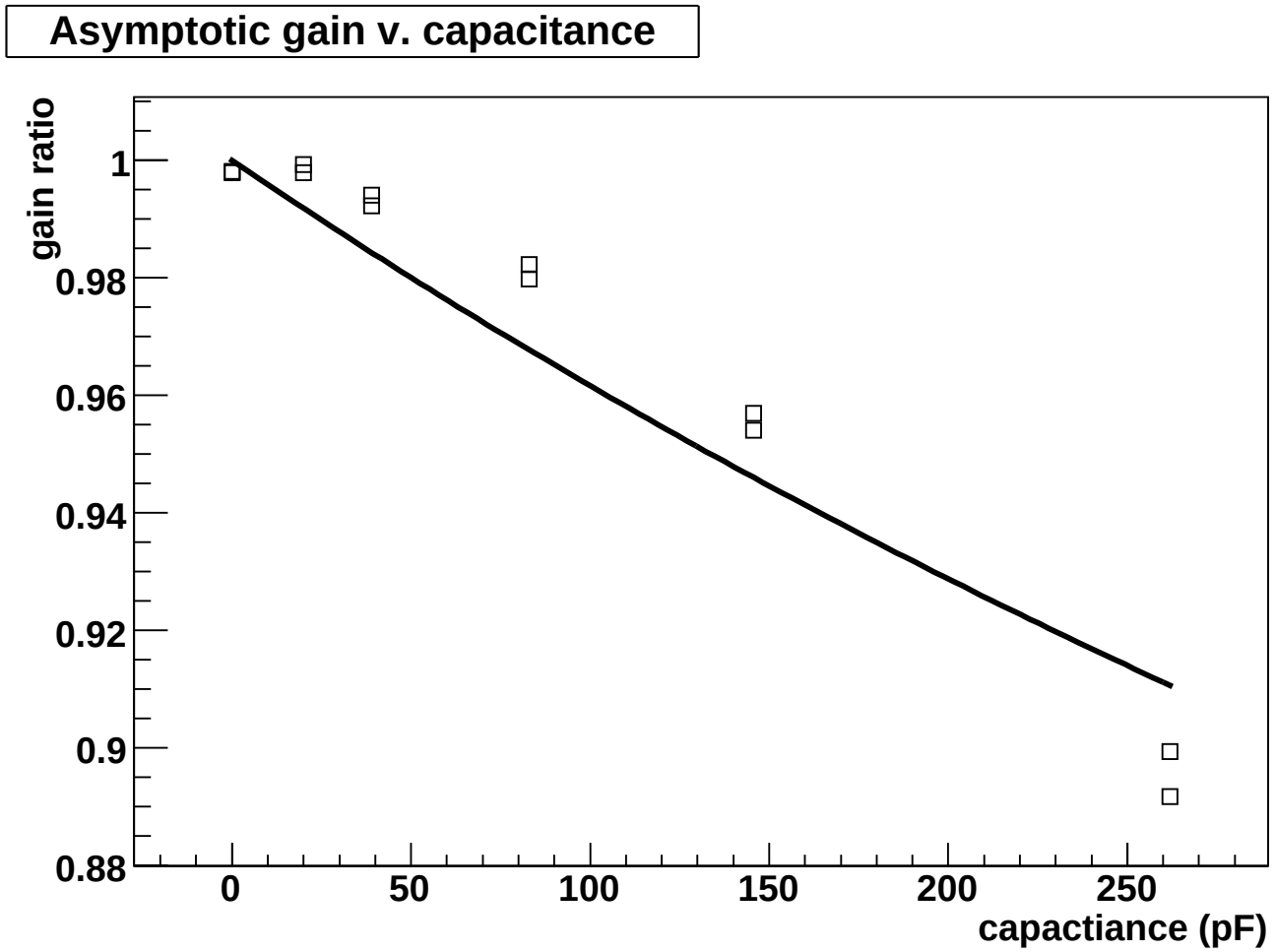




Inferred current in current source agrees with simulation.

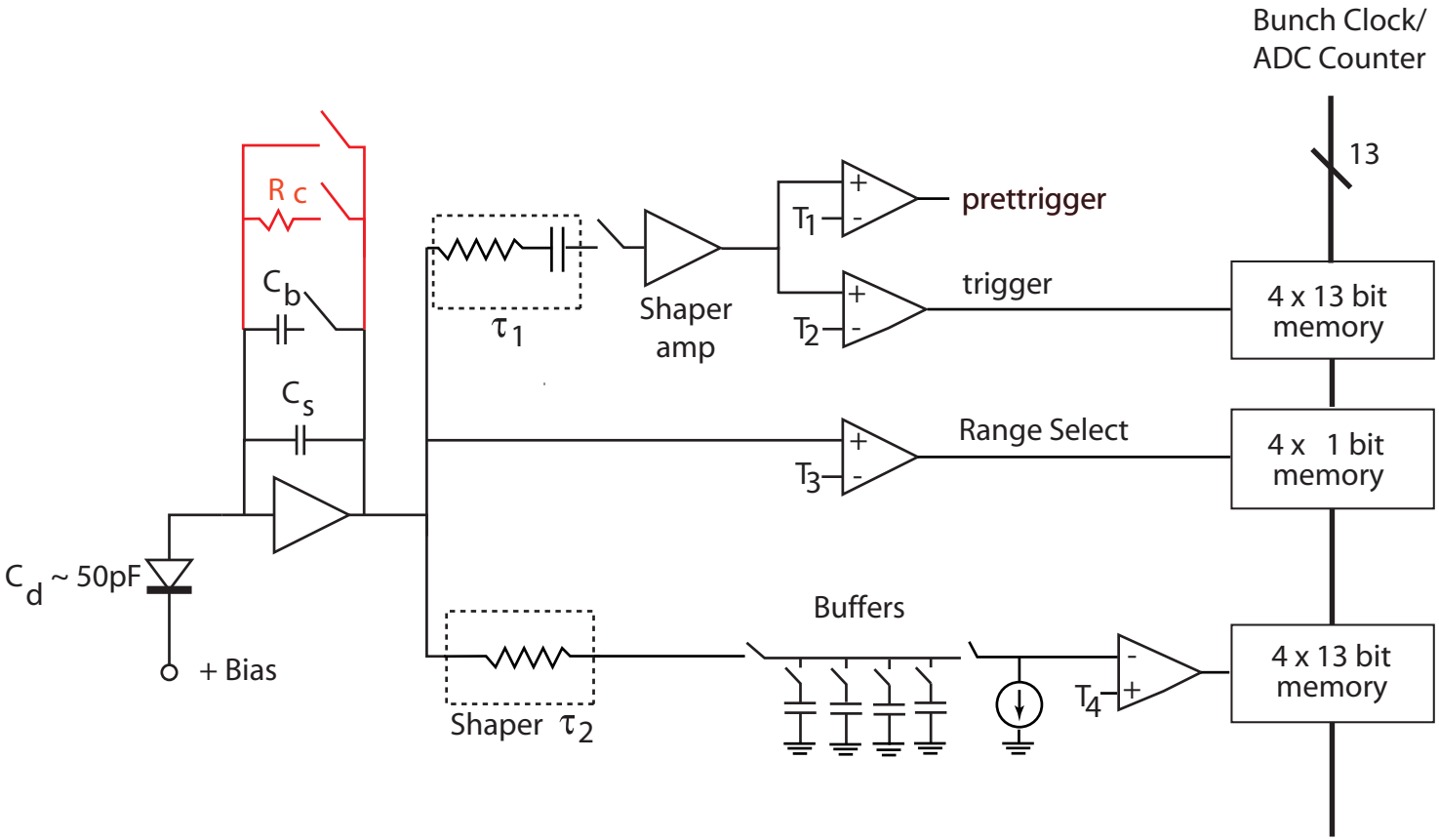
(We will effectively lose about 1 bit of granularity from this spread. This is not expected to be a problem
$\Rightarrow$ still have 16.6 bits of dynamic range.)

Cross talk – depends on "dynamic capacitance" of charge amplifier
Asymptotic gain versus capacitance between two channels



Dynamic capacitance is $\sim$ 2.4nF implies very small cross talk from pF stray capacitances.

Main architectural change for KPiX 7



- Use continuous reset provided by $R_c \sim 10 M\Omega$.
- Remove when trigger or prettrigger occurs

– can accommodate almost any linear collider bunch spacing.

– old functionality available under register control

- Will still need low resistance reset after a DAQ cycle.

Plans

- Broad overview in this talk doesn't do justice to all of the detail changes that are desired for KPiX (Dieter has a list of 36 proposed changes of which 9 are completed)
- Changes to digital core are needed to accommodate a flexible number of bunches, etc.
- At least one intermediate submission is needed with more than 64 channels (e.g. 128 or 256)
- Submissions will be at least four month apart
- Earliest date for 1024 channel chip is eight months from now