# SiD Pigtail Cable Design

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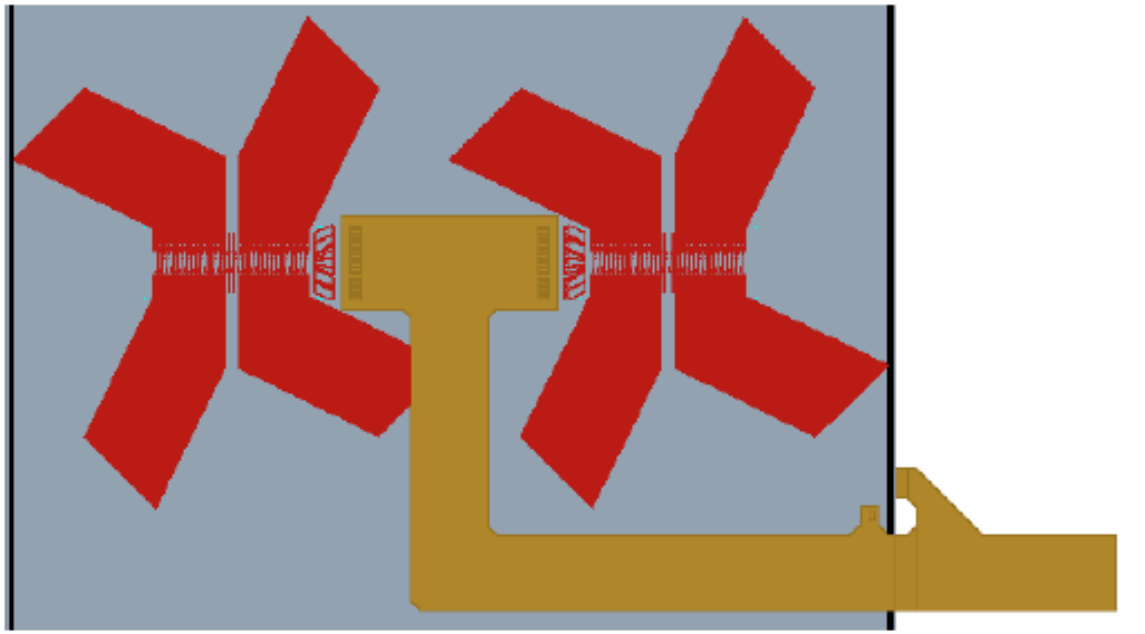
# Introduction

- Low-mass readout cables connect tracker modules to the concentrator boards mounted at the ends of each barrel.



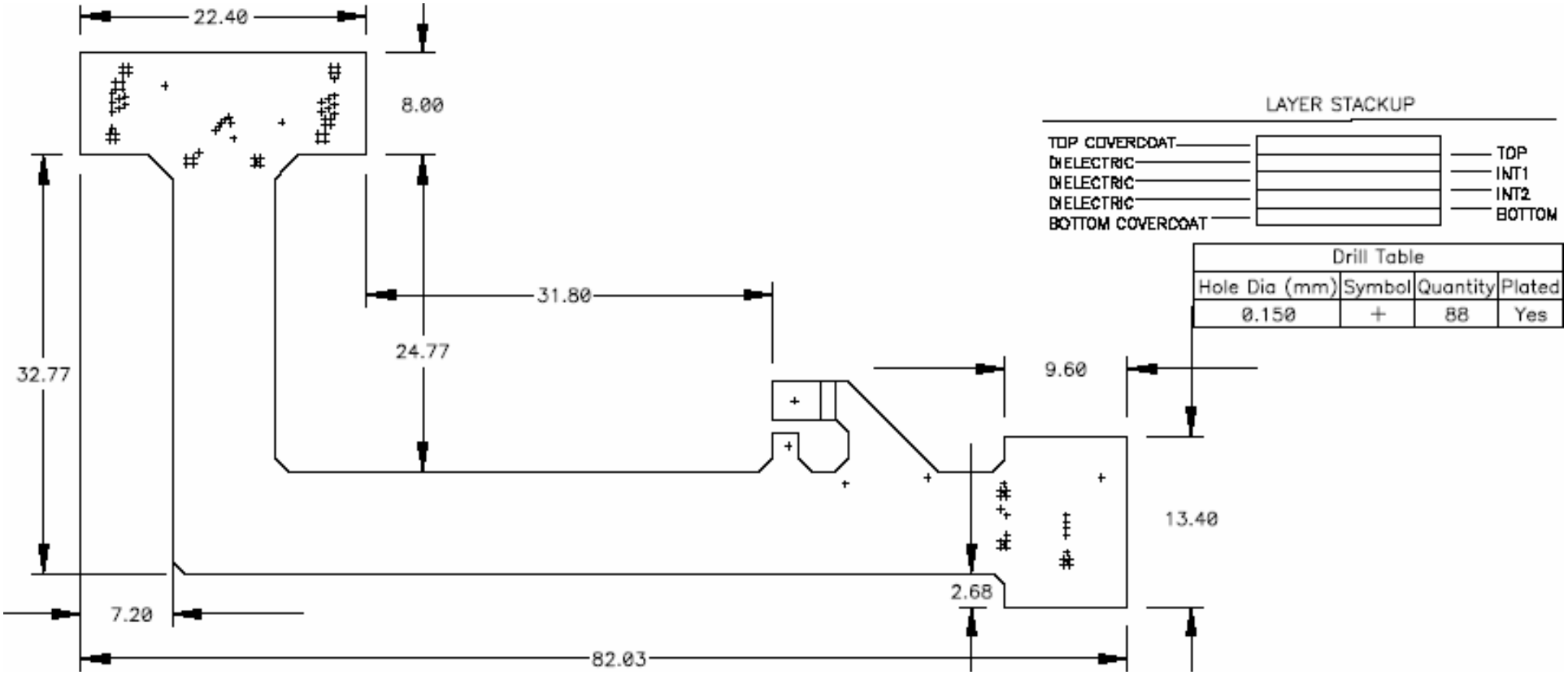
- This cable has two components:
  - Pigtail, a short cable glued to the module
  - Extension, a long cable connecting the Pigtail to the concentrator

# Pigtail Cable Specifications

- Length: ~ 82 mm
- Width: ~ 8 mm
- Thickness: ¼ Oz Cu , 50 micron Kapton thickness
- Connectivity: Detector end connected with wirebonds,
  Extension cable end has a connector,
  HV Bias tabs at sensor edge
- Traces: two pair for Analog & Digital Power
- Traces: one pair for High Voltage Bias
- Traces: 16 traces for Digital Control and Readout, no longer bussed
- Metallization: Gold plating on all wirebond pads only
- Resistance: Pwr and Gnd traces < 1ohm roundtrip including extension
- Filtering: of KPIX and HV Bias on the Pigtail Cable
- Signals: Digital signals are LVDS (low voltage differential signaling)
- Pickup and Crosstalk: big concern, want to minimize

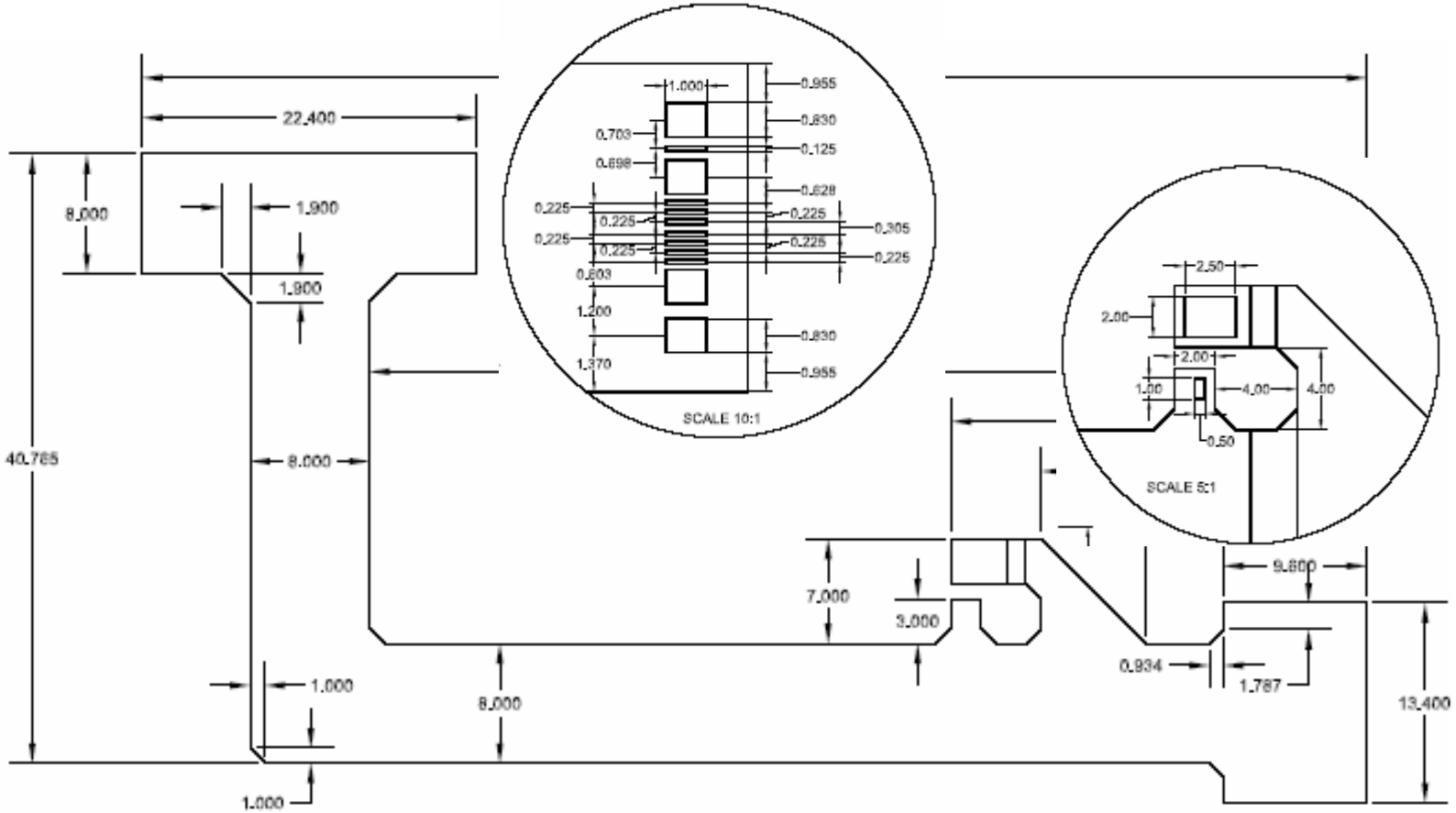
# Dimensions

- Length: ~ 82 mm, Width: ~ 8 mm, Thickness: ~ 250 μm



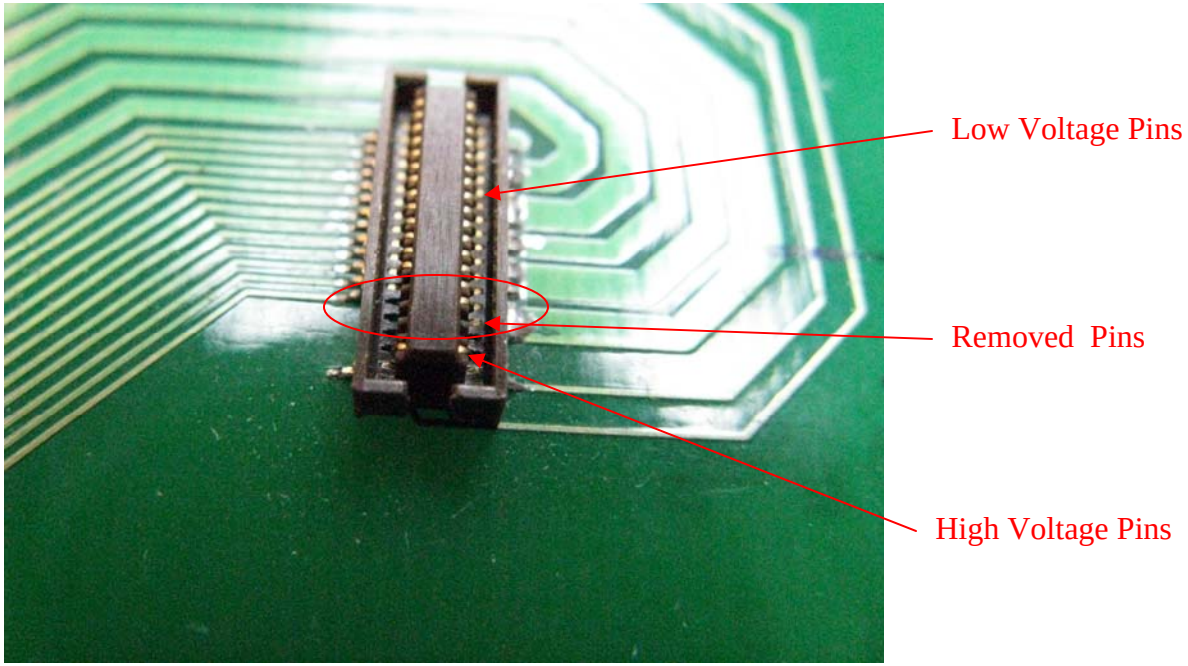
# Connectivity

- Detector end connected w/wirebonds, cable has gold plated pads
- HV Bias tabs at sensor edge have gold plated pads
- Connector to Extension cable (Elco 5087, Hirose DF18, Molex)



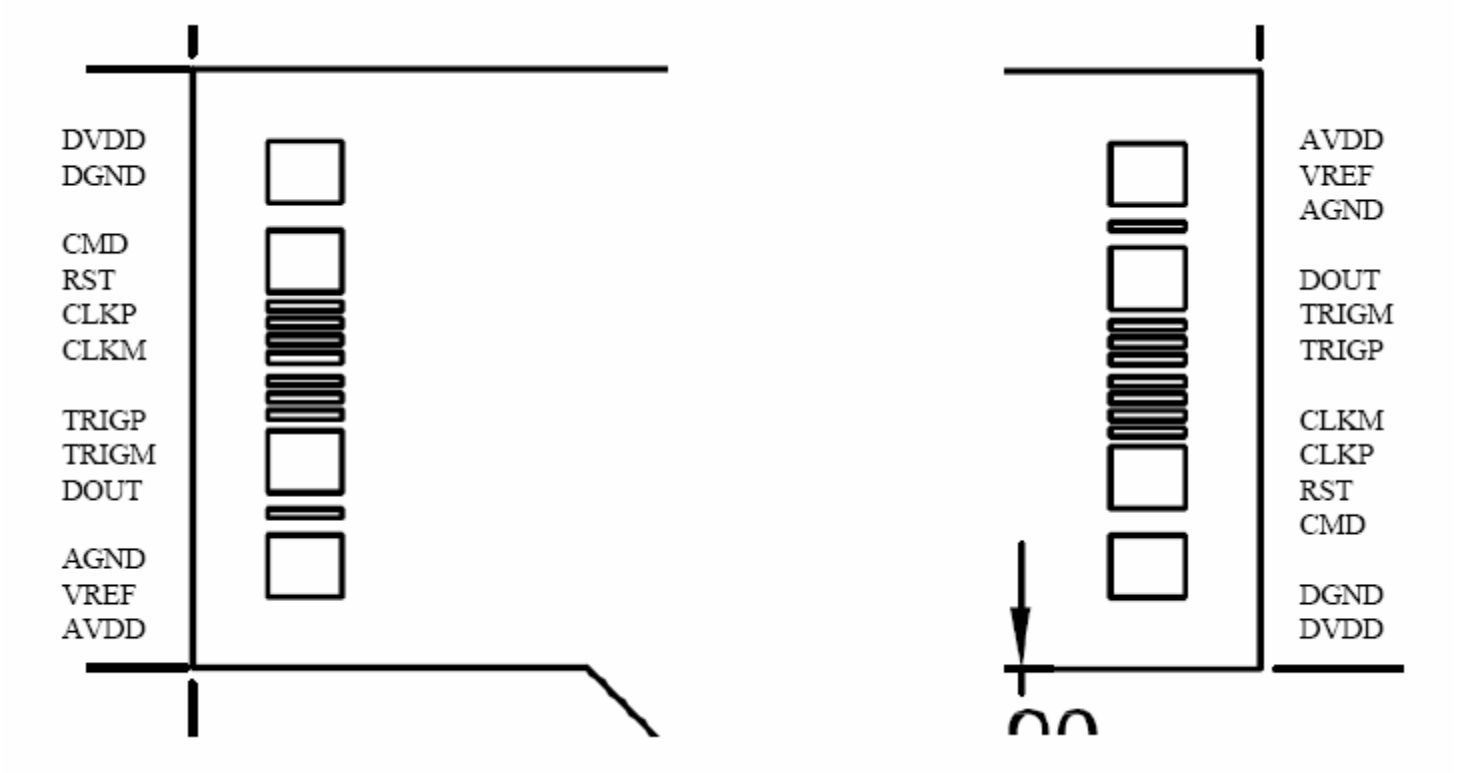
# Connectivity

- High density connectors only have a 30V to 50V rating. Maximum detector Bias voltage ~ 150V.
- High Voltage pins must be isolated from low voltage signals.
- One option is to remove unused pins between high and low voltage signals.
- On D0 pins between High/low voltage were left blank with bias up to ~ 600V



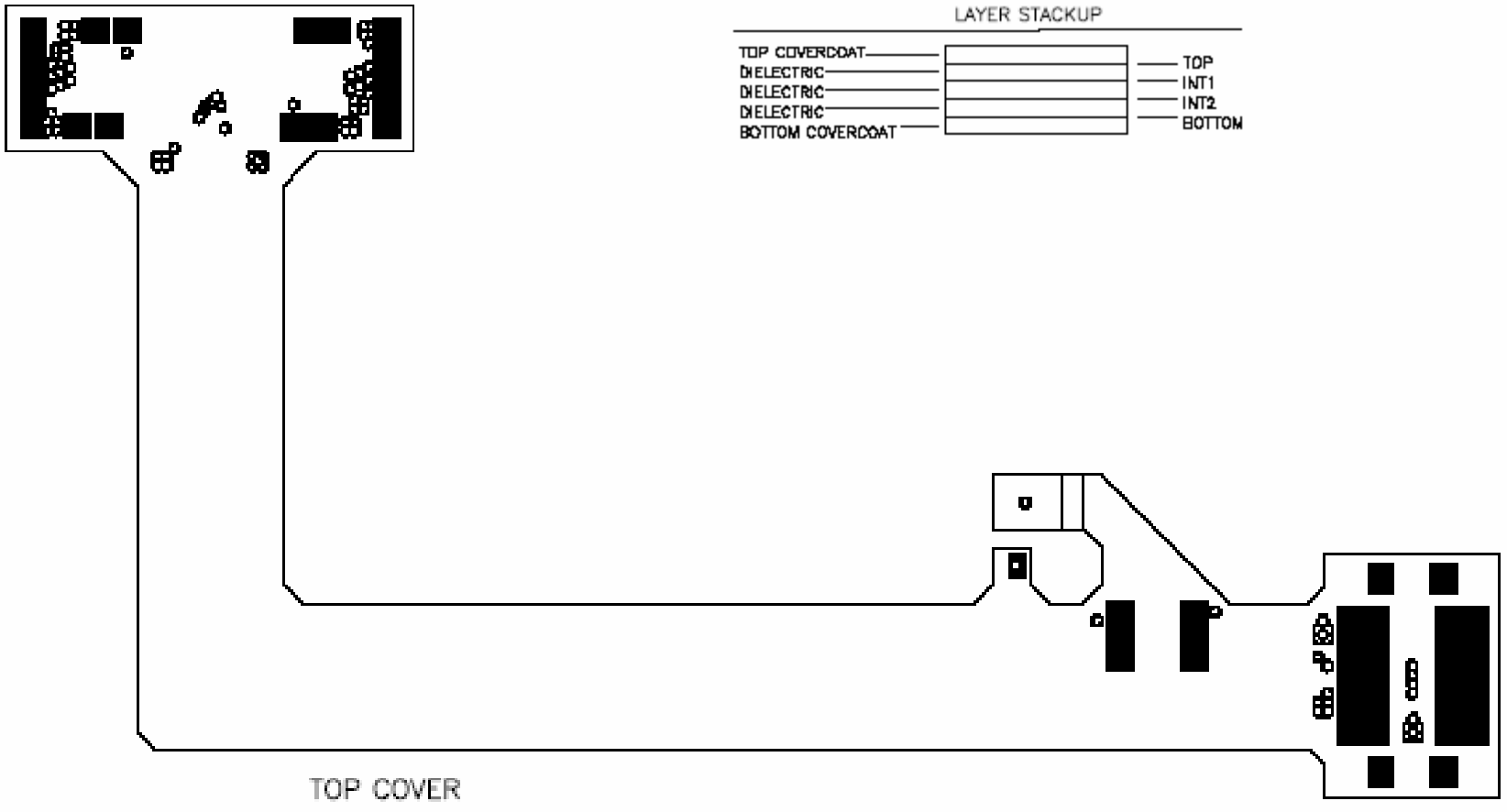
# Wirebond Pads

- Pads & Traces: two pair for Analog and Digital Power
- Pads & Traces: eight for Digital Control and Readout



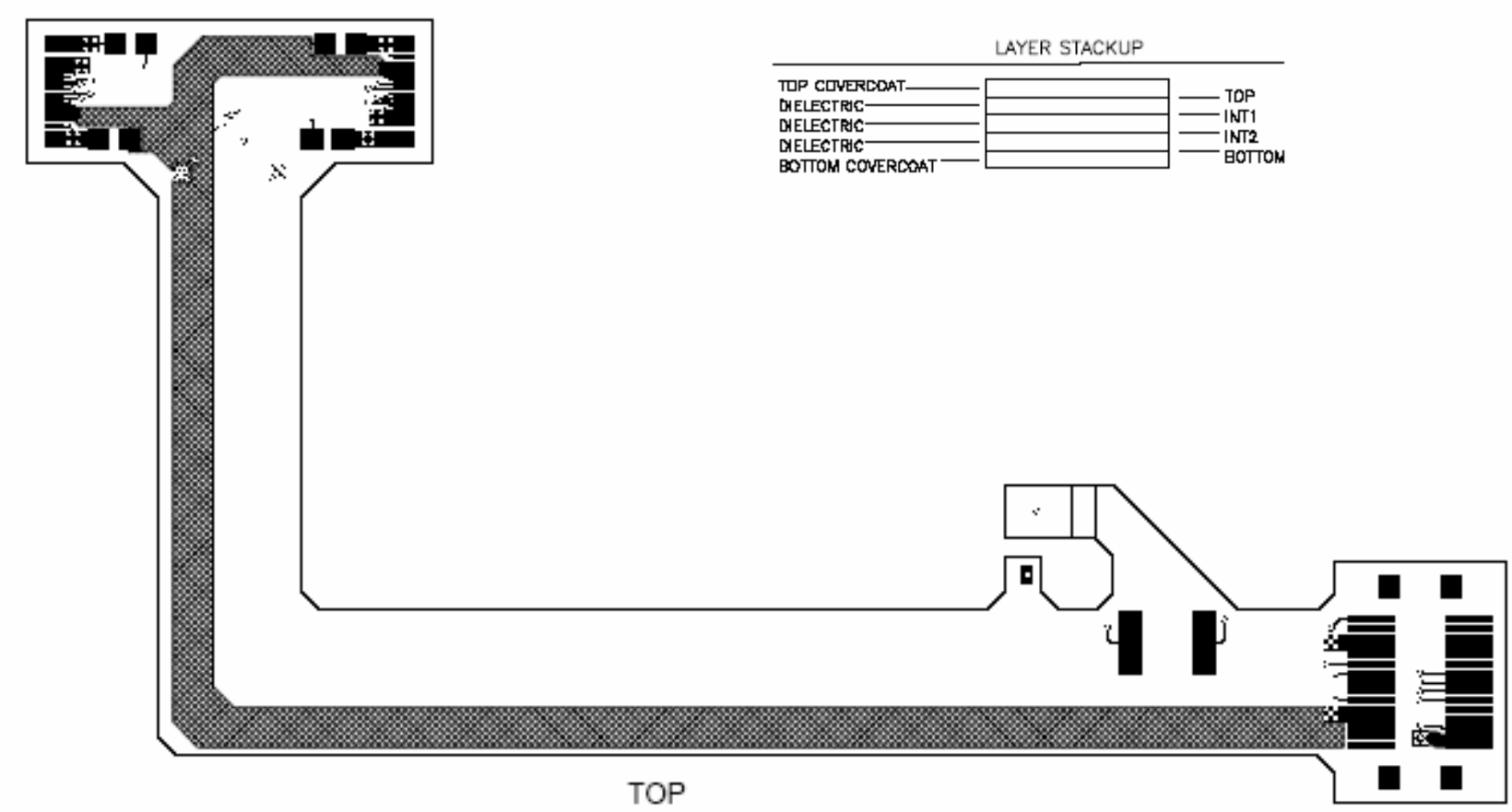
# Layers, Top Cover

- Surface layer of photoimageable covercoat 38 μm thick, to protect the exposed traces.



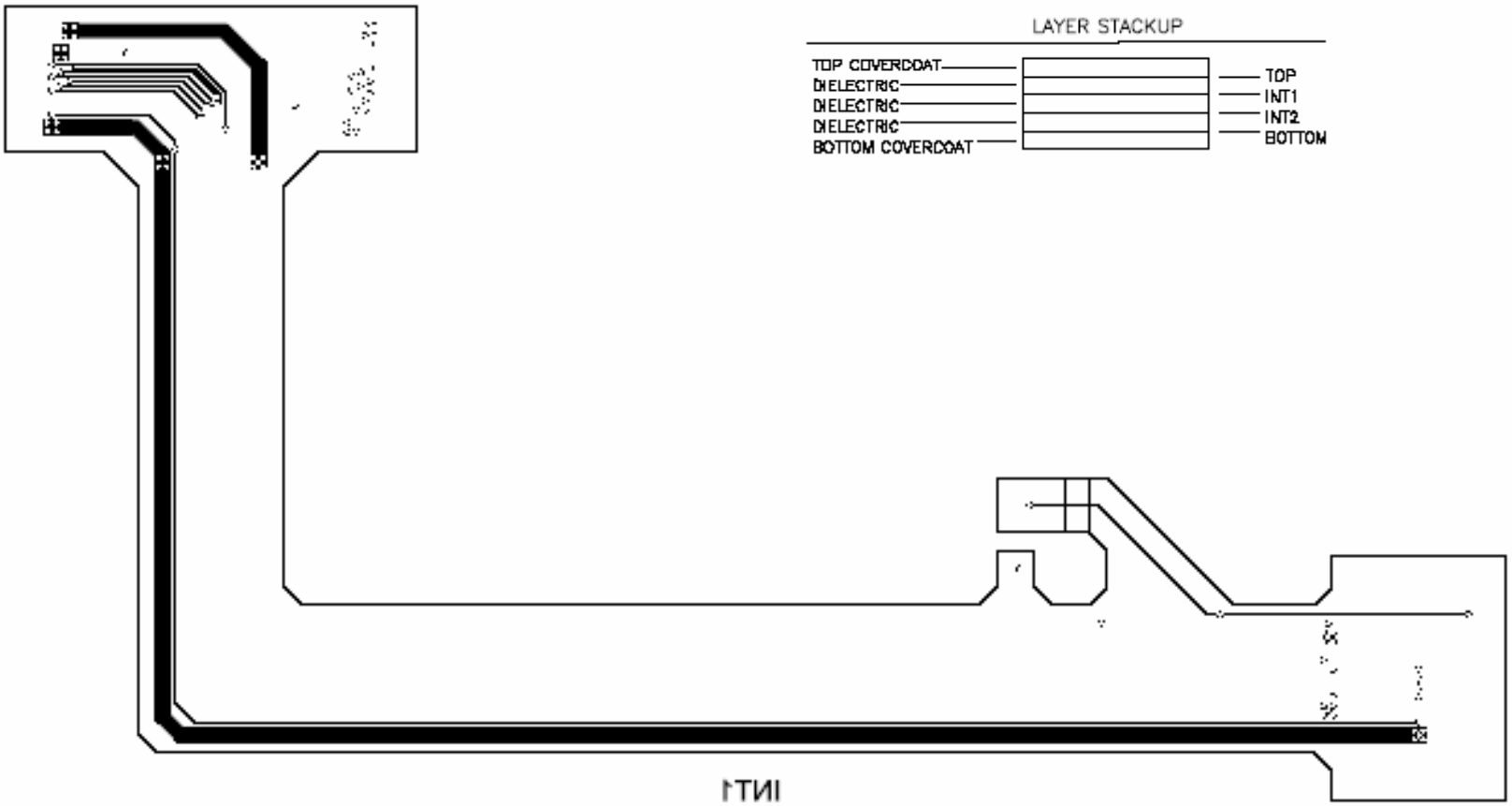
# Layers, Top Layer

- Analog Return



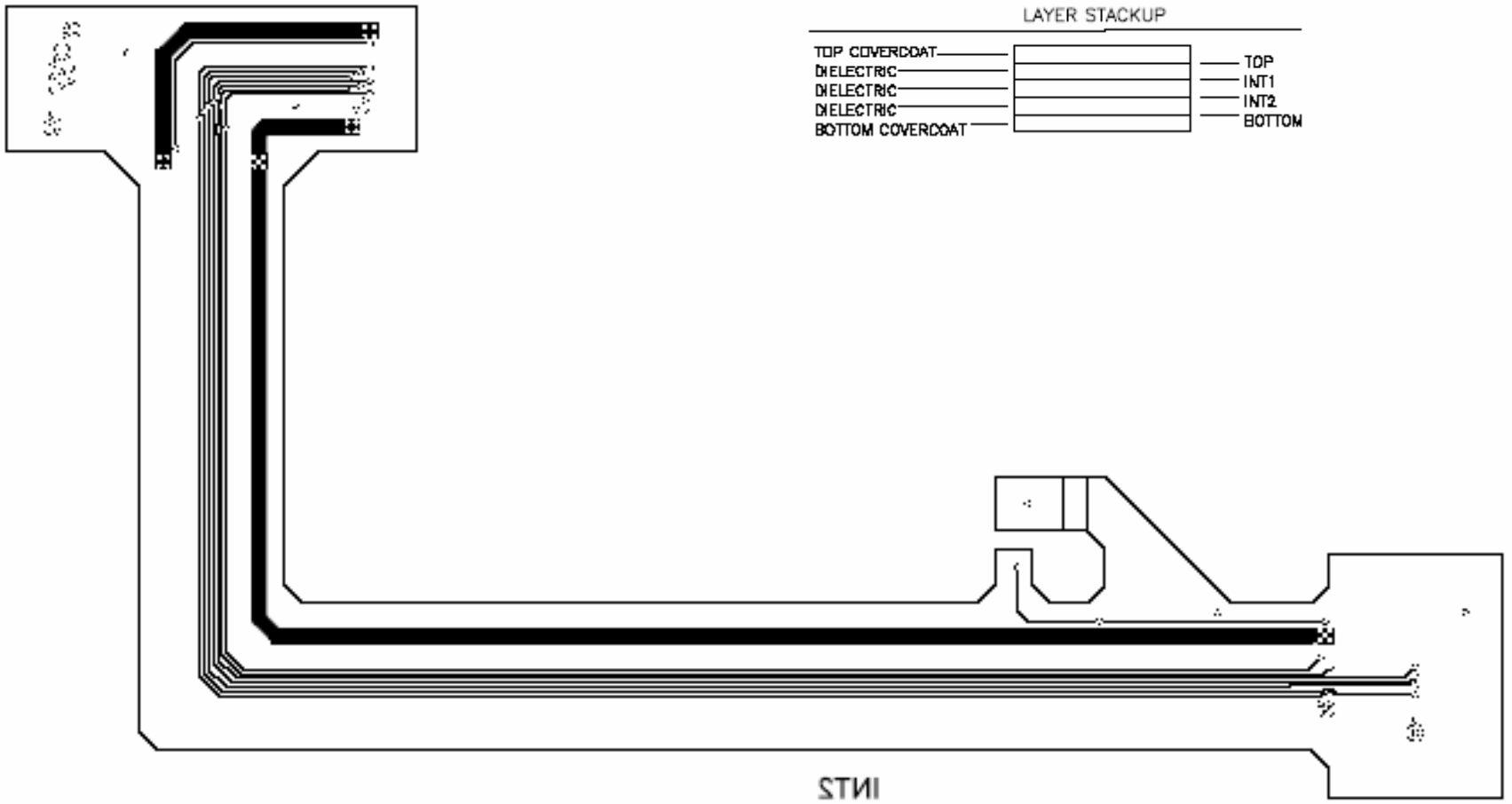
# Layers, Internal 1 Layer

- Analog and Digital Power
- Vref, Digital Control and Readout
- High Voltage Bias



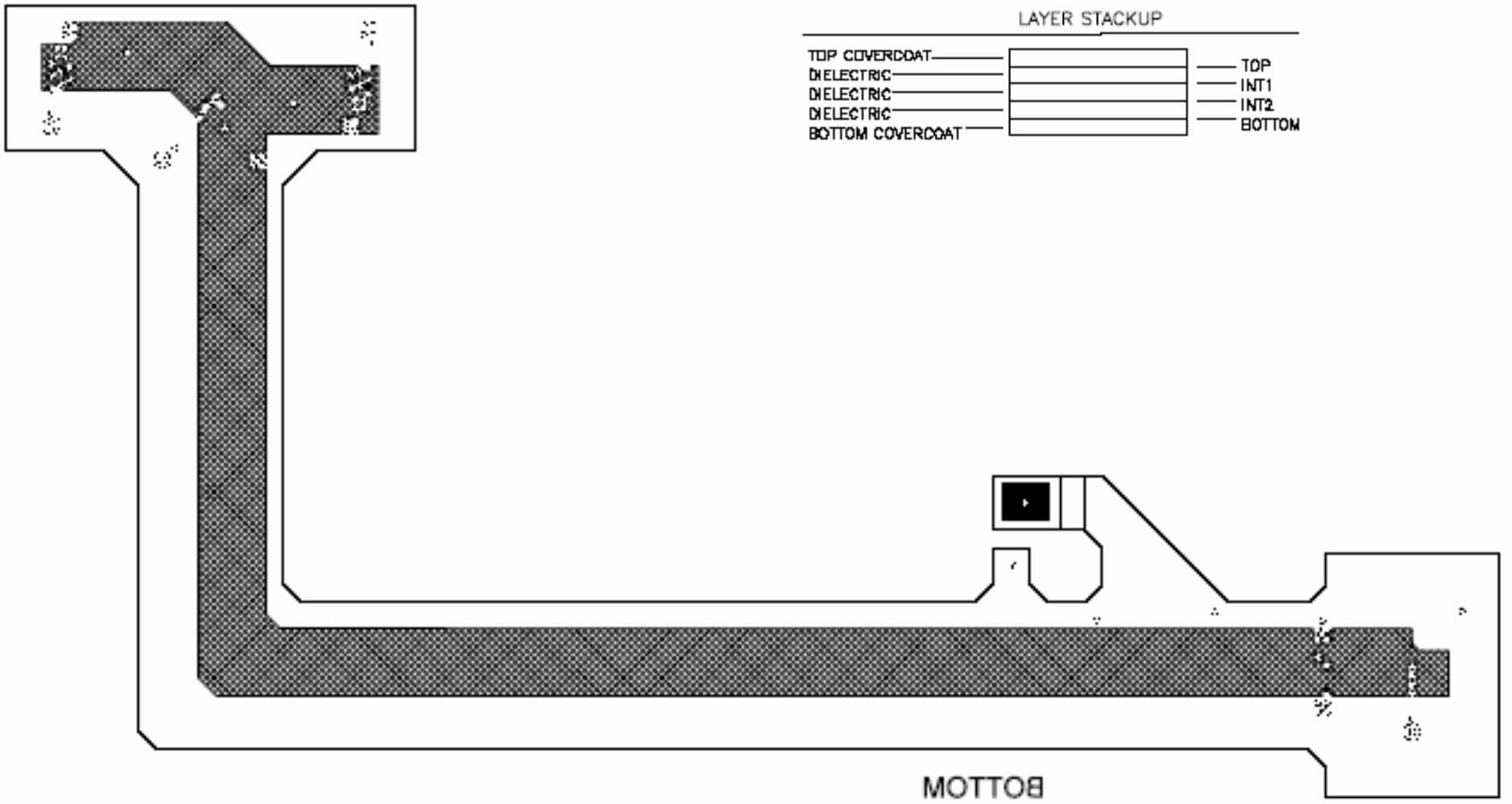
# Layers, Internal 2 Layer

- Analog and Digital Power
- Traces for Digital Control and Readout
- Bias Return



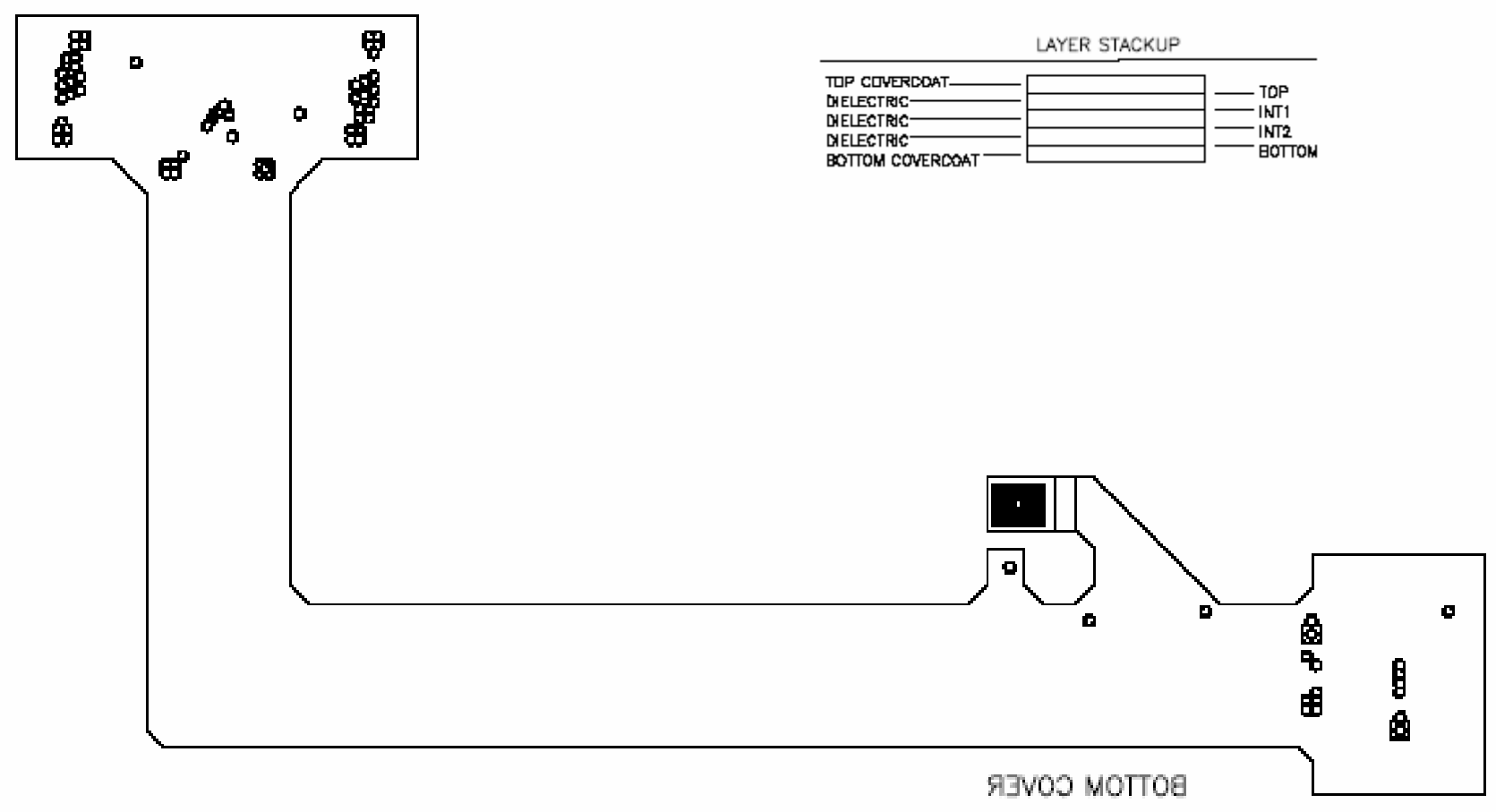
# Layers, Bottom Layer

- Digital Return



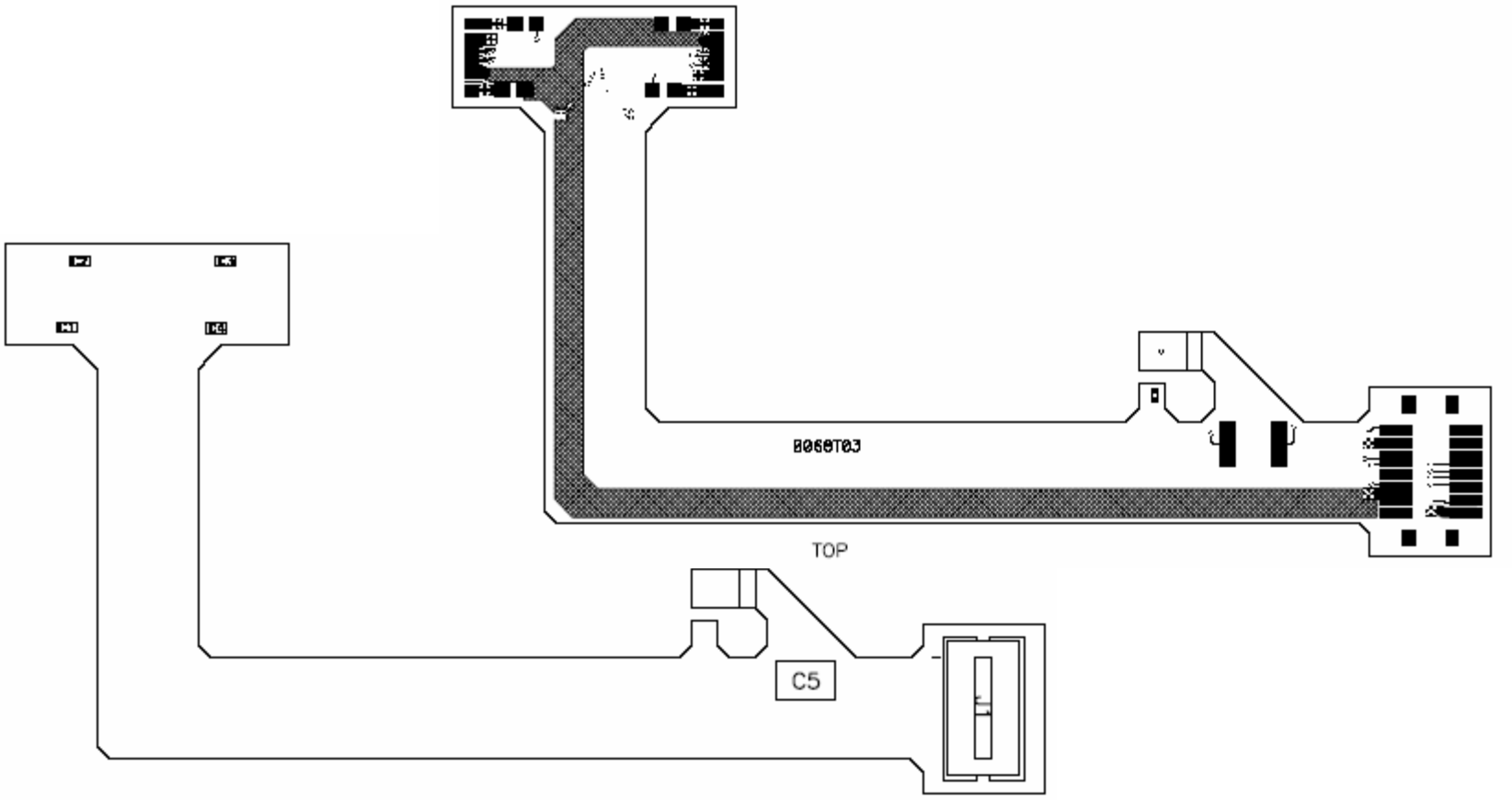
# Layers, Bottom Cover

- Need to cover all plated thru vias with a layer of photoimageable covercoat 38 μm thick on the surface which contacts the sensor, to avoid scratches or shorts.



# Power Filtering

- Filtering of KPIX power and HV Bias on the Pigtail Cable
- C1-C4 are standard 1206 sized surface mount, C5 is 1812 sized HV (ex, AVX or Johanson MLCC 0.1μF 500V , height ~ 3mm)

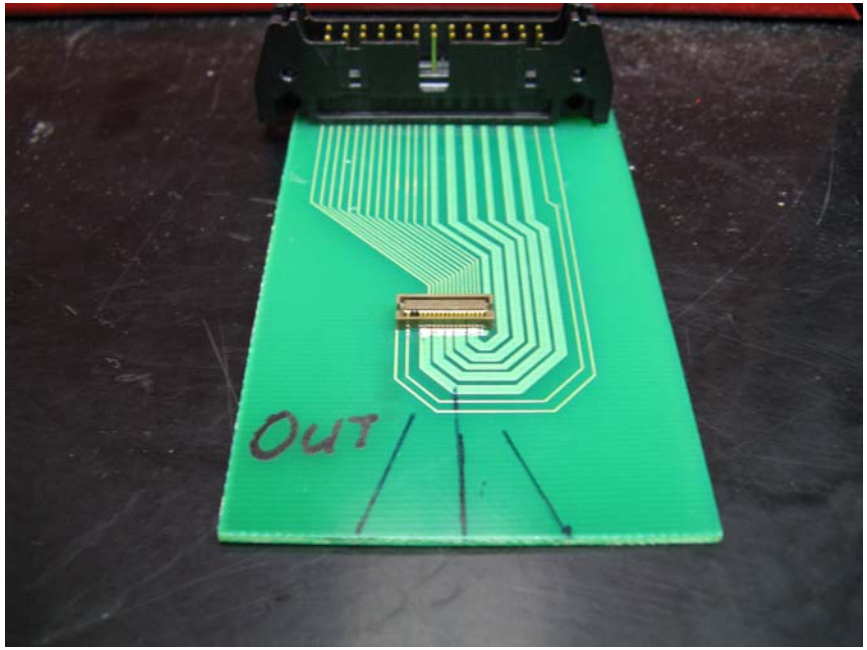


# Signals, Pickup and Crosstalk

- Digital signals are LVDS (low voltage differential signaling)
- Pickup and crosstalk must be minimized
- LVDS: balanced differential lines have tightly coupled polar opposite signals which reduce EMI pickup and crosstalk.
- LVDS: signal rise and fall times are very fast, < 1 ns typical so one must consider the possibility of reflections depending on the length of the Extension cable.
- We may need to consider options for terminating the LVDS lines

# Extension Cable

- The Extension can be up to 2 m in length.
- As soon as Pigtail cable is verified the Extension cable design should be straightforward.
- Pigtail cable alone can be used for sensor testing if we make an adapter (connector saver) to interface to a standard connector
- This way we don’t have to wait for Extension cable to begin testing.



# Summary

- The Pigtail cable design is in process of being updated with the following:
  - Add option to jumper connect Analog and Digital Grounds
  - Have gold plating only on wirebond pads (and not on component or connector pads)
  - Add an additional High Voltage filter cap from HV Bias to AGND
  - No longer bus the digital Control & Readout lines to the two readout chips, now we have 8 separate lines to each KPIX chip.
  - Evaluate Molex connector since ELCO is difficult to get.
- Need a final design review before fabricating prototypes.