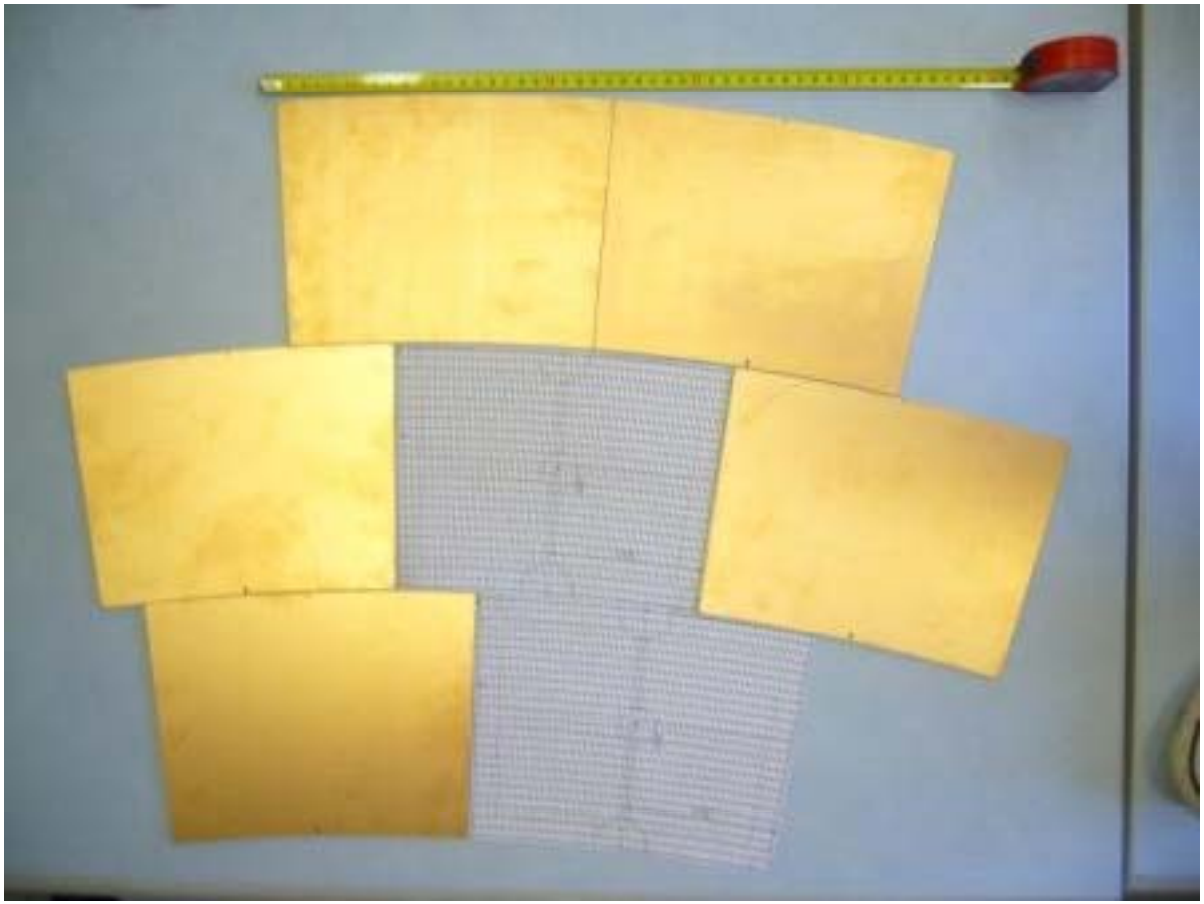
Micromegas panels

Status and plans

D. Attié, P. Colas, X. Coppolani, M. Dixit,
M. Riallot, F. Sénée, S. Turnbull

News since Zeuthen

- 4 days of discussion/plans with M. Dixit et al., in Saclay, CERN and Neuchatel
  - Go for N7000 PCBs (250 deg.)?
- 5 dummy panels back from PCB maker
  - For metrology, gluing tests, resistive layer test
- Connectors ordered to ERNI company
- Lots of progress with LP trigger, see meeting tomorrow. Visit at DESY to plan for installation.

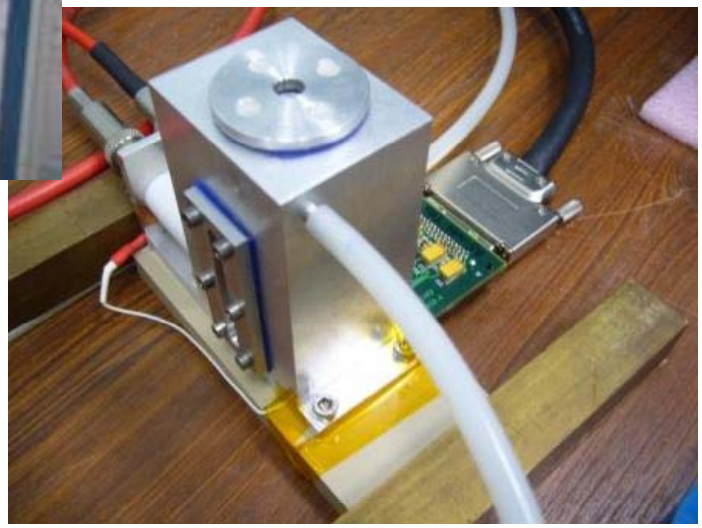


Studies with the 1-chip SiTPC ongoing in the new lab at Saclay

(D. Attié et al.)

Second 1-chip detector under construction.

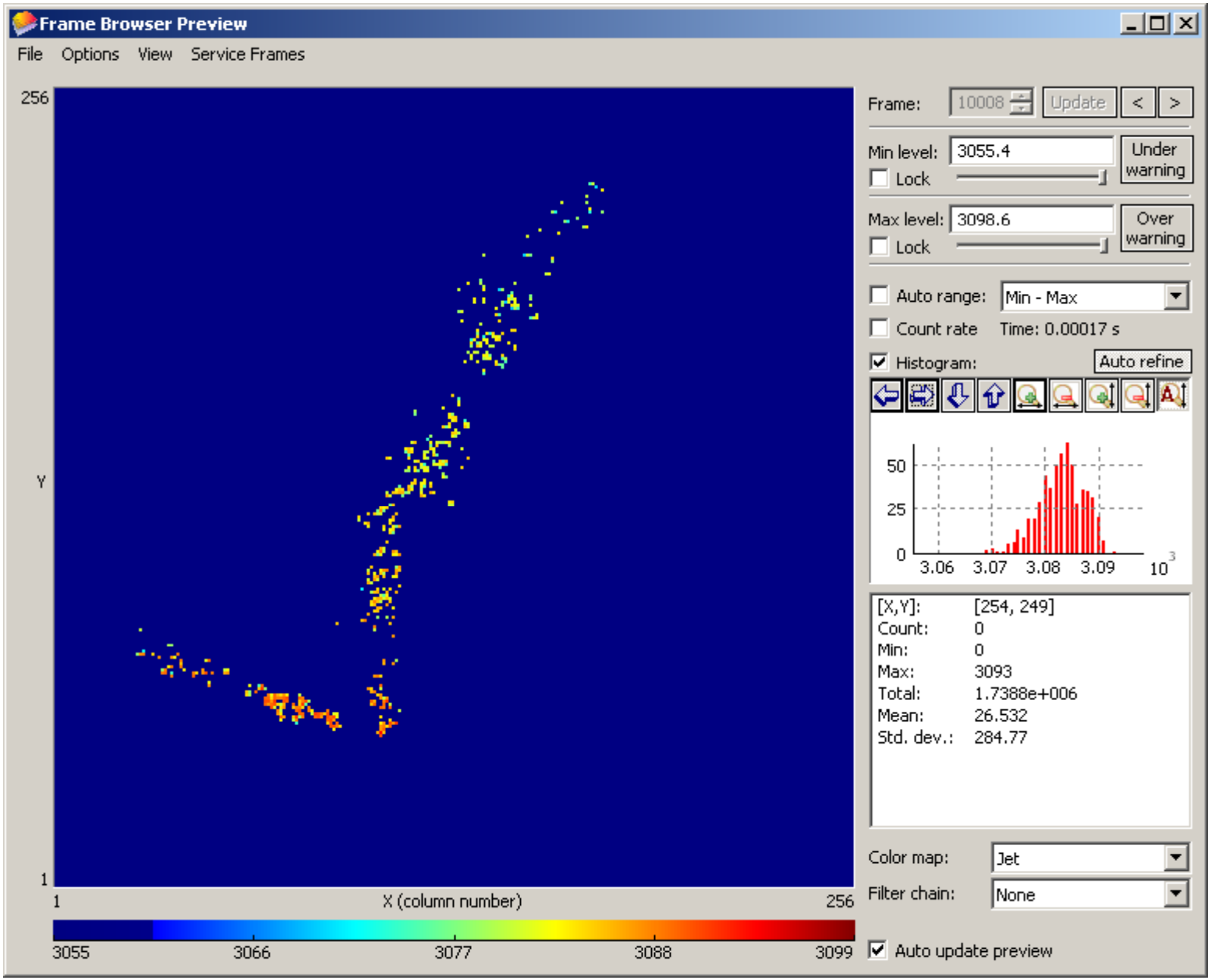
USB readout upgraded to accept TimePix



Multichip board being routed at Saclay (ready end of next week?)

^{90}Sr source

- Date: 29/01/2008
- Gas mixture: Argon/Isobutane 95:5
- V_{mesh} = 350 V
- E_{drift} ~ 500 V/cm
- Shutter time: 176 µs
- TimePix clock: 67.1 MHz
- TimePix chip: I07 - W0014 + 20 µm SiProt
- Filter to save evts
- DATA ANALYSIS in progress (also 130000 evts of 55Fe on disk)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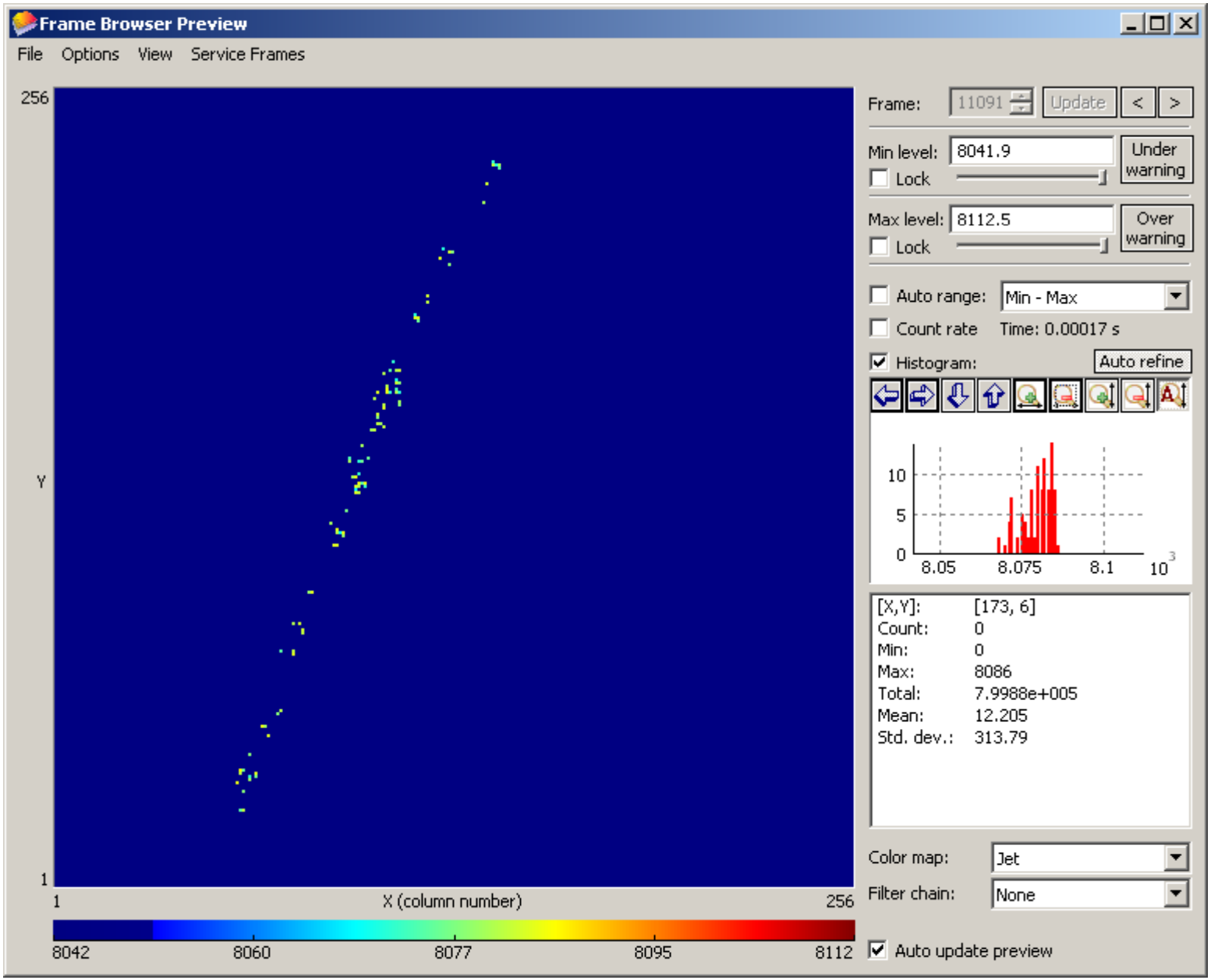
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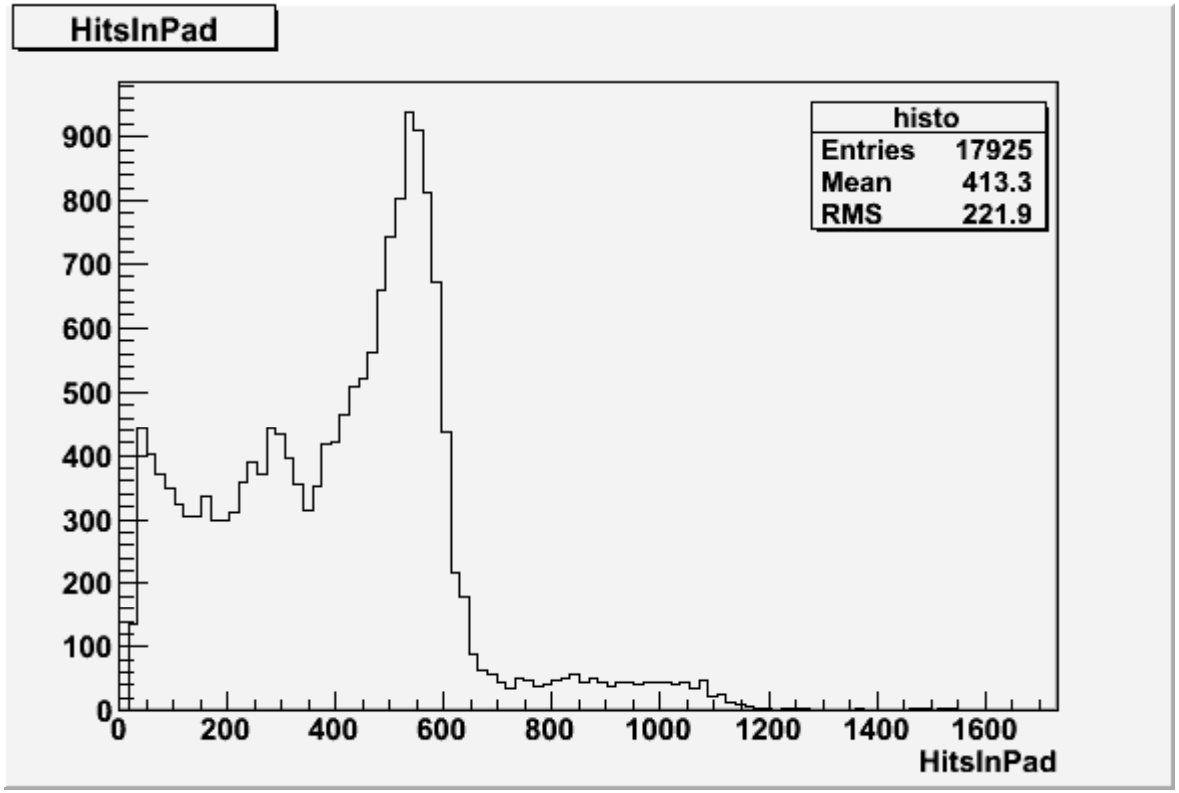


RAW DATA, 55Fe : number of pixels on (1 electron ~ 3 pixels)

Escape line visible

COSMIC-RAY TRIGGER

Mechanics in progress. Orders being passed.

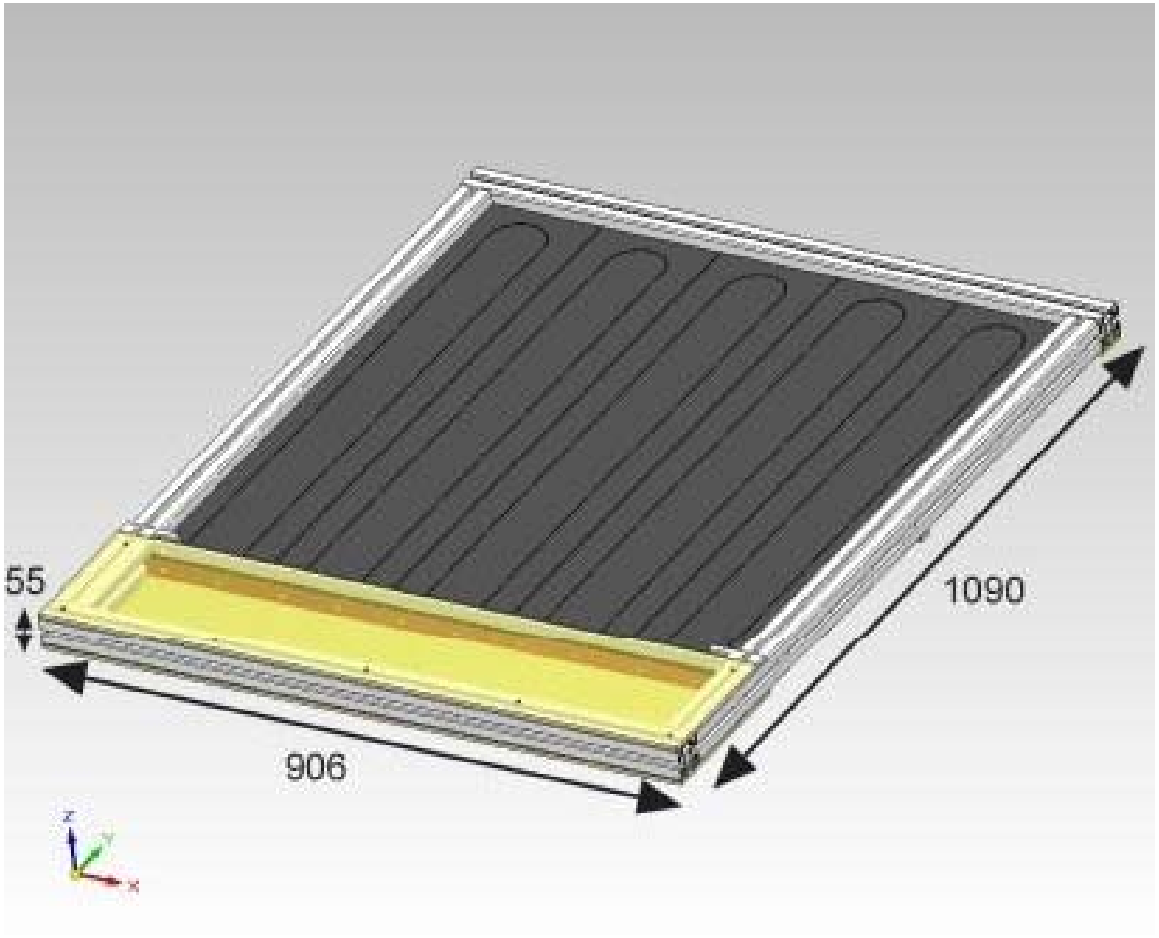
(F. Senée, M. Riallot)

Significant progress on MPPC operation and characterization.

(T. Chaminade, M. Karolak)

Slabs with U-shape fibers ready. Shipment from Moscow being prepared. Ready for wrapping at Saclay

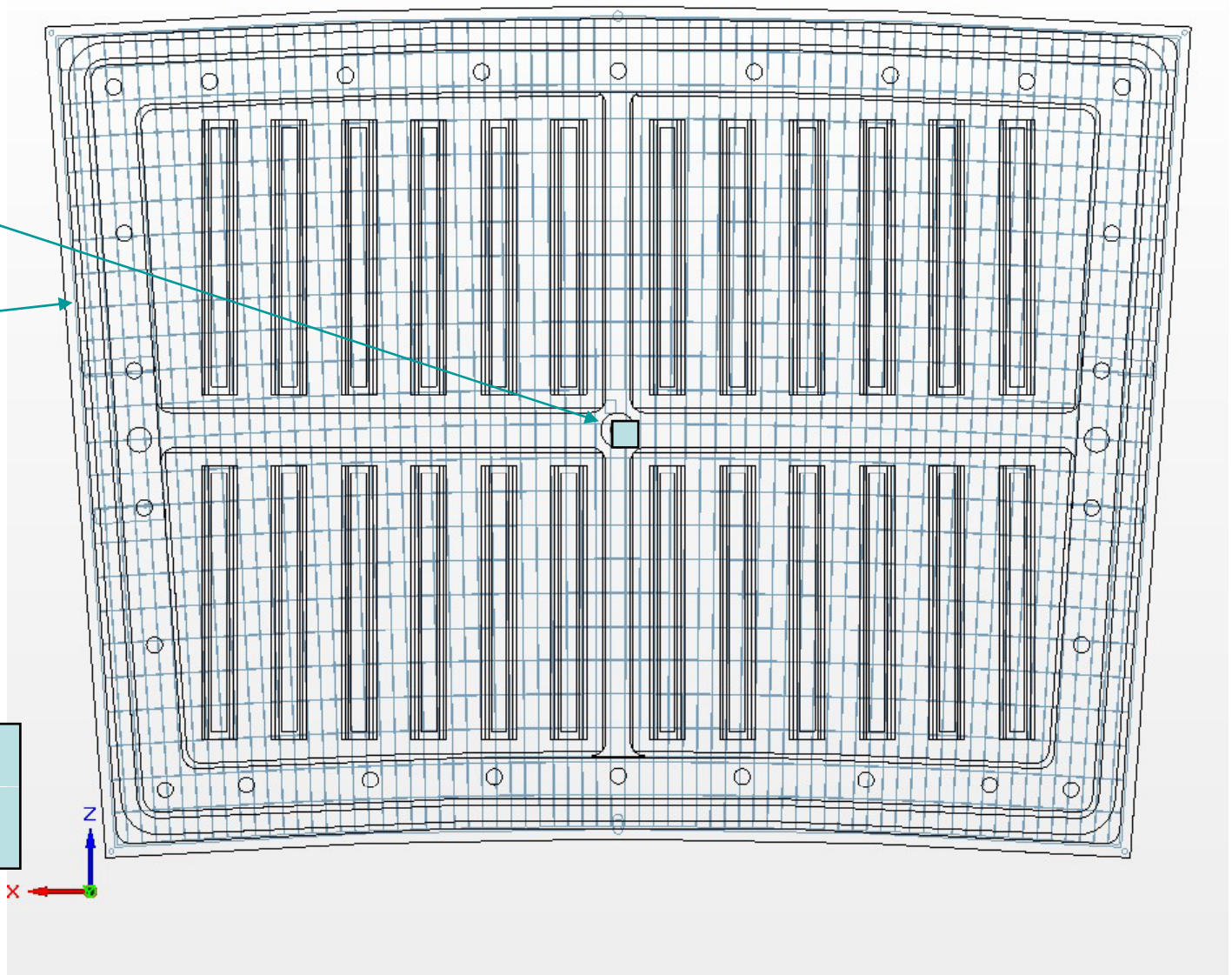
Meeting with Klaus Dehmelt et al. at DESY, for planning for installation.

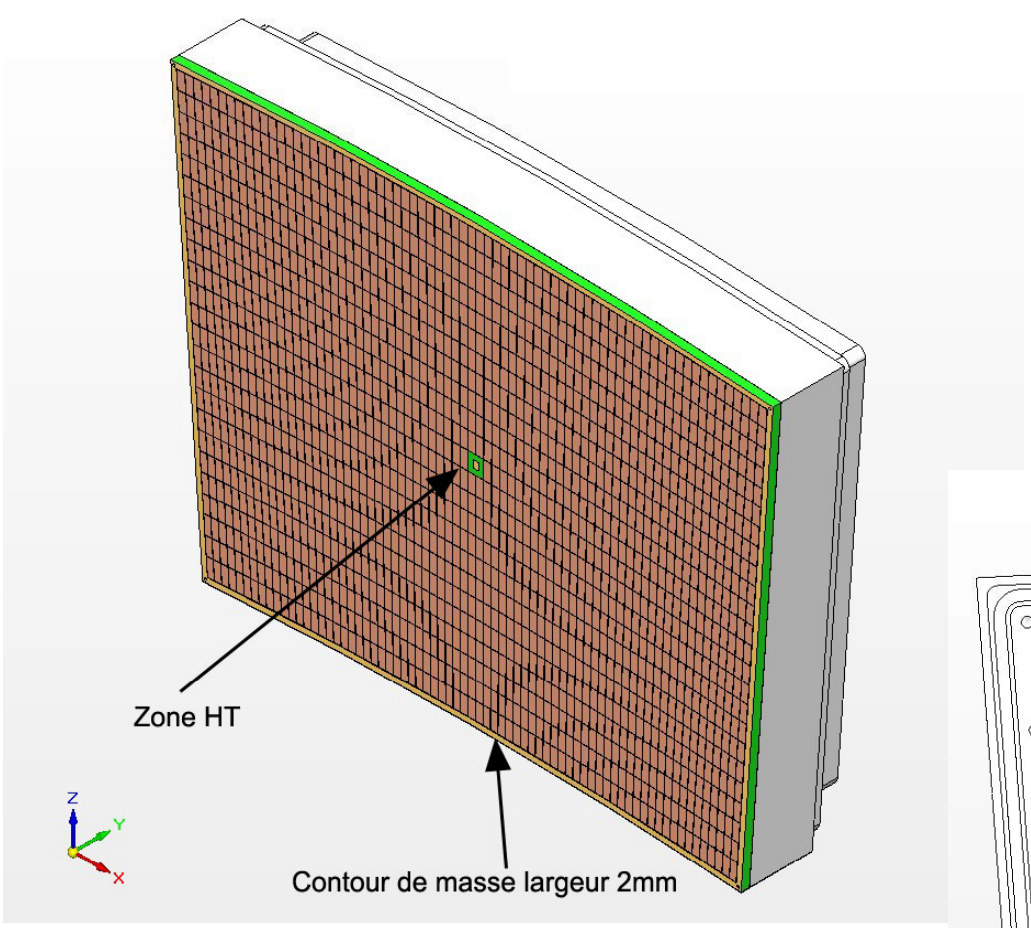


Plan is to perform analogic sum of signals of the two ends of each fiber.

MICROMEGAS + RESIST. FOIL PANEL

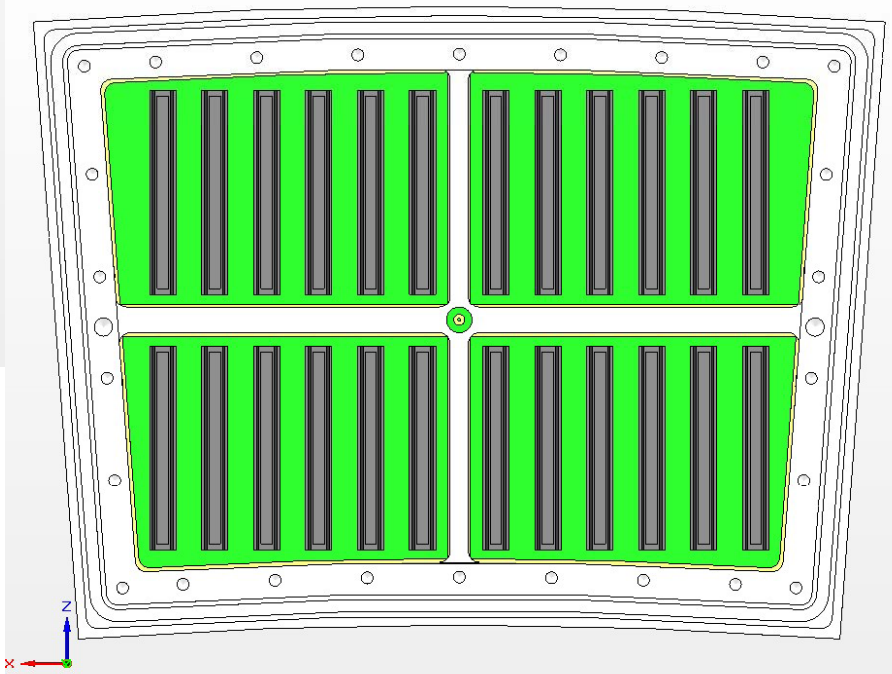
24 rows x 72 pads





Detector side

connector side



Resistive coating

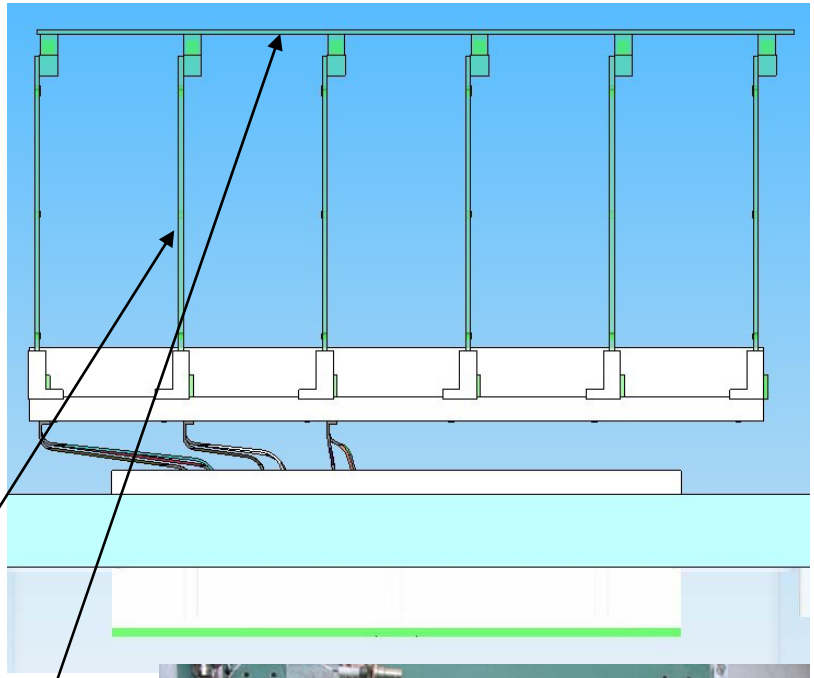
- 3 techniques
  - Pursue resistive foil with a solid thermic glue foil (satisfactory, but difficult to couple with bulk technique)
  - Try resistive ink serigraphy (Rui de Oliveira, CERN)
  - Try photovoltaic techniques with vapour deposited thin layers (Neuchatel)
- Find the best way to ground the resistive coating on the panel perimeter, when needed
- This is a R&D, do not expect it works perfectly from first try.

Connection to electronics

For the start: use T2K config. of the readout (6 cards, with 4 80-pin-connectors each), read out by 1 mezzanine card –> single output optical fiber. Adapt with flat cables.

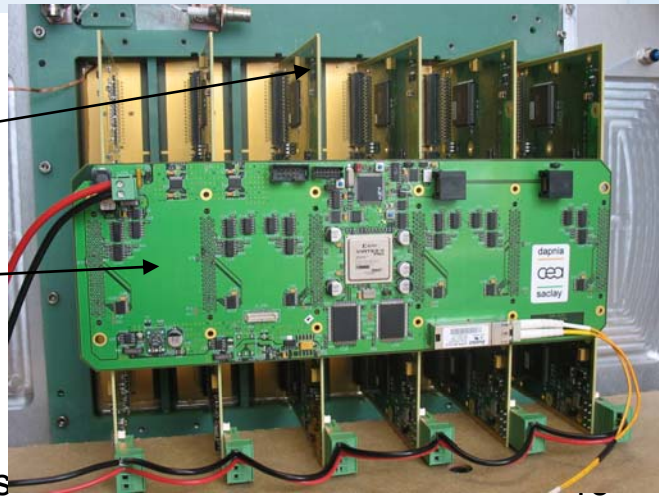
(next step: make 12 2-connector cards + new mezzanine)

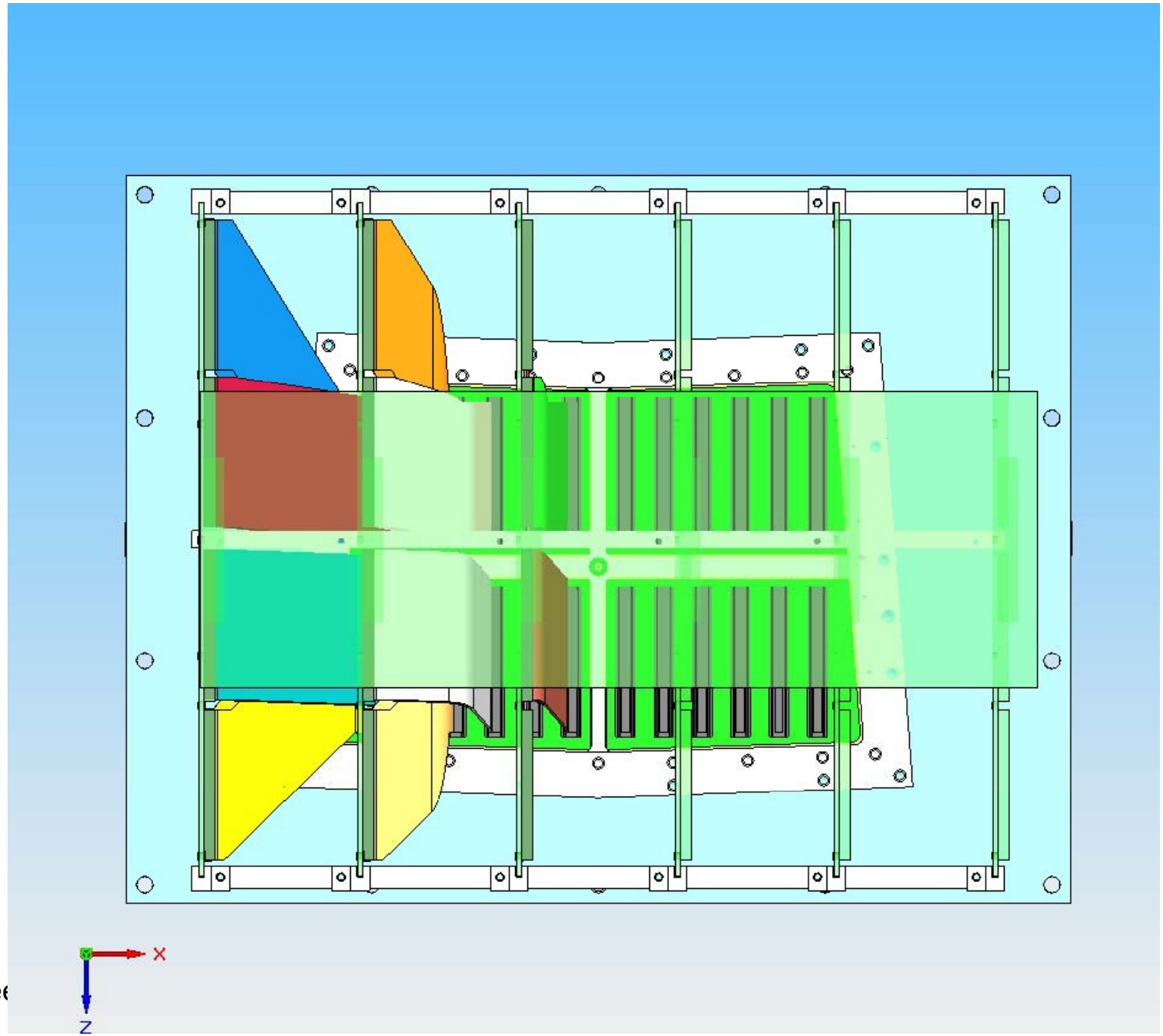
For the 10000 channels (end 2009) integrate 900 channels at a time and replace all front-end by 2 mezzanines with special connectors



Front-end cards

Front-end mezzanine

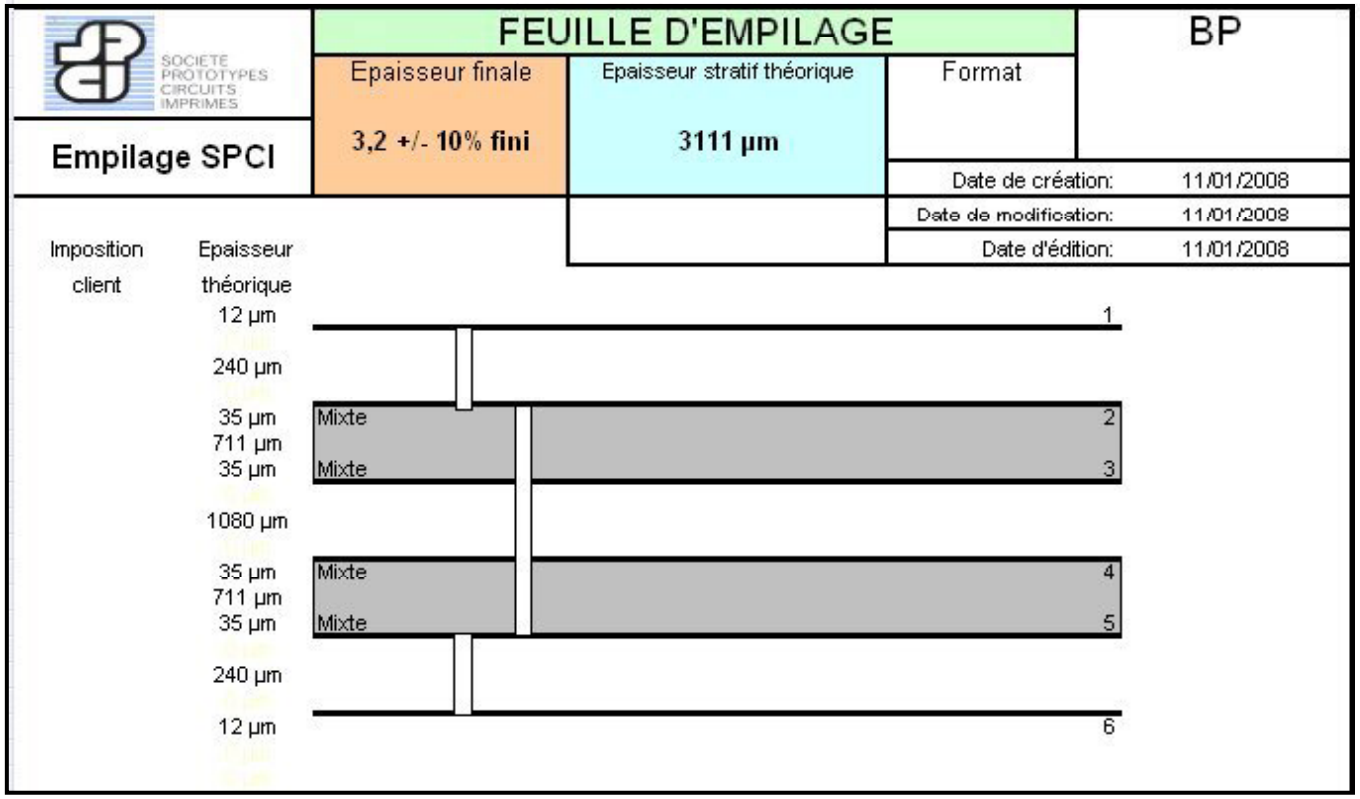




Phone mee

PCB structure

- 6 layers
- Details of vias, etc, decided in a meeting with CIRE on December 15
- several plain anode (dummy) modules ordered for tests (mechanics, bulk manufacturing, glueing)



Readiness of electronics

- FECs (X. de la Broise, A. Le Cogüe)
  - Feb. 21
- FEM (D. Calvet)
  - Week 4
- Others
  - Optical fibre
  - Power supply
  - DAQ kit
- See with Stephan Aune

Software

- DAQ software from T2K.
- On-line display
  - Geometry file (pad number, x1…4,y1…4)
  - Pad to channel relation
- Analysis programs
  - Adapt T2K and FTPC analysis programs

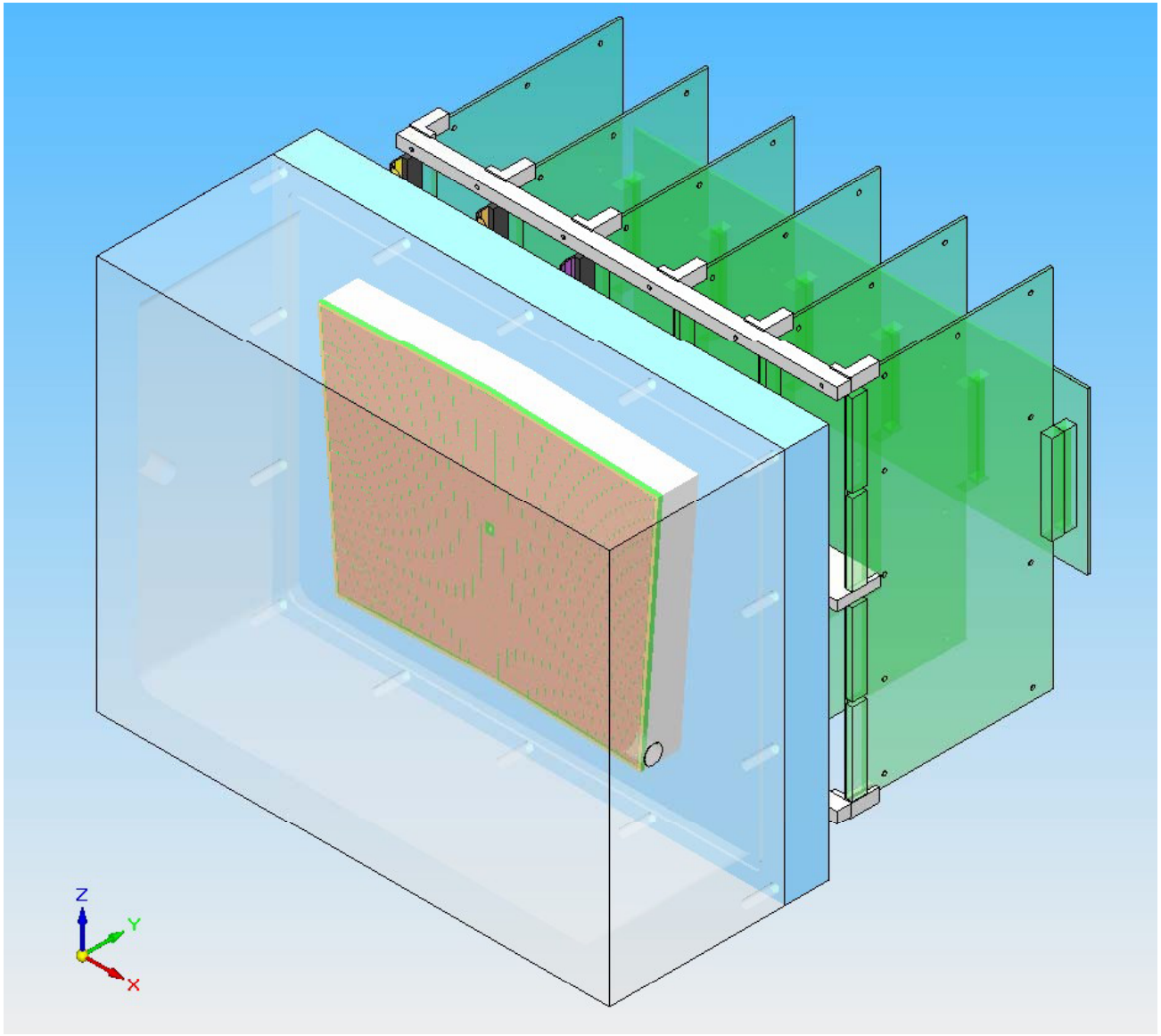
Routing

- 2 routings in Progress (at Saclay and at CERN). Allows optimization of cross-talk, noise minimization, etc…
- CERN routing submitted before Christmas.
- Saclay routing to be starting January 27

Schedule

- Tests of the various methods for resistive layers and bulk fabrication : in progress with plain copper anodes. 5 ‘dummy’ panels ready.
- Routings ready by end of February
- Submit PCB and get them back by March 20
- First detector ready by mid-April.
- Source tests, then cosmic tests, then beam tests this summer

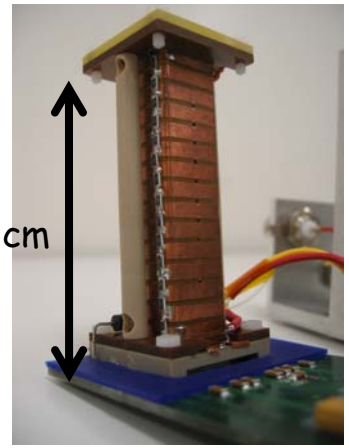
Test box

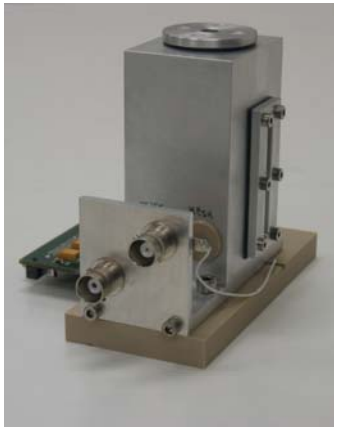


Single-chip SiTPC ‘diagnostic detector’

D. Attié, P.C,

J. Derré, M. Riallot

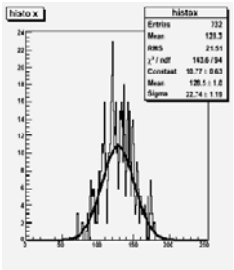


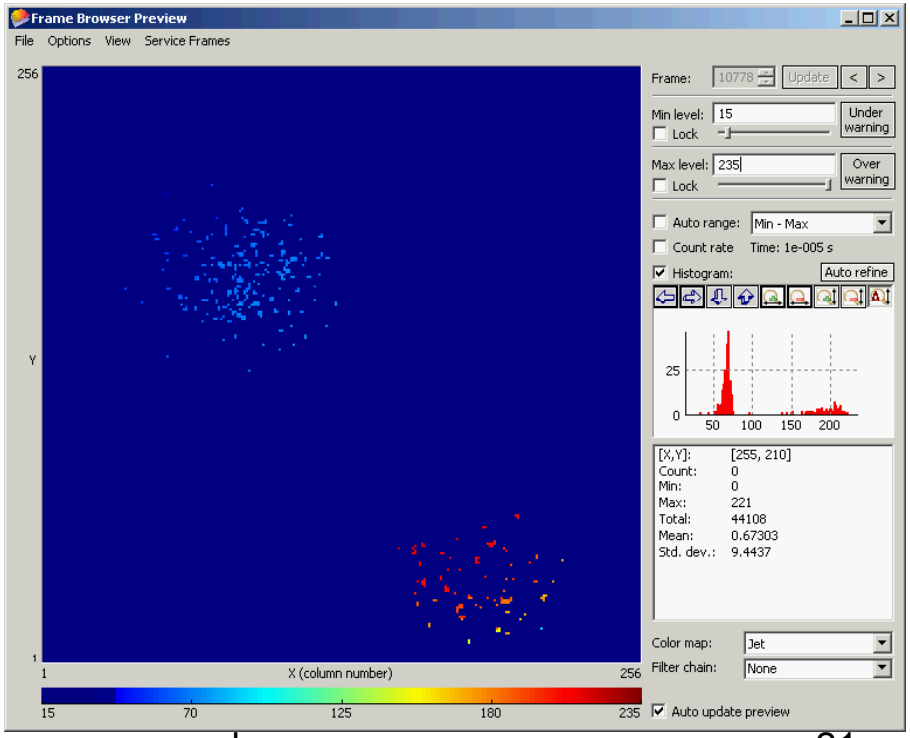


Deliverable for EUDET end 2007, Saclay responsibility.
Equipped with a 20 micron SiProt resistive layer

In operation since mid-October, analysis started

On av. 3-pad clusters as expected due to resist. coating



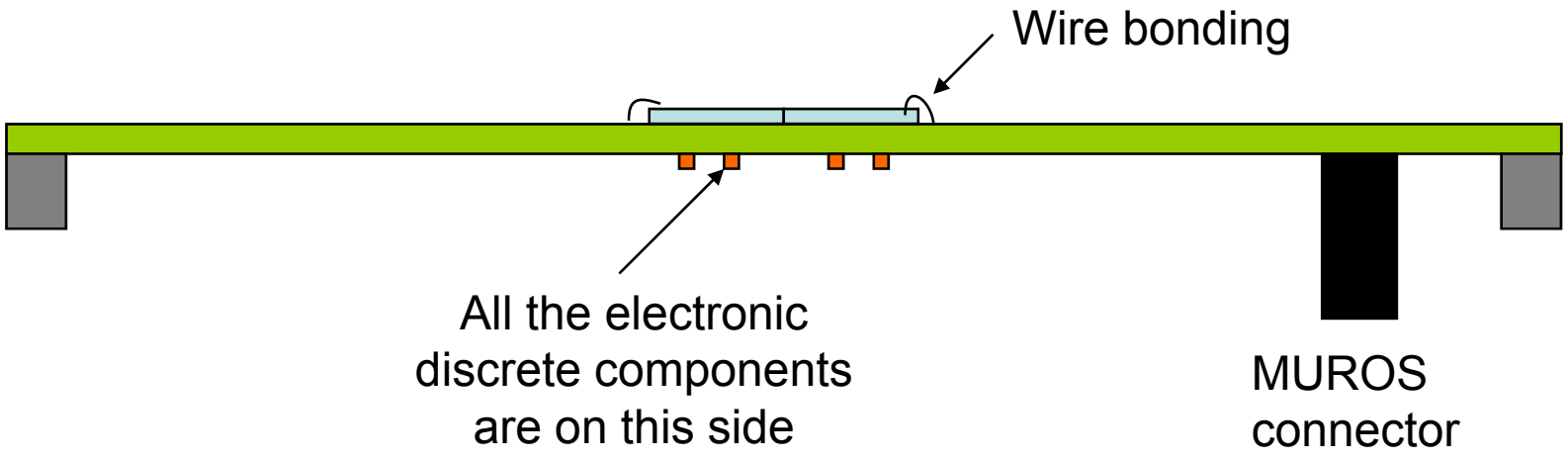


Multi-chip SiTPC panel

Deliverable for EUDET (‘endplate infrastructure’) end 2007,
Saclay responsibility. Routing in progress, submission in 10 days

Need more chips to test it

End 2008: working multichip endplate (InGrid-equipped)



8-TimePix panel (1 MUROS)