ECAL SLAB Interconnect – Why Multi-Rows?

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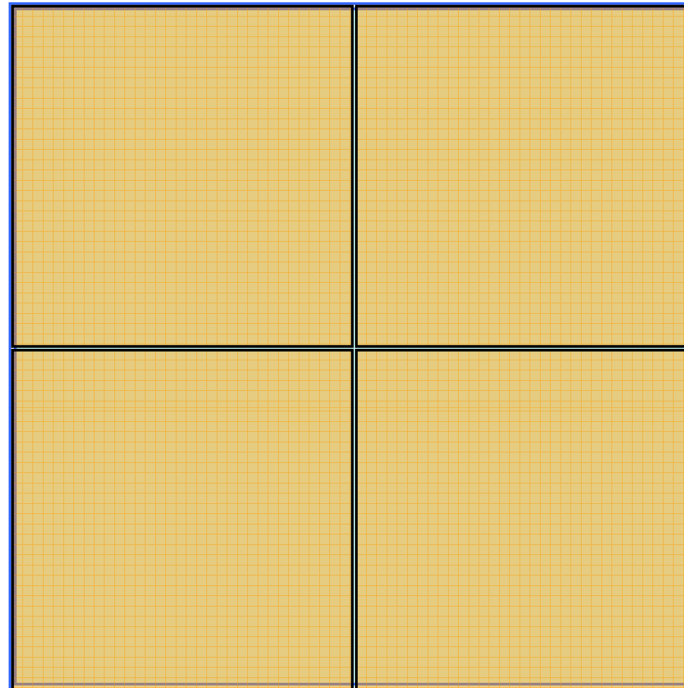
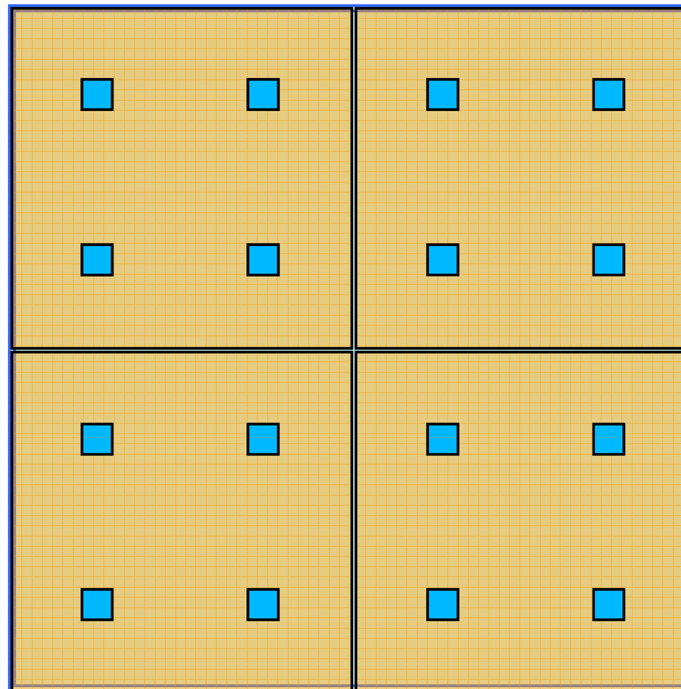
Assuming 9x9 cm Silicon Wafers:

4 wafers on an
18x18cm ASU



Where the VFEs go: Assume 81 channel VFEs:



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How to read them out – **single path** or in **4 rows**

Single path

4 rows

Single path	4 rows
Per ASU: L ~ 720mm, C ~ 72pF	Per ASU: L ~ 180mm, C ~ 18pF
Per Slab of 9 ASUs: L ~ 6.5m, C ~ 650pF	Per Slab of 9 ASUs: L ~ 1.6m, C ~ 160pF

Do these look **BIG ??** - we'll look at that later

How much difference will this make?

Read-Out Rates and Power

# Rows	R-O Rate/Row (Mb/s)	R-O Power/Row (mW)	R-O Power Total (mW)	Trace Length (m)
1	5.4	4.4	4.4	6.5
4	1.4	0.3	1.1	1.6

The power savings may not be important compared to the power budget of a complete Slab

But achieving data rates of several Mbits/sec over complex traces of several metres length will be **difficult** ☹ or **impossible** ☹☹☹

The existing plan is to use conductive adhesive to make these interconnections.

… but:

- power pads need to be large – say 3 pads of 1cm width
- only 3 signal pads per cm
  - gives 45 pads for signals – this is barely enough for a 2 row scheme – and there are good reasons to favour a 4 row solution
- will large pads upset signal transmission properties?
- will the connections deteriorate with time?
- will the mechanical joint be good enough?
- if the joint is not to be mechanical, is the rigidity a problem?
- the lap joint with clean pads on the step will make PCB more expensive (unless already needed on ASU)
- re-work will be difficult

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We have been looking at alternative forms of interconnect.
The most interesting is the use of “Bridge” component.
This could be a short Kapton-backed Flat Flexible Cable (FFC-Bridge), or a short thin PCB-Bridge.

The Bridge would be soldered onto pads on the ASU (/DIF/Term) PCB

ECAL SLAB Interconnect: Bridge use

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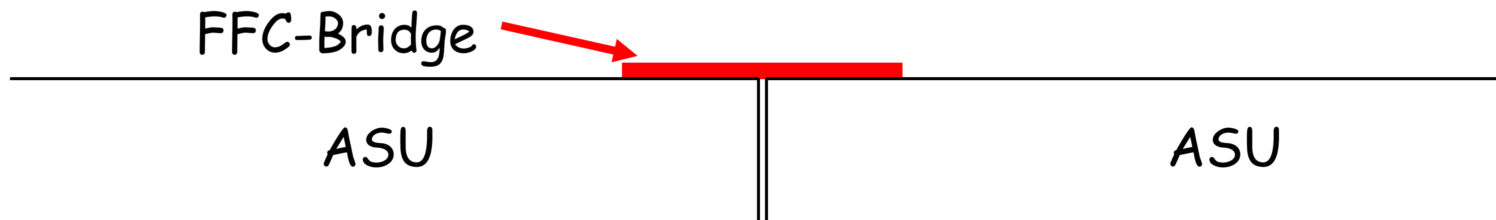
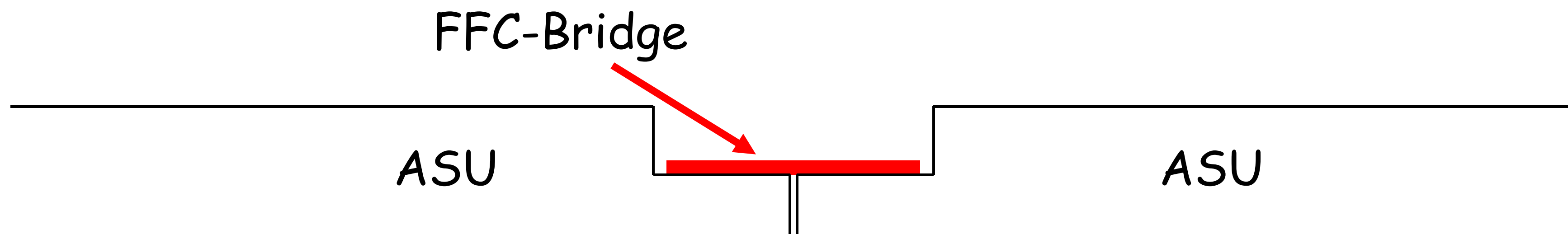
If the overall thickness of the ASU were reduced by ~50um, connections could be on the top of the ASU – avoiding the need for a step at the edge



Alternatively, the step can be kept, and the Bridge will add no extra height



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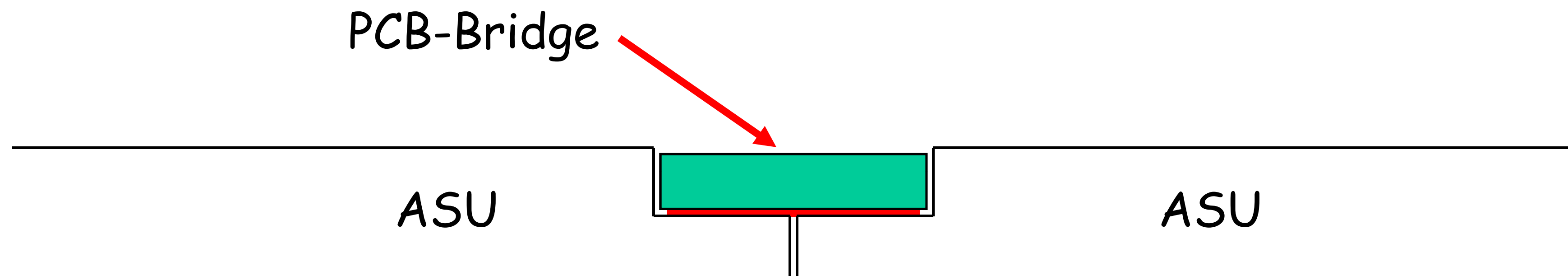
The PCB-Bridge option also provides a mechanical connection.



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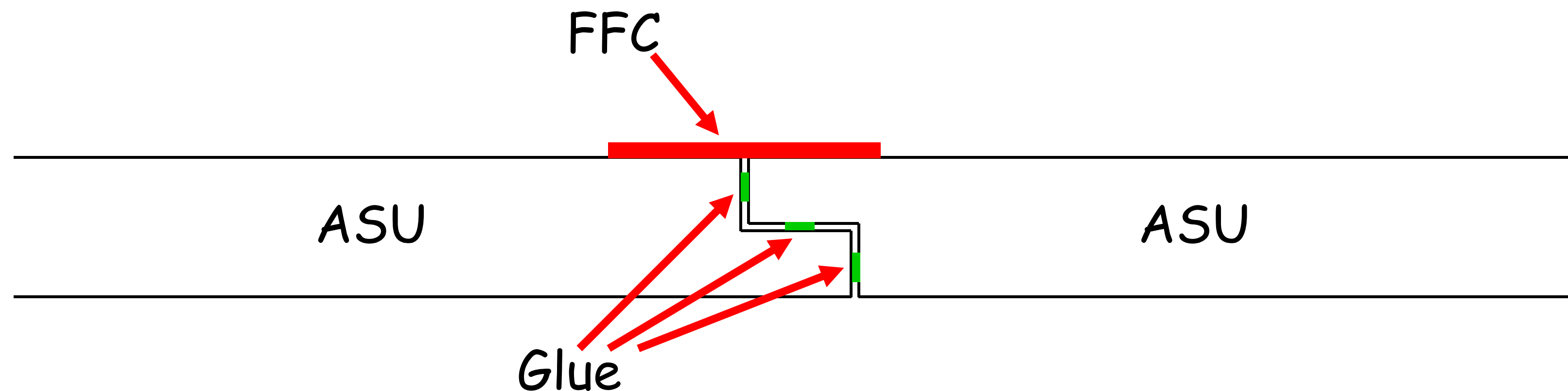
A glued, stepped joint could also be used ….



Good mechanical joint
… but hard to rework ☹☹

ECAL SLAB Interconnect - using Bridges

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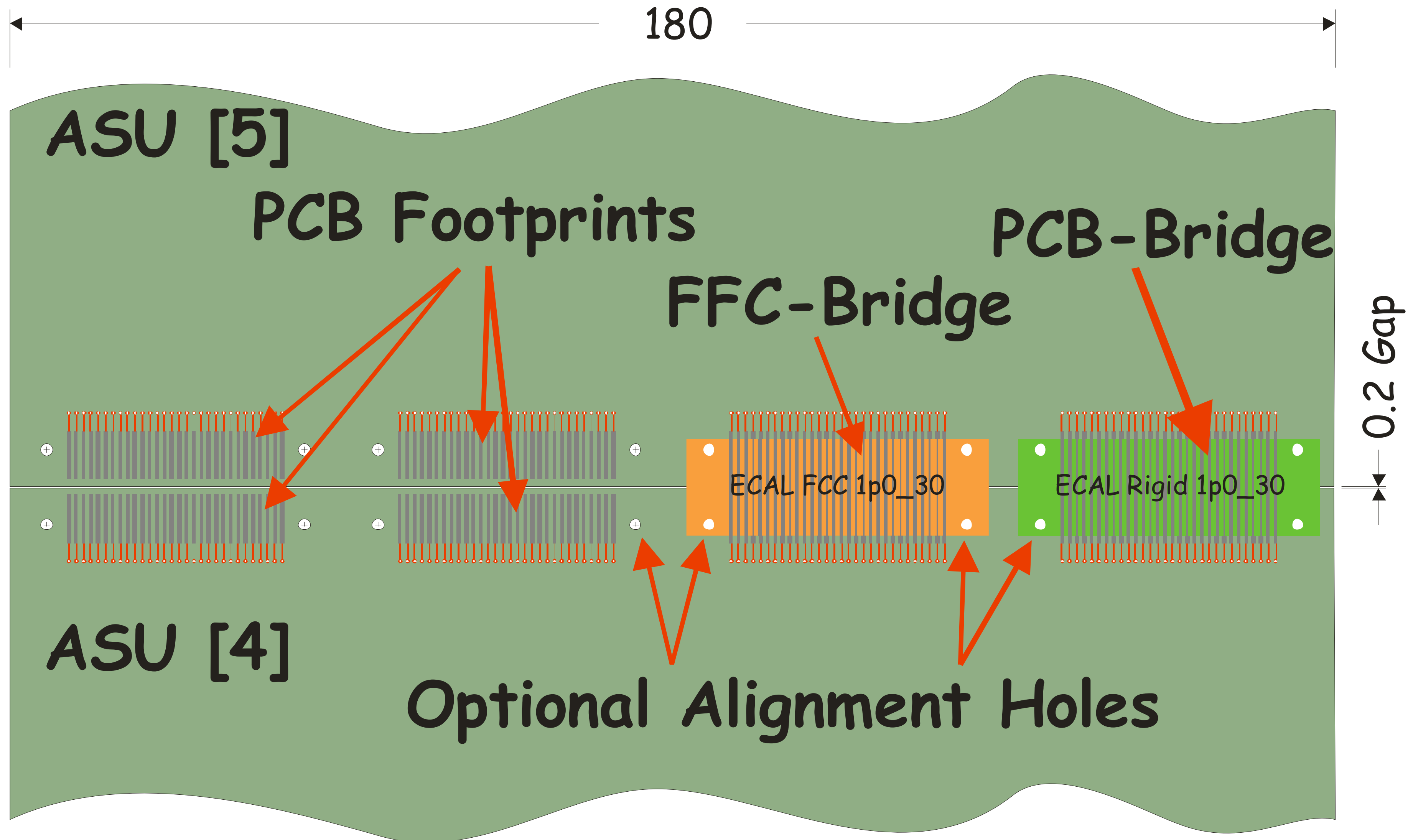

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ECAL SLAB Interconnect - ASU/PCB-Bridge

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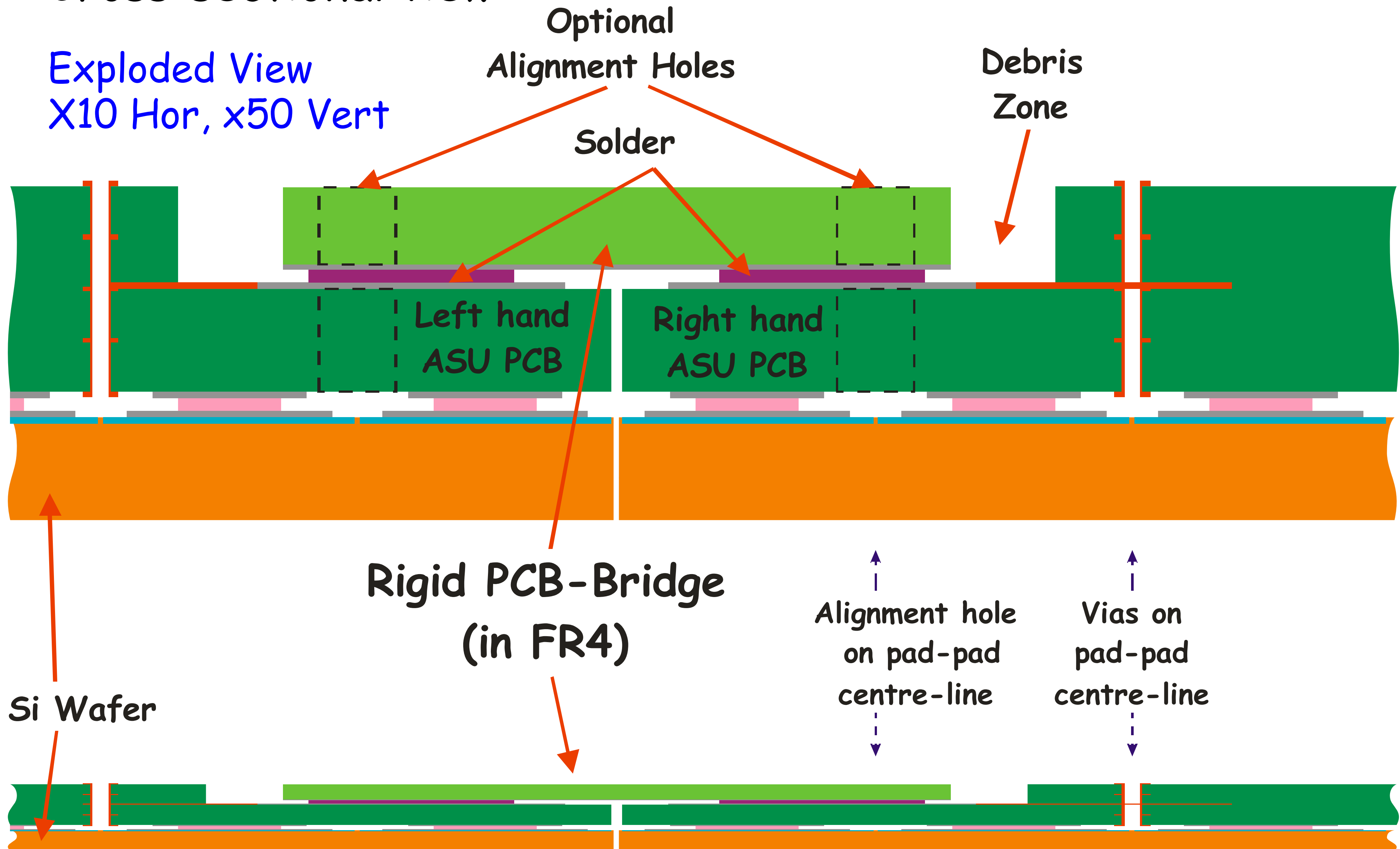
Cross-sectional view



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ECAL SLAB Interconnect: PCB-Bridge Detail

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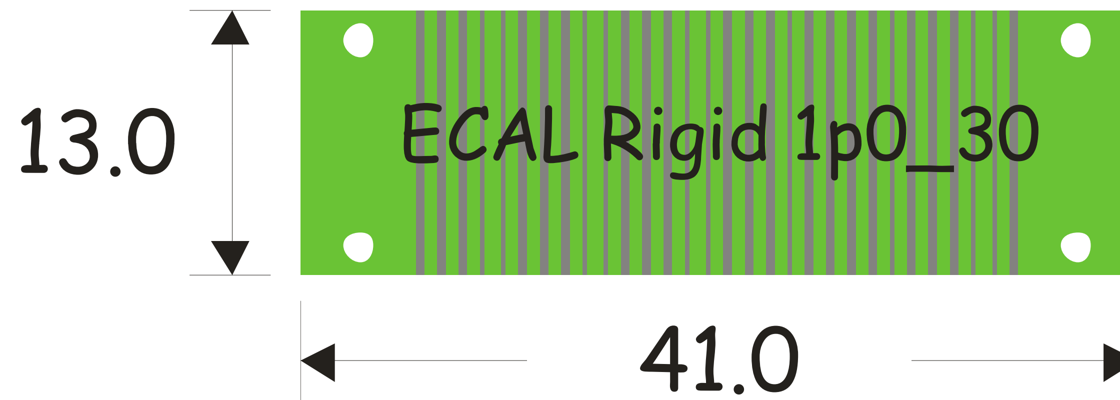
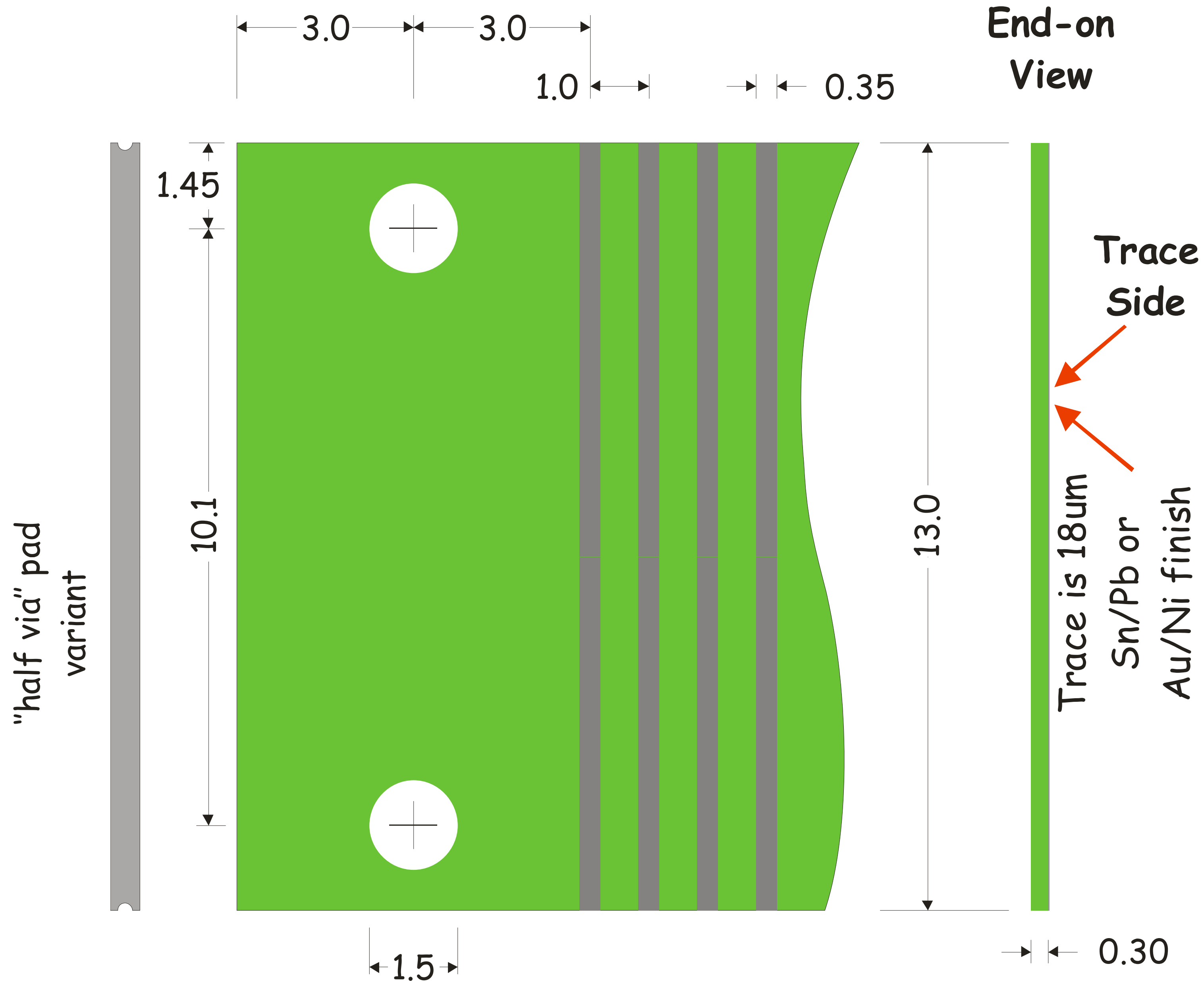


Rigid Bridge Notes

- Thickness ideally 0.4mm; thinner probably OK
- Traces should extend to edge of board for joint visibility
- Will want variants with different pad widths
- Would also like a version to test "half via" at end of traces: this is a full via cut in half by the edge routing
- Multiple copies of the different versions would be incorporated in one design

ECAL SLAB Interconnect: PCB-Bridge Detail



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SLAB Interconnect - Bridge Advantages

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- Provides copious connections (4 x 30 fit)
  - plenty for Power Planes
  - would allow 4 or more row VFE connections
- Solder joints well proven electrically
- Signal transmission likely to be less compromised
- Rework possible

- FFC makes mechanical joint independent
- PCB-Bridge gives reasonable mechanical joint too
- Could still use glued lap joint, but using stronger and more reliable non-conductive adhesives
- Other mechanical joints possible

How to solder:

- Hot-Bar Soldering (Thermode) is usual technique
- Laser Soldering
- IR soldering

Force may be needed:

- Clearly a major issue when Si wafers on ASUs
  - Hot-Bar soldering typically uses ~50N (10 lbf)
  - Laser and IR need far less force – if any
- Vacuum chuck is a possible solution – but designing one to fit in Slab assembly procedure will not be easy

Laser Soldering not widely used, and will need expensive equipment

So … concentrate on IR at this stage ??

SLAB Interconnect - Panel of PCB-Bridges

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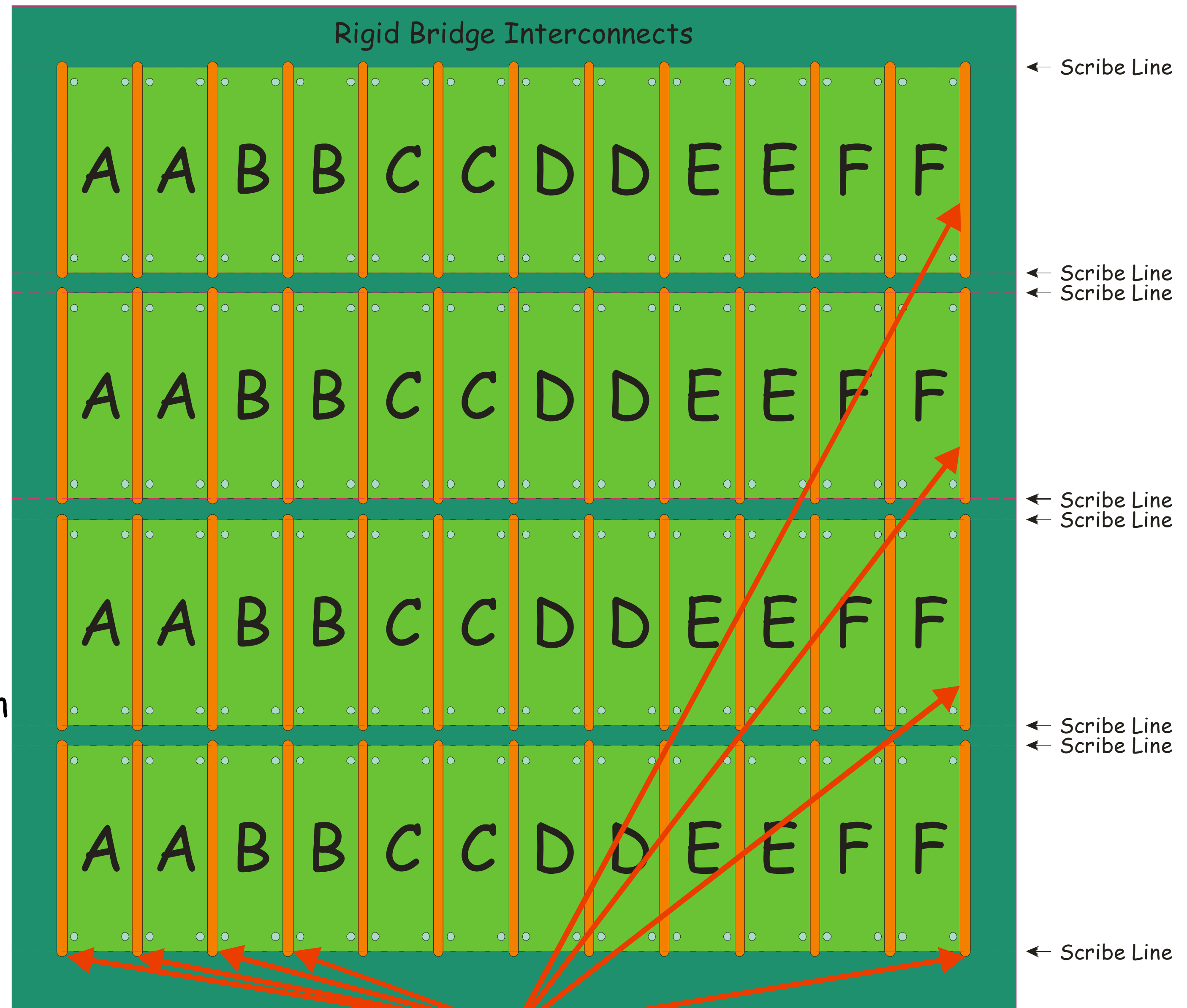
1) The panel has 6 variants (A-F) to explore the options
2) They are in columns of 4 of the same variety
3) The horizontal scribe lines allow the bridges within a vertical column to be separated: or they can be kept as a group of 4
4) Some variants are double-sided (pads top and bottom)
5) Some also have vias to improve heat conduction
6) To provide a joint with a more visible fillet of solder, one variant has plated thru vias on the edge: the slots should slice through these to give a plated half-cylinder



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ECAL SLAB Interconnect - Bridge Test PCB

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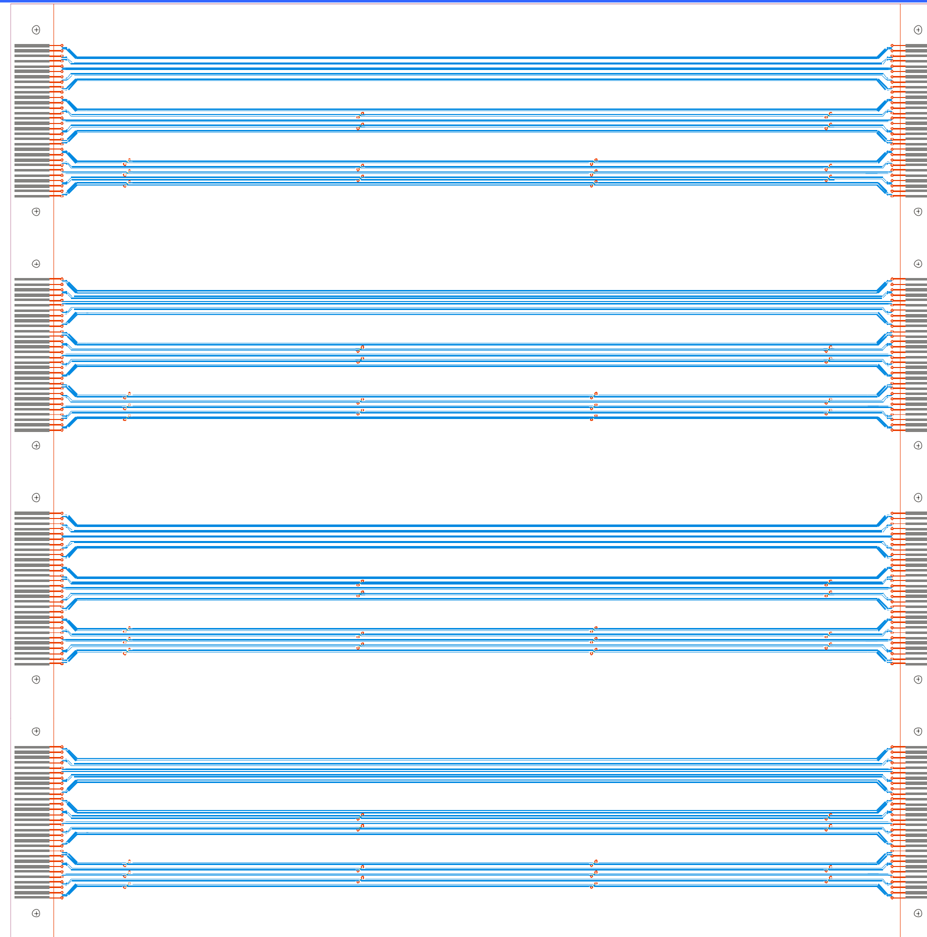
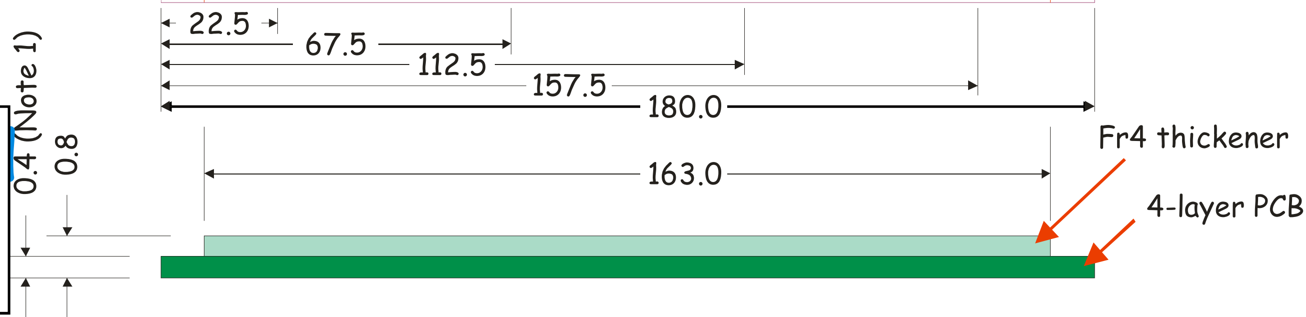
We already have a PCB with many footprints to explore bonding techniques and parameters

This PCB allows long structures to be built
The long differential traces will not only check the continuity and shorts, but allow signal integrity to be investigated.
- Prey and Aggressor pairs with variety of spacings
- 2 "twisted pair" schemes to check reduction of cross talk



Track details more visible on next slide



Exploded View X10 Vert

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ECAL SLAB Interconnect - Test PCB Tracks

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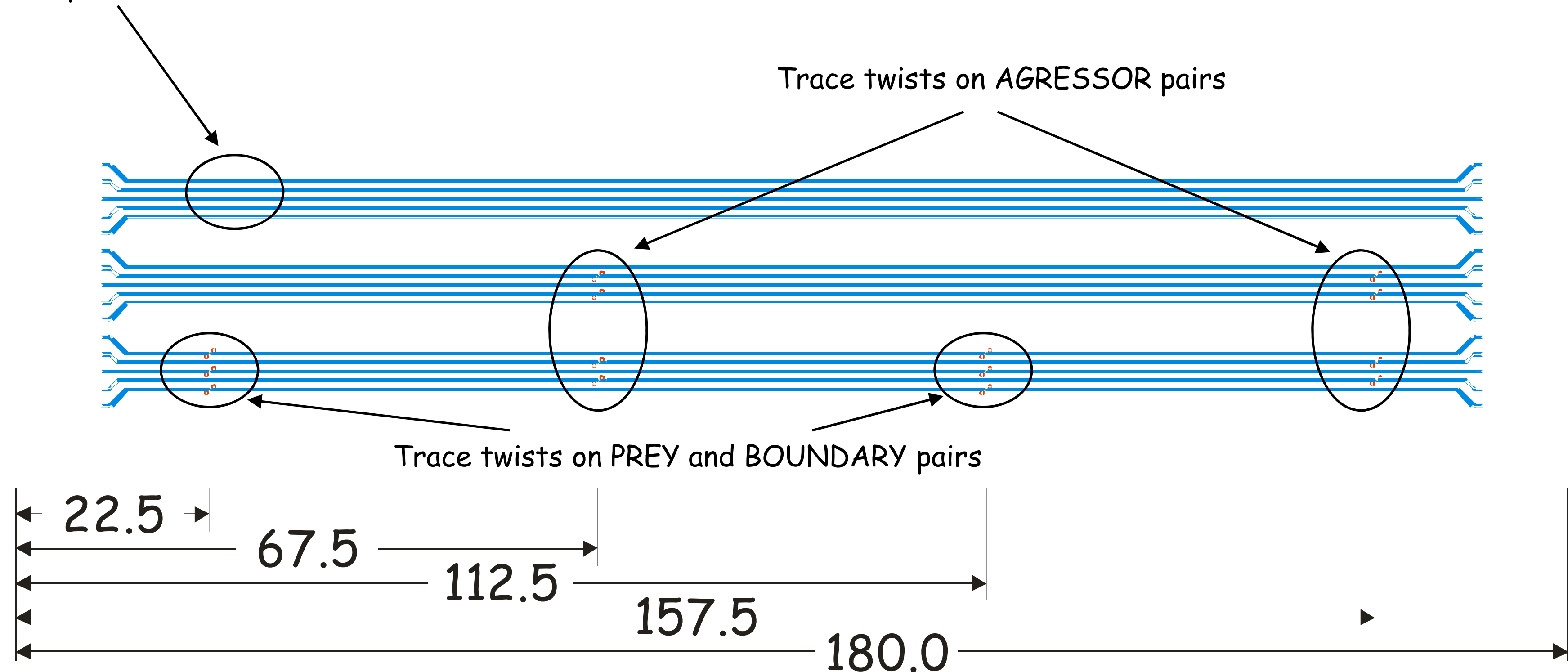

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- Bridges offer major advantages :
  - Remove major bottleneck in number of connections
  - Promise greater reliability
  - Rework likely to be easier
- There are issues that need to be tackled:
  - Bonding force is the most serious
    - IR or Laser Soldering will minimise this
    - Vacuum chuck (or other) offer a solution
- Phase 1 project looks promising:
  - Cost less than £3000 (within WP2.2 ??)
  - Good candidate companies and contacts

Spare Slides Follow

ECAL SLAB Interconnect

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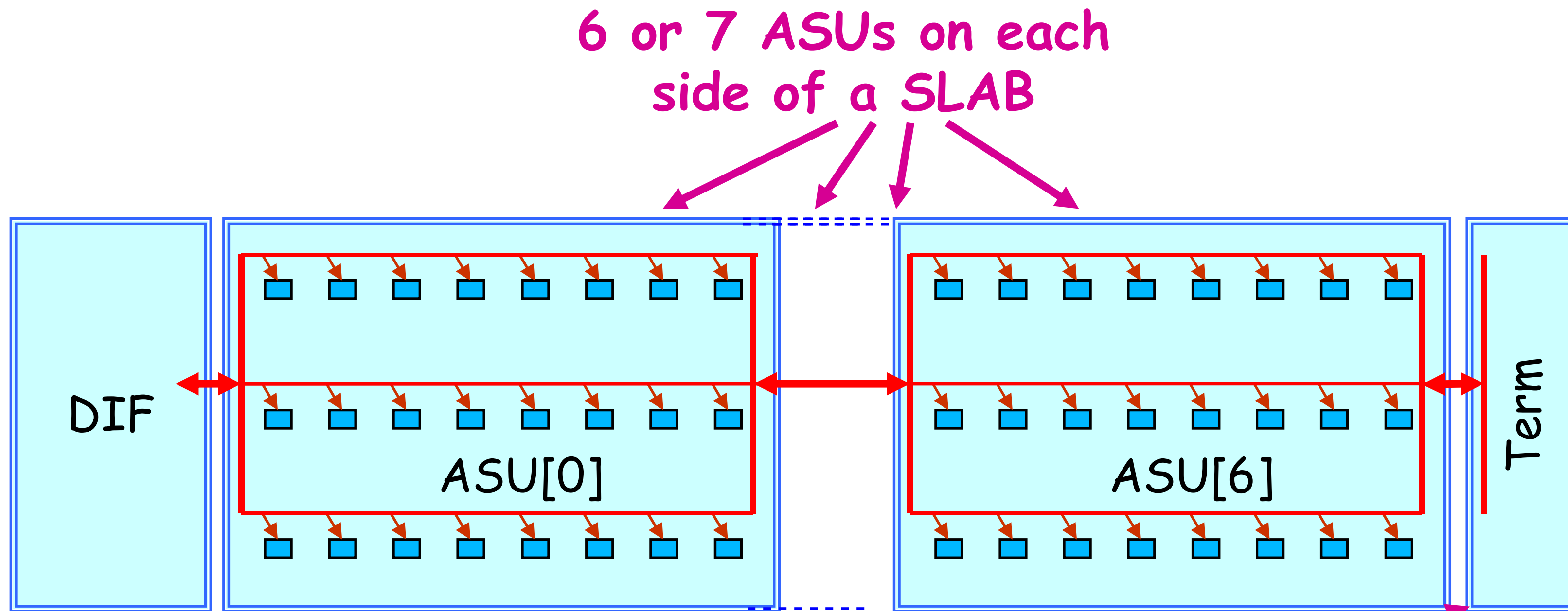


7 or 8 interconnections - each of many ways

- But each extra row needs >= 8 extra signals !!

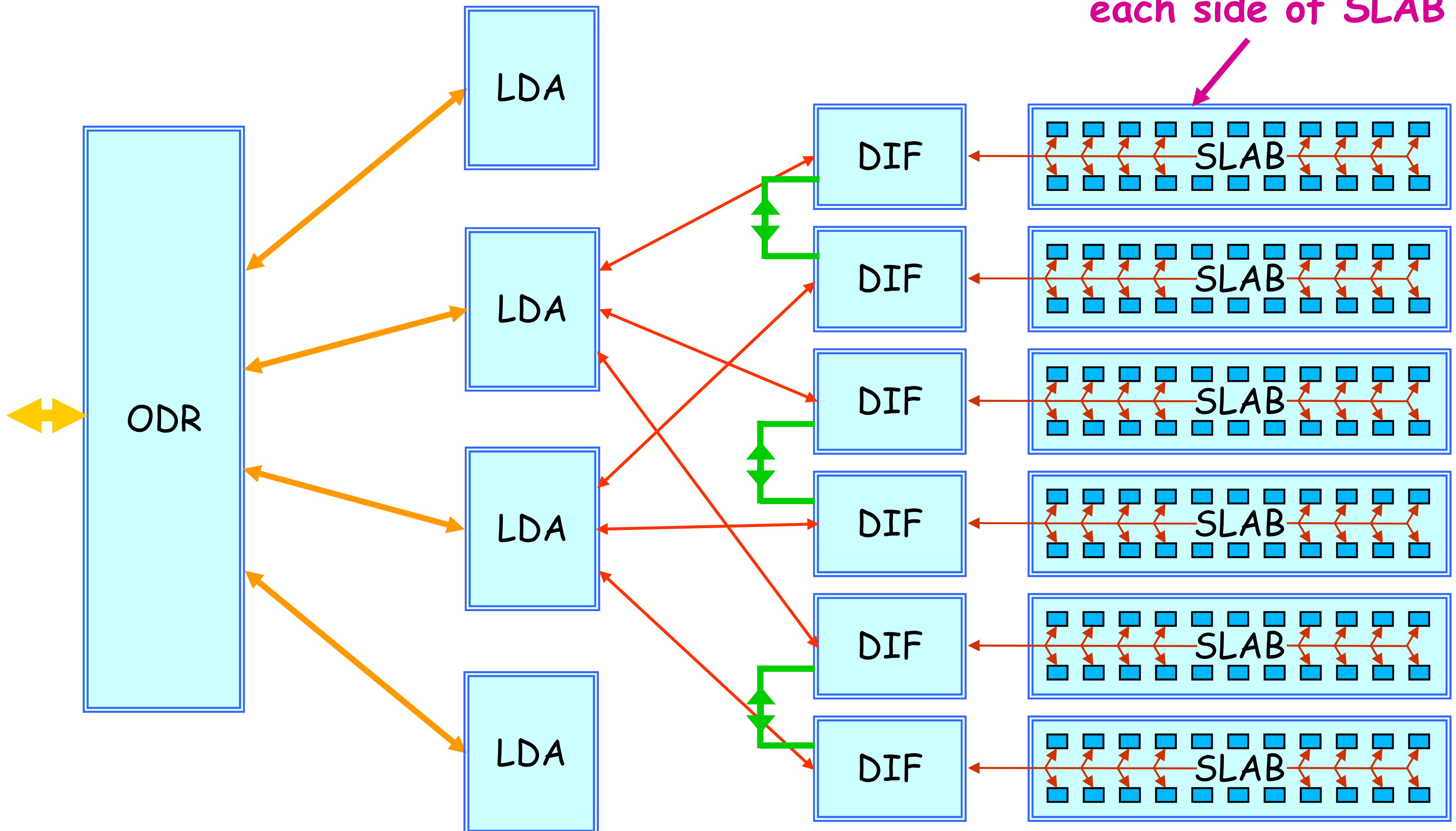
Multiple rows make sense

34 plus power at the last count

The use of a short FFC (Flat Flexible Cable) to make the interconnections between the Slab component PCBs looks a promising way ahead. The following slides discuss:

- The general interconnect problem
- The way in which FFCs could be used
- The initial design work
- The investigations and assessment work needed
- A programme for the work
- Some initial costing

DAQ Architecture – Overall view



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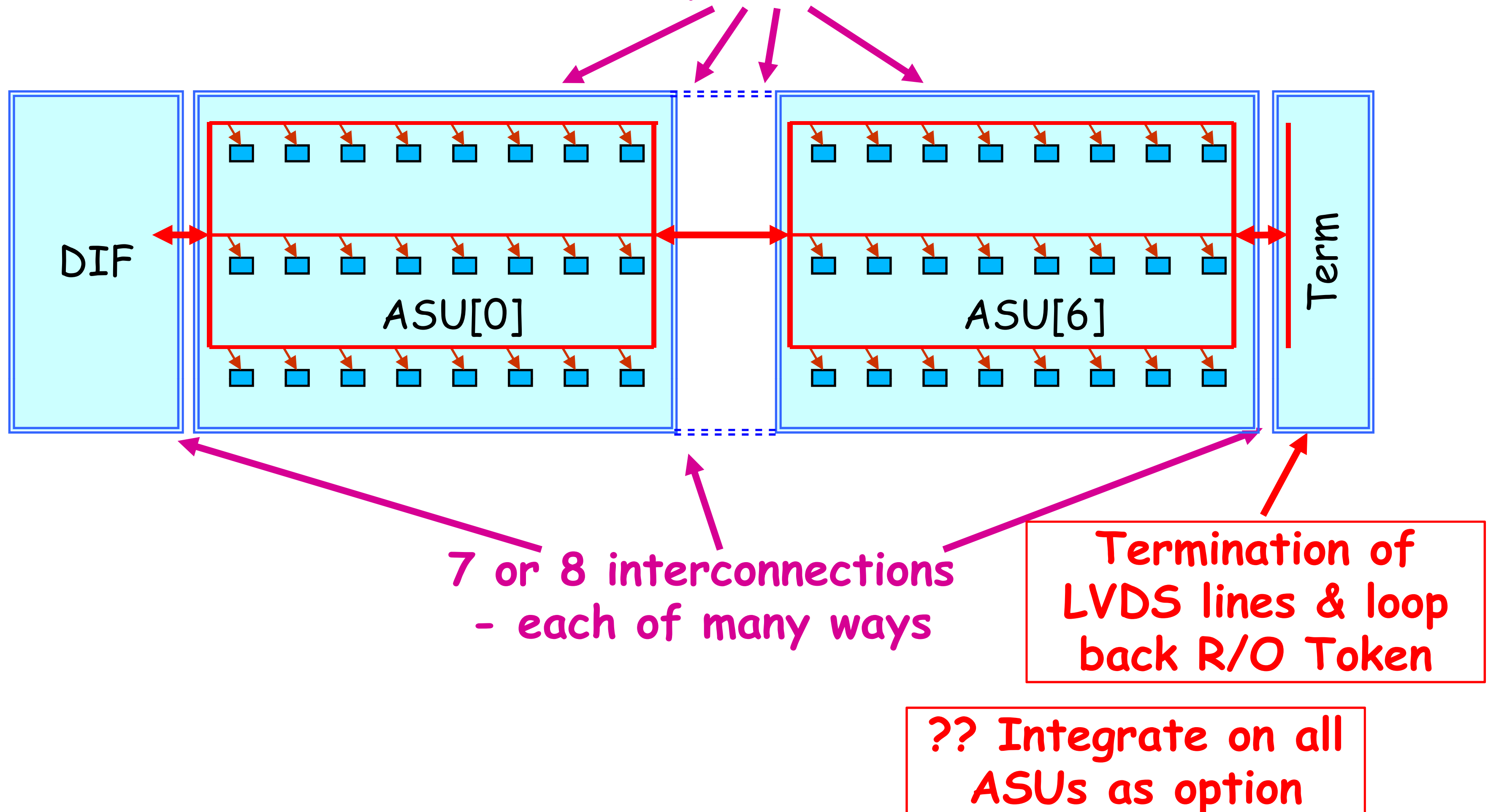
DIF – ASU – ASU -,,,- Terminator



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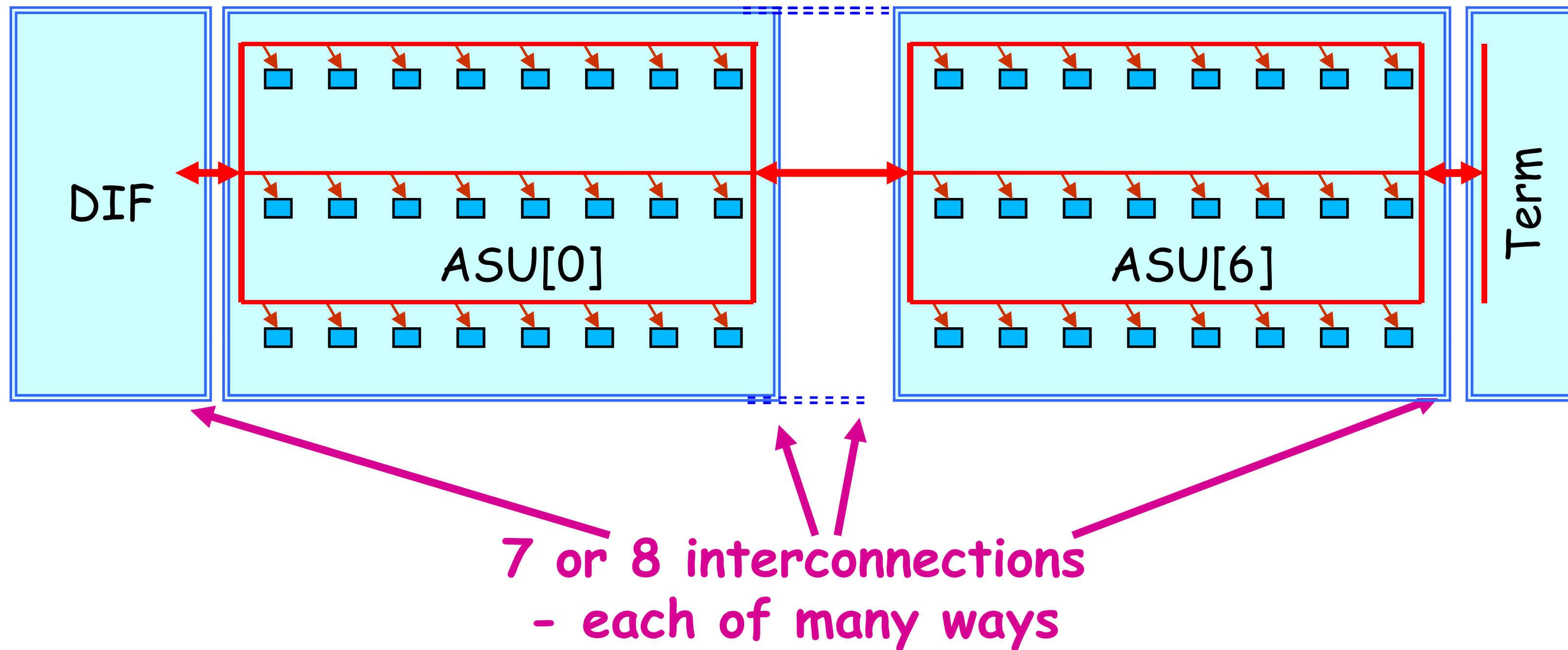
Interconnections



34 plus power at the last count

How much difference will this make?

Multi Row is aesthetically **much more pleasing** ☺☺☺☺

- but what material advantages does it offer?

Clock and Control Lines: LVDS, controlled impedance

- length of each C&C trace reduced below $1/N_{ROWS}$:
  - less signal degradation
  - far cleaner routing – no need for stubs

Read-Out Lines: low voltage swing CMOS

- data load is shared between the rows, so lower rate needed
- length (and hence capacitance) of each R-O trace reduced below $1/N_{ROWS}$
- power for R/O reduced in same ratio

ECAL SLAB Interconnect - PCB Footprint

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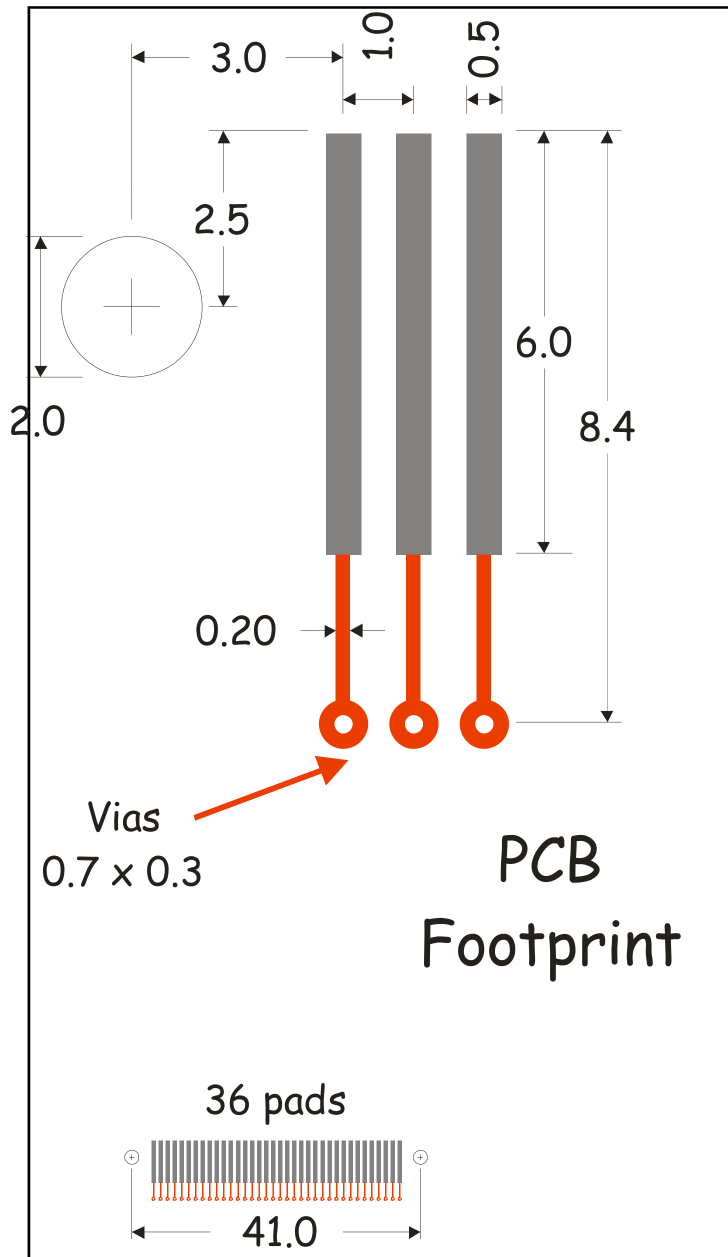
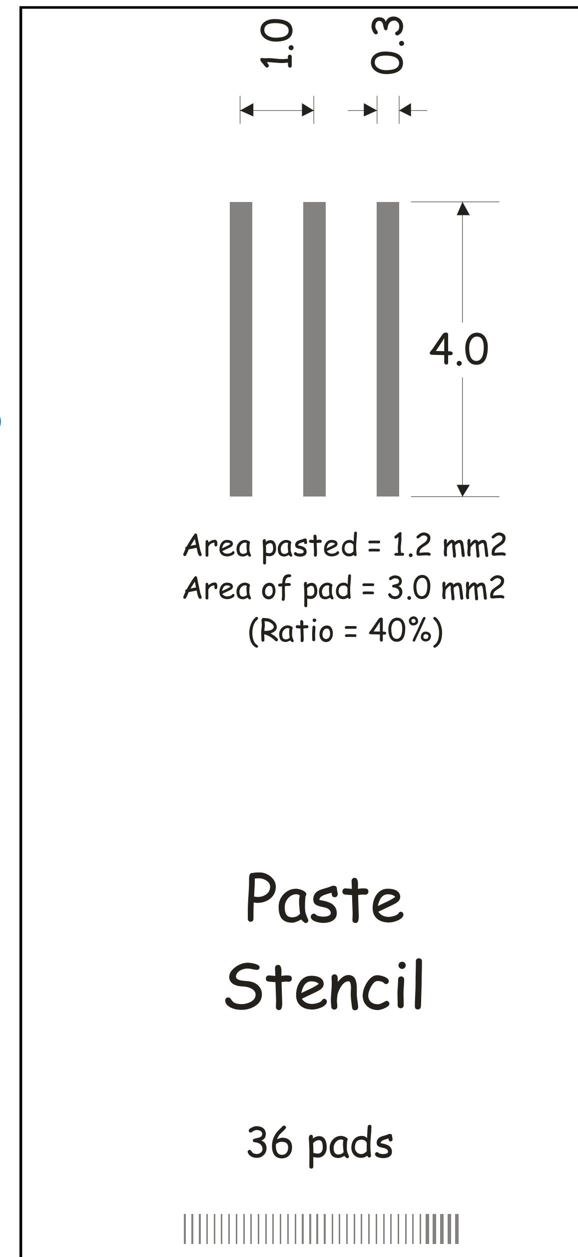


Detail x10



ECAL SLAB Interconnect - FFC Detail

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End-on View

3.0
1.0
0.35
2.5
2.0
5.0
1.0
See Note 1
5.0
2.0
5.0
2.0
5.0
2.5
1.0

Alignment notches

Trace Side

Optional Pre-form to reduce inter-ASU forces

0.4 - 0.7

Pre-Form

Detail x10

36 traces

12.0

ECAL FCC 1p0_36

41.0

FFC Notes

Need to keep thickness down: 100um is max.
- Kapton thickness = 25um (or 50um ?) for this and Hot-bar bonding reasons.
- Trace & Pad thickness = 17um (or 35um?)

Pre-form height 0.3 - 0.7 mm

Need stiffener on one end for use with FFC connector: see separate drawing

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ECAL SLAB Interconnect: Assembly Sequence

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1. Attach FFCs on input edge of ASUs (leave other edge footprints empty)
2. Build ASU, testing with temporary connections to FFCs (ZIF connector or using custom jig)
3. Assemble Slab from ASUs, Terminator and DIF, soldering free ends of FFCs to neighbouring PCB

Alternatively (and now preferred):

1. Build ASU, testing with temporary connections to FFCs using custom jig
2. Assemble Slab from ASUs, Terminator and DIF, adding FFCs to join neighbouring PCBs

Much more difficult once wafers added!!

ECAL SLAB: FFC Programme Phase 1

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1. Sample FFC tests using FFC-Test PCB
   a. Have samples from Axon Cables
   b. PCB design started
2. Get custom FFC
3. Hot-Bar soldering trials:
   a. Oxford have machine we an use for trials
   b. Unitek-Miyachi (Derby) will do half day of tests f.o.c., would then charge £650/day – preferred route?
   c. Custom Thermode tool: £650
4. Laser Soldering:
   a. Group at Univ. of Hull working on this – in contact
   b. equipment likely to be expensive
5. IR: may turn out simplest – but unproven!!
   a. Kapton pretty transparent at IR
   b. Cambridge HEP have IR rework station that may be adequate for this stage. Upgrade planned.

ECAL SLAB: FFC Programme Phase 2

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Phase 2 would aim to refine and equip for EUDET Prototype Assembly:

1. Re-iterate FFC design
2. Close collaboration with mechanical design and SLAB production
3. Establish what equipment/ service provider
4. Handling techniques and production jigs
   a. Considerable tooling effort, e.g. vacuum chuck for Hot-Bar work
5. Rework techniques:
   a. IR rework station ?
   b. Pad levelling
   c. Rework of any mechanical joints
6. Connnection Jig design and production for ASU testing

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Cost of FFC Programme Phase 1

1. FFC-Test PCB: £600
2. Custom FFC run: £350 - £550 for ~200 pieces
3. Hot-Bar soldering trials at Unitek (including custom Thermode tool): allow £1700
4. Laser Soldering: no indication as yet as to whether Hull would charge to carry out investigation.
5. IR: no major costs foreseen – a bit for tooling ?