IN2P3

Omega

LAL LPNHE

Improvements of ROC chips

VFE - ROC

Frédéric DULUCQ

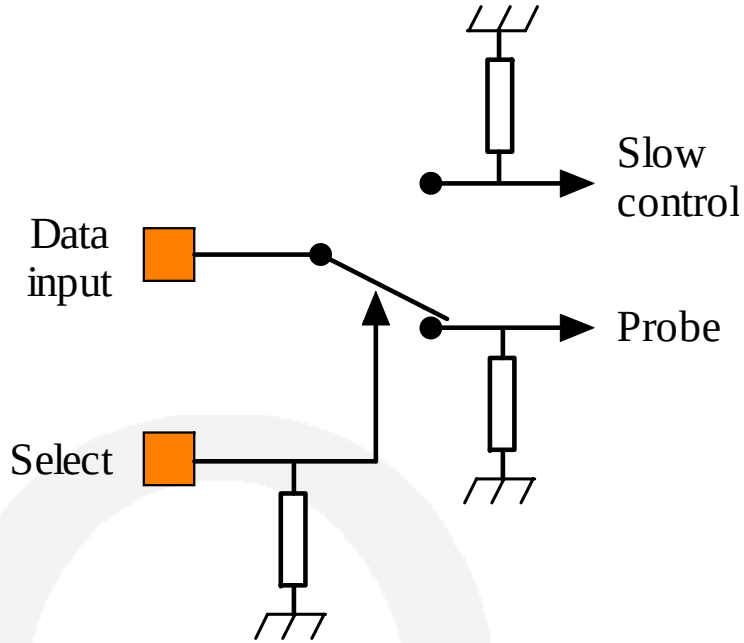
CALICE Calorimeter for ILC

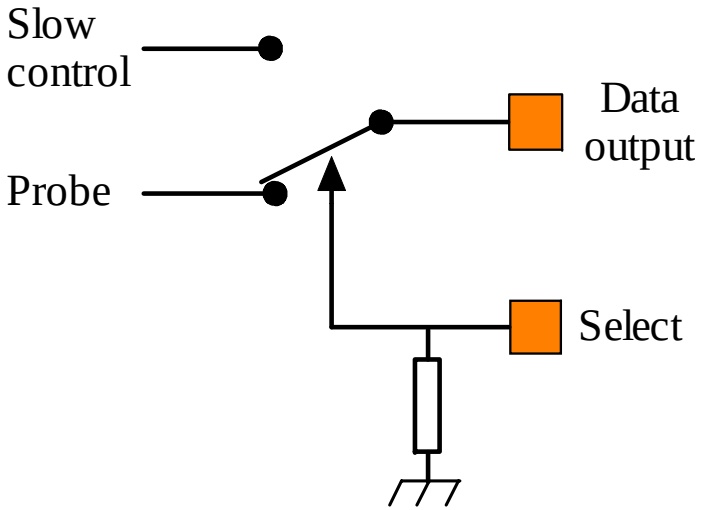
17-19/03/2008

Orsay MicroElectronic Group Associated

Probe and Slow Control shift registers

- Multiplex these 2 registers (in, out, clock, reset) ➔ save PADS (8 ➔ 5)

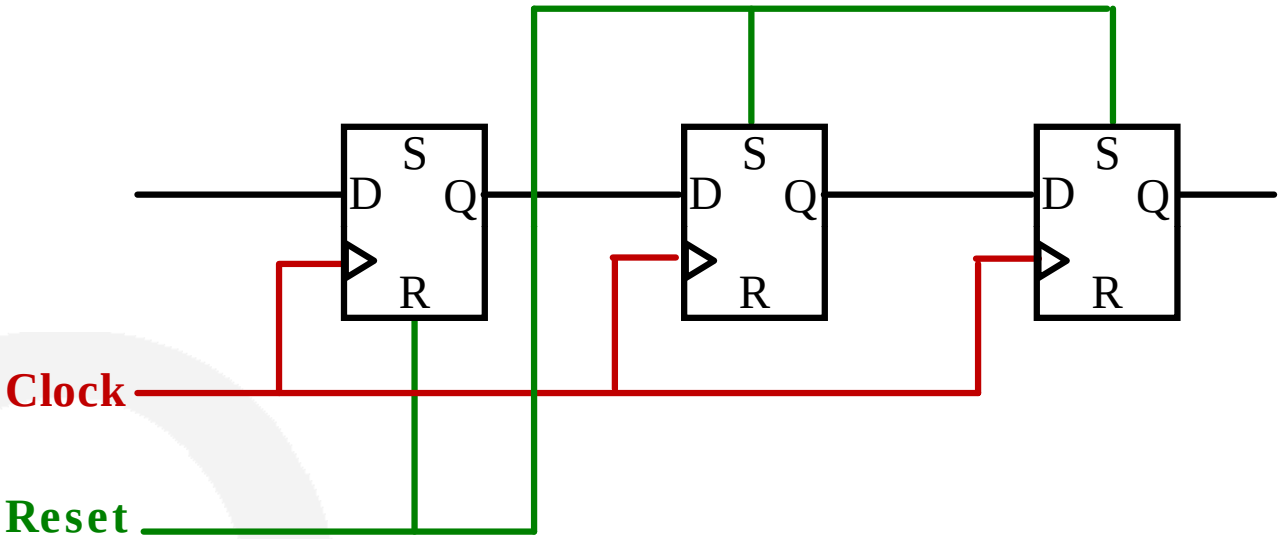




- Select line added : default register is probe to prevent glitch on SC
- Extra PADS can be added for direct access to registers

Default SC configuration

- Use Set / Reset of Flip-Flops for default configuration

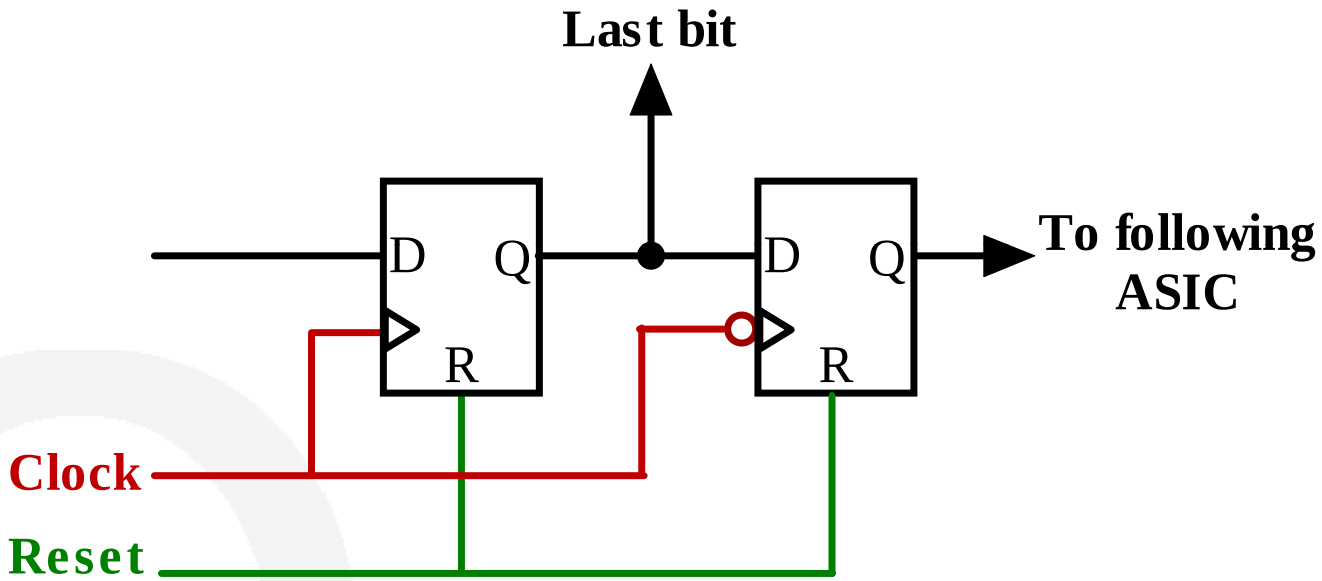


Example default configuration : “011”

- Can also be done with Q and Q* of Flip-Flops (already done for some bits)

SC daisy chain

- Improve daisy chain between ASICs :
  - Add opposite edge FF at the end of shift registers

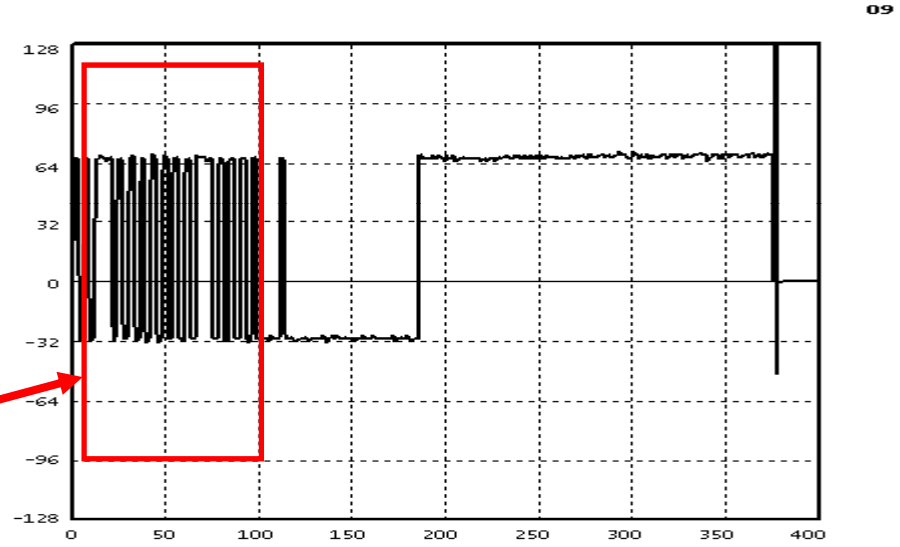


- Allow to meet timing requirement between last FF of chip “N” and first FF of chip “N+1”
- Inside chip ➔ use clock reversing to prevent timing problem

DHCAL : Readout

- During readout, remove “bad frame” (address pointer error when chip is not full)

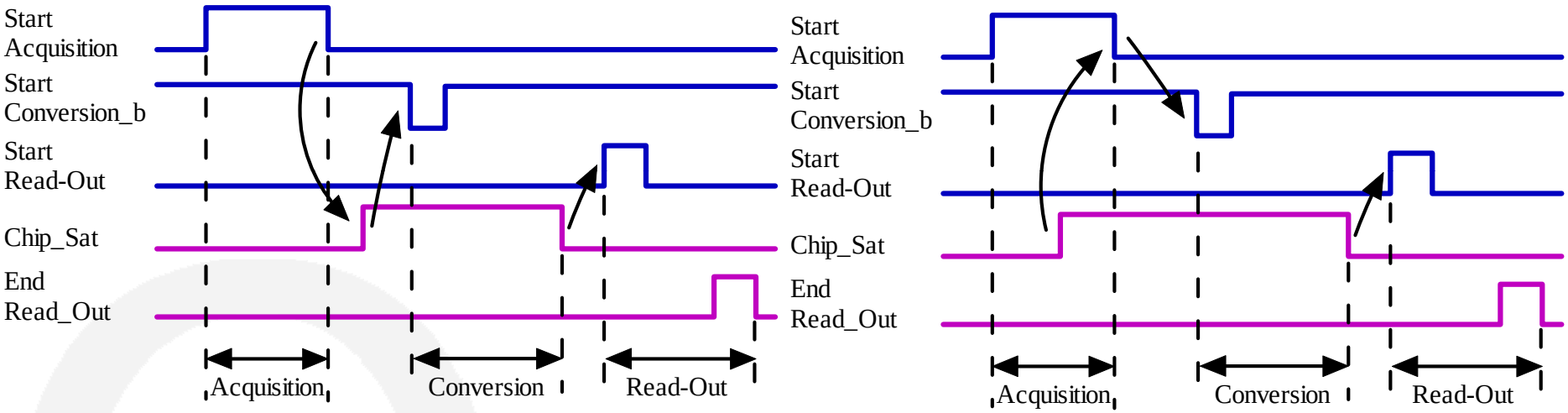
First irrelevant frame



- Capacity of 127 trigger instead of 128 ➔ change digital limitations (should be minor change in VHDL)

DHCAL : StartAcquisition

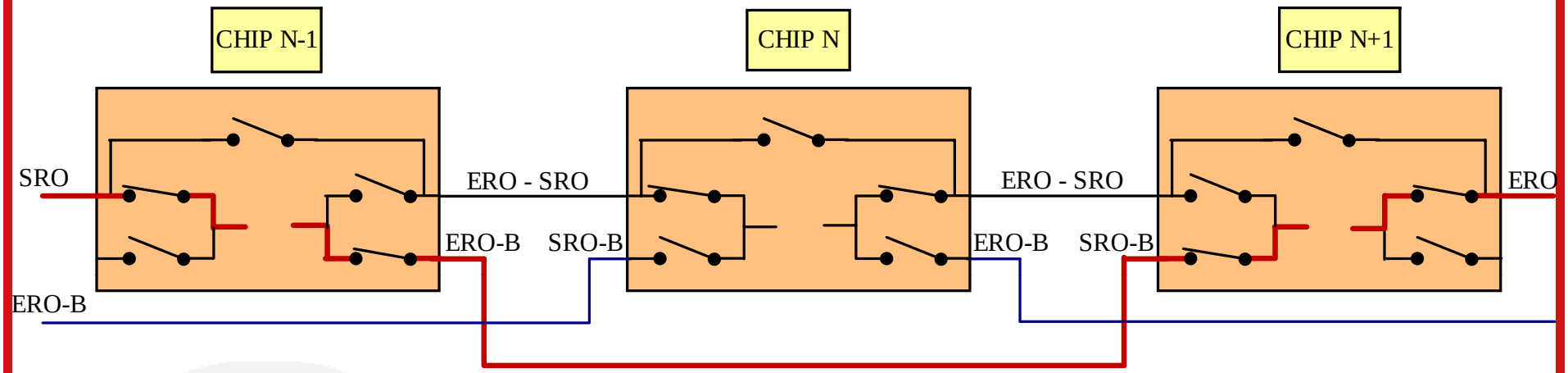
- Change for SPIROC like ➔ “StartAcquisition” active on level.



- RamFull ➔ ChipSat (OK for SPIROC and HARDROC)
- Allow to remove “RamFullExt” signal and to let DAQ stop acquisition
- “StartAcquisition” should be now named “CtrlAcquisition”

StartReadOut and EndReadOut

- Add bypass for these 2 signals (SRO, ERO ➔ SRO-B, ERO-B).

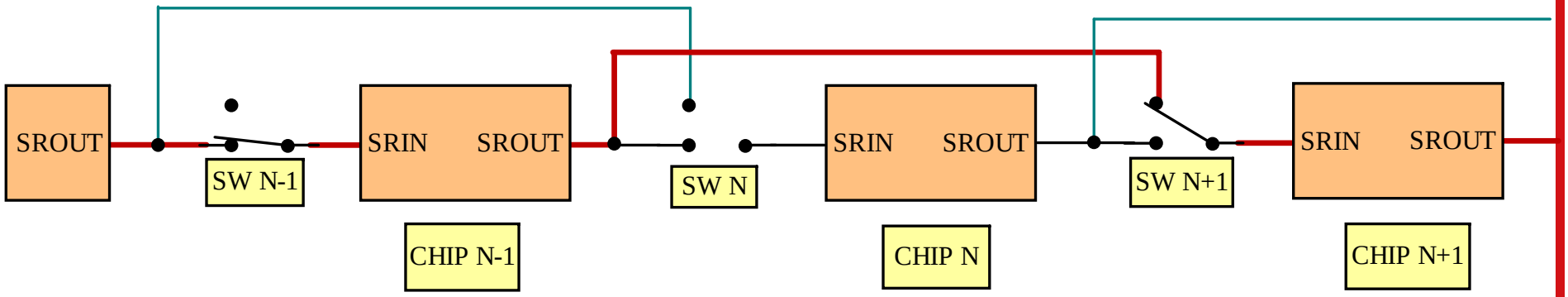


In red, StartReadOut and EndReadOut flow if chip “N” fails

- Chip N can bypass itself by SC
- Chip “N-1” and chip “N+1” can bypass chip “N” by SC
- If Chip N fails :
  - Chip N-1 sends EndReadOut signal on EndReadOutBypass
  - Chip N+1 reads StartReadOut signal on StartReadOutBypass

Slow Control

- Add bypass jumpers on PCB

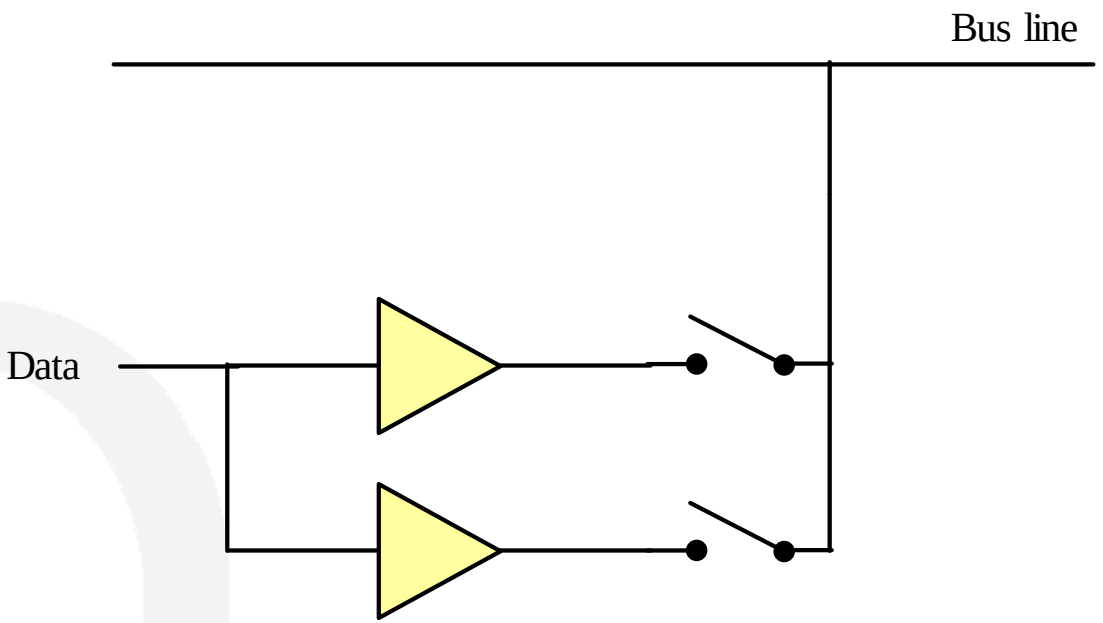


In red, SC flow if chip “N” fails

- Default position is chip “N” reads chip “N-1”
- If Chip N fails :
  - Switch N removed
  - Switch N+1 ➔ in position to read chip “N-1”

Data and TransmitOn

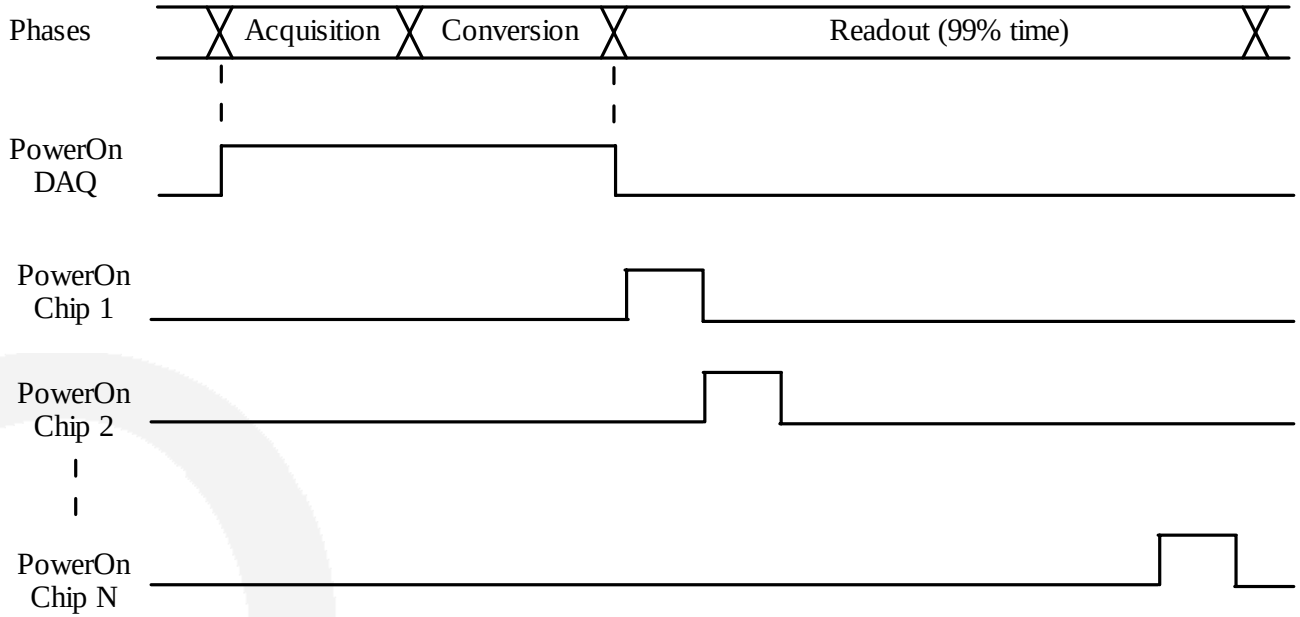
- Add 1 extra buffer on these 2 signals
- Each one is removable from bus line by SC



- Allow to remove one buffer that stick the bus line

Power On digital (very preliminary): 1/3

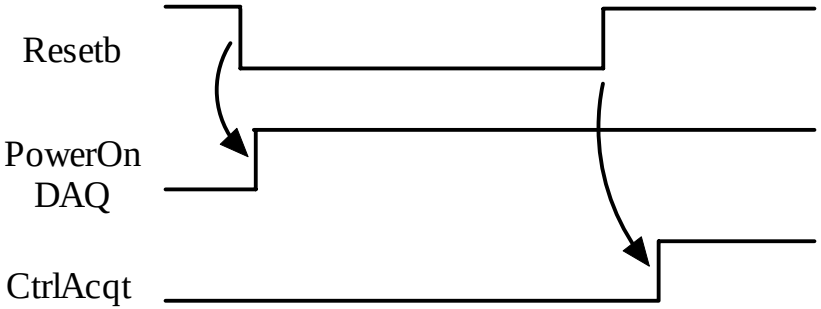
- PowerON must start/stop clocks and LVDS receiver to meet power budget.



- 2 working modes :
  - Acquisition, Conversion (common to all) ➔ managed by DAQ
  - Readout ➔ managed internally
- Internal PowerON ➔ OR of “PowerOnDAQ” and “PowerOnChip”

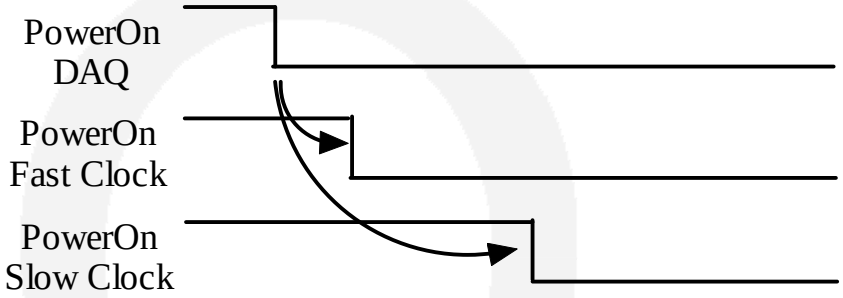
Power On digital from DAQ : 2/3

- PowerON set during a reset phase before each acquisition



  - Completely managed by DAQ
  - Reset pulse > LVDS start time

- PowerON release at the end of conversion

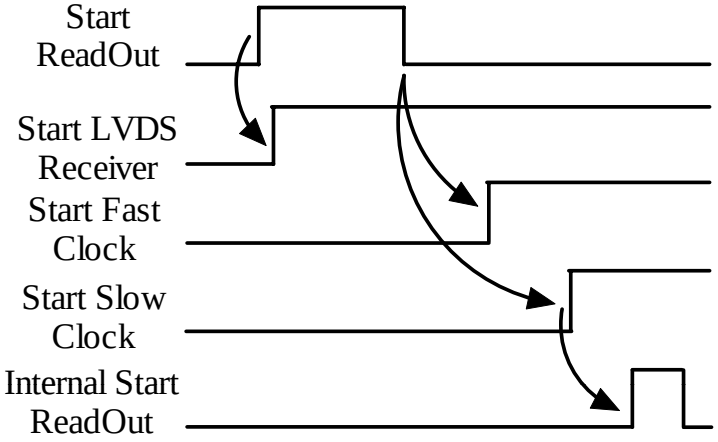


  - Synchronized internally to properly stop clocks
  - Effective PowerOn release ➔ after max 2 ticks of Slow Clock

- PowerON DAQ is asynchronously set and synchronously release (internally in each chips)

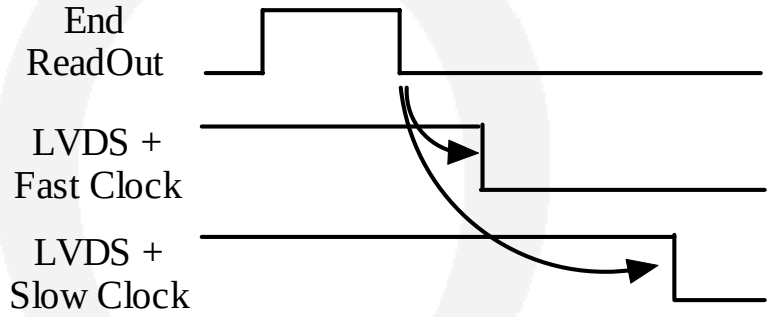
Power On digital for Readout : 3/3

- PowerON of Chip N set by chip “N-1”



  - Internally managed by ASIC
  - StartReadOut pulse > LVDS start time
  - Synchronous clocks start
  - Internal StartReadOut starts state machine

- PowerON release at the end of Readout of chip N



  - Synchronized internally to properly stop clocks
  - Effective PowerOn release ➔ after max 2 ticks of Slow Clock
  - PowerON stops LVDS and clock at the same time synchronously

- PowerON split into 2x“StartLVDS” and 2 x“StartClock”

CONCLUSION

- Many improvements on Slow Control
  - Default mode
  - Last FF for daisy chain timing requirements
- Reduce PAD number
- Increase reliability:
  - Double some drivers
  - Possibility to disconnect bus drivers
  - Add bypass on critical signals
- Remove “dummy frame” and improve digital working
- Management of PowerON for digital part
  - Start / Stop clocks
  - Start / Stop LVDS receivers