SiW ECAL: the status before Fermilab

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CALICE caollaboration meeting 18/03/08, Argonne

Outline

- Wishlist Prague
- What happened since Prague?
- Some issue to tackle
- What will happen until Fermilab?

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Wishlist of Prague

- Solution to instable pedestals (improved regulators?)
- Revisions of bottom slabs
- Spare power cables and maybe a test of the existing cables + new ones will be needed when the detector is completed
- Data of ECAL slow control should be included in data stream (the most useful would be currents and voltage at each wafer)
- Improved accessibility of ECAL cables (for now removing the fans requires moving the ECAL out of its nominal center – time consuming)
- Revision of program for control of ECAL stage
- ECAL position on stage in database
- Online Monitor:
  - Possibility to limit visualisation to center/upper part
  - Correction for moving pedestals ?
- Possibility to improve the space available for ECAL rotation?
- DESY test with all experts on site (with beam if possible!)

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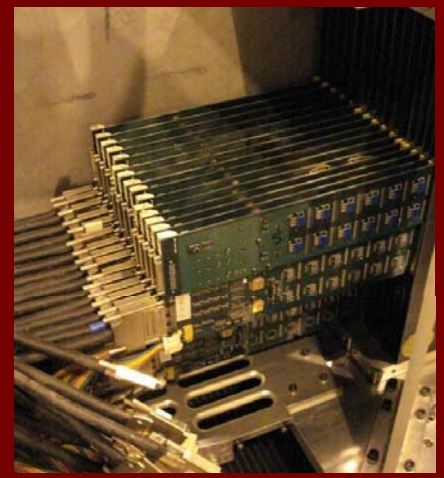
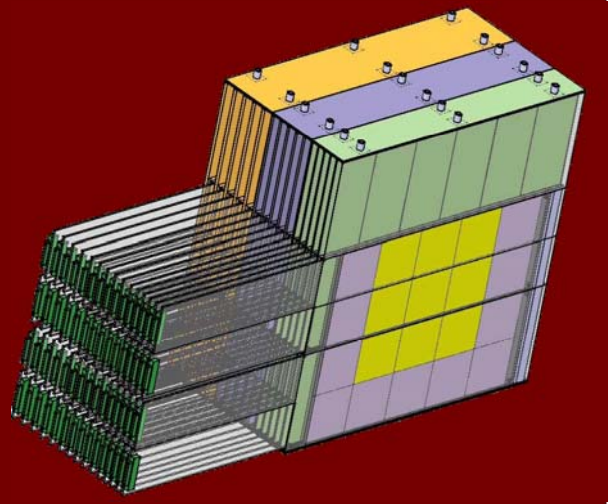
Reminder: configuration in the CERN 2007 TB

- Center part fully equipped (30 layers, 6480 channels)
- Bottom part (equipped subsequently from back to front):
  - June 23rd: 12 layers
  - July 4th: 6 more layers added
  - July 26th: 6 more layers added, tungsten dummies in empty slots

    -> 24 layers, 2592 channels
- 9072 channels in total





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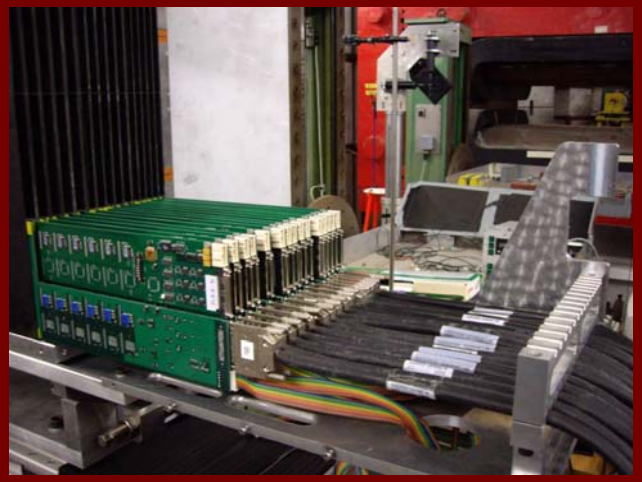
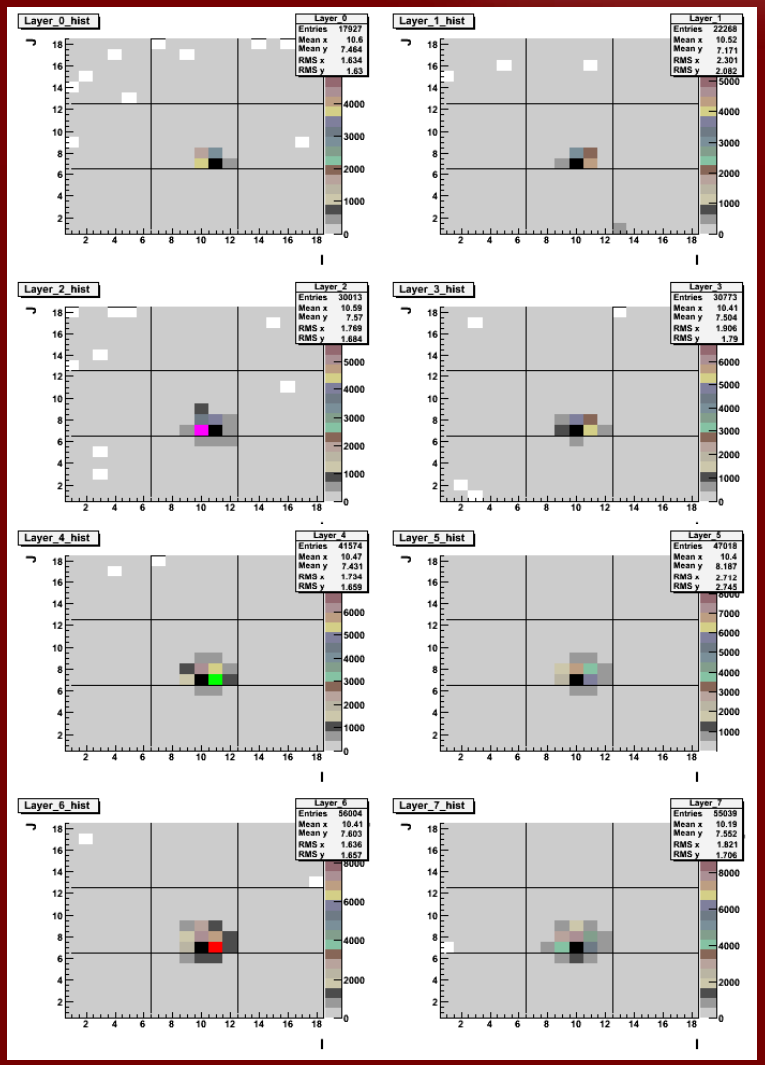
Tests at DESY 12/07

- ECAL fully equiped: 9720 cells
- Some beam data to validate additional buttom slabs
- Electronics tests revealed weaknesses of patch panel as source of noise problems





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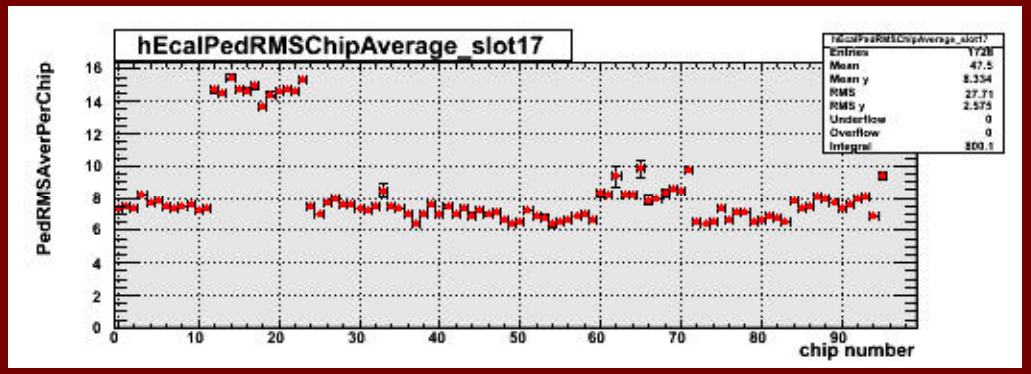
Reminder: Noise problems

- All noise values for the cells on a PCB are too high
- Very sensitive to the delivered power, thus to the power supplies and/or the power cables
- Changing of power cable can solve the problem
- Several cables marked as „problematic“
- Noise varying with positioning of patch panel



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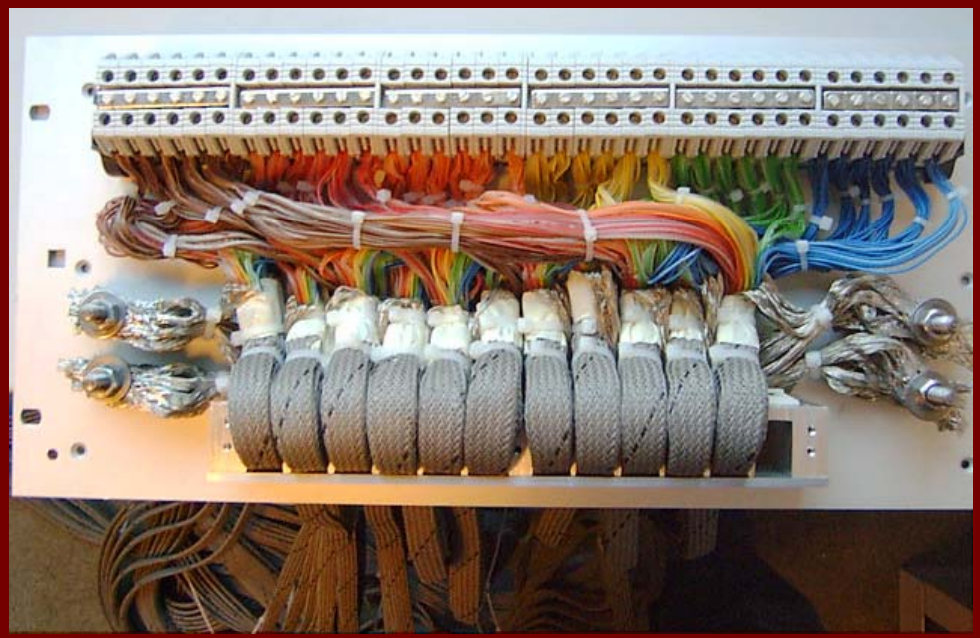
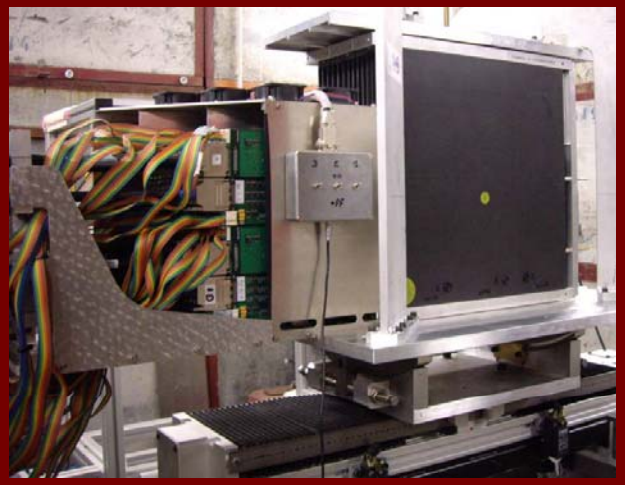
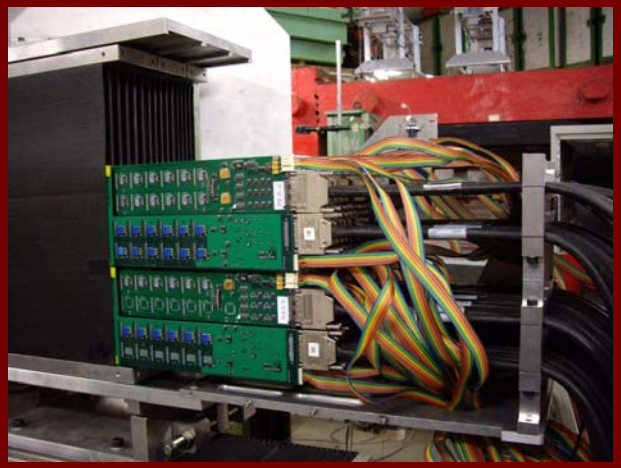
New Patch Panel

- Built from scratch
- All Power cables with extra shielding
- Ground of all cables connected on the detector side
- Big thanks to Patrick Cornebise From LAL







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Electronics and integration tests at DESY 02/08

- Complete mounting on the new AHCAL stage
- Installation of new patch panel and routing of power cables
  - Noise tests prove new pp a complete success

- Big thank you to Jean-Charles Vanel & Patrick Cornebise

On the way to Fermilab

- Shipment prepared
  - ECAL support stays on AHCAL stage
  - Slabs and W structure in their boxes

- Installation at Fermilab:
  - Start at 21st of April

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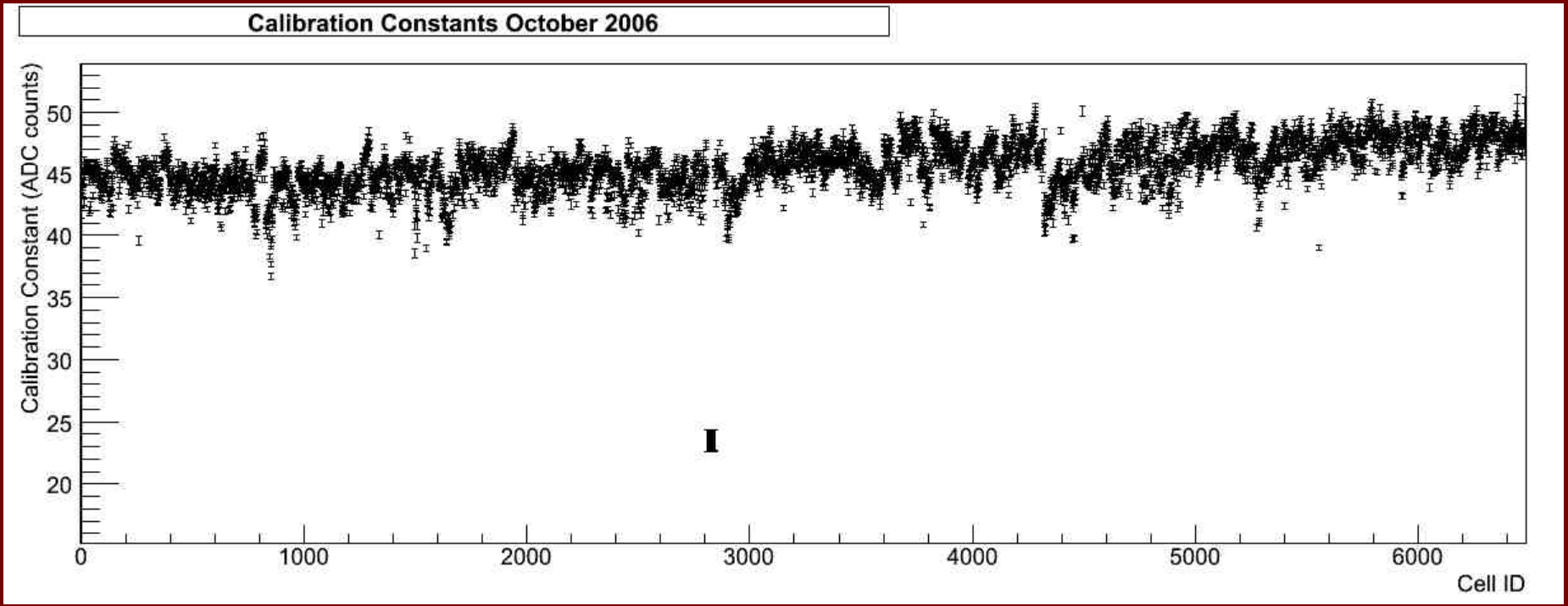
Some issue: Focus on calibration studies

- Currently in database: 1 set of constants obtained with muon runs from october 2006 CERN period



- Now additionally: constants for 3 other periods (August 2006, July 2007 (0 deg), August 2007 (20 deg)

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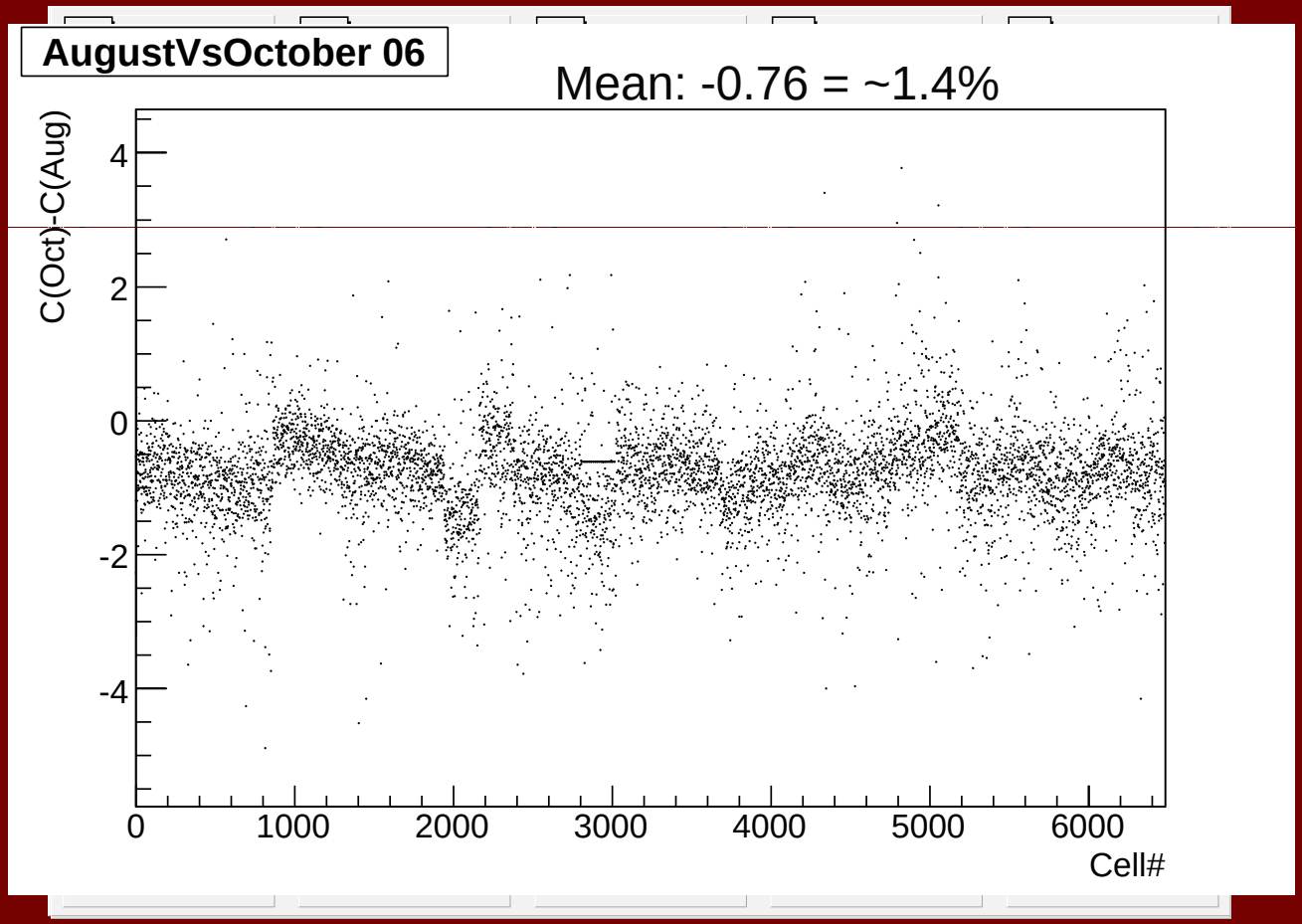
August 2006

- Dead map looks good
- Significant systematic shift of calibration values



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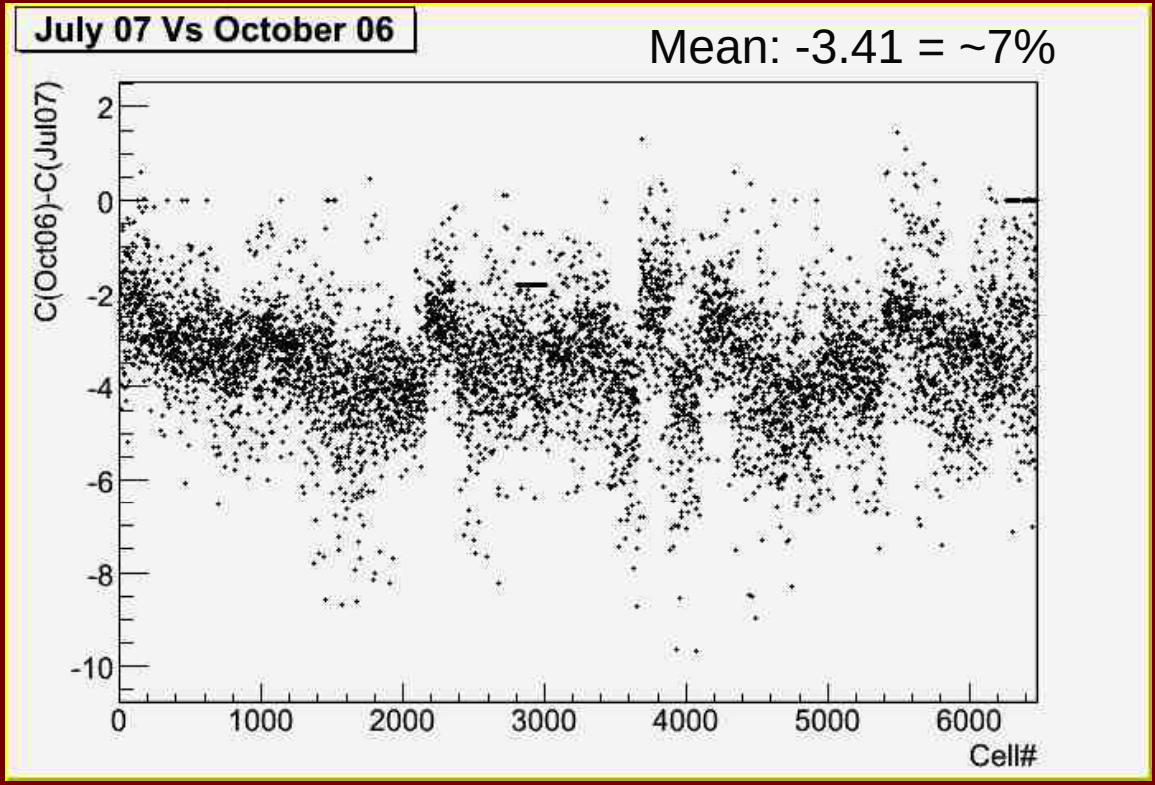
July 2007 (0 deg): central slabs

- Dead map looks ok, readout problem of last layer, 44 dead
- Confirms data quality checks in Prague
- Significant systematic shift of calibration values
- Few slabs with less effect: influence of old patch panel ?



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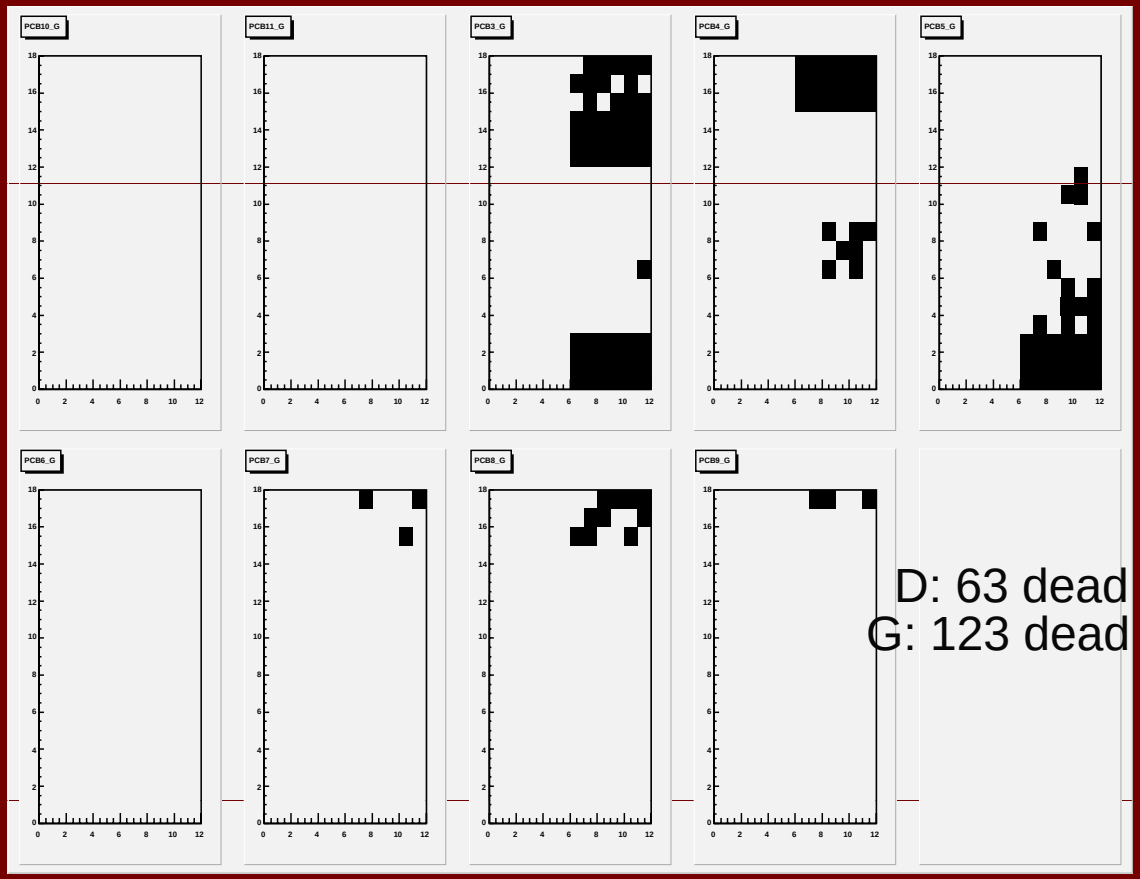
July 2007 (0 deg): buttom slabs

- Quite some dead cells, even entire chips
- Confirms data quality checks in Prague



D: 63 dead
G: 123 dead

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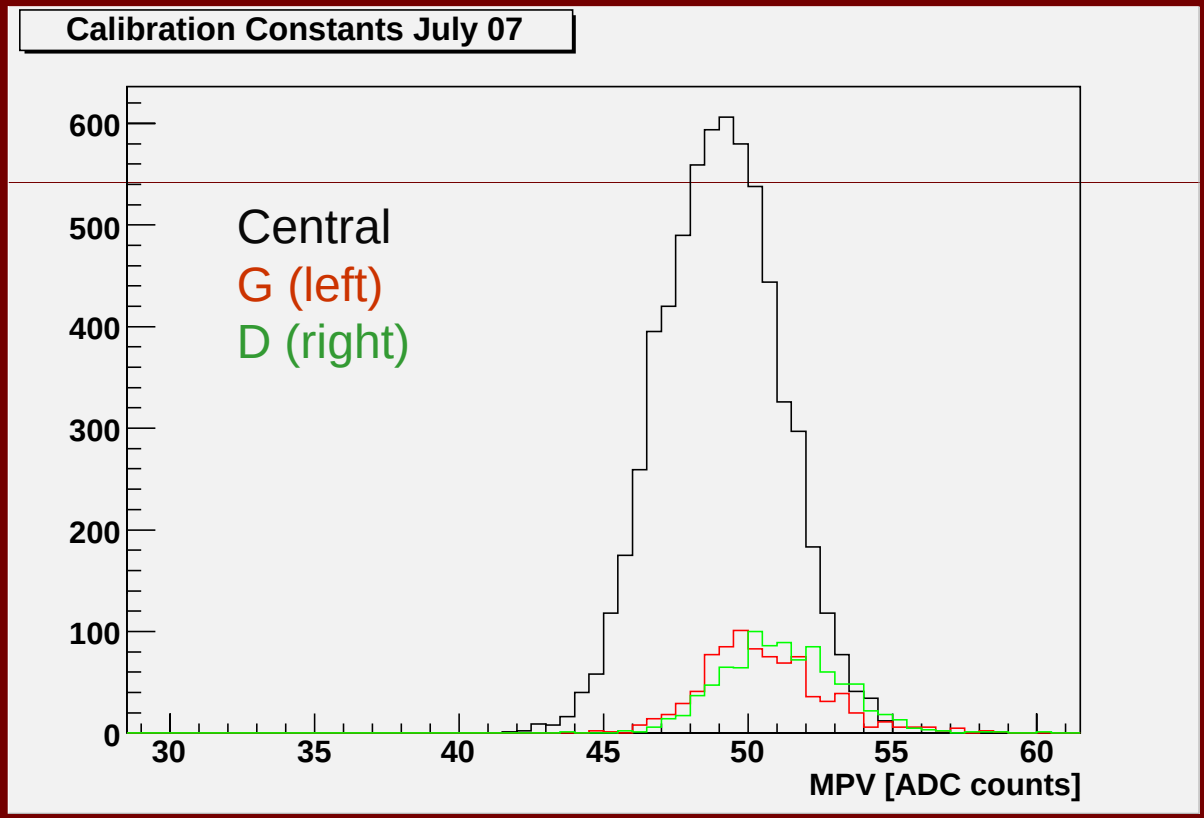
July 2007 (0 deg)

- Shift in peak between central and buttom (wafer production)
- Shift between left- and right-handed slabs (?)



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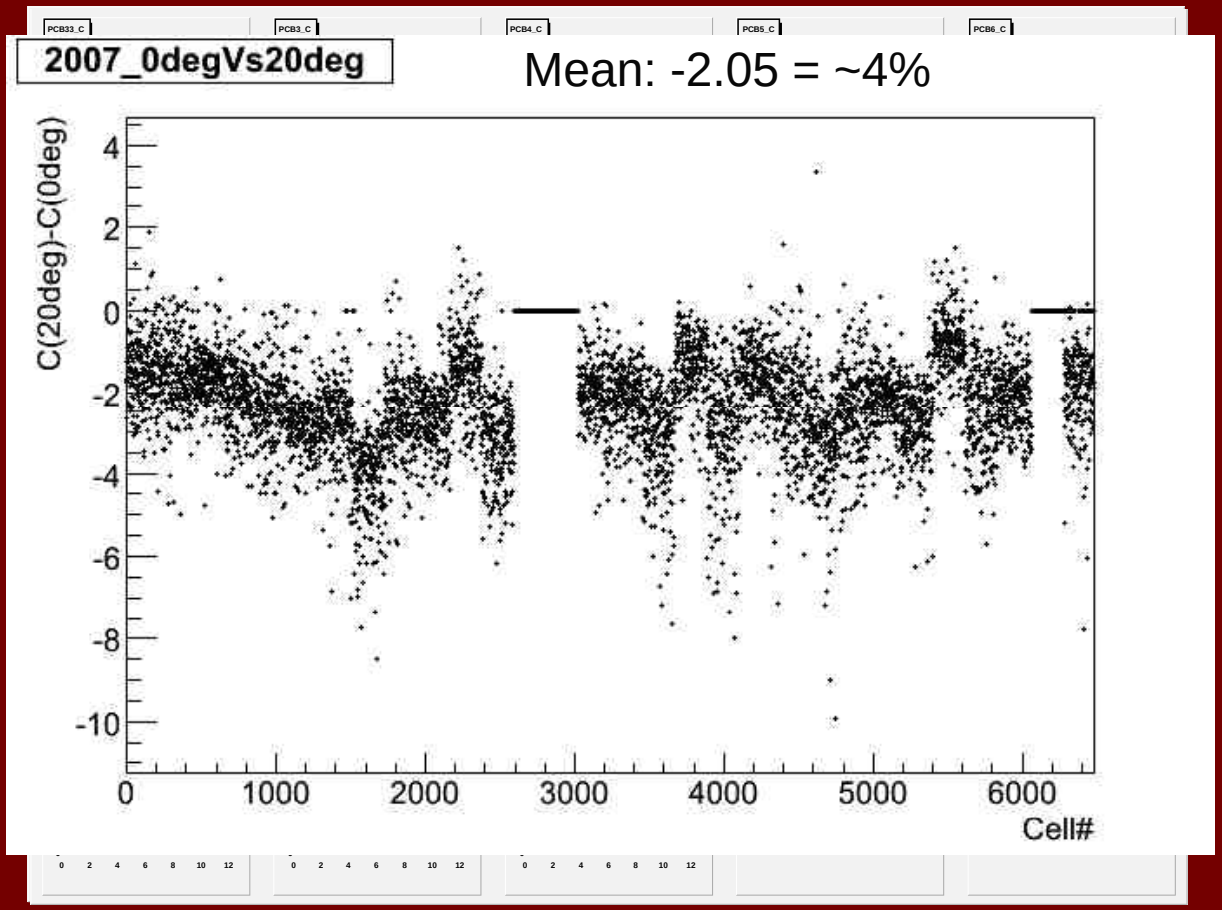
Aug 2007 (20 deg): central slabs

- More dead channels than before rotation, additional r/o problem, 141 dead
- Higher values expected, again significant shift



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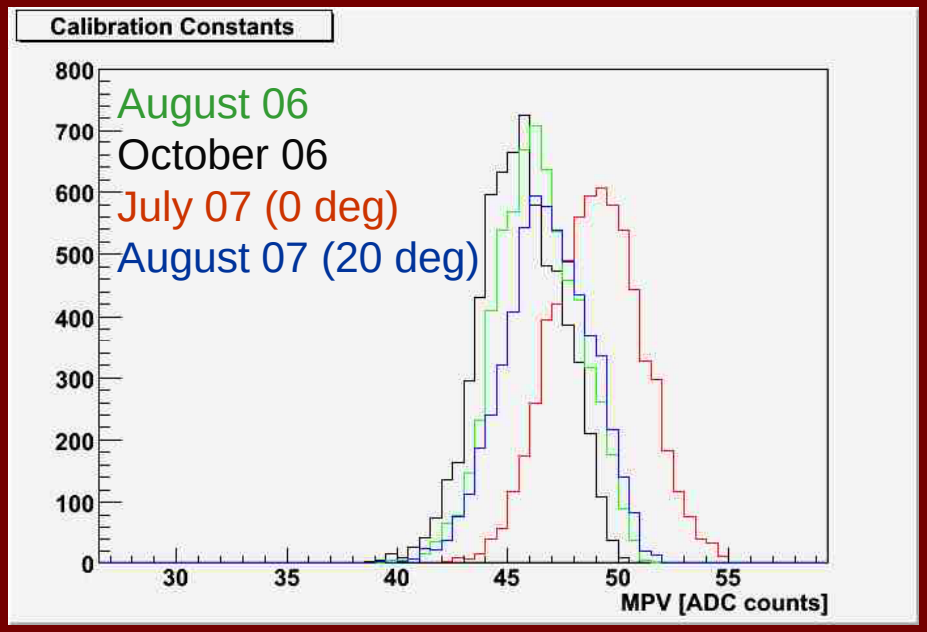
Calibration Constants overview central slabs

- Significant shifts between all periods – why? Not seen in e- runs
- Si diodes known to be stable regarding temperature, operated on saturation plateau at 200V
- 2 (?) possibilities
  - 1st: Hold Value/Trigger issues (same setup in Jul/Aug 07 !)
  - 2nd: stability of on-board electronics (gain variation with Temp and Voltage)



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...to come back to this:

- Solution to instable pedestals (improved regulators?)
- Revisions of bottom slabs
- Spare power cables and maybe a test of the existing cables + new ones will be needed when the detector is completed
- Data of ECAL slow control should be included in data stream (the most useful would be currents and voltage at each wafer)
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Conclusion

- ECAL ready for data taking at Fermilab
- New patch panel eliminates noise problems
- ECAL slow control monitoring during all the test period obligatory
- Tackle dead cells: chips and read-out problems
- Need faster feedbak to identify r/o problems
- Should find reasons of changes in Calibration Constants
- 3 calibration sets for now (Aug06/Oct06/Jul07) – which to use for next reconstruction?

Backup

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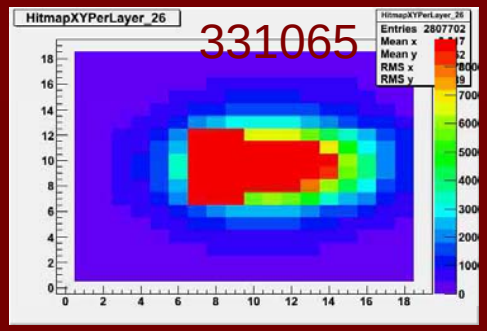
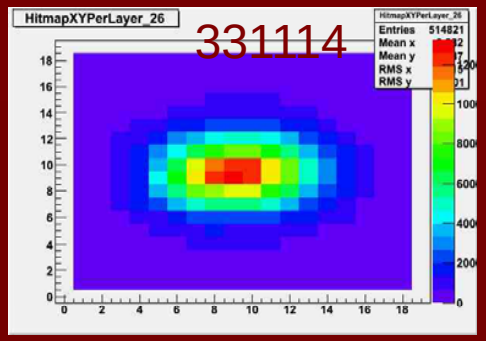
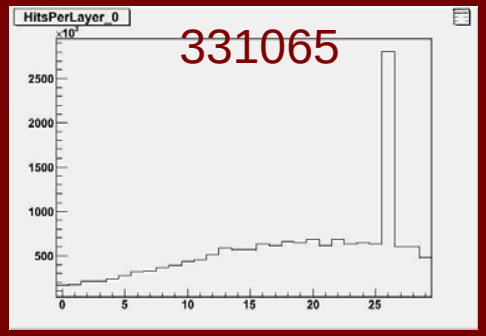
Noisy chips

- Some chips can develop higher noise for a certain period in time

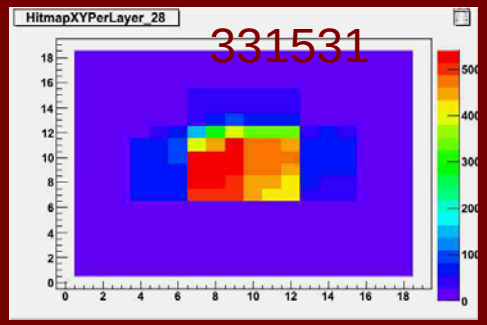
Layer 26

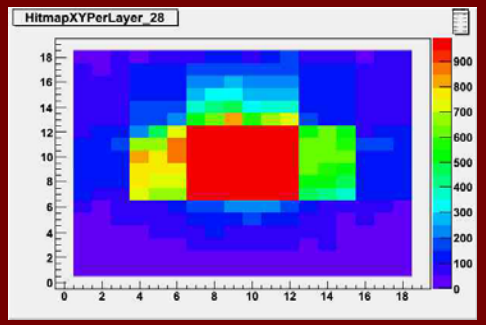


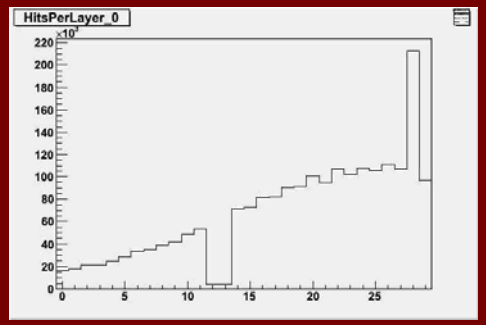




Layer 28







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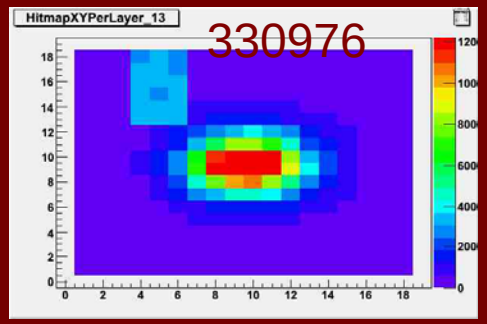

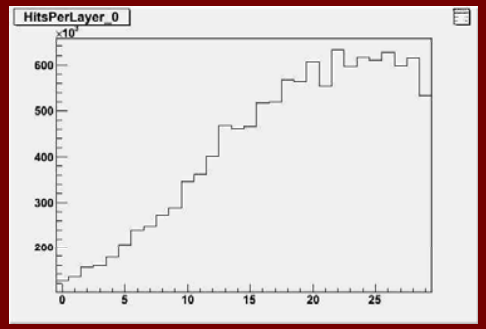

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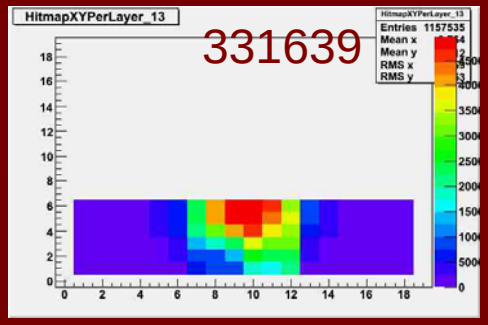
Behavior of bottom slabs

Layer 13



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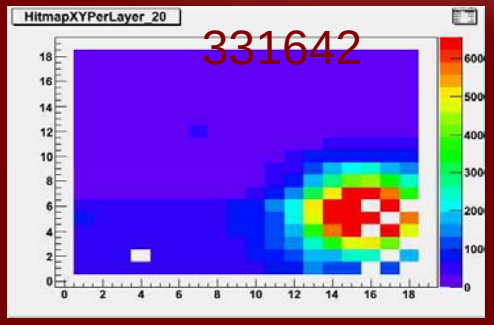

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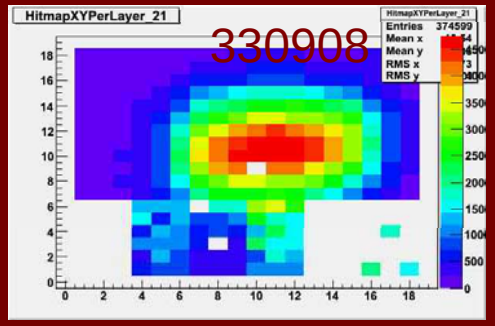

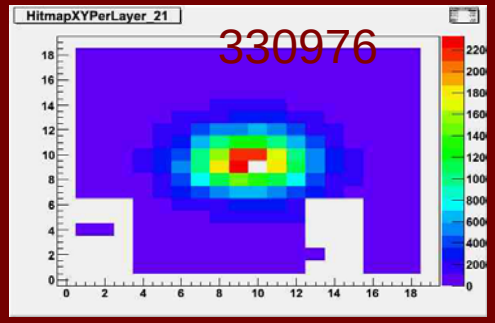

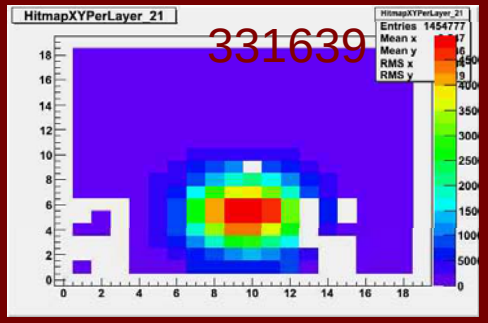

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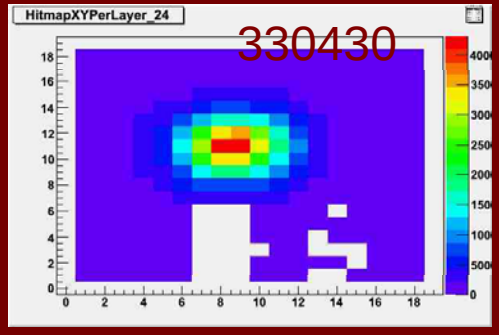

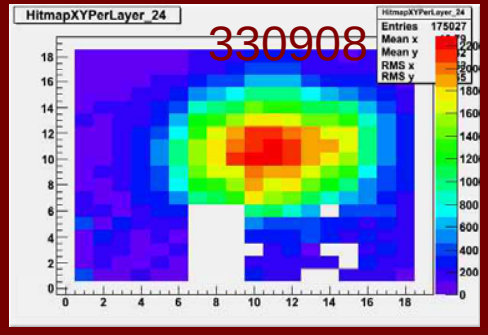

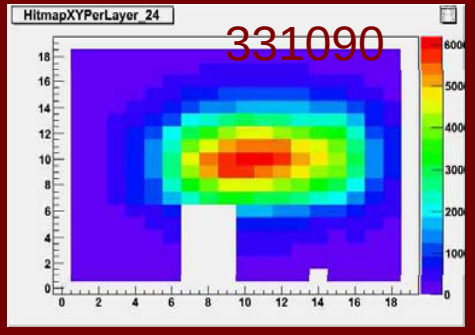

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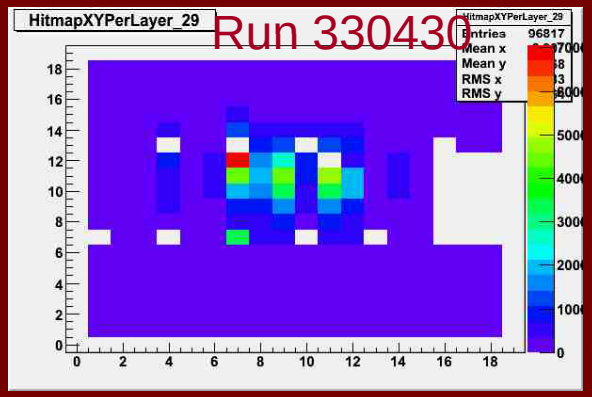
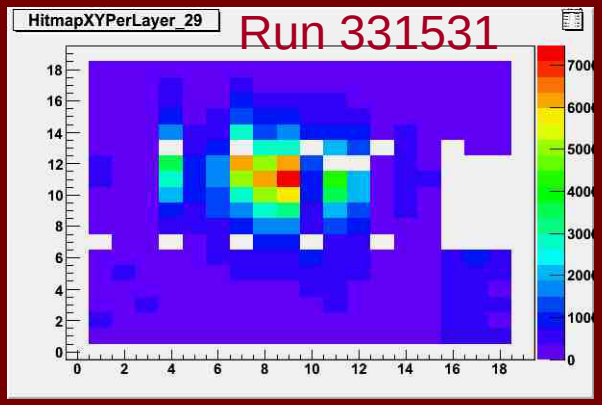
Problems due to the connectors (?)

- Can cause noise in several cells
- Typical structure that one chip is not connected
- In some cases is the access impossible due to limited space
- No guarantee by de- and replugging
- Read-out problems (?)





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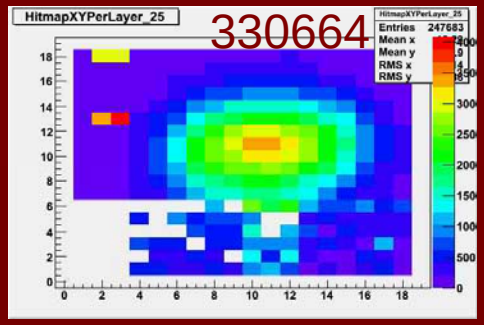
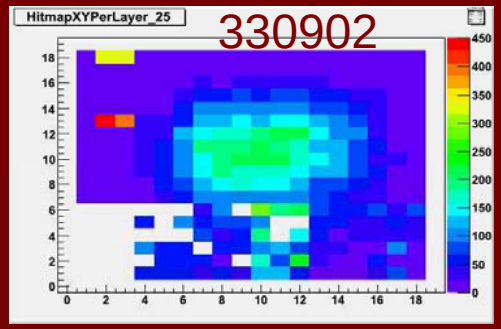
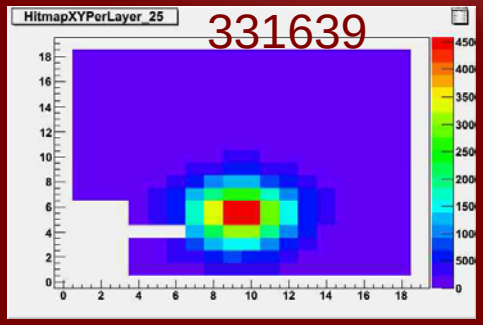
More bottom slabs

Layer 25







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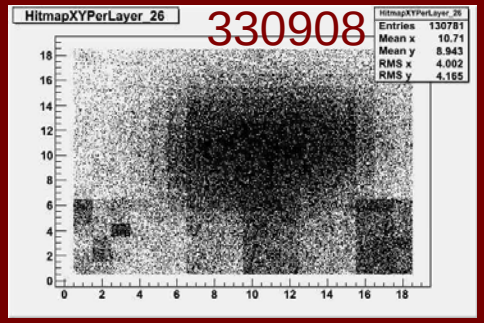

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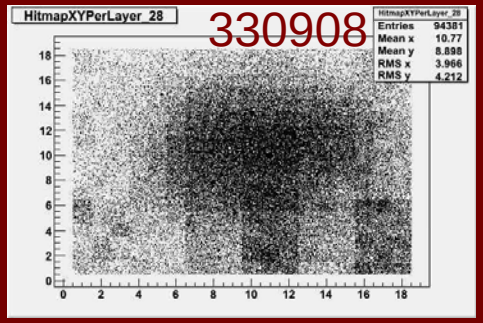

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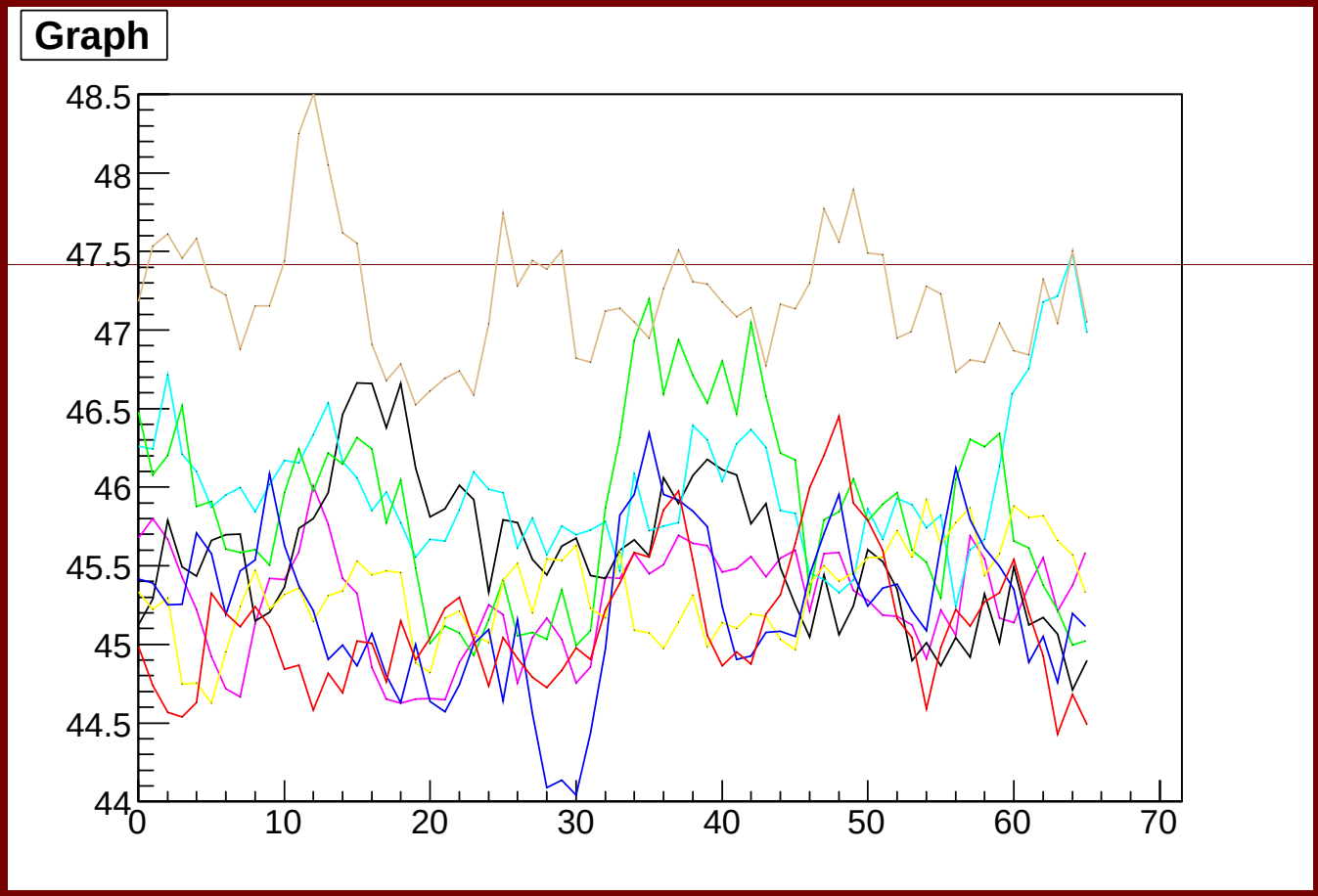

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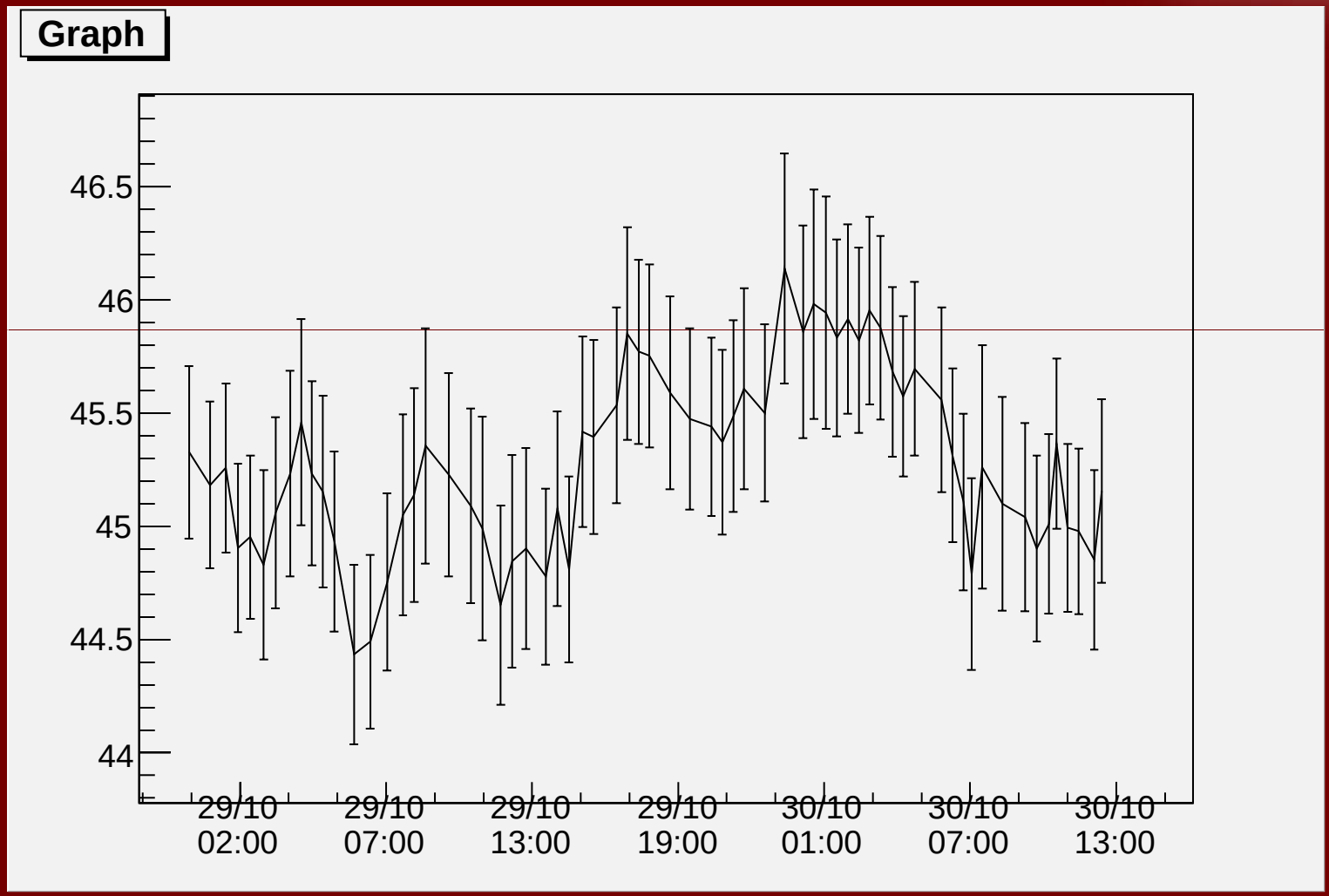

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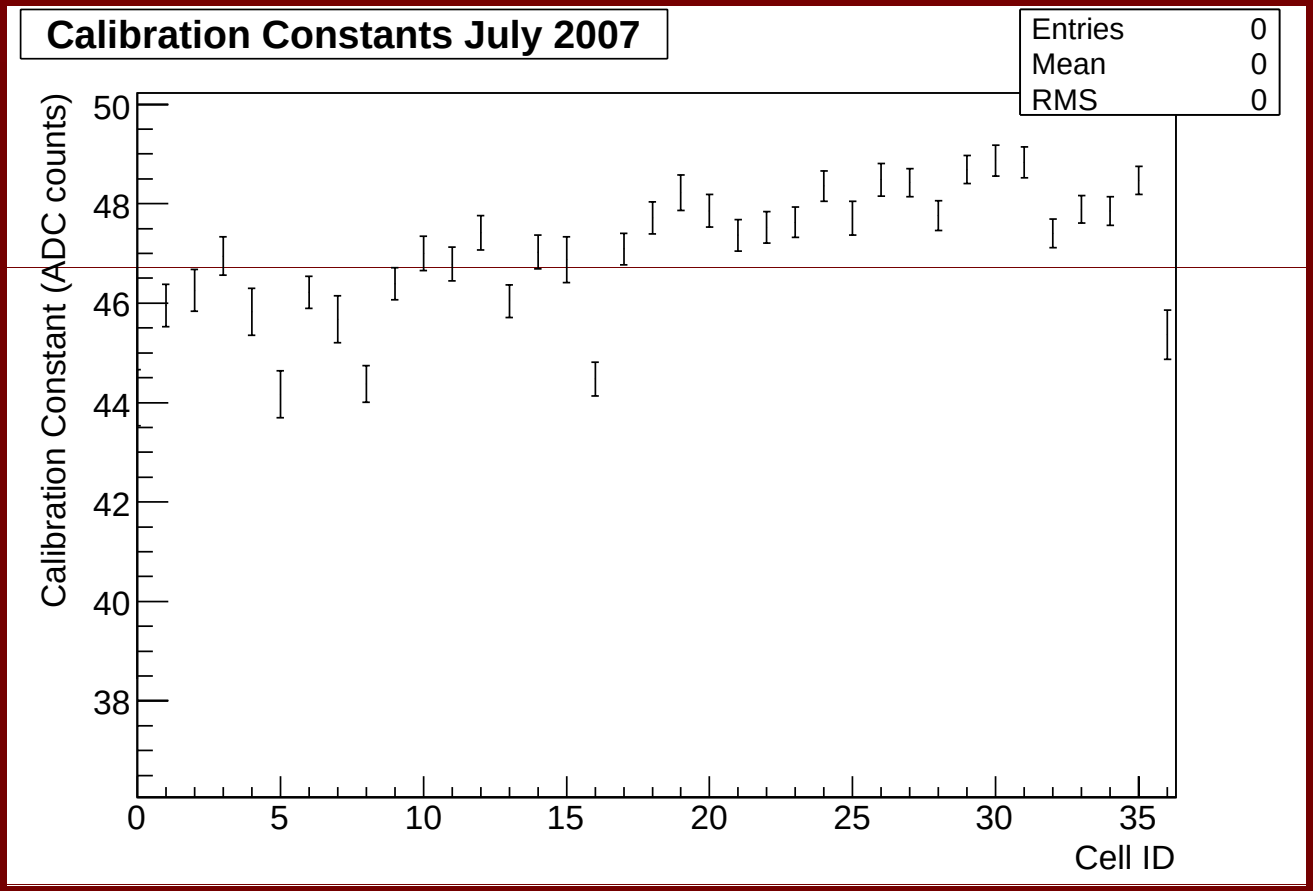

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