EDHCAL

- DHCAL project in Europe
- First results with the 4-hardroc board
- Outline

I.Laktineh

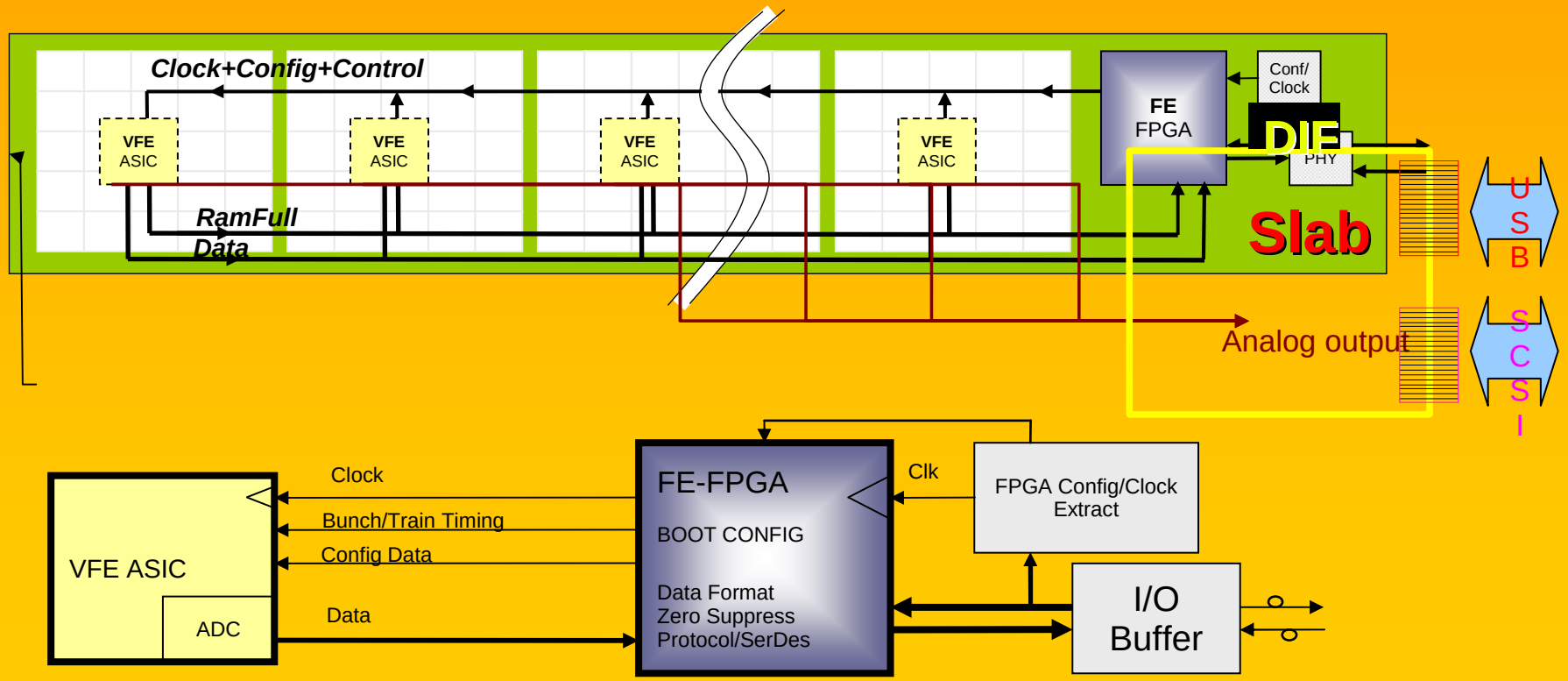
DHCAL project in Europe

Detectors : IHEP,IPNL,LAPP,SACLAY
Electronics : IPNL,LAL
Acquisition : IPNL,LAL,LAPP,LLR
Mechanics : CIEMAT,IPNL,LAPP,LLR
Simulation : IPNL,LLR
Coordination : IPNL

4-chip board

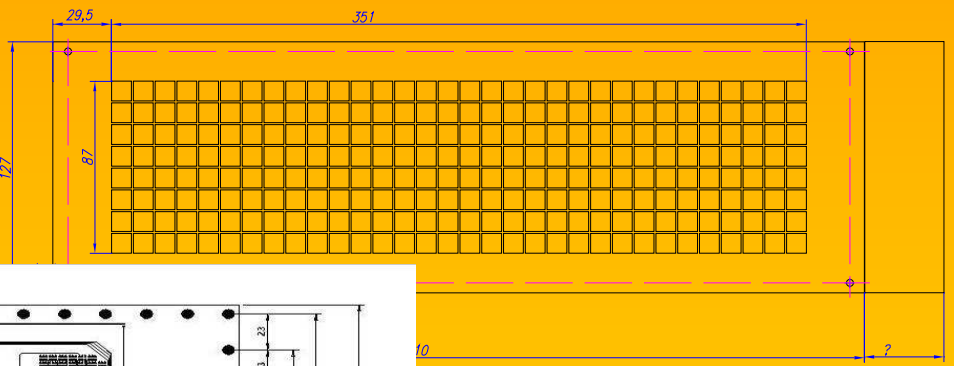
IPNL,LAL,LLR

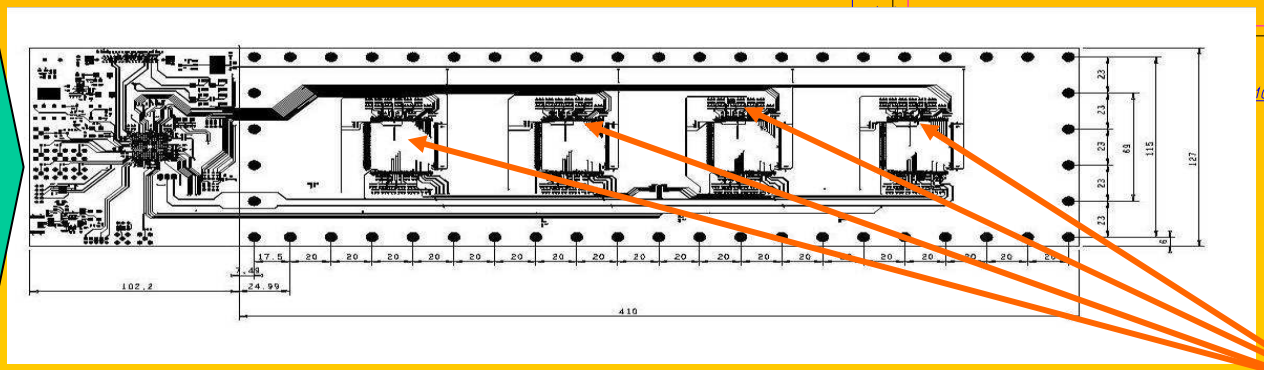
The board was conceived to test the new generation of semi-digital electronics on GRPC detectors

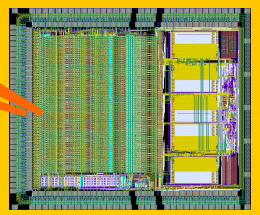


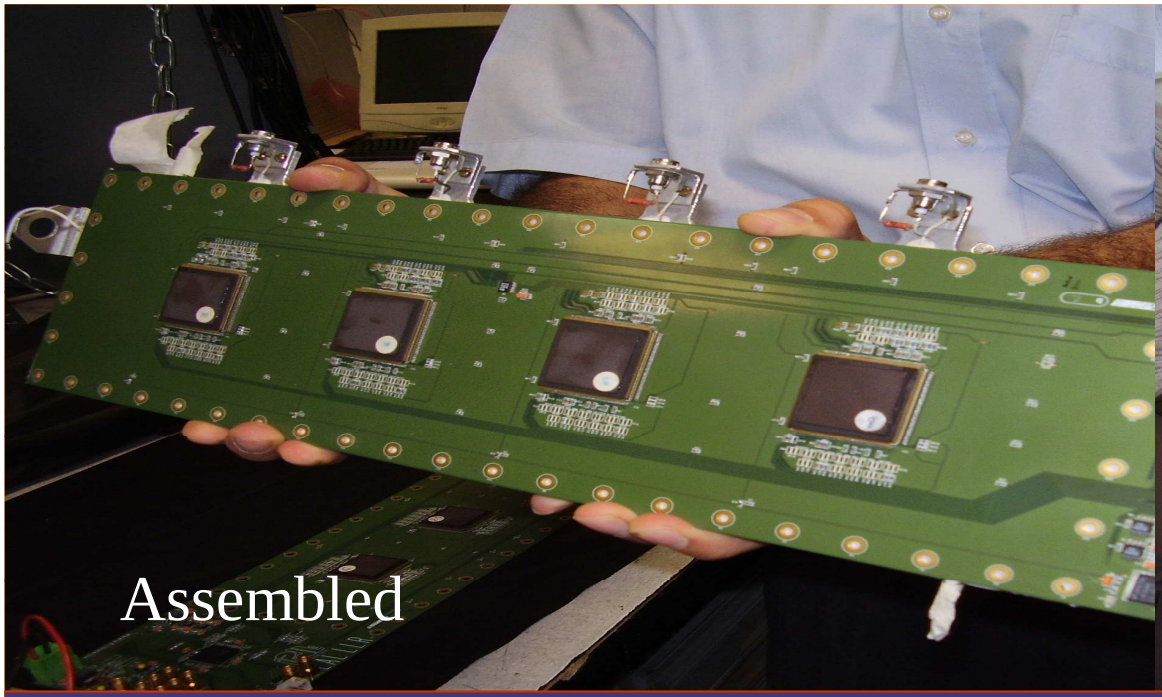
4-chip board

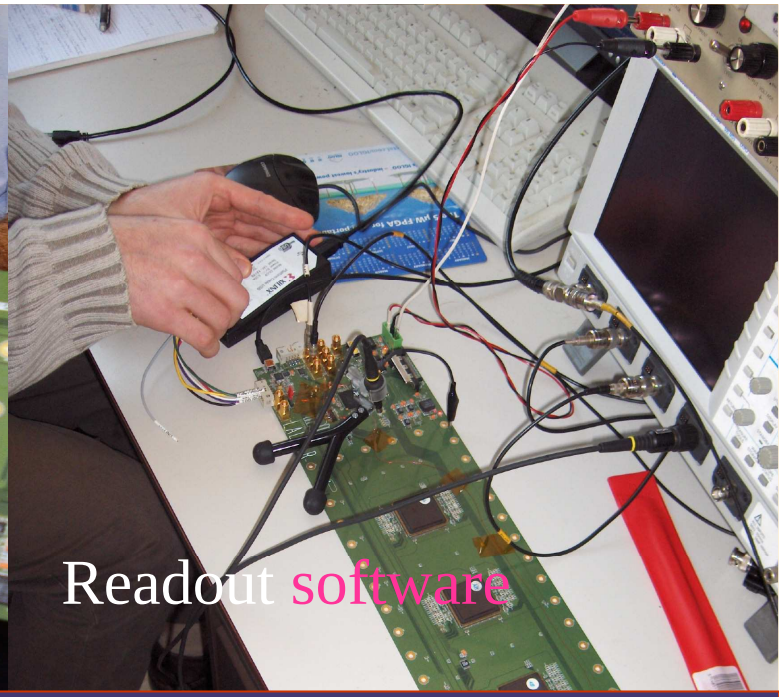
- **8X32 pads detector (GRPC and µMEGAS)**
- **8-layer PCB (IPNL)**:32X8 pads of 1 cm2 separated by 500 µ
- **4 HARDROC(LAL)**
- **Readout** USB + FPGA(LLR)

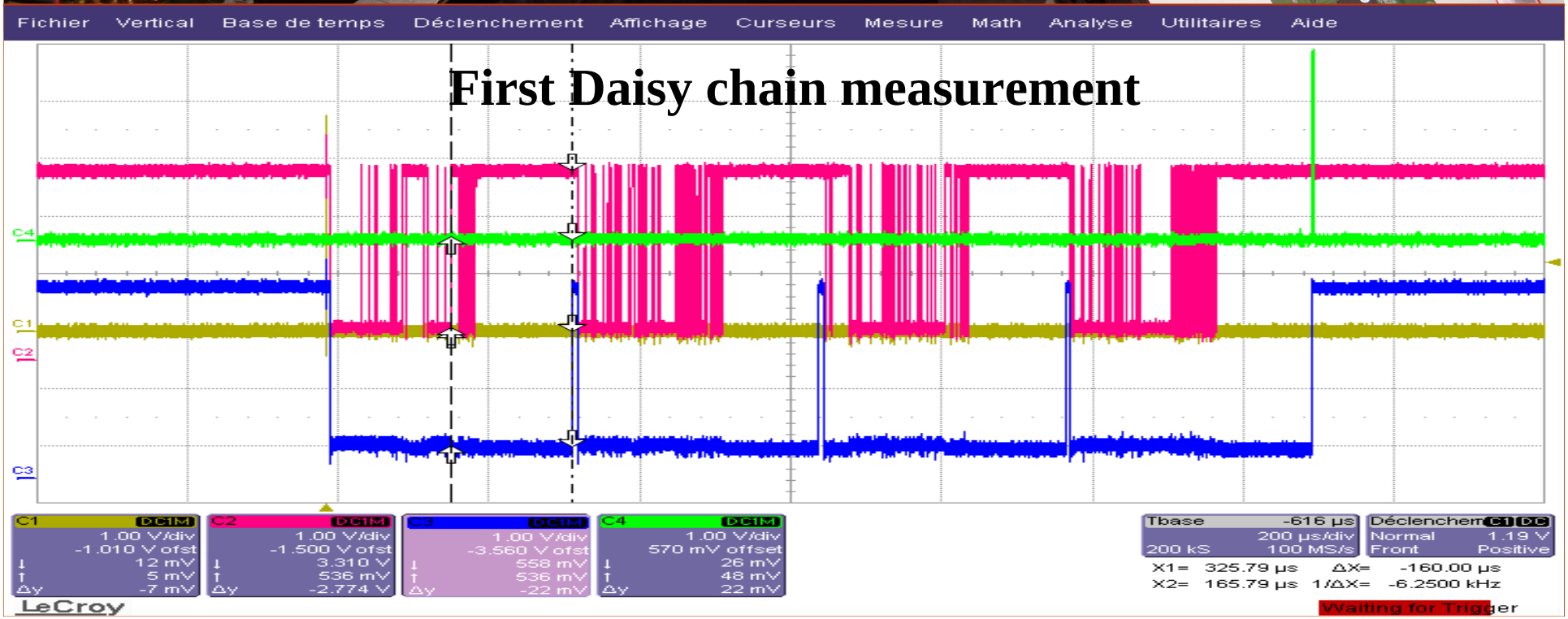







Assembled


Readout software

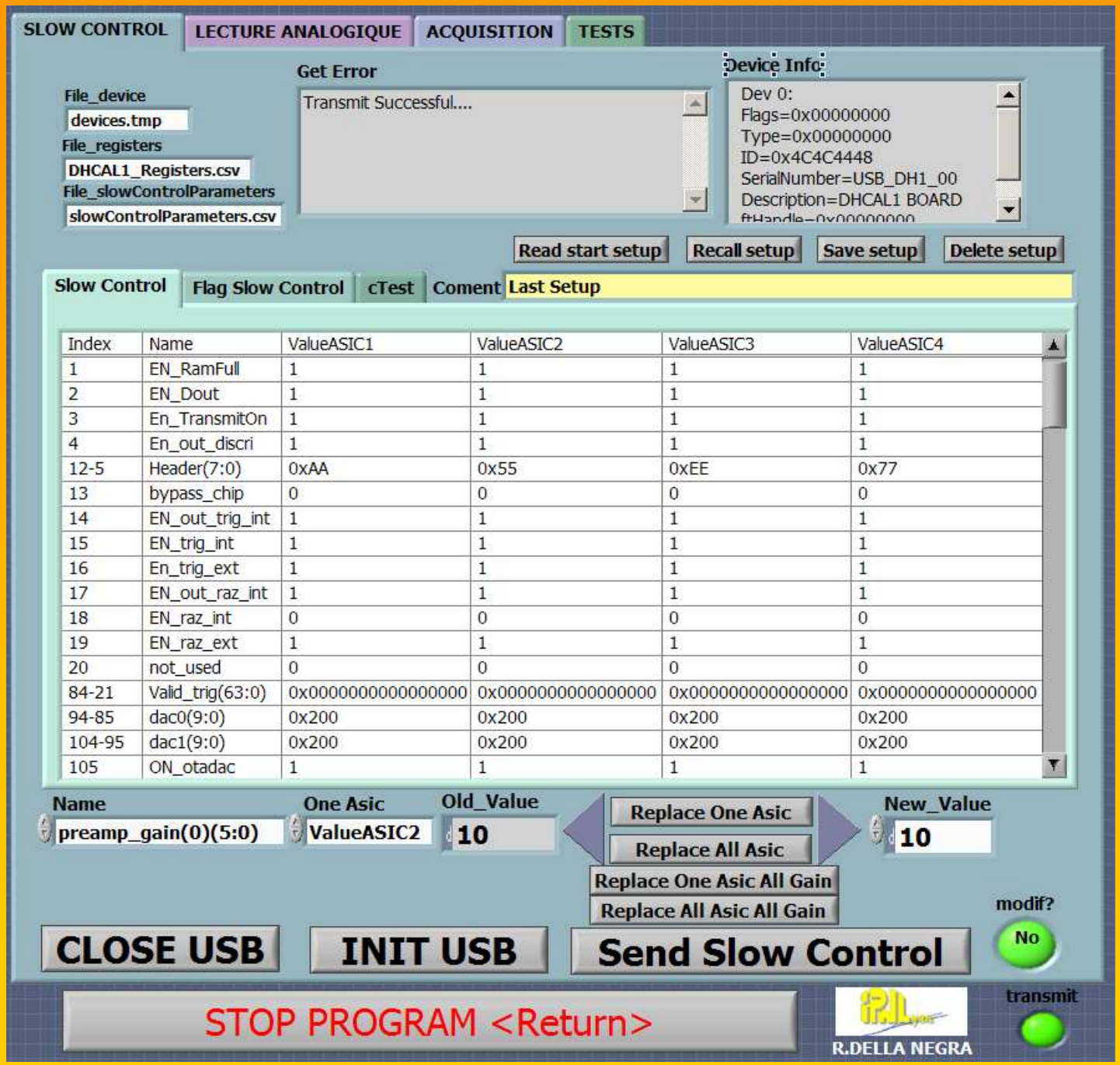

Fichier Vertical Base de temps Déclenchement Affichage Curseurs Mesure Math Analyse Utilitaires Aide
First Daisy chain measurement
C4
C1
C2
C3
C1 DC1M 1.00 V/div -1.010 V ofst 12 mV 5 mV -7 mV
C2 DC1M 1.00 V/div -1.500 V ofst 3.310 V 536 mV -2.774 V
C3 DC1M 1.00 V/div -3.560 V ofst 558 mV 536 mV -22 mV
C4 DC1M 1.00 V/div 570 mV offset 26 mV 48 mV 22 mV
Tbase -616 µs 200 µs/div 200 kS 100 MS/s
Déclenchem C1 DC Normal 1.19 V Front Positive
X1= 325.79 µs ΔX= -160.00 µs
X2= 165.79 µs 1/ΔX= -6.2500 kHz
LeCroy
Waiting for Trigger

4-chip board

Readout system (LLR):

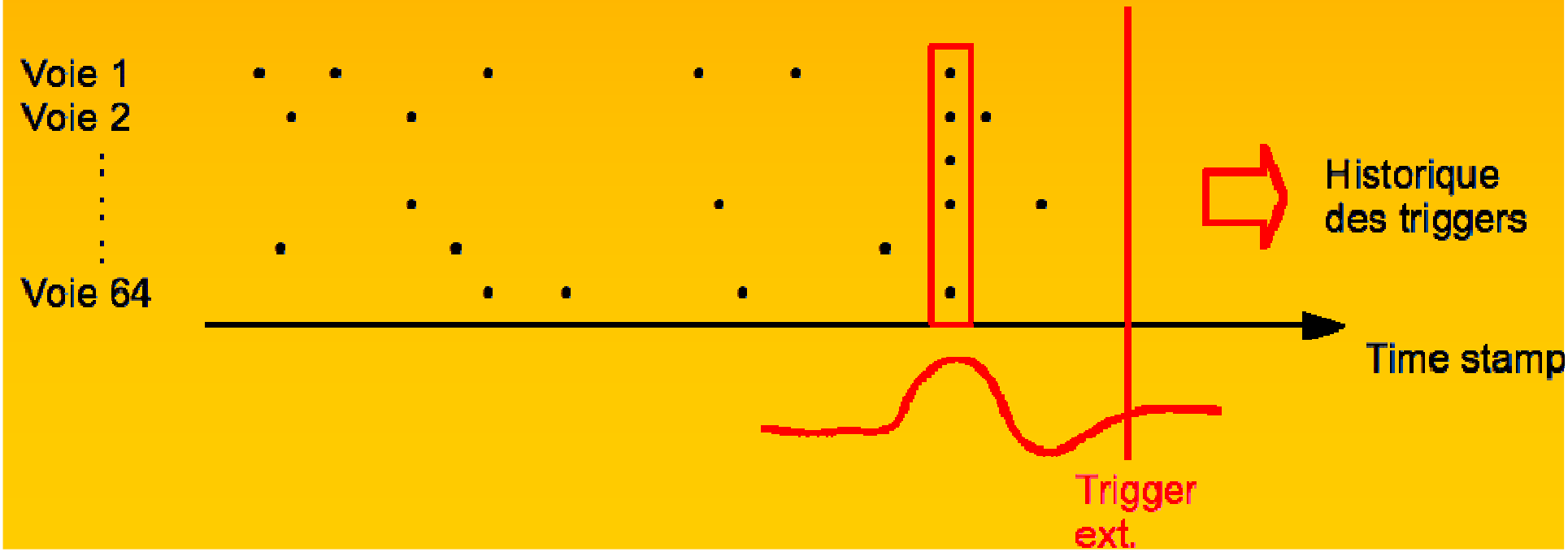
Firmware + Software (interface library) were developed to allow charging the slow control parameters from file/flux and controlling the procedure.

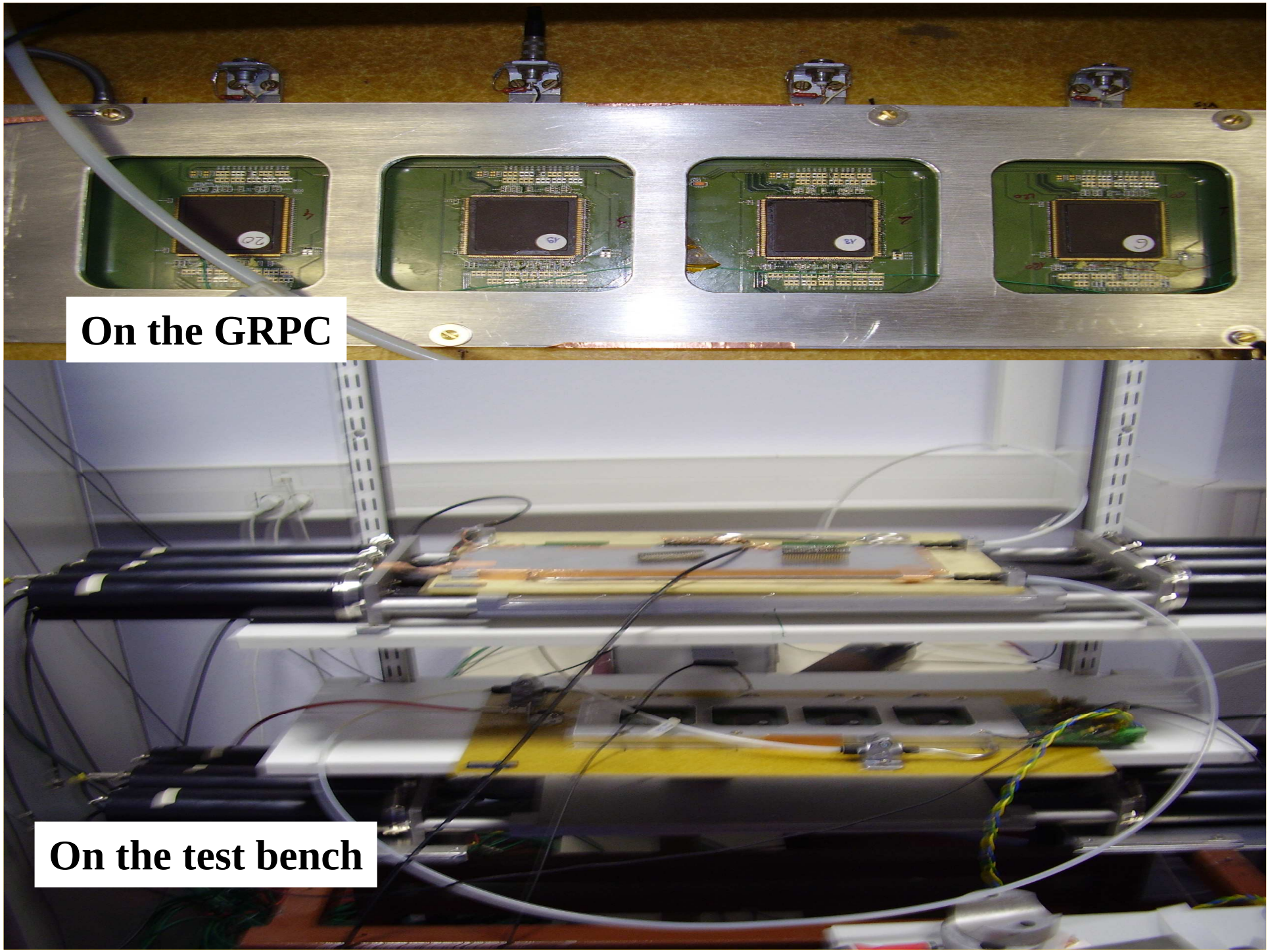
Acquisition modes : different modes are allowed:
a) Internal triggers
b)External triggers : cosmics & test beam
Data output: The two kinds of data output of the hardroc chips are accessible: digital and analogue
Friendly labview based system was developed(IPNL)


SLOW CONTROL
LECTURE ANALOGIQUE
ACQUISITION
TESTS
Get Error
Transmit Successful....
Device Info
Dev 0:
Flags=0x00000000
Type=0x00000000
ID=0x4C4C4448
SerialNumber=USB_DH1_00
Description=DHCAL1 BOARD
File_device
devices.tmp
File_registers
DHCAL1_Registers.csv
File_slowControlParameters
slowControlParameters.csv
Read start setup
Recall setup
Save setup
Delete setup
Slow Control
Flag Slow Control
cTest
Coment
Last Setup
Index Name ValueASIC1 ValueASIC2 ValueASIC3 ValueASIC4
1 EN_RamFull 1 1 1 1
2 EN_Dout 1 1 1 1
3 En_TransmitOn 1 1 1 1
4 En_out_discri 1 1 1 1
12-5 Header(7:0) 0xAA 0x55 0xEE 0x77
13 bypass_chip 0 0 0 0
14 EN_out_trig_int 1 1 1 1
15 EN_trig_int 1 1 1 1
16 En_trig_ext 1 1 1 1
17 EN_out_raz_int 1 1 1 1
18 EN_raz_int 0 0 0 0
19 EN_raz_ext 1 1 1 1
20 not_used 0 0 0 0
84-21 Valid_trig(63:0) 0x0000000000000000 0x0000000000000000 0x0000000000000000 0x0000000000000000
94-85 dac0(9:0) 0x200 0x200 0x200 0x200
104-95 dac1(9:0) 0x200 0x200 0x200 0x200
105 ON_otadac 1 1 1 1
Name
preamp_gain(0)(5:0)
One Asic
ValueASIC2
Old_Value
10
Replace One Asic
Replace All Asic
Replace One Asic All Gain
Replace All Asic All Gain
New_Value
10
modif?
No
CLOSE USB
INIT USB
Send Slow Control
STOP PROGRAM <Return>
R.DELLA NEGRA
transmit

First results

The whole system was tested using **cosmics**.
PMs system provides the external trigger
The **chip memory is then damped and read**.
The time difference between the external trigger
and the GRPC signal is known with precision of **±25 ns**
(readout clock period)




On the GRPC
On the test bench

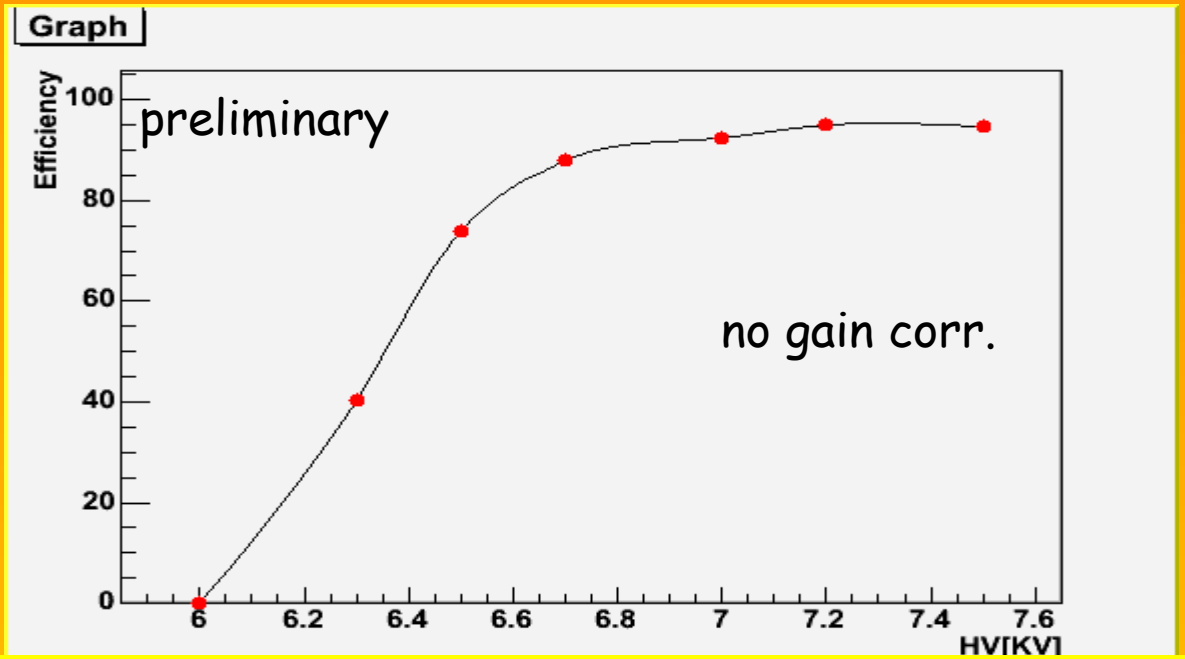
Second threshold

First threshold

Example of a recorded mip

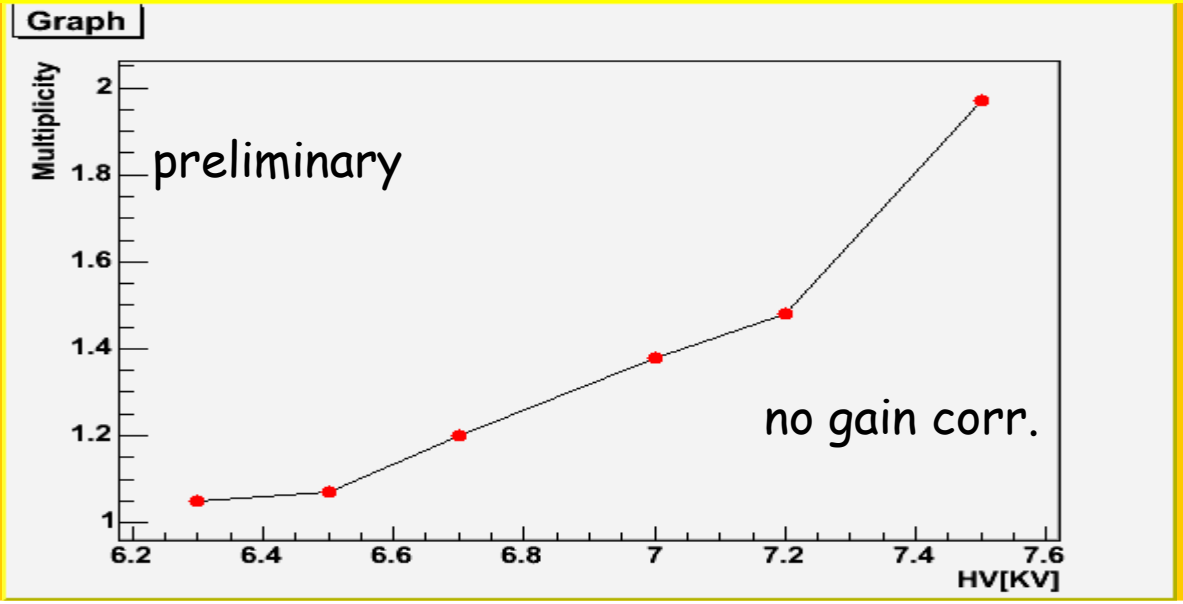
First results

GRPC-IHEP
32X8 pads



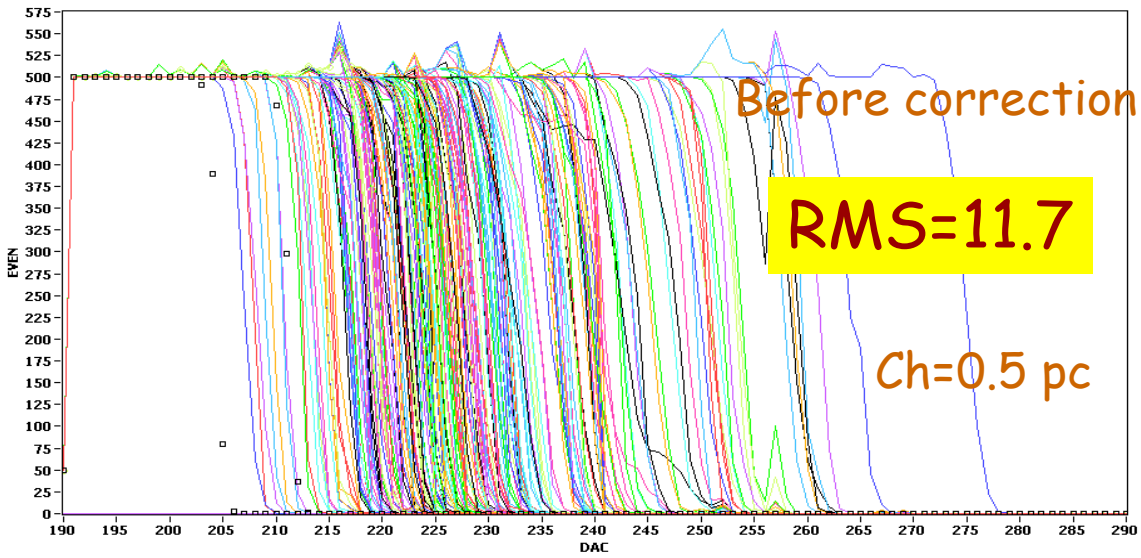
TFE 93%
Isobutene 5%
SF6 2%

Threshold= 190 DAQ.U ≈ 100 fc



Ongoing

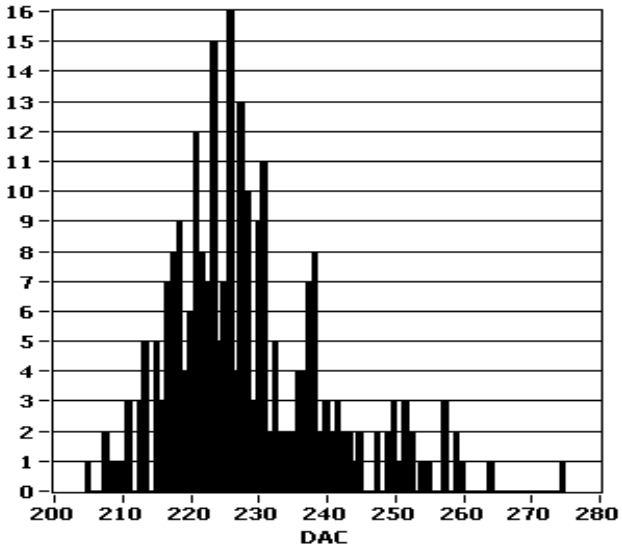
Gain correction by injecting known charges throw internal capacitors

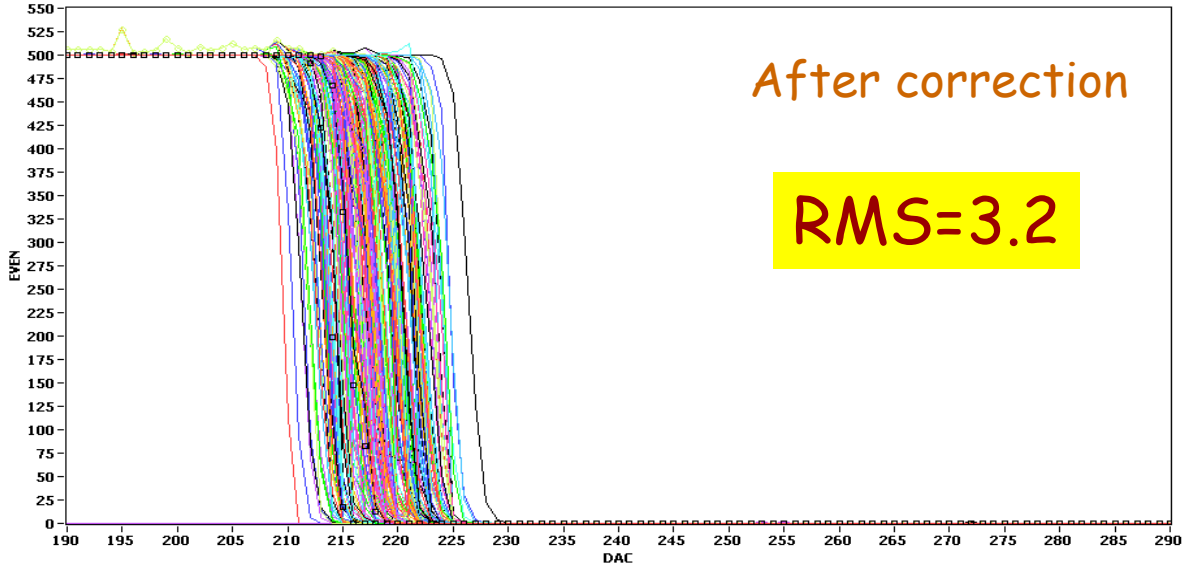


Before correction

RMS=11.7

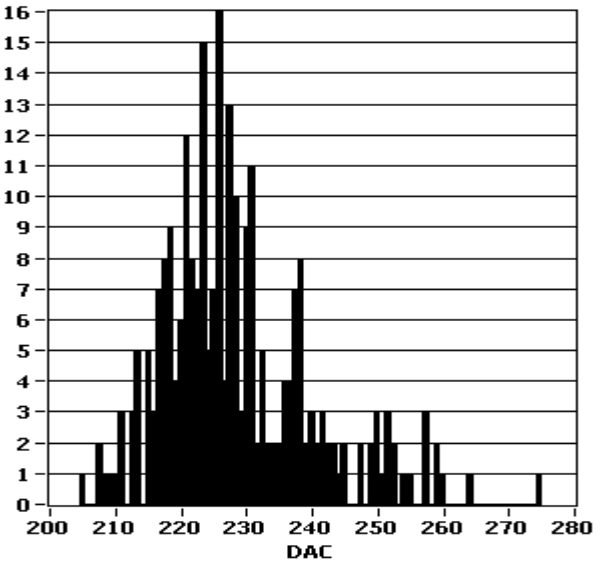
Ch=0.5 pc





After correction

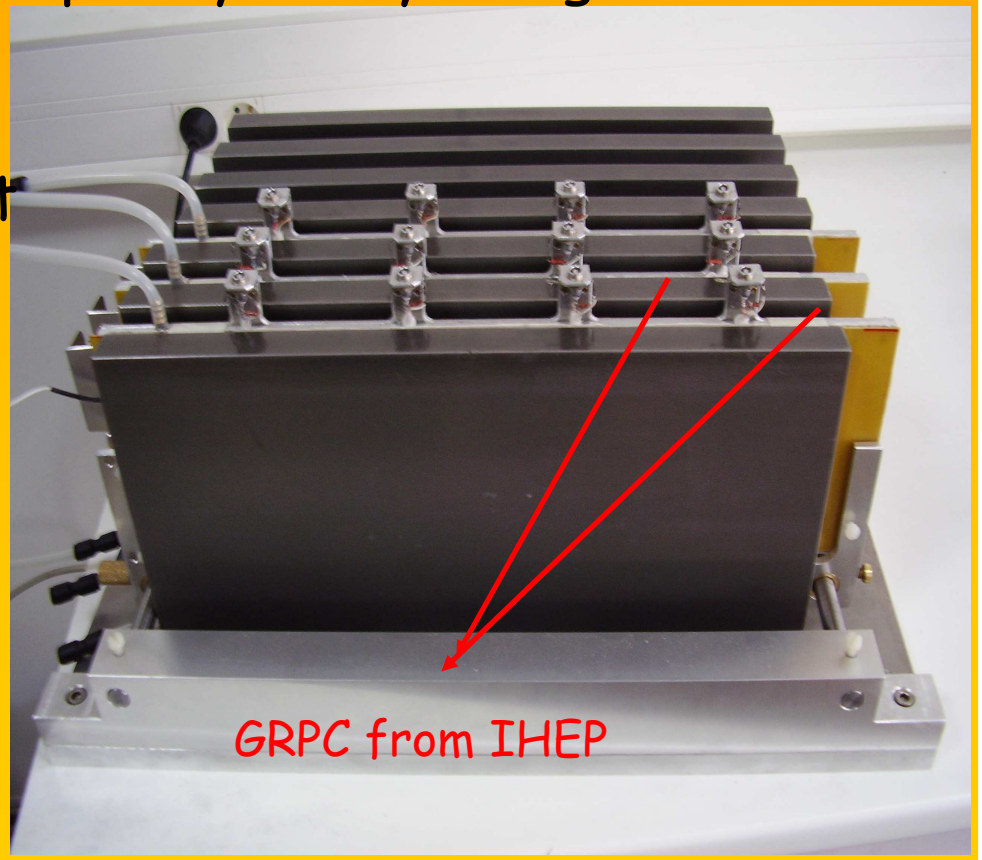
RMS=3.2



Next to come

- Complete the gain correction to have the smallest dispersion of S-curves at the threshold
- Complete the efficiency% multiplicity study using cosmics for the others GRPC
- Use cosmics for the slice test
- Go to beam test

N.B : The analog readout is almost completed and will be used to improve on the threshold selection



Preparation for the 1 m^2

Four aspects are under development :

- Detector performance :

  development is going on for GRPC(IHEP,IPNL)

  and for µMEGAS(LAPP)
- Asics (LAL,IPNL) to extend the hardroc capacities and performance.
- Electronics connection

  Study is going on for GRPC(CIEMAT,IPNL)

  and µMEGAS(LAPP)
- Readout (LLR,LAPP,IPNL) : DIF, Data concentrator and software.

OUTLINE

The European DHCAL concept: detector +electronics+ readout is now a reality and it works.

Preliminary results are very satisfactory and improvement is going on.

Ready for the slice test on beam

The 1m2 GRPC project is on progress. Improvement on the detector design in collaboration with IHEP. Hopefully ready before fall 2008.
The μMEGAS 1m2 project is well advanced. Hopefully in the first part of 2008.

The technical prototype is scheduled for 2009-2010
Budget : ANR+ IN2P3 OK