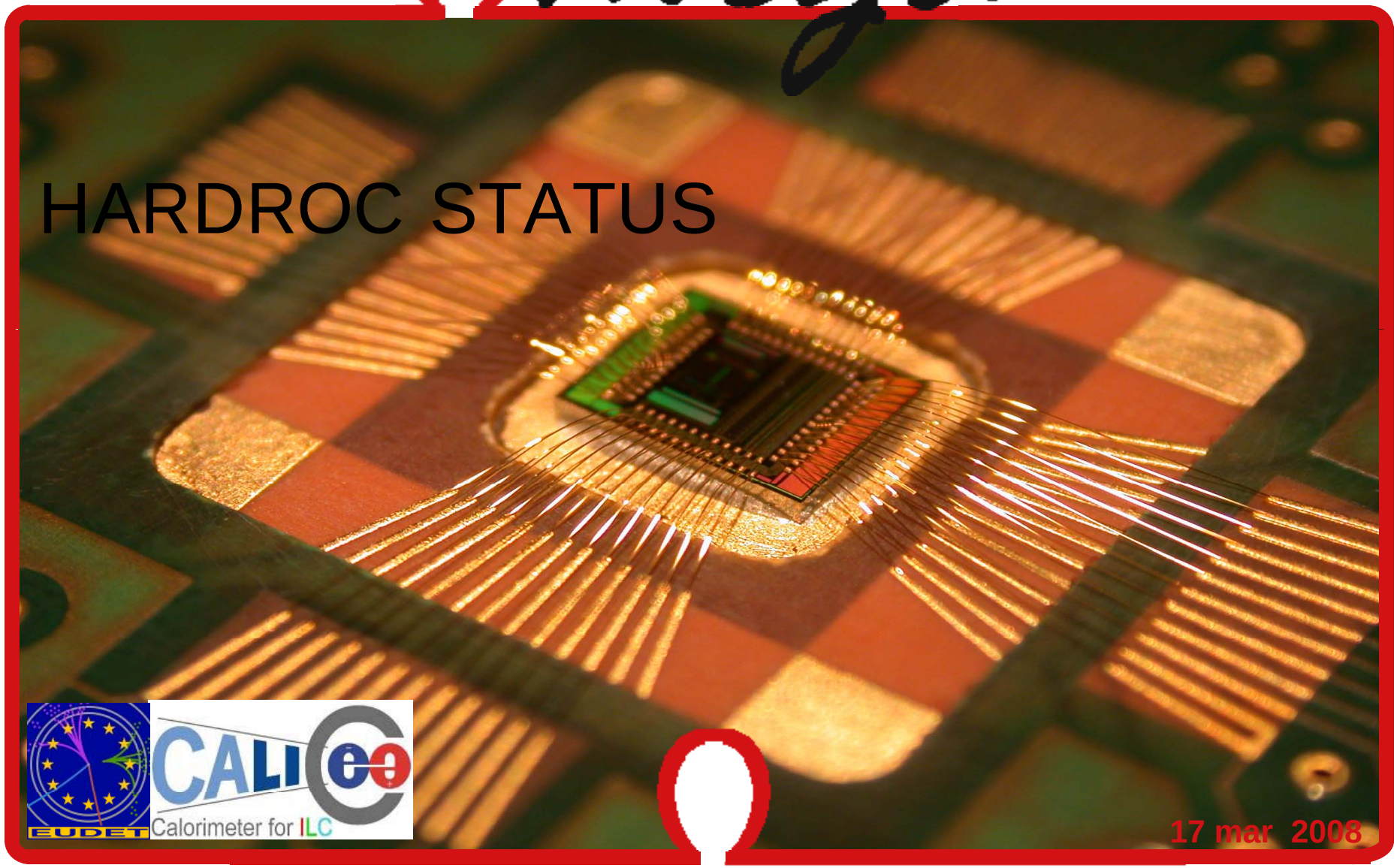
IN2P3

Omega

CAC LAL IPN Orsay

HARDROC STATUS



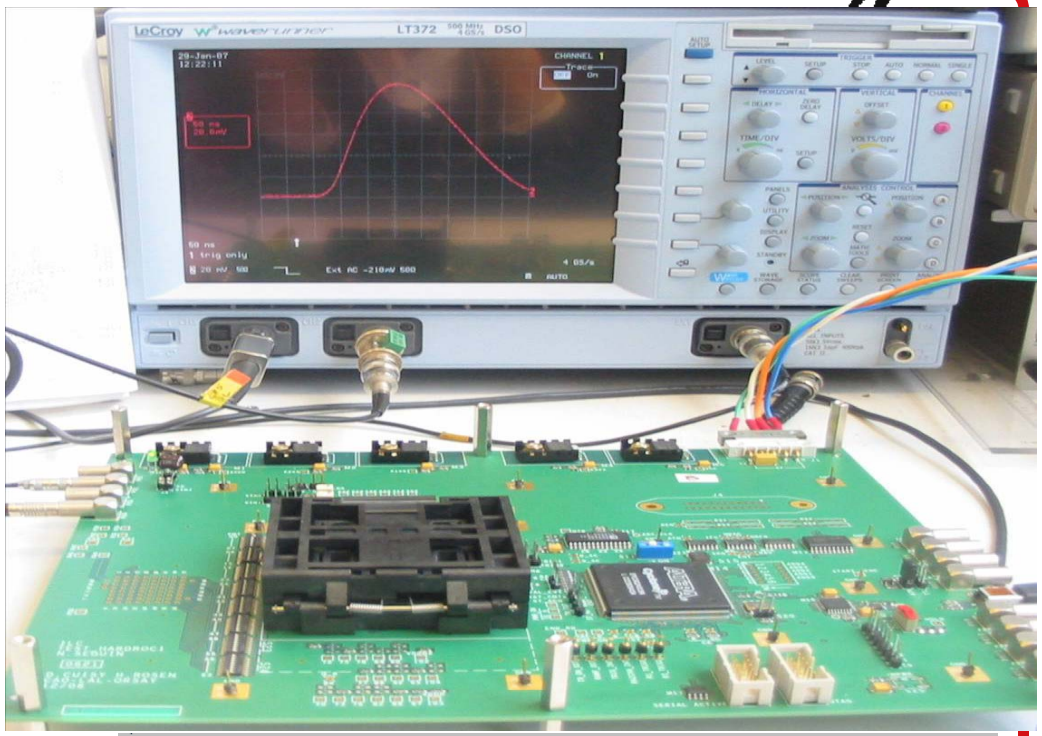
CALICE Calorimeter for ILC

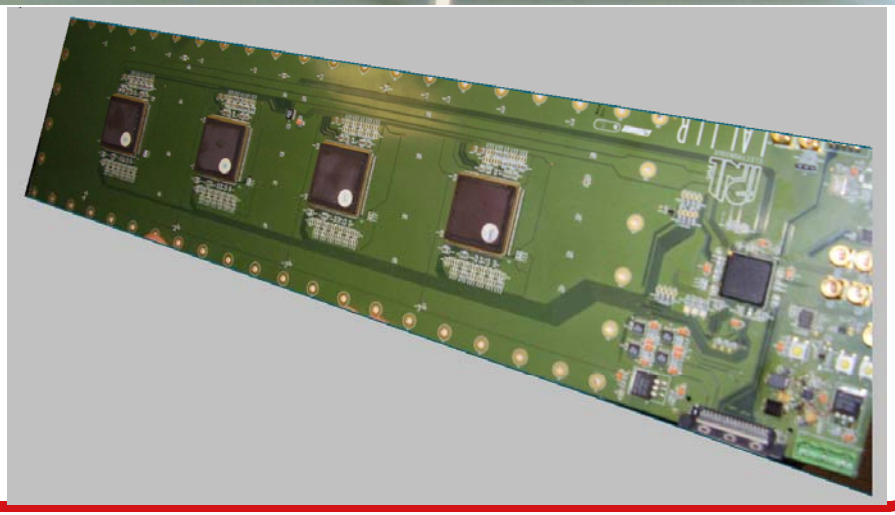
17 mar 2008

Orsay MicroElectronic Group Associated

PLAN

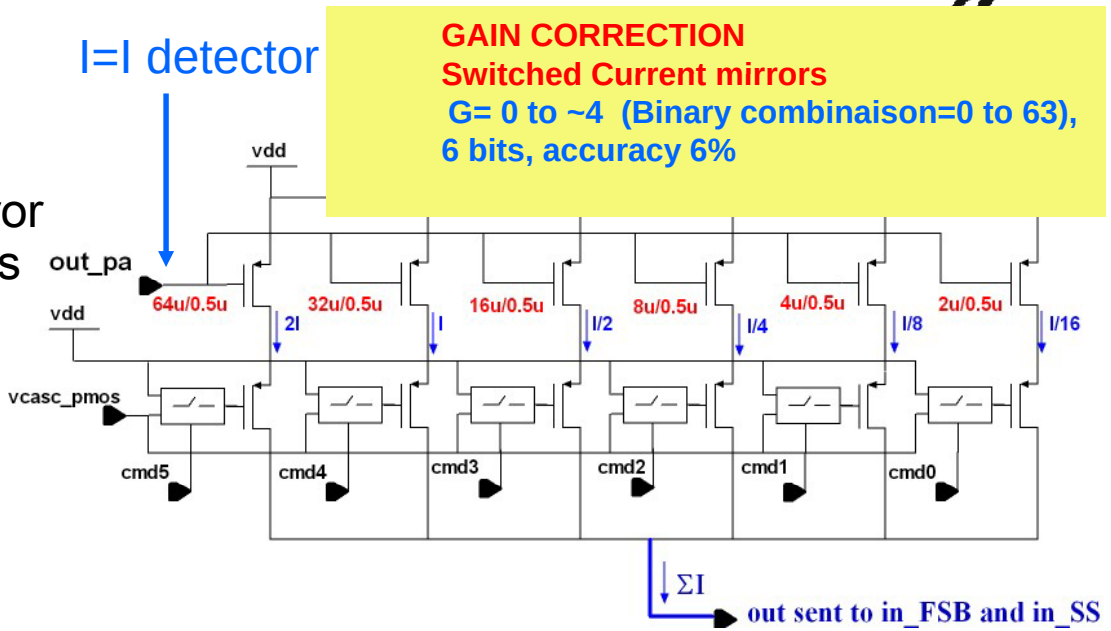
- Summary of measurements performed on HARDROC1
  - FE Asic designed for GRPC or Micromegas detector forseen for the European DHCAL
  - HARDROC1 extensively measured since December 06
- Forseen modifications of HARDROC1= HARDROC2
- Packaging for Hardroc2
- HV protection

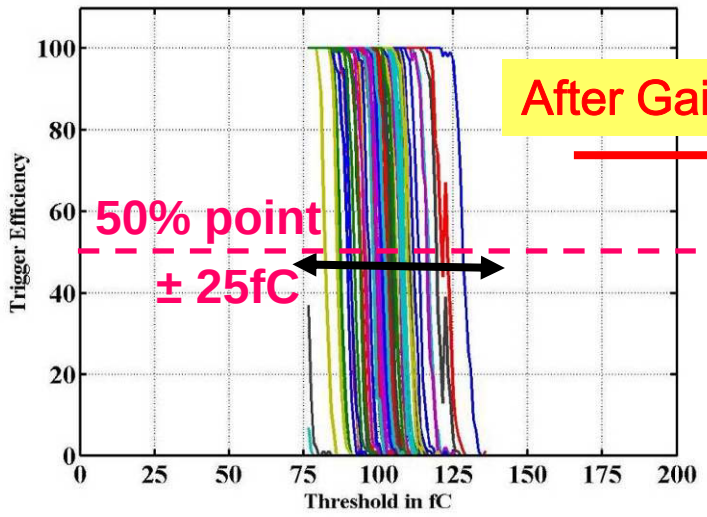




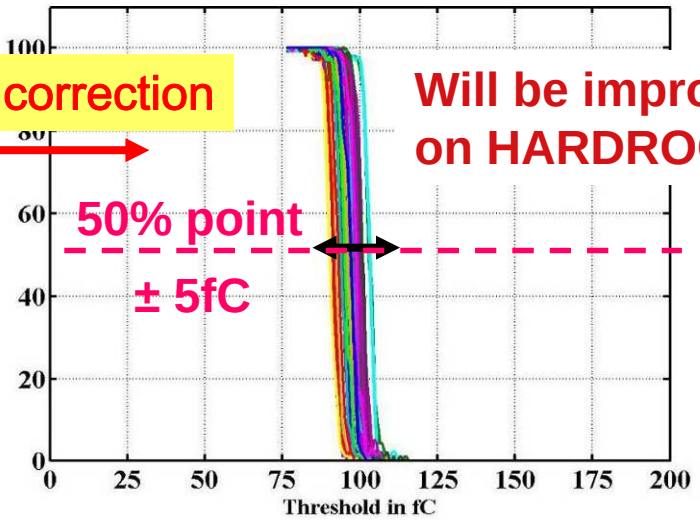
Scurves of the 64 channels : 100fC

- Charge injected in each channel: 100fC
  - non uniformity quite large (±25%) due to current mirror mismatch (small transistors to optimise speed at low current)
  - Can be compensated by tuning the gain of each channel





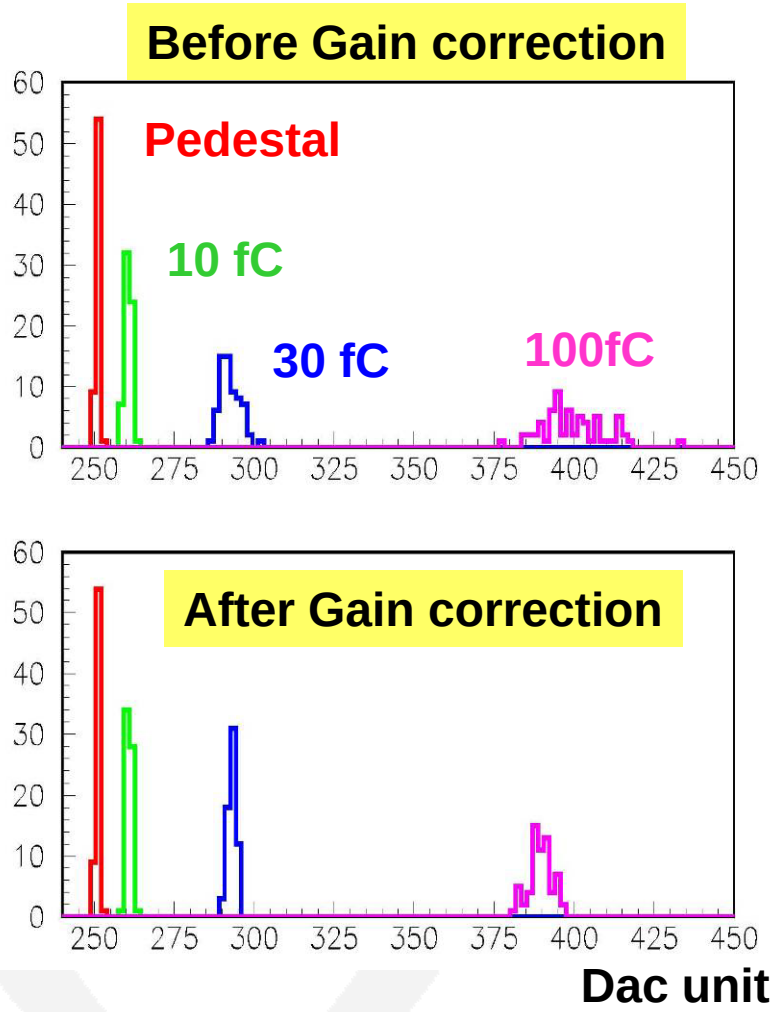
After Gain correction

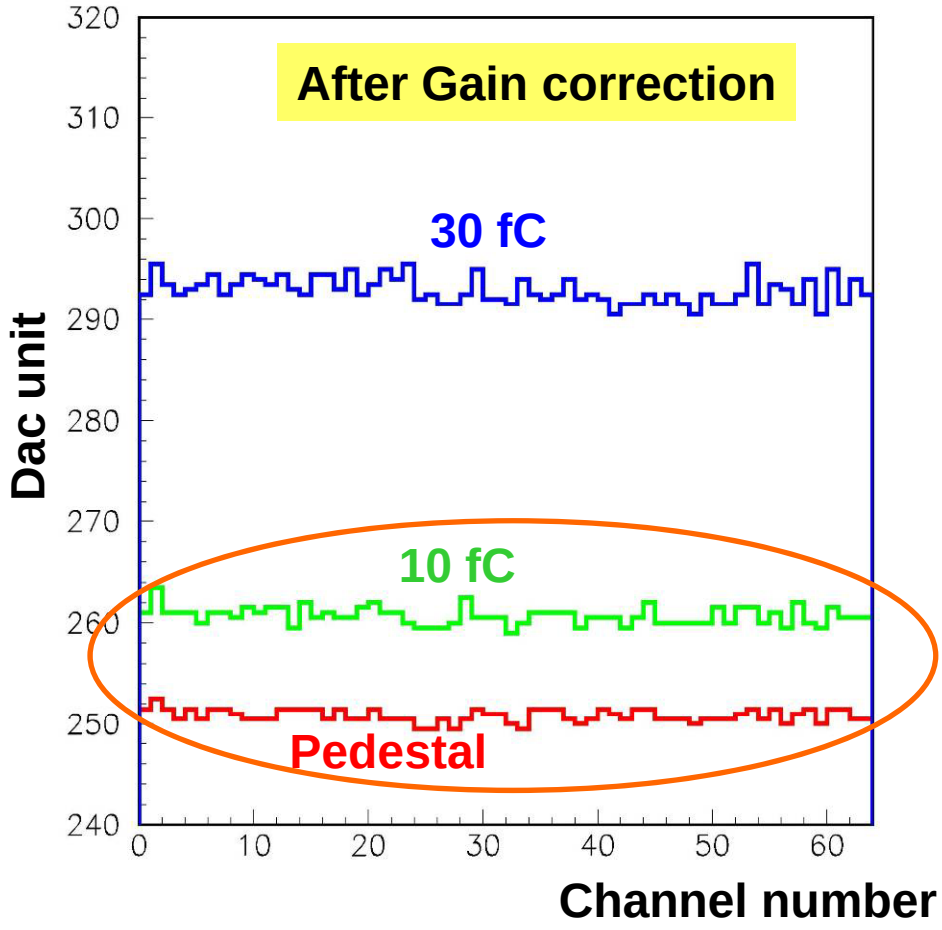


Will be improved on HARDROC2

Scurves of the 64 channels:10,30 and 100fC

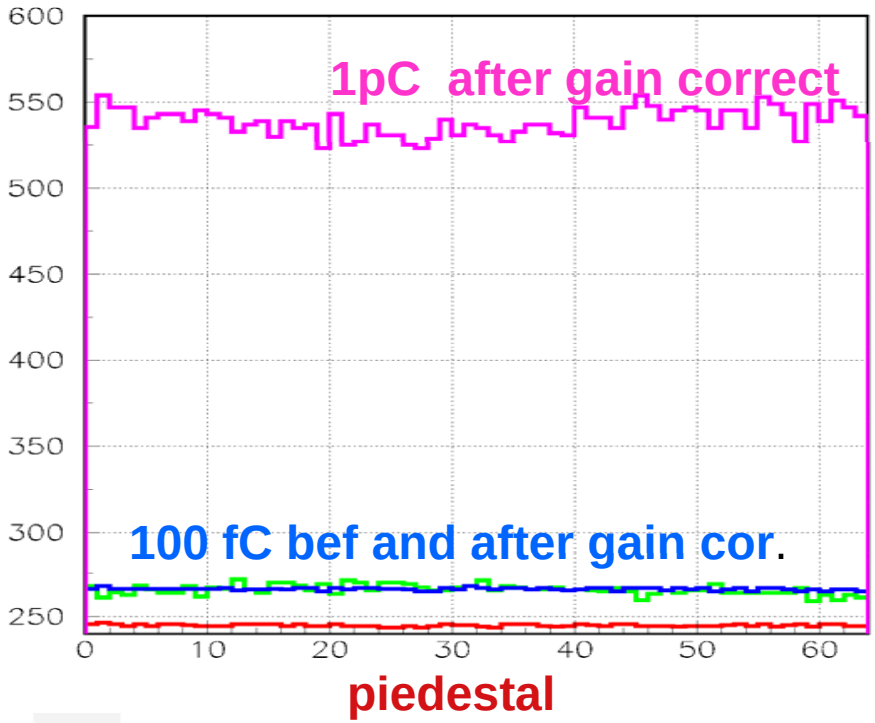
Plot of the 50% efficiency point for 10, 30 and 100fC (µMegas config.)





Scurves of the 64 channels: 100fC, 1pC

- RPC configuration:
  - Bipolar FAST SHAPER: ALL the Rf and Cf ON => SMALLEST GAIN

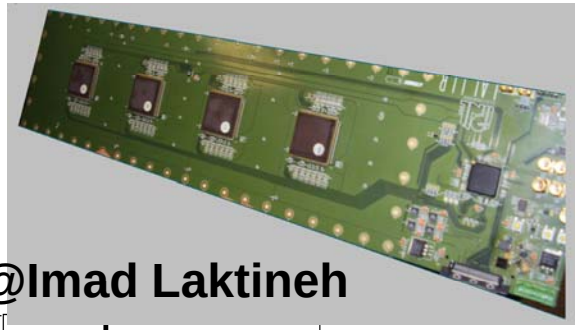


- Gain correction performed at Qinj=100fC:
  - Bef: σ=2.8/(265-240)=11%
  - After: σ=0.7/(265-240)=3%
- Same correction for Qinj=1pC
  - σ=7.7/(538-240)=3.5%

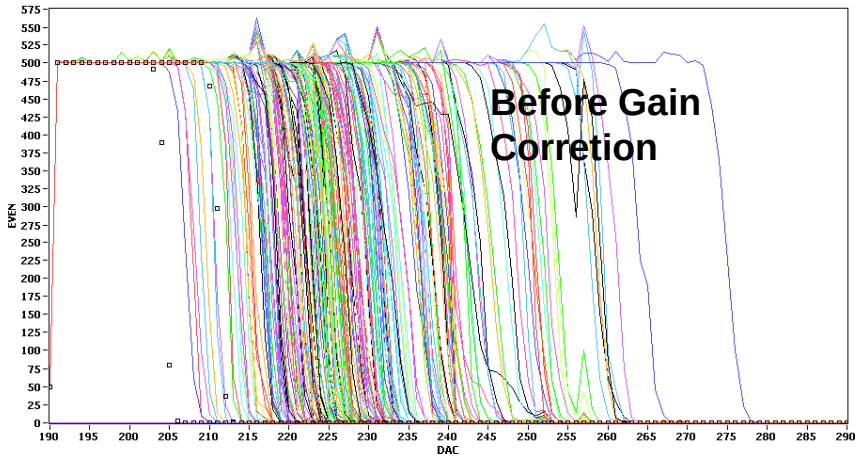
GAIN CORRECTION:
Will be improved in Hardroc2
(accuracy +range)

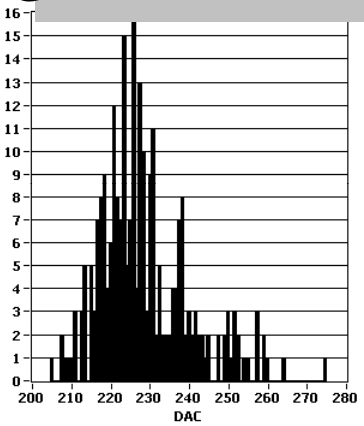
PCB with 4 HARDROC: Scurves

ALL ASIC, ALL CHANEL= 256 channels
G12
Qinj=500 fC

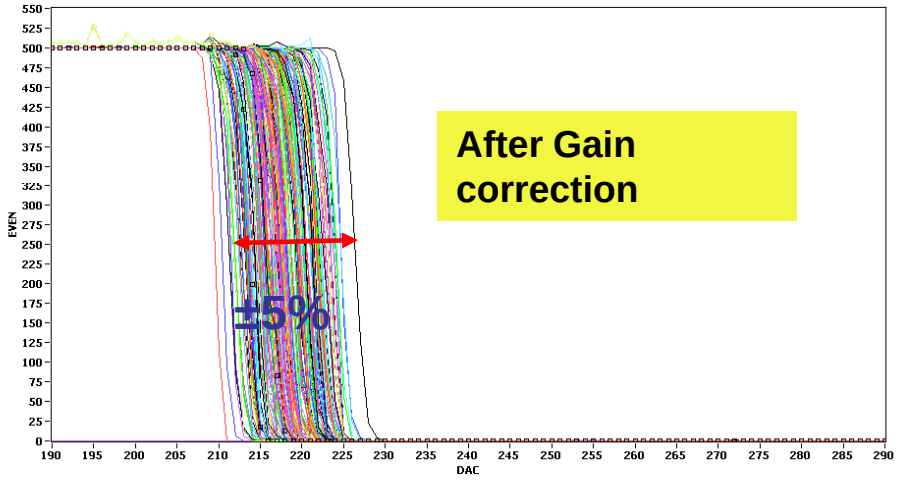


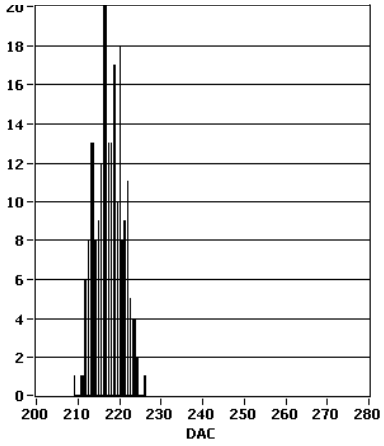
@Imad Laktineh





MEAN=228.21
RMS=11.66





MEAN=217.53
RMS=3.2

Summary of the measurements

- **Auto trigger with Qinj=10fC:**
  - **Qinj=10fC in Ch7**
  - **Vth0 and Vth1~5fC**

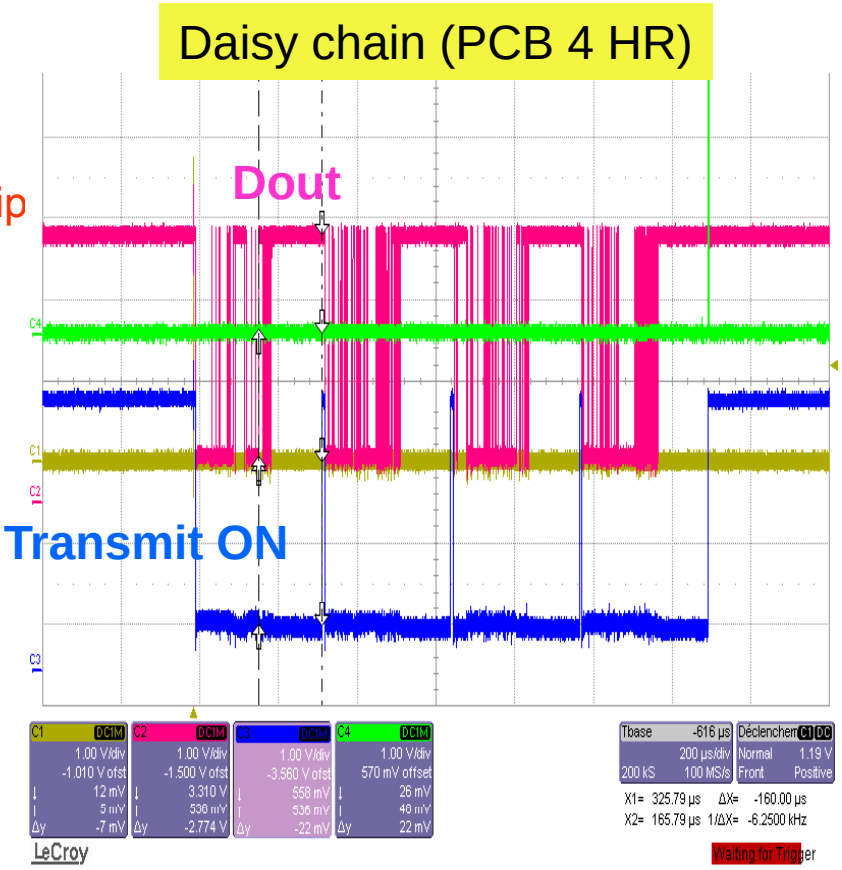
- **Auto trigger without signal:**
  - **Thresholds can be set down to a few fC without any autotrigger, despite the digital noise**
  - **Random counting< 1Hz/chip**

- POWER PULSING
  - TARGET: 10 µW/ channel with 0.5% duty cycle=> 640µW/3.5V=180 µA for the entire chip
  - Measurement: 125 µA for the entire chip
  - 1 bug (easy to fix): Bandgap V not power pulsed
  - PP of the analog part: (Injection of 100fC, Threshold= 30fC)

  => Awake time= 2 µs (All decoupling capacitors removed)
  - Power pulsing of the DAC:

  => 25 µs (slew rate limited)

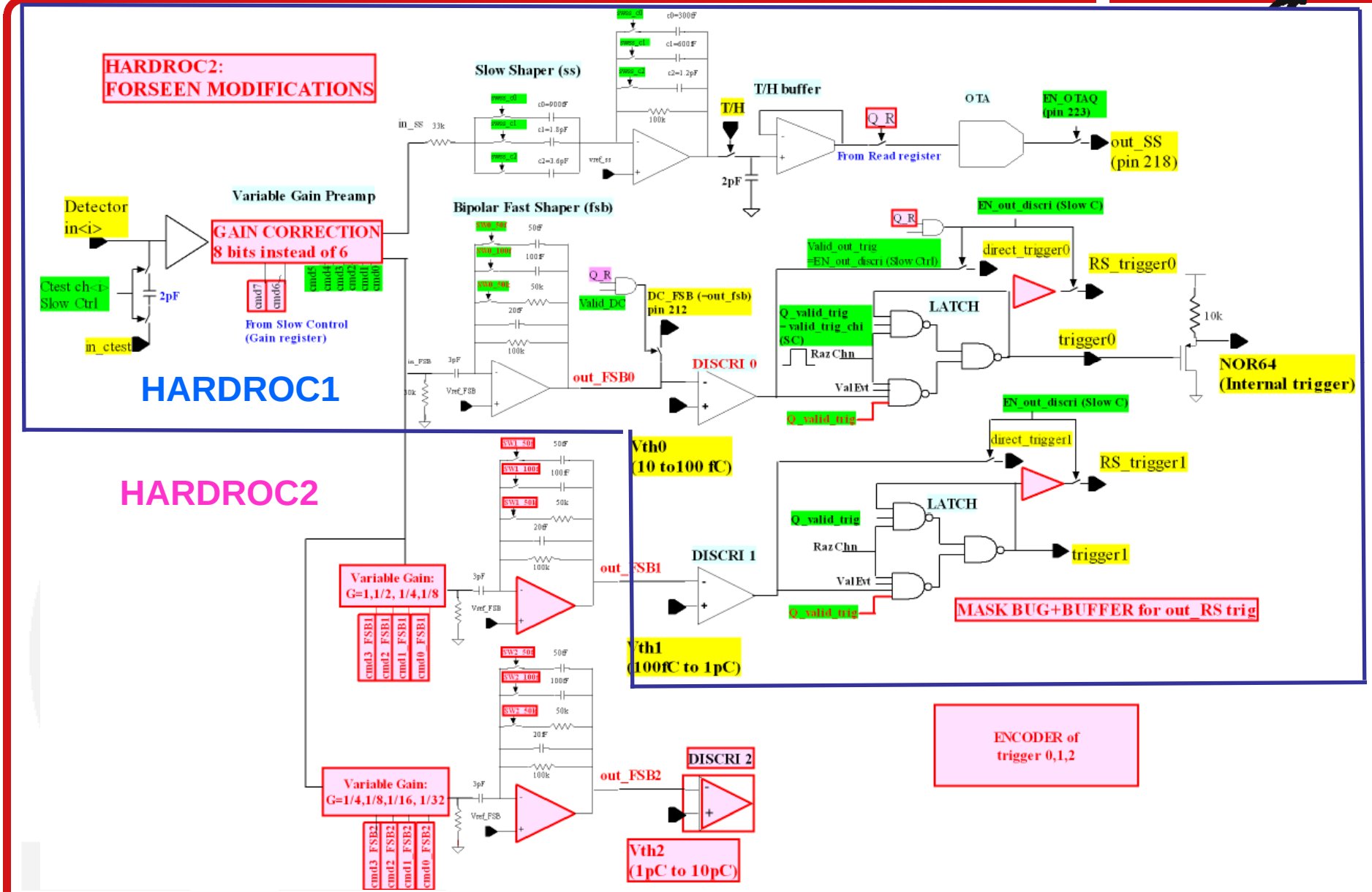
- **Daisy chain of 4 Hardroc: PCB 4 Hardrocs** (see Imad's talk in the DHCAL session)



HARDROC2 :

- Bugs correction:
  - mask, memory pointer: dummy frame, power pulsing of the Bandgap, reference voltages…
- Dynamic range extension
  - Gain correction: 8 bits instead of 6 (G=0 to 2, accuracy=0.8%)
  - 3 shapers and 3 thresholds very far apart (1,10,100):
    - Vth=10 fC, 100fC, 1pC (megas)
    - Vth= 100fC, 1pC, 10pC (RPC)
- DAC absolute accuracy can be improved (~10 mV from chip to chip)
- HARDROC2= HARDROC1 + modifs
  ⇒ HARDROC1= BACKUP
- Will be submitted in June 08, MPW run

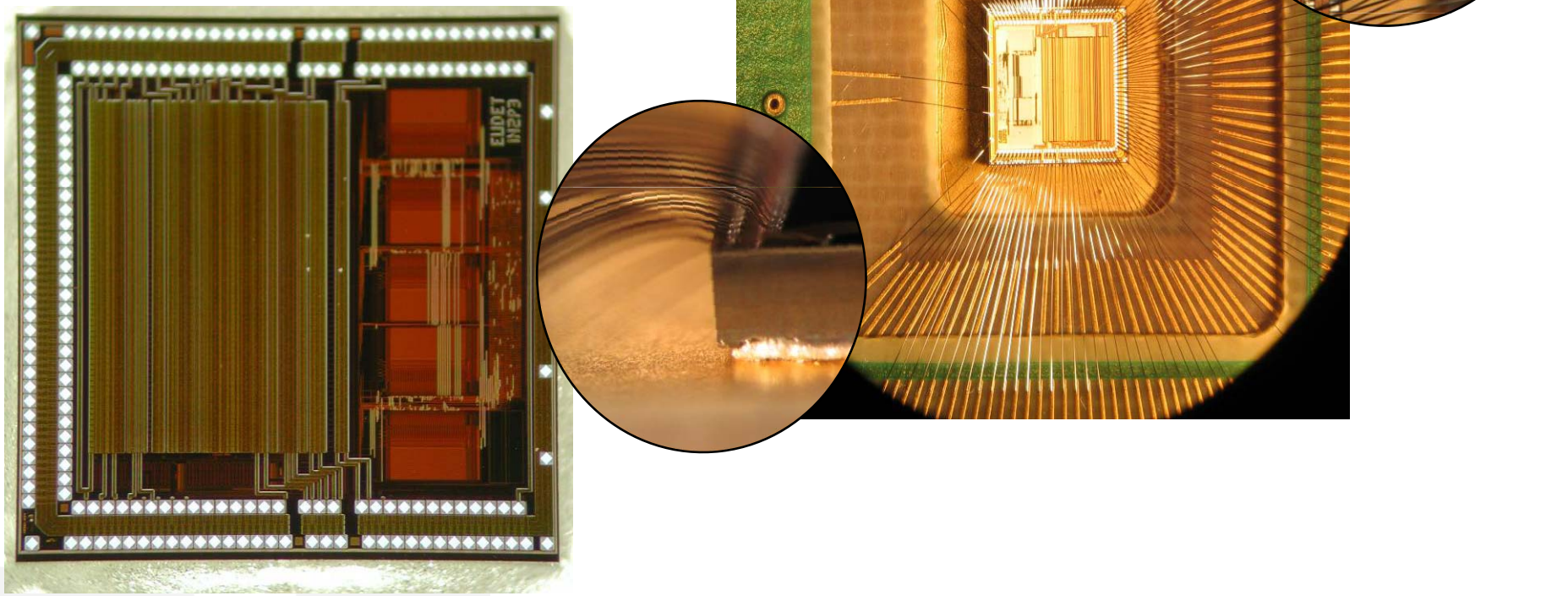
HARDROC2: FORSEEN MODIFICATIONS



PACKAGE CHOICE

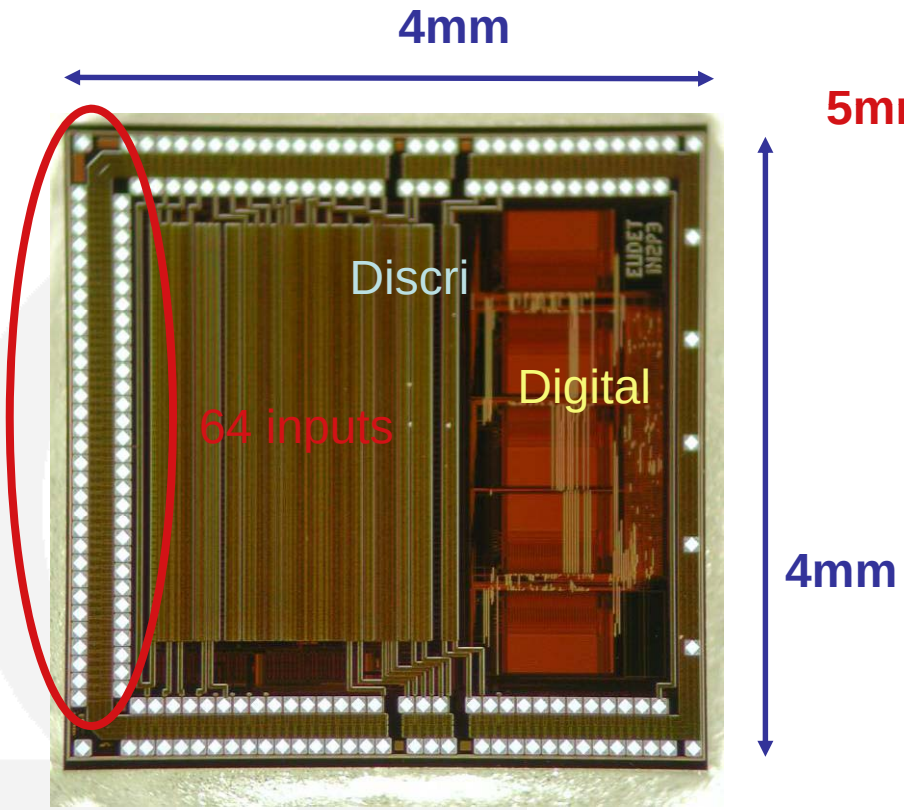
- HARDROC1: CQFP240
  - thickness=3.4 mm
  - Staggered pads

  => BAD YIELD

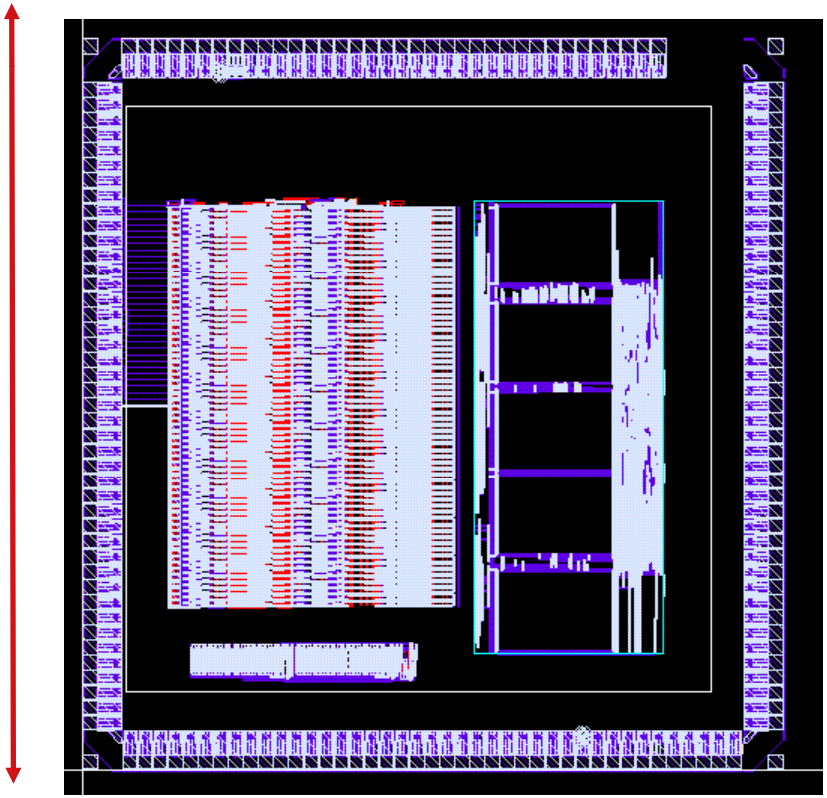


PACKAGE CHOICE

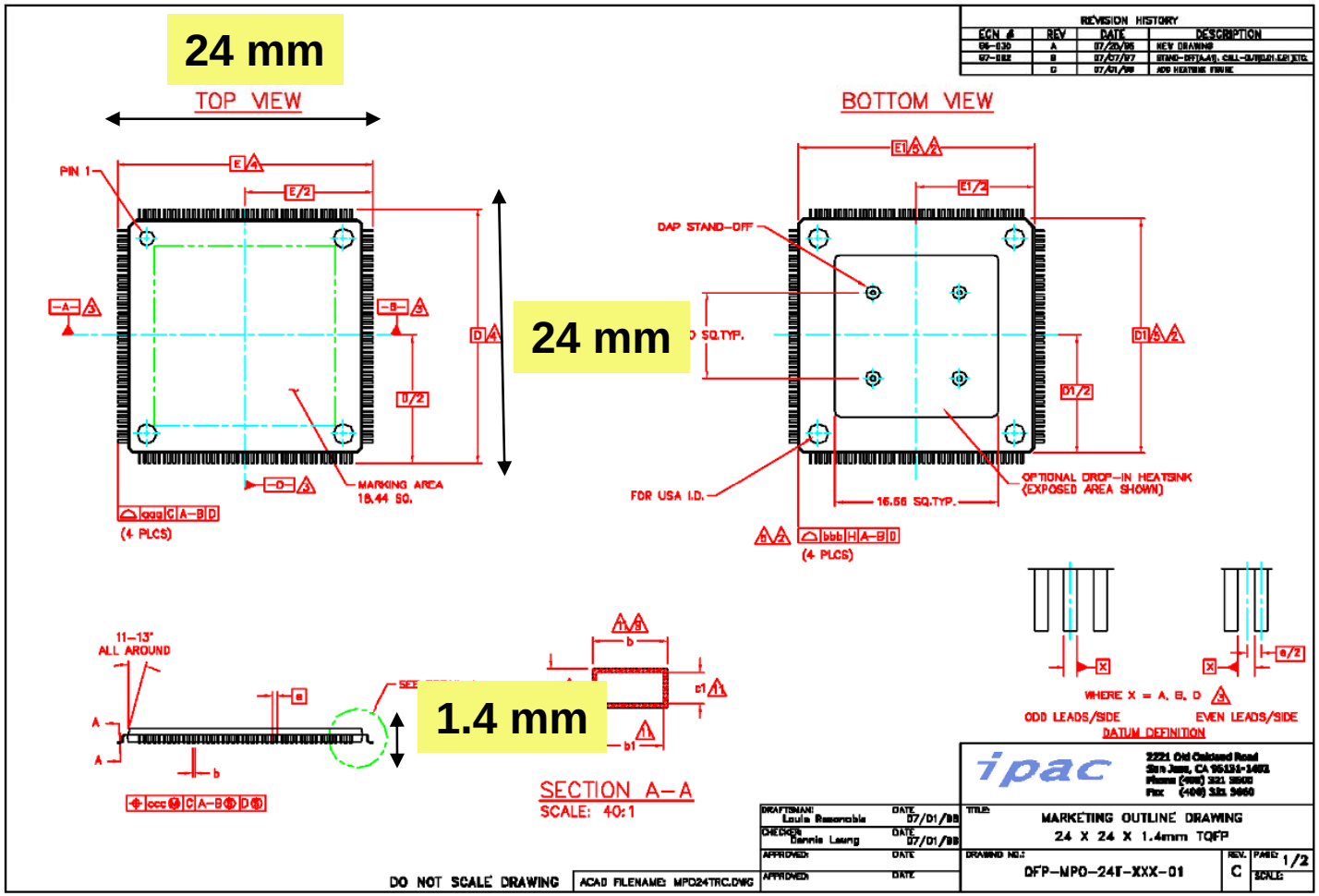
- HARDROC1: CQFP240
  - thickness=3.4 mm
  - Staggered pads (=> bad yield)
  - ~180 pins to be bonded (Bias and test points included)



- HARDROC2: Thin plastic package: TQF176. I2A Technology (Fremont California)
  - Thickness= 1.4mm
  - 1 row of PADs
  - Price: ~3500$ for 100 dies or 1000

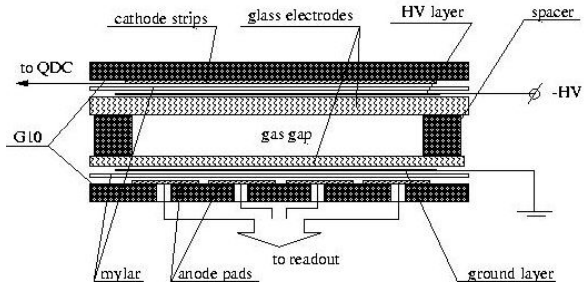


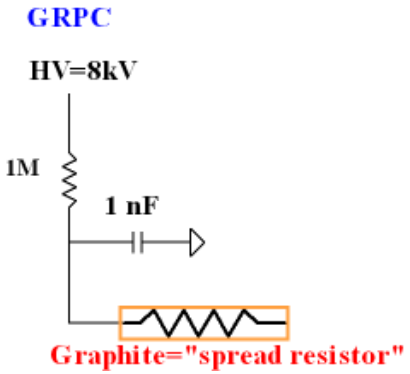
PACKAGE TQPP176



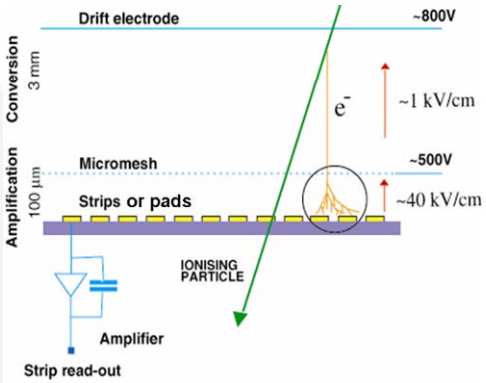
HV sparks (ESD)

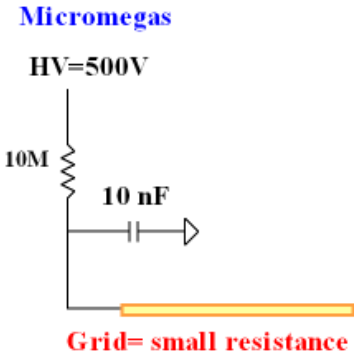
- **GRPC**: HV=8 kV, PADs= a few pF
  - High spread resistor= isolates FE inputs





- **Micromegas**: HV=400V, Pads= a few pF
  - Small spread resistor= NO ISOLATION of the FE inputs



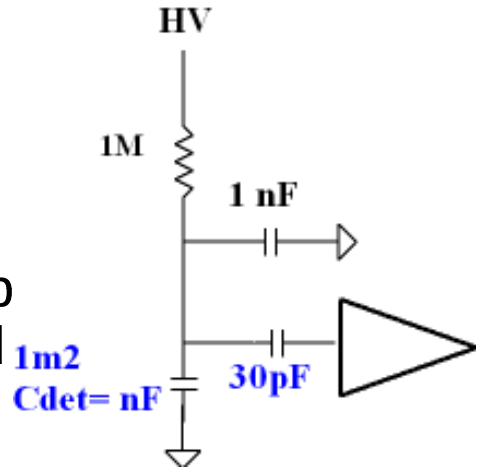


- **1m²** => C_{HV} ~ **1nF**

HV sparks (ESD)

- ASIC inputs:
  - protection PADs (AMS library): robustness up to 2kV HBM (100pF)

- From T2K large µmegas, **AC coupling necessary for detector > 10 cm²:**
  - **Maximum decoupling** capacitor that can b **integrated: ≈30pF** (50µm x 600 µm) and **lost of signal**
  - **EXTERNAL CAP=500 pF/ch** to ensure protection
  - Drawbacks of a decoupling cap: Xtalk, space
  - Tests to be performed on HARDROC to determine the decoupling capacitance necessary to protect the FE against ESD



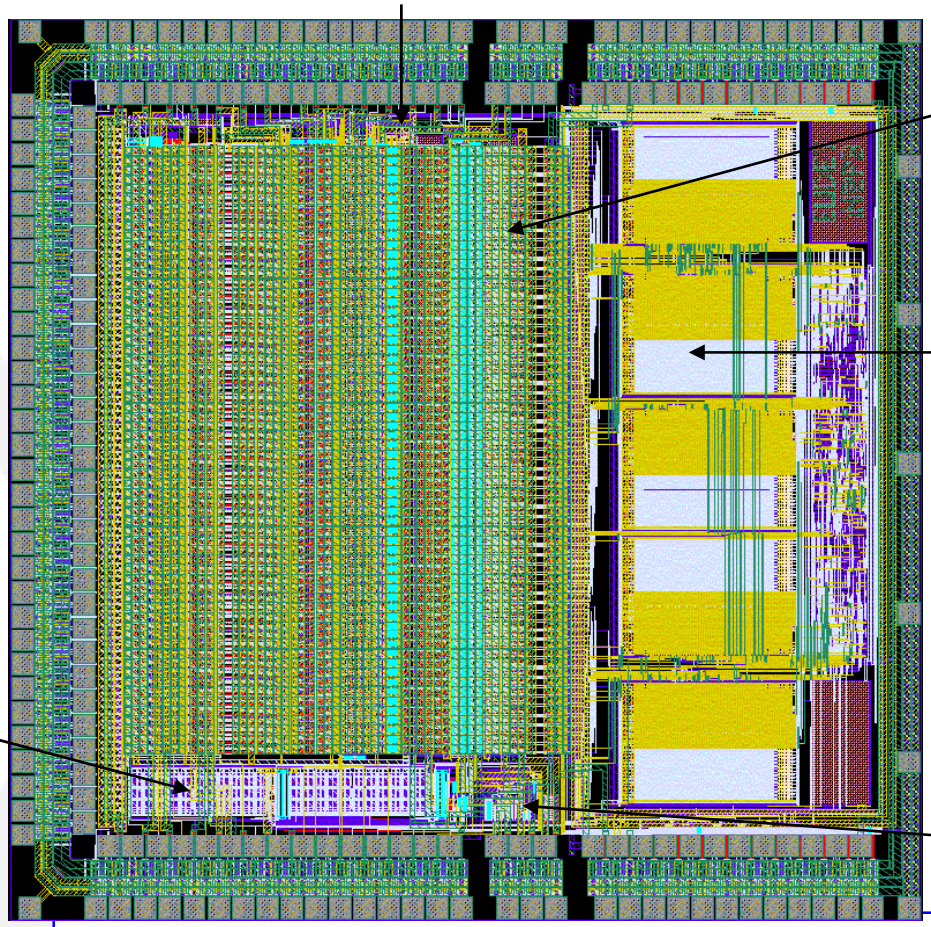
CONCLUSION

- HARDROC1: Fully functional for RPCs
  - Autotrigger on 10fC
  - No autotrigger with threshold= few fC
  - Power pulsing
  - Memory +Daisy chain
- HARDROC2: submission in june 08, keeping HARDROC1 as a backup
  - 3 thresholds (1, 10,100)
- HV discharge and protection: to be studied.

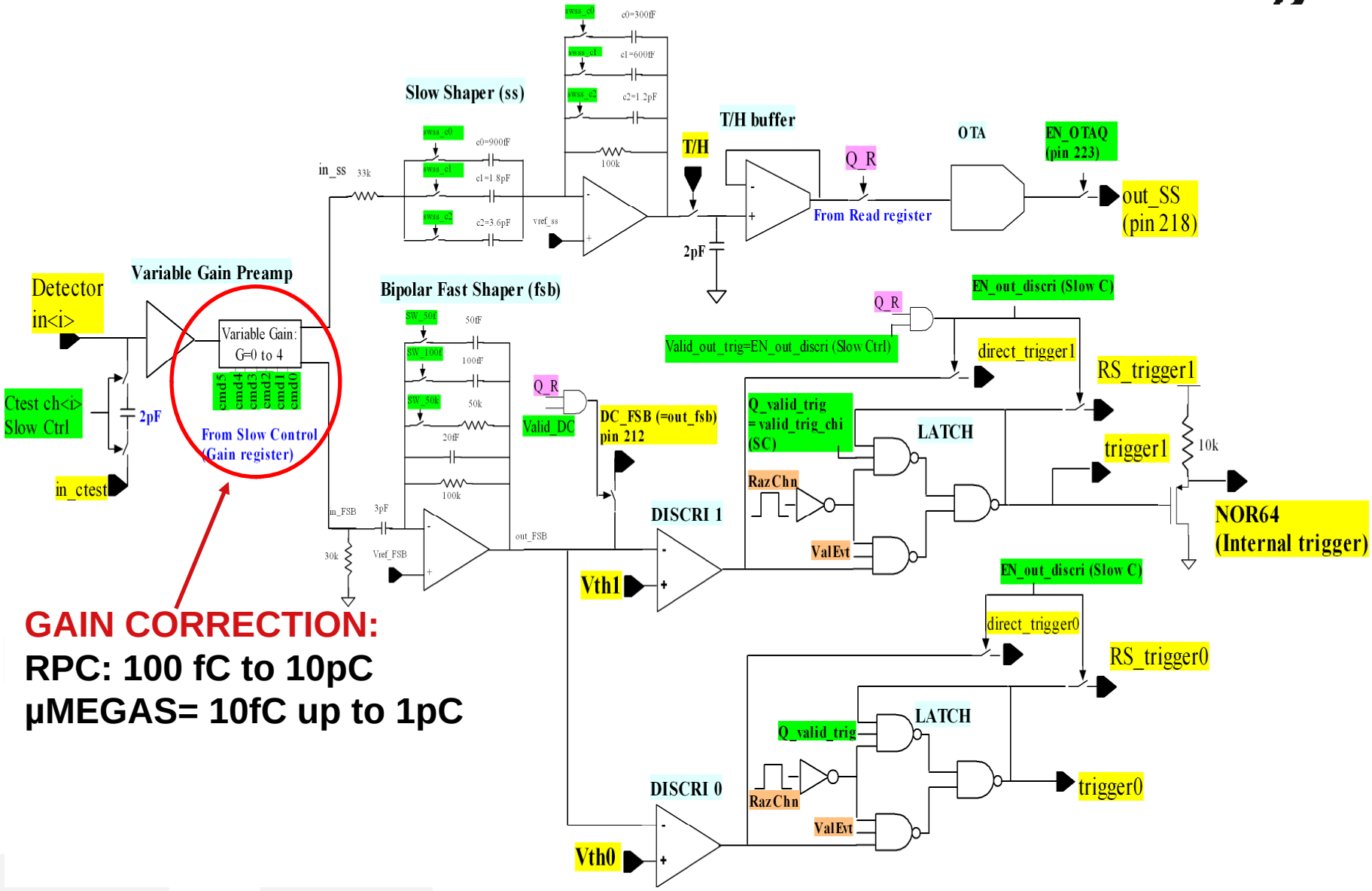
ANNEX

HARDROC1 layout

- Hadronic Rpc Detector Read Out Chip (AMS SiGe 0.35µm, Sept 06)
  - 64 inputs, preamp + shaper+ 2 discris + memory + Full power pulsing
  - Compatible with 1st and 2nd generation DAQ : only 1 digital data output



HARDROC1: ANALOG. PART



GAIN CORRECTION:

RPC: 100 fC to 10pC

µMEGAS= 10fC up to 1pC

HARDROC1: Digital part