The problem of power distribution (PPD) for tracking detectors. A SLHC R&D snap shot

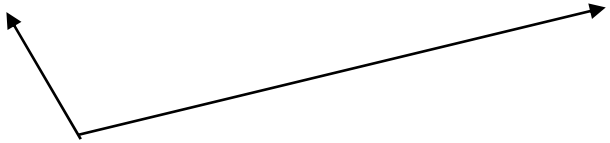
Marc Weber (RAL)

ILC and LHC/Super-LHC trackers share two major challenges

(albeit at different scale):

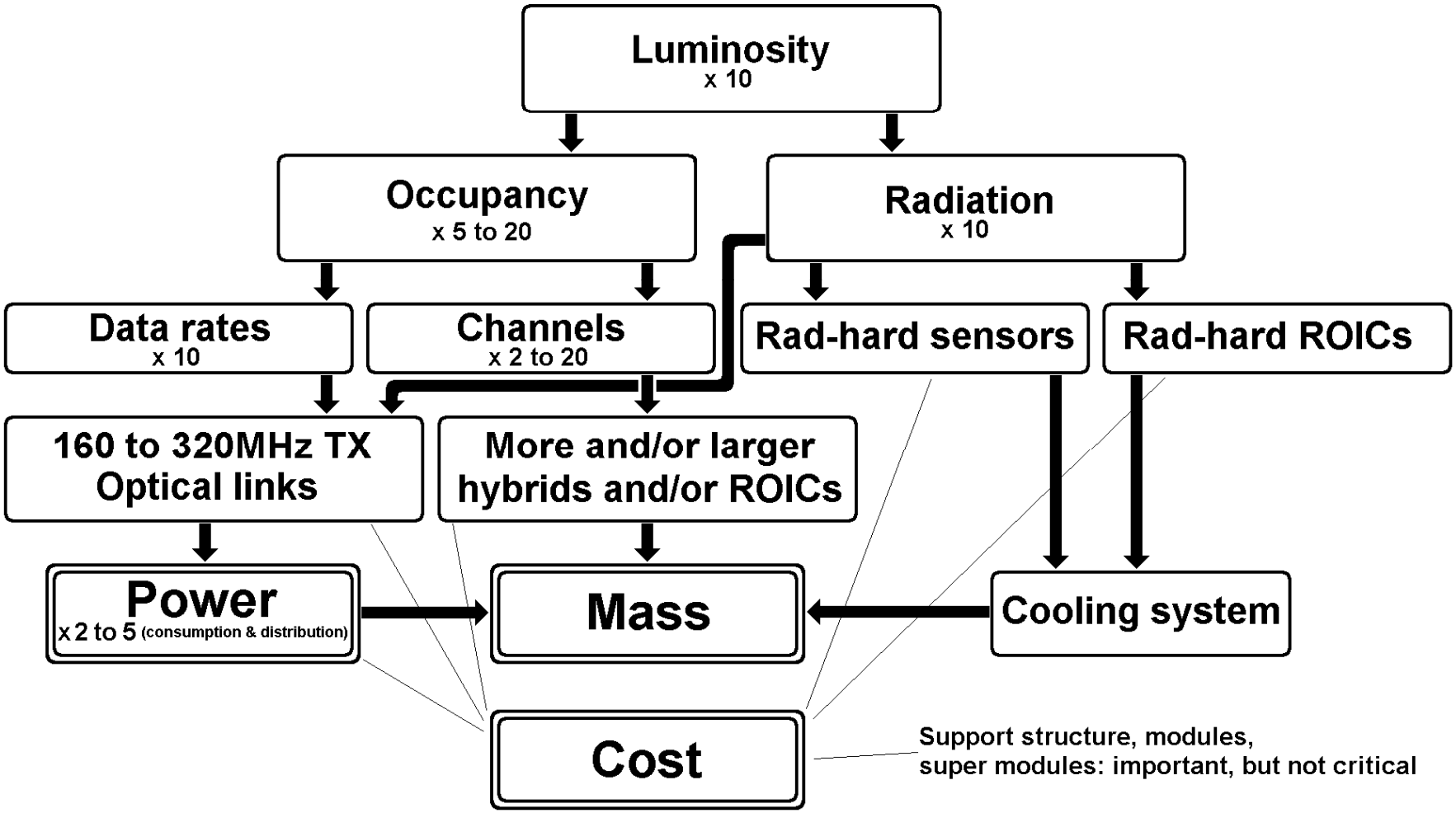
How to limit

Power consumption and **detector mass ?**



Power distribution, the topic of this talk relates to both of these

Challenges for SLHC trackers



Powering at LHC proved tough and led to an undesired performance penalty, in particular for forward tracking

	ATLAS pixels	CMS pixels	ATLAS strips	CMS strips
Number of modules	1744	1440	4088	15148
Total number of channels	80 M	66 M	6.2 M	10 M
Total rack power incl. optical links and cable losses	30 kW	7 kW	45 kW	67 kW
ROIC name and technology	FE-I3 0.25 μm CMOS	PSI46 0.25 μm CMOS	ABCD 0.8 μm bi-CMOS	APV25 0.25 μm CMOS
ROIC analog (digital) voltage	1.6 V (2.0 V)	1.5 V (2.5 V)	3.5 V (4 V)	1.25/2.5 V (2.5 V)
ROIC power consumption/channel	84 μW	40 μW	3.6 mW	2.9 mW
Total ROIC current	3.8 kA	1.5 kA	6 kA	15 kA
Cable length (one way)/resistance (round trip)	~110 m	~50 m	~110 m/4.5 Ω	34-62 m
Power efficiency	~20%	~42%	~50%	52%
Power distribution schemes	IP[4]	PP[5]	IP	PP
Local regulators (near/on-detector)	Yes	Yes	No	Yes

Power distribution at LHC

Depending on experiment (ATLAS and CMS) and detector type (pixels or strips):

- 6 – 80M channels
- 4 – 15K detector modules
- 7-70 kW of rack power for readout electronics *(due to radiation)*
- 50 m to 110 m long power cables (one way) *(due to detector size/energy)*
- 20-50% power efficiency

Constraints: limited space to feed through cables; requirement of minimum mass; need to minimize thermal losses in cables; packaging constraints on detector

SLHC trackers will have 5 to 10 times more channels than LHC ⇔

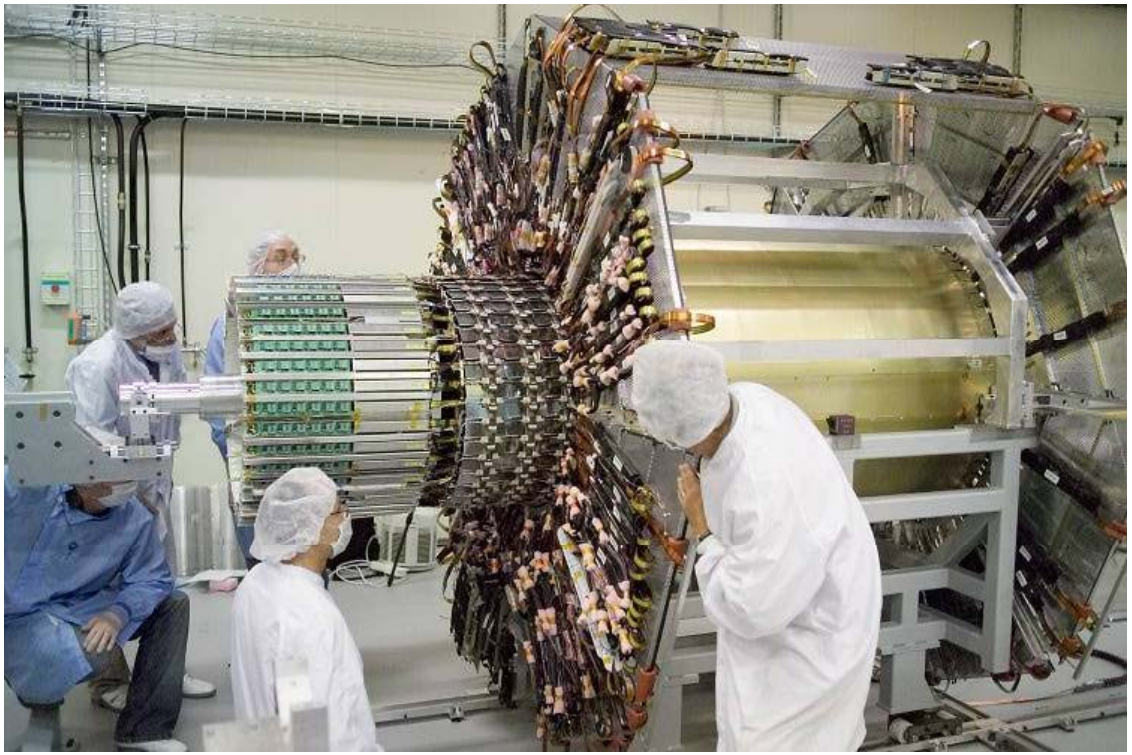
Power distribution concept must change radically

Why independent powering fails at SLHC ?

Current per electronic channel ~ constant, but many more channels

1. Don't get 5 or 10 times more cables in
2. Power efficiency is too low (50% ATLAS SCT ⇔ ~15% SLHC)
3. Cable material budget: 0.2% of R.L. per layer (barrel normal incidence) ⇔ 1% or 2% SLHC
4. Packaging constraints

Each reason by itself is probably sufficient for a No-No



Why powering R&D ?

Front view on ATLAS tracker barrel

Cannot afford cable pollution anymore and don't need to.
New systems will be much better

(cable number, material performance; packaging; power efficiency)

How we will fix the cable pollution?

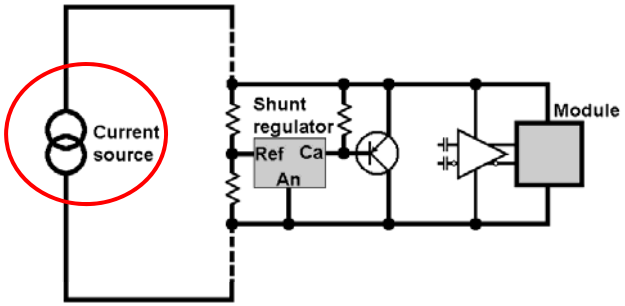
Minimize module power consumption in the first place.

Minimize the current through cables. There are only two ways:

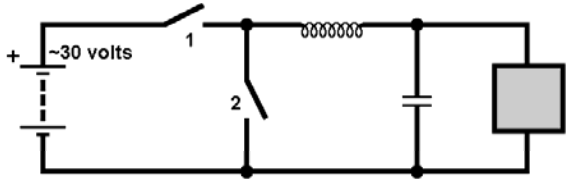
a) recycling current (Serial Powering) or
b) "high-voltage" power lines plus DC-DC conversion

Both require local "power supplies" (regulators or converters) on the detector module ⇔ PS design challenge + system challenge

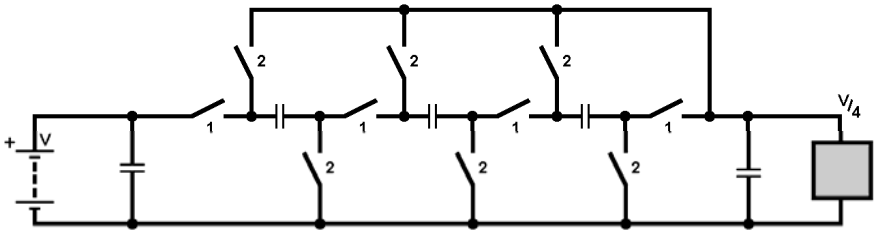
How we will fix the cable pollution?



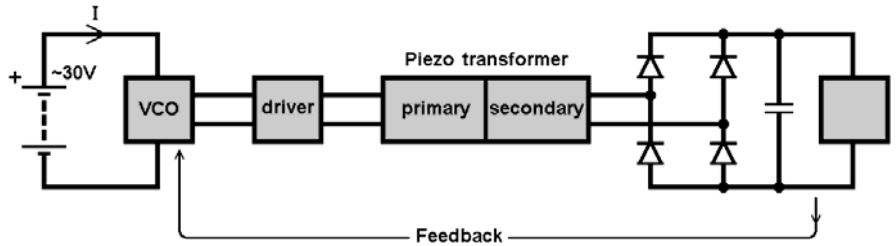
Serial powering



DC-DC buck converter

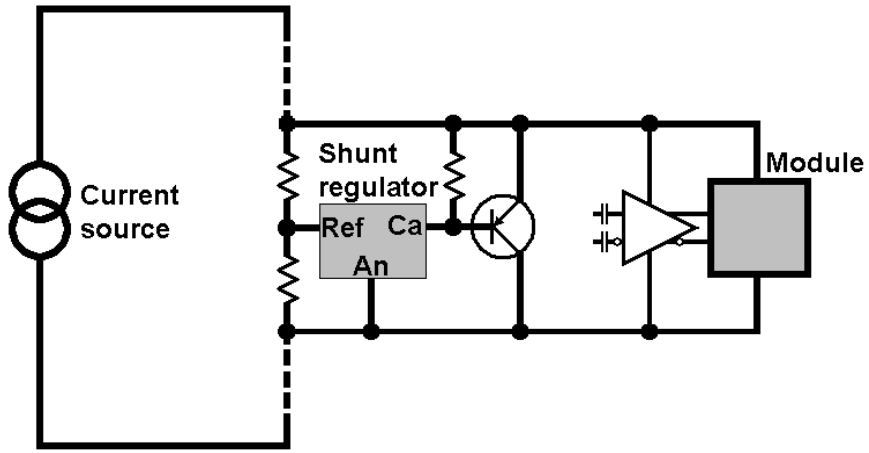


DC-DC charge pump



Piezoelectric transformer

Serial powering



Send constant current from module to module; local shunt regulators to define module voltage.

Different modules sit at different potential ⇔ need AC-coupling of signals (was a bit of a nuisance but not an issue)

Unorthodox, “crazy”, but elegant. Also used for LHC magnets…

New approaches offer remarkable benefits: reduction of cable volume by factor 10-20; increase of power efficiency by factor 2-5…

A few comments

Serial powering is an old idea. First implemented for ATLAS pixels by Bonn University. Picked up ~2 years ago by RAL for strips

Initially we were mostly worried about noise/electrical performance of these multi-module systems (apart from failure and loss of many modules)

Wrongly! *SP systems tend to be quiet:*

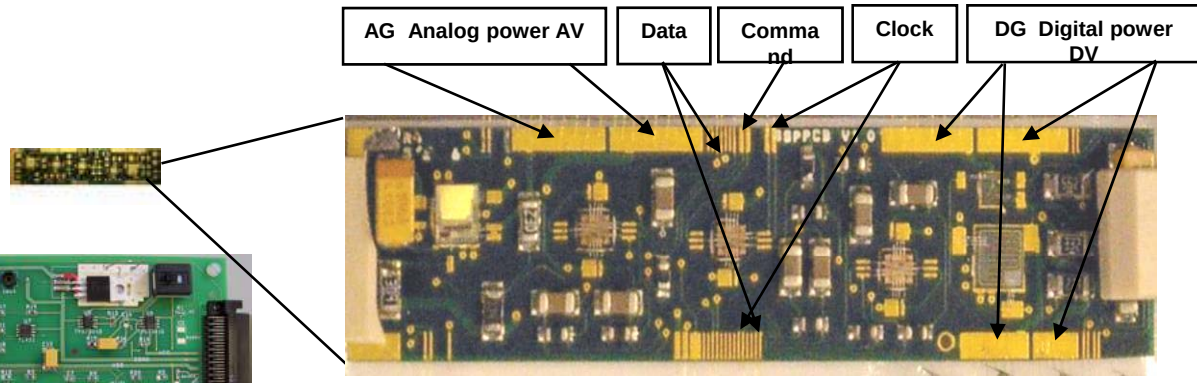
a) local regulator on module helps
b) Current in the chain is constant ⇔ no IR drops

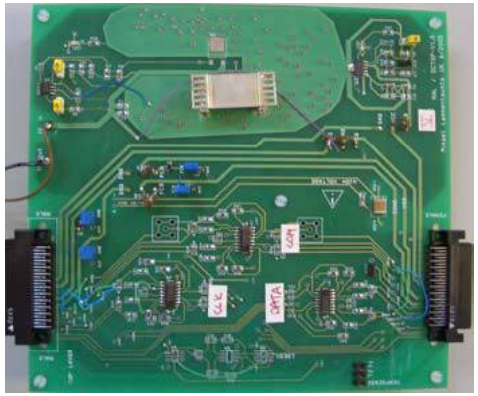
Serial powering circuitry evolution

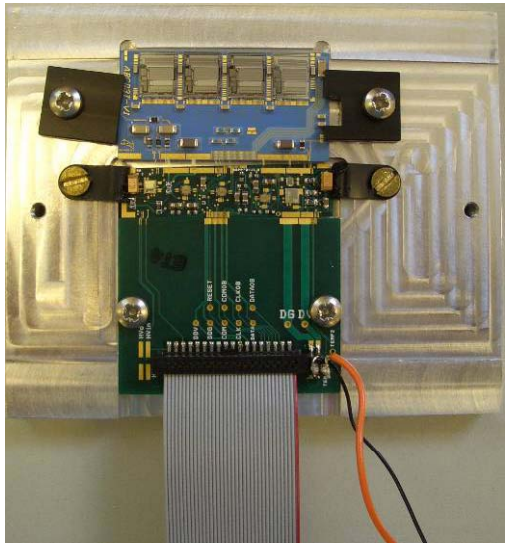
SSPPCB - 2006/7 -
38 mm x 9 mm

SPPCB - 2006 -
111 mm x 83 mm

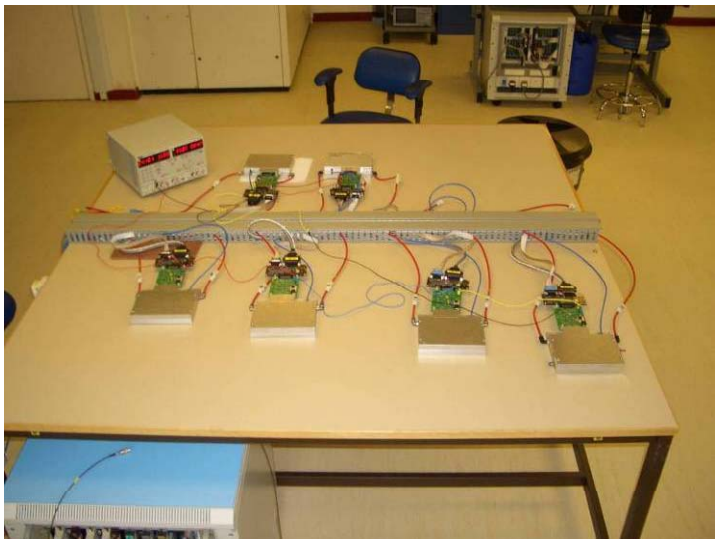
SPPCB - 2006 -
150mm x 150mm



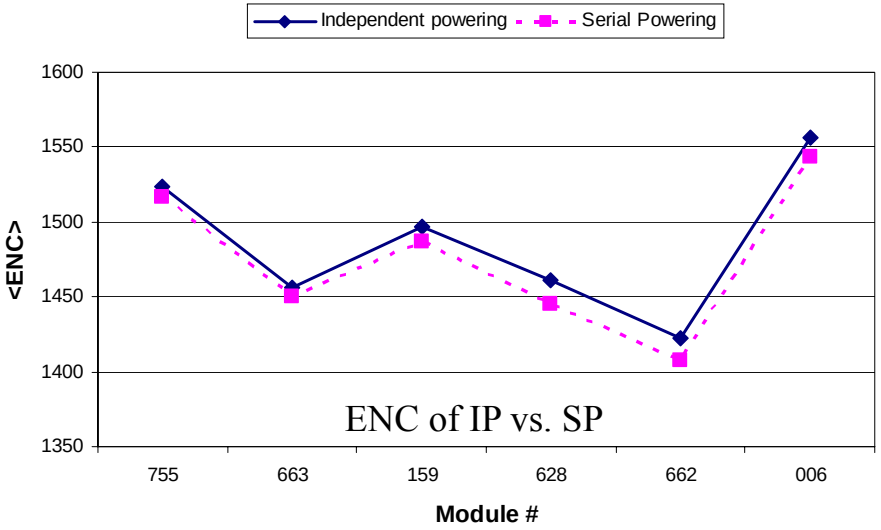


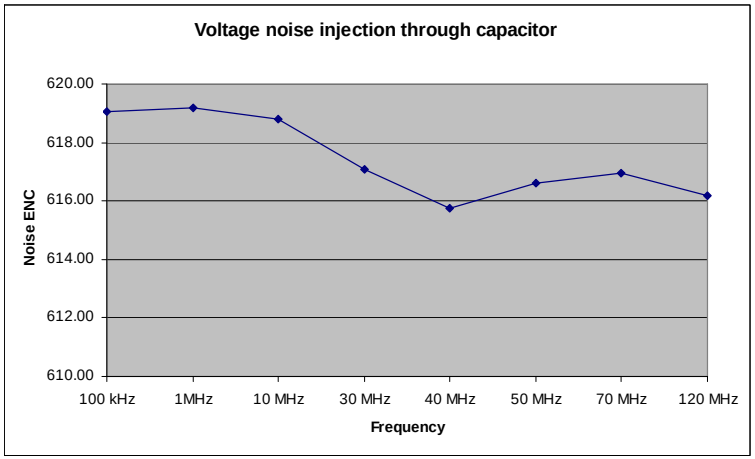


Tests with ATLAS SCT modules or hybrids

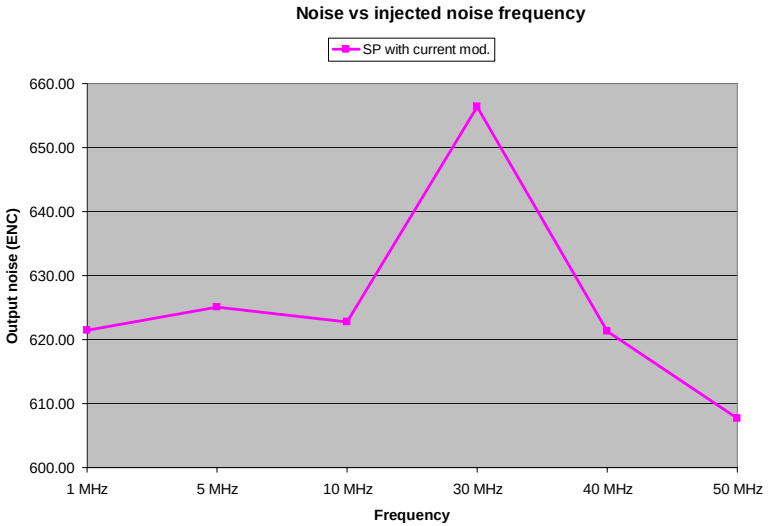


SCT module test set-up





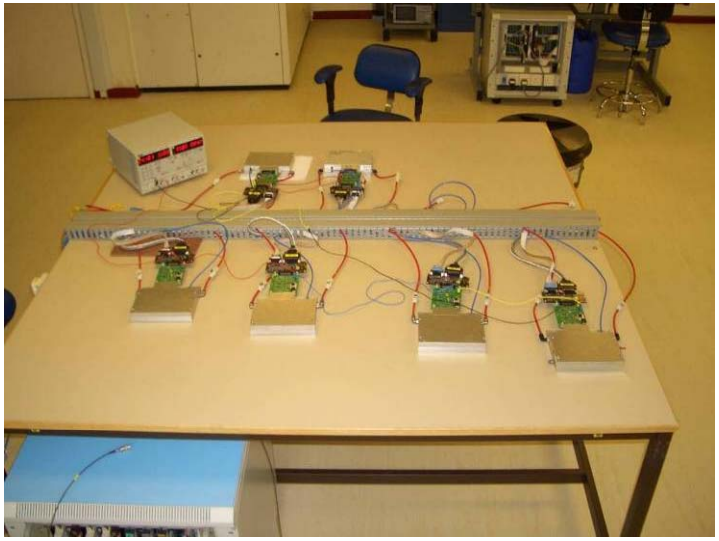
ENC with injection of external voltage pulse into power line (1V pp through 15 pF)



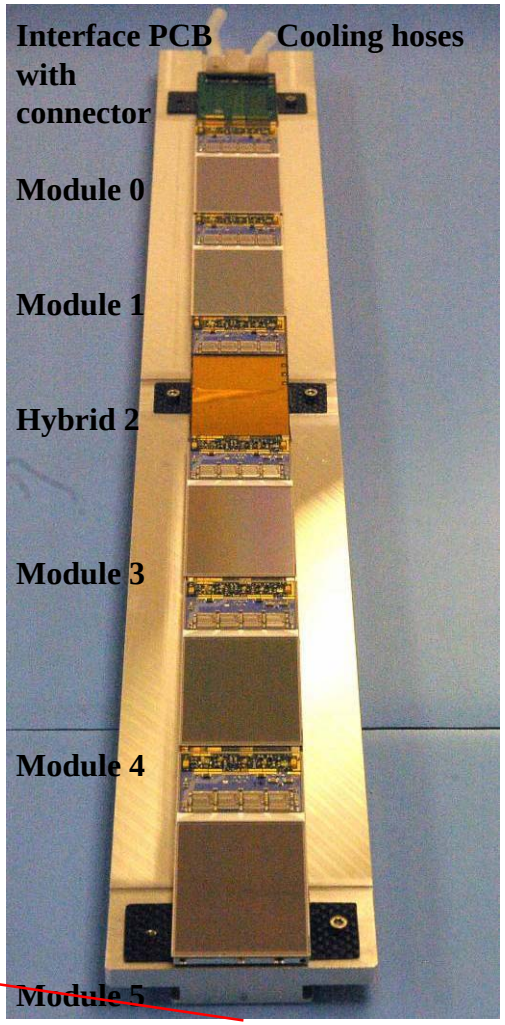
ENC with current modulation of 20 mA

Many results, noise looking good. So far only commercial electronics

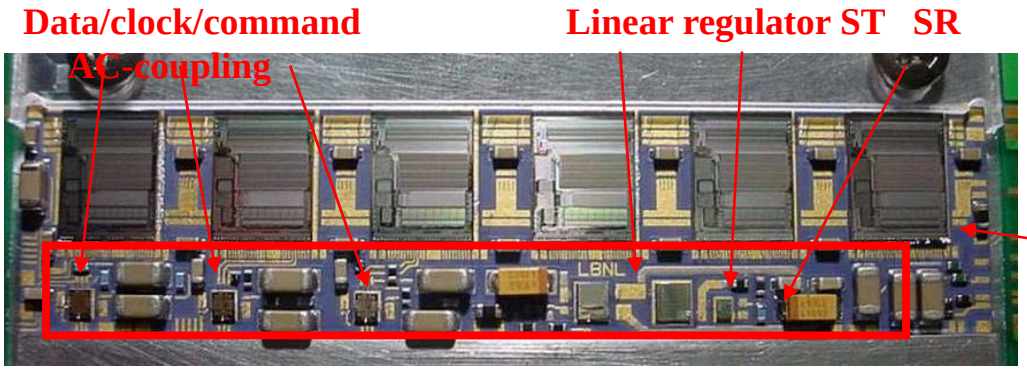
Objects we built and tested so far



ATLAS SCT module tests



6-module serial powering stave



Six ABCD hybrid with SP for 30 module stave

Next step are design of custom electronics

Main difficulties: high current requirement and limited HEP IC design experience in this area.

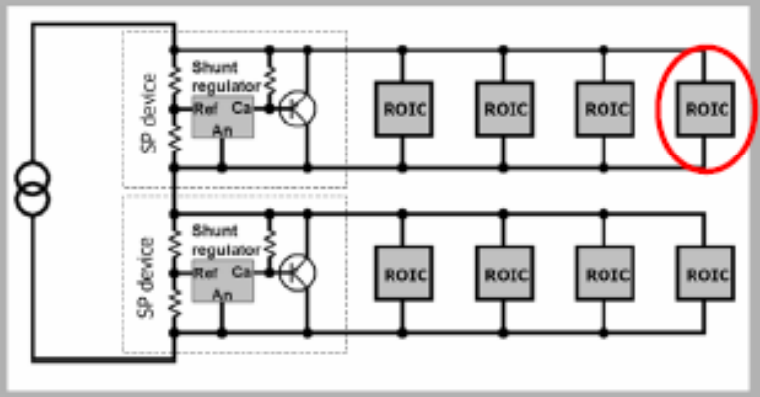
Benefits: much reduced output impedance; much reduced real-estate; radiation-hardness

	Required range	Desirable range
Output voltage	1.2 V – 1.8 V	1.2 – 2.8 V
Output current	> 2 A	> 4 A
Dynamic output impedance	10 Ω at < 10 MHz	0.1 Ω at < 100 kHz 0.5 Ω at < 10 MHz
Magnetic field operation	> 4 T	> 4 T
Radiation-tolerance	10^{15} n/cm^2 100 MRad	10^{16} n/cm^2 500 MRad
Size		100-250 mm^2
Inefficiency	<20%	~5%
Minimum EMI	EMI susceptibility is detector specific. Limits for radiative EMI (e.g. from inductor coils) are not yet understood. For conducted EMI, 40 dbμA of common-mode should not be exceeded in the frequency range of 100 kHz to 30 MHz.	
High reliability	System dependent. Targeted module power failure rate: < 1% per module over 5 years of operation	

Table 2: Specification for SLHC power regulators, converters or transformers. See the text for explanations.

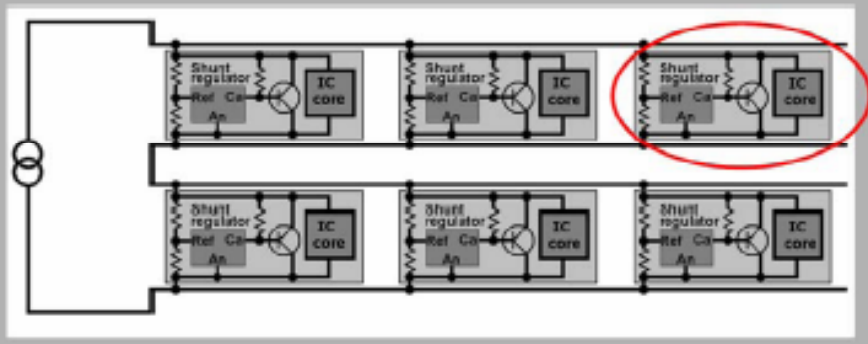
Serial Powering Schemes - Motivation

1) External shunt regulator + transistor



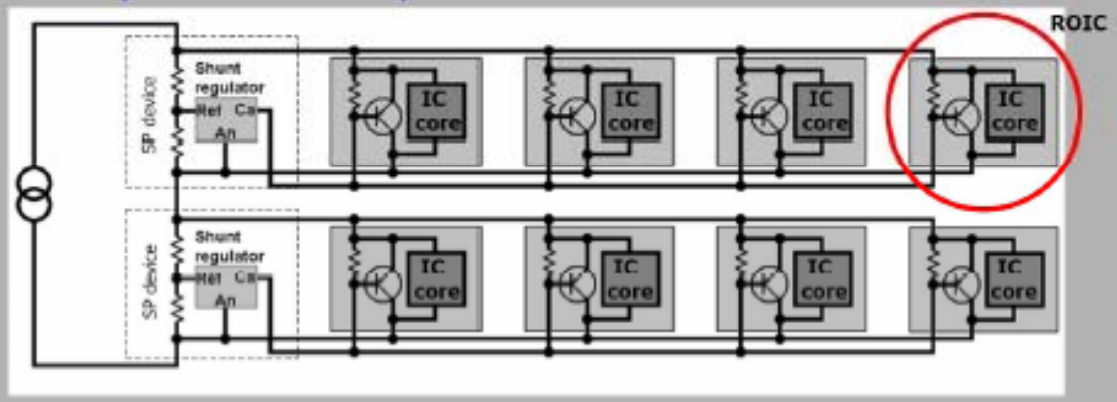
Good approach, but implies a **high current shunt**
-> limited experience in HEP-IC community
SP device enables to operate non SP-ROIC in SP mode

2) Internal shunt regulator + transistor in each ROIC



Disadvantage: many power supplies in parallel
Matching issue can cause hot spots and potentially kill chips

3) External SR + parallel shunt transistor in ROIC

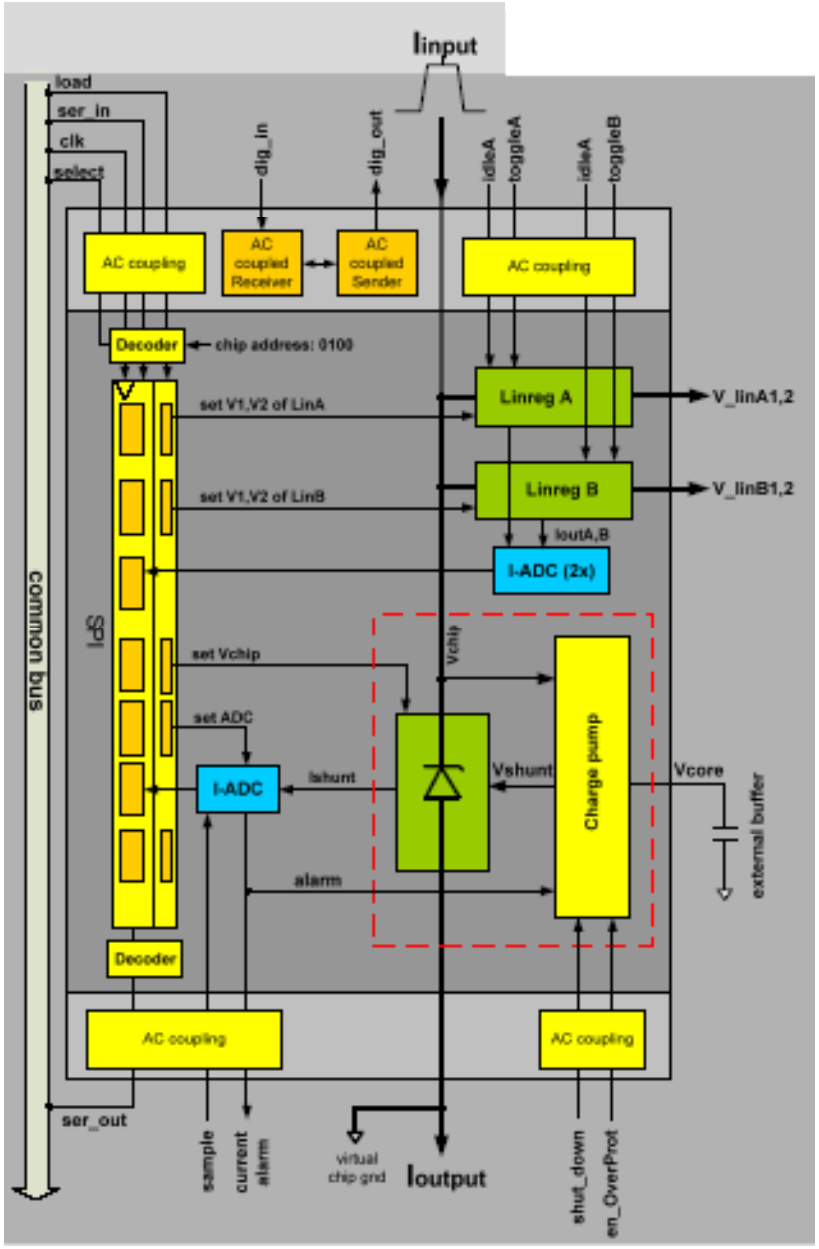


feedback however **more challenging** and depends on implementation

- choice of architecture **not obvious**, detailed studies anticipated by RAL/LBNL (M.Weber, C.Haber)
- **SPI chip should cover scheme (1) and (3)**
- scheme (2) can be realized by any ROIC standalone

Interlude: SPi chip

General purpose SP interface



Overall layout and design: Marcel Trimpl, FNAL

LVDS part and stand-alone SR: Mitch Newcomer and Nandor Dressnandt, Penn

Specification and KE: Giulio Villani, RAL

Main blocks and features:

Shunt regulator(s) and shunt transistors;

LVDS buffers; over current protection;

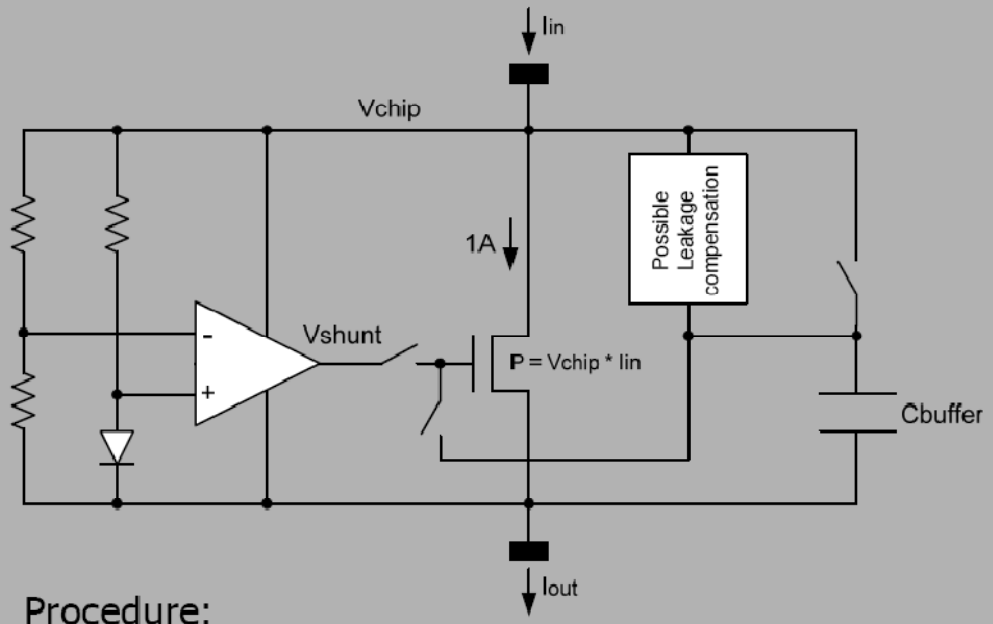
Shunt current sensing ADC;

TSMC 0.25µm CMOS with rad-hard layout;

Max. shunt current: 1 A design, “expected” 2.5 A;

Size: ~ 14 mm^2; bumping

Principle of OverPower Protection



1. OverPower is **NOT** OverCurrent
   -> current should stay the same
   in SP scheme!
2. Power reduction by
   collapsing the chip voltage
3. Goal: reduce Vchip to minimum
   e.g. 50mV and 4A -> **P ~ 200mW**
   - in the order of nominal operation
   - comparable to ROIC on module

-> no hot spot!

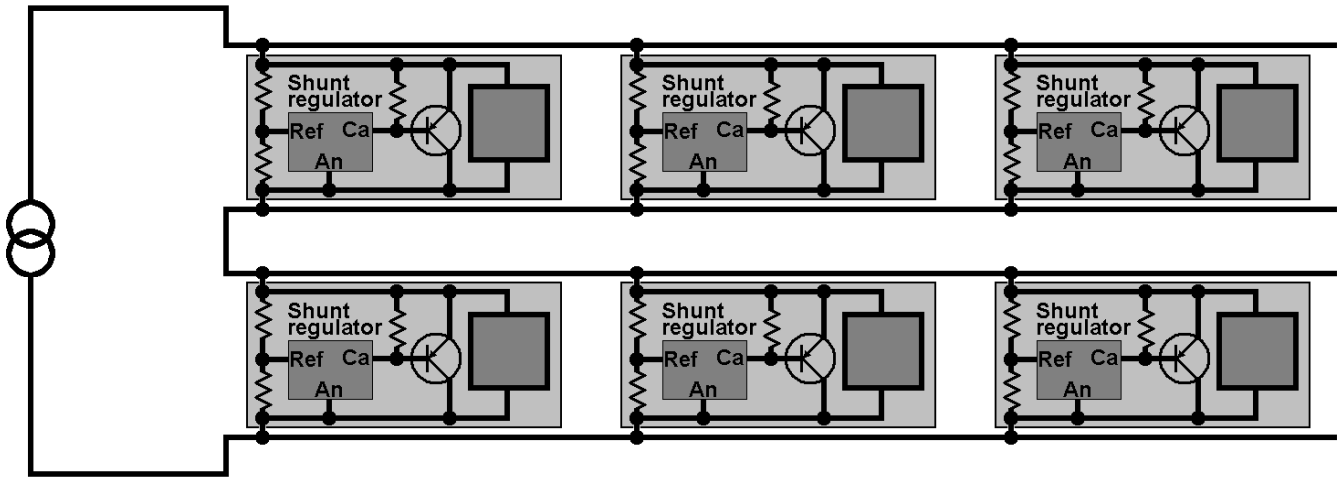
Sounds crazy, but serial powering is already!

Procedure:

1. ADC reports current alarm or power down command
2. Amplifier decoupled, Vshunt connected to Vbuffer (2.5V)
   -> forces shunt-mos in lin.region & reduces Vchip (Ron*I)
   -> whole chip collapses, only shunt maintains operatio
3. let's see how far (long) we can go using a simple buffer cap
   - very attractive for **pulsed powered schemes**
   - for permanent power down basically leakage effects need to be compensated (short ramp up to recharge)

SP architecture choices

b) Shunt regulator + transistor in each ROIC



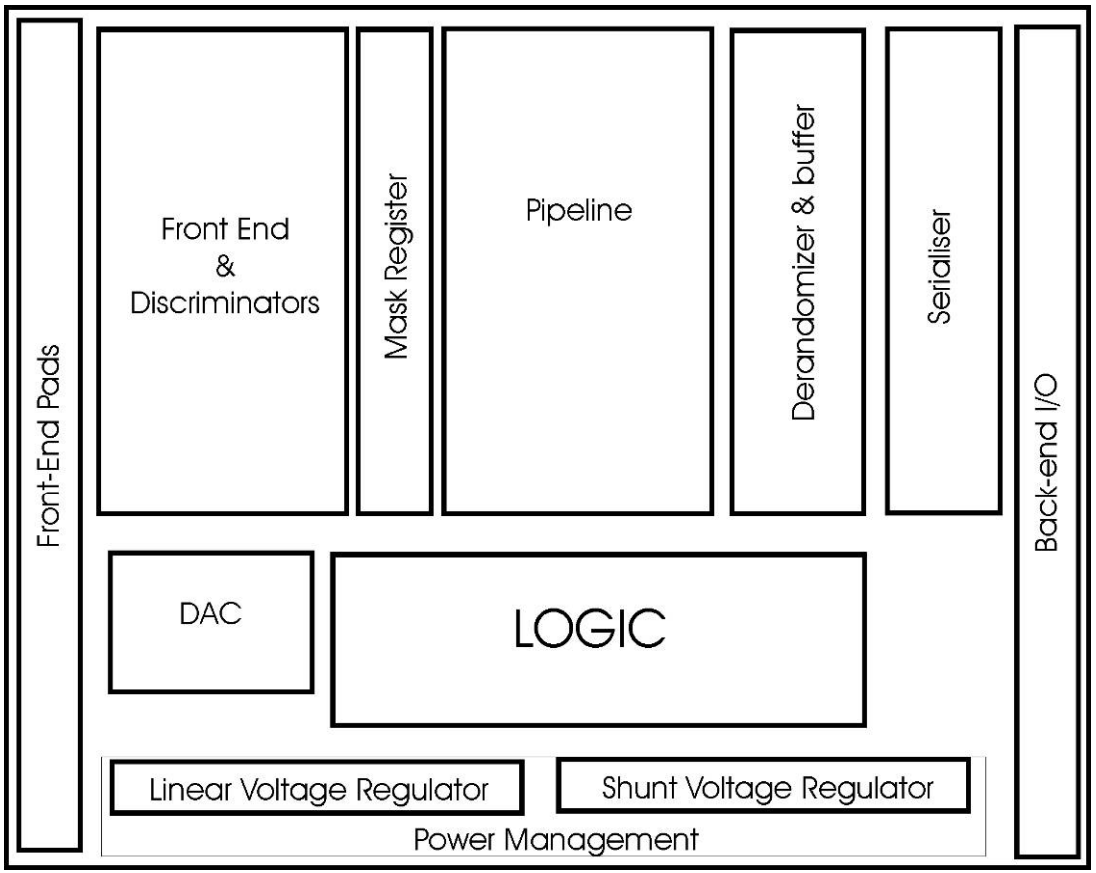
Integrated (custom) SR and transistor designed by Bonn worked well for pixels.

Many power supplies in parallel; Addresses high-current limitation and provides protection. Difficulty is matching and switch-on behaviour of shunt transistors. Must avoid hot spots that kill one shunt transistor after the other.

Specific implementation in ATLAS ABC-Next

Prototype chip for Si strip readout in Upgrade Inner Tracker

- **Binary readout**
- **Front-end optimised for short strips**
- **Positive or negative input charge**
- **Readout clock up to 160 Mbits/sec**
- **250 nm CMOS (IBM) technology**
- **2.5 V digital power supply (100 mA)**
- **2.2 V analogue power supply (30 mA)**
- **Compatible with serial powering scheme**



Full shunt regulator on chip - design concept

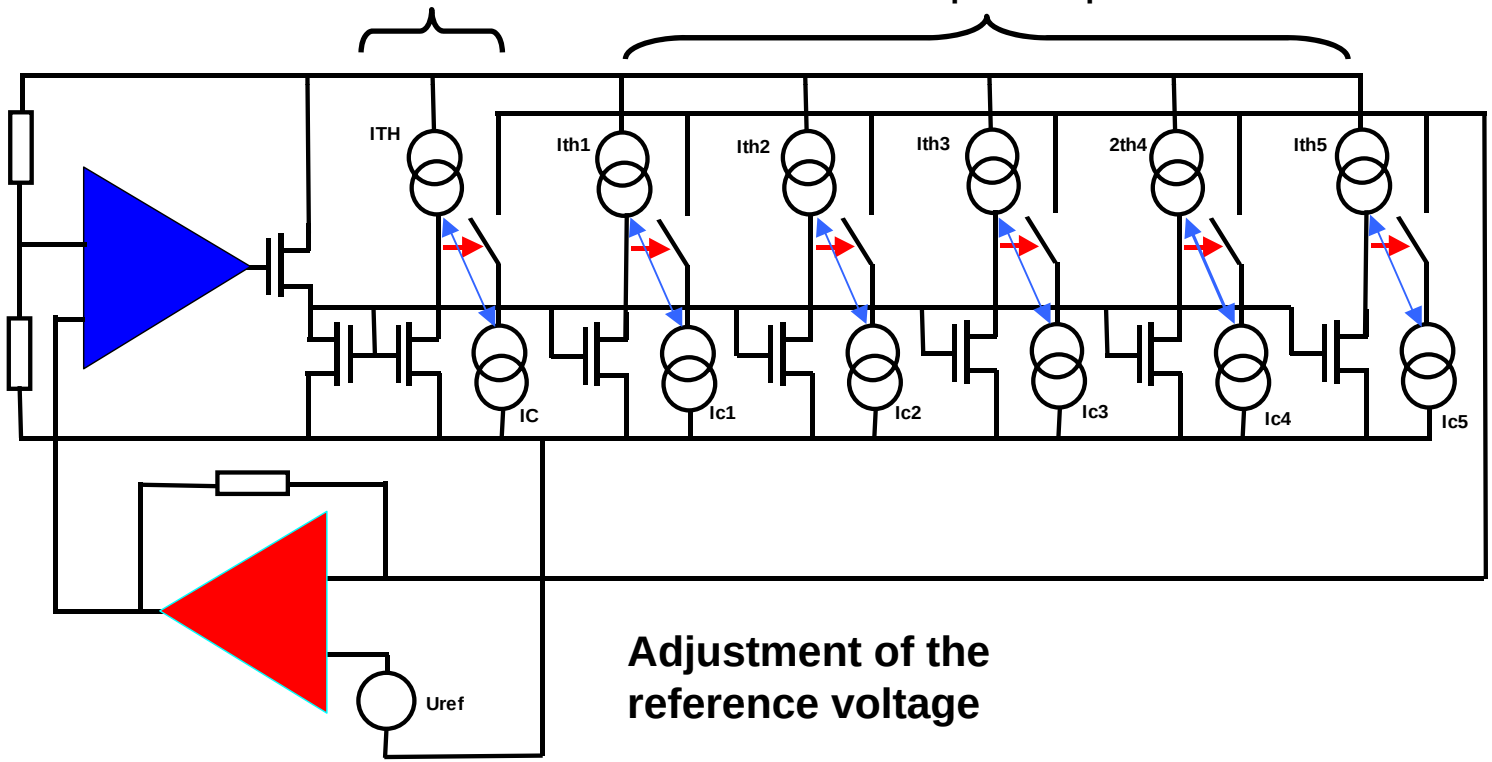
Need democratic distribution of shunt current, not winner takes it all.

Shunt current limiter

Current limit set by an internal resistor and selected by bonding

Re-adjustment and redistribution of the shunt current

Number of stages depends on the assumed spread of parameters



Adjustment of the reference voltage

Conclusions

Solving PPD for SLHC trackers is crucial, extremely challenging and urgent.

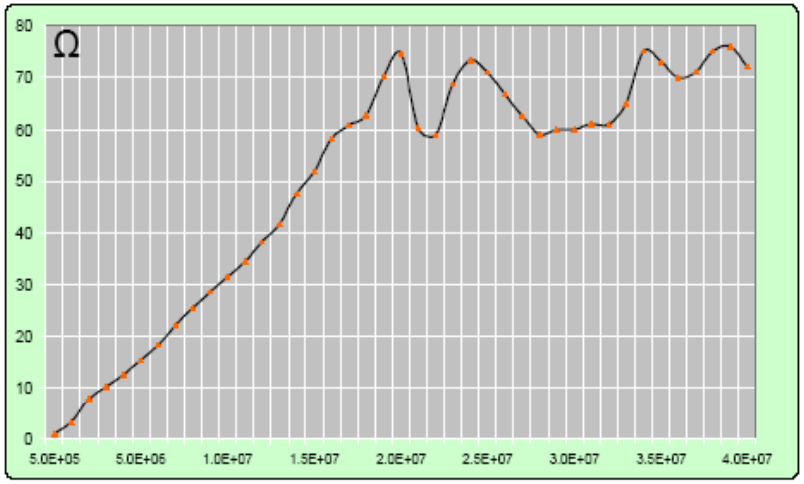
It is unusual to gain such significant factors in a technology as mature as silicon detectors.

Power distribution R&D is a new and exciting field. International collaboration is growing. http://indico.cern.ch/conferenceDisplay.py?confId=31377

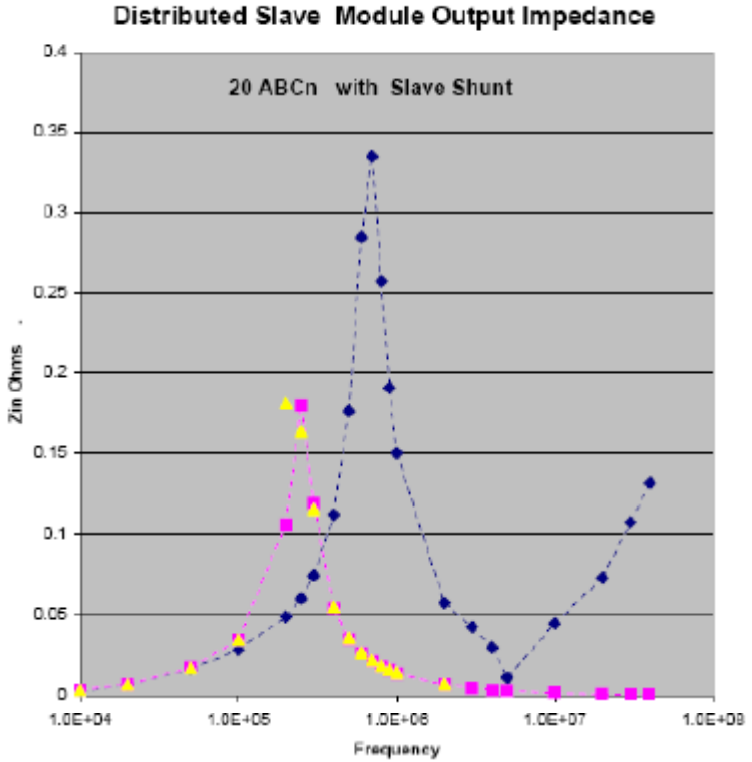
I expect significant spin-offs outside of PP, e.g. space and synchrotron detectors. Benefits not limited to tracking.

Appendix

Expected performance benefit of custom SP circuitry



Measurement (RAL): Prototype with commercial components



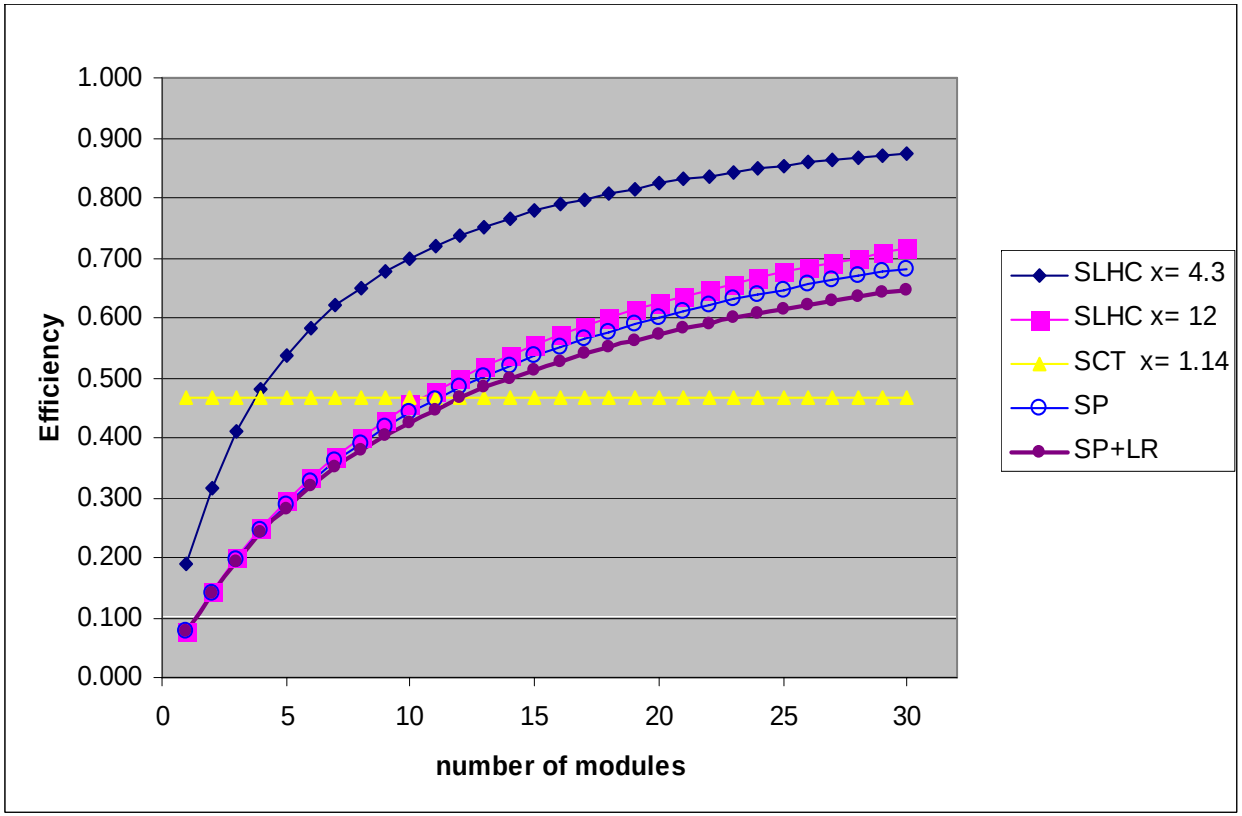
Simulation (Mitch Newcomer): External Shunt Regulator and Integrated Shunt Transistors

Dynamic impedance: reduced by one or two orders of magnitude!

Power efficiency for SP at LHC and SLHC

Illustration of various cases:

SCT ⇔ 4V, 1.5 A, R= 4.5 Ω ⇔ x=1.14; IP
SLHC ⇔ 2.5V, 2.4 A, R= 4.5 Ω ⇔ x=4.3; SP (only cable losses)
SLHC ⇔ 1.5V, 4 A, R= 4.5 Ω ⇔ x=12; SP (only cable losses)
same but including SR power and LR power (extrapolated from ATLAS SCT measurements)



Keep hybrid current low!

SR inefficiency ~7% for 10% digital current variation

LR for analog has similar losses

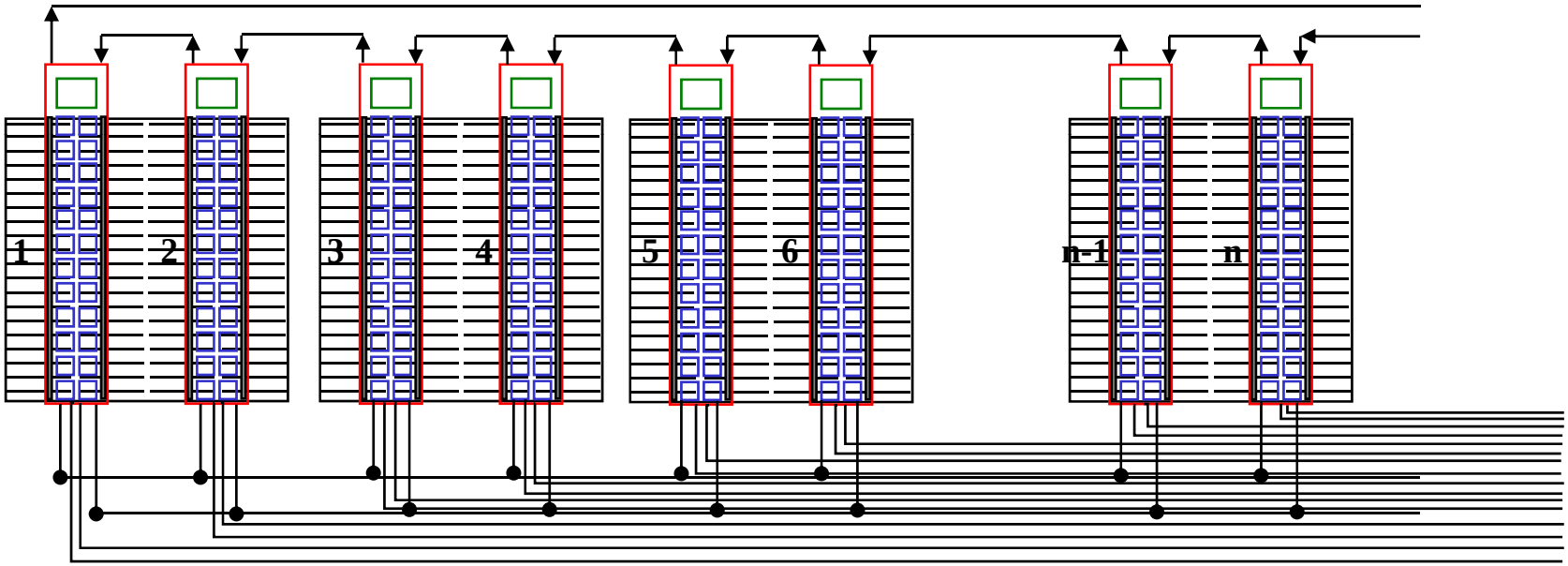
SR inefficiency is reduced for 0.13 μm CMOS

Let's work out a powering example

here V_{ROIC} = 2.5 V; I_H = 2.4 A; 20 hybrids; DC-DC gain = 20

SP: n=20; $I_H = I_{PS} = 2.4$ A; $V_{PS} = nV_{ROIC} = 50$ V

Features: saves factor ~8 in power cables/length over ATLAS SCT



DC-DC PP: n=20; g = 20; $I_{PS} = n/g\ I_H = 2.4$ A; $V_{PS} = gV_{ROIC} = 50$ V

Features: saves factor ~8 in power cables as SP, watch IR drops ⇔ $R_{cable} \sim 0.1\text{-}1\ \Omega$

DC-DC IP: n=1; g = 20; $I_{PS} = I_H/g = 0.12$ A; $V_{PS} = gV_{ROIC} = 50$ V

Features: 2x more cables than SCT ⇔ problematic for strips

Features of IP and alternative schemes

	IP	SP	DC-DC	Comment
Power efficiency	10-20%	60-80%	60-80%	Varies with I, **n** (SP); gain (DC-DC)
Local regulator inefficiency	0%	~10%	<20%	This is without linear regulator for analog
number of power cables	4 per hybrid	Reduction by factor 2n	Reduction by factor 2n	**n** = number of hybrids
Voltage control over ind. hybrids	Yes On/Off; fine-adjustment	Stand-by mode: 2.5V/1.5V -> 0.7 V; Limited fine-adjustment	Yes On/Off; limited fine-adjustment	New schemes have regulators; no fine adjustment needed
Hybrid current info	Yes	Yes (sensing current through power device)	Yes	Some power penalty for DC-DC
Hybrid voltage info	Yes (need sense wires)	Yes	Yes	Not strictly needed, since regulators
Floating hybrid power supplies	Yes	No, voltage chain	No	
Protection features	Separate set of cables for each hybrid	Local over-current protection; redundant regulators	Don't know yet	Protect against open (SP) and short (DC-DC)

Let's preserve the good features of IP ⇔ **have voltage control, current monitoring, and protection features**

Overview of activities in a nut shell

*DC-DC **buck converters** and **charge-pumps***
On-(read-out) chip** and dedicated **stand-alone converters

Serial powering regulators implemented in
(read-out) chip** and dedicated **stand-alone generic chip

Studies so far were largely limited to bulky commercial devices

Program requires development of these devices for one:

-good electrical performance
-radiation hardness
-low mass/ small size
-high reliability
-high current capability
-magnetic field tolerance
-low EMI

Development of these devices also requires their validation with detector modules or chains of detector modules