The ATLAS Pixel Detector

Part 1: the active elements

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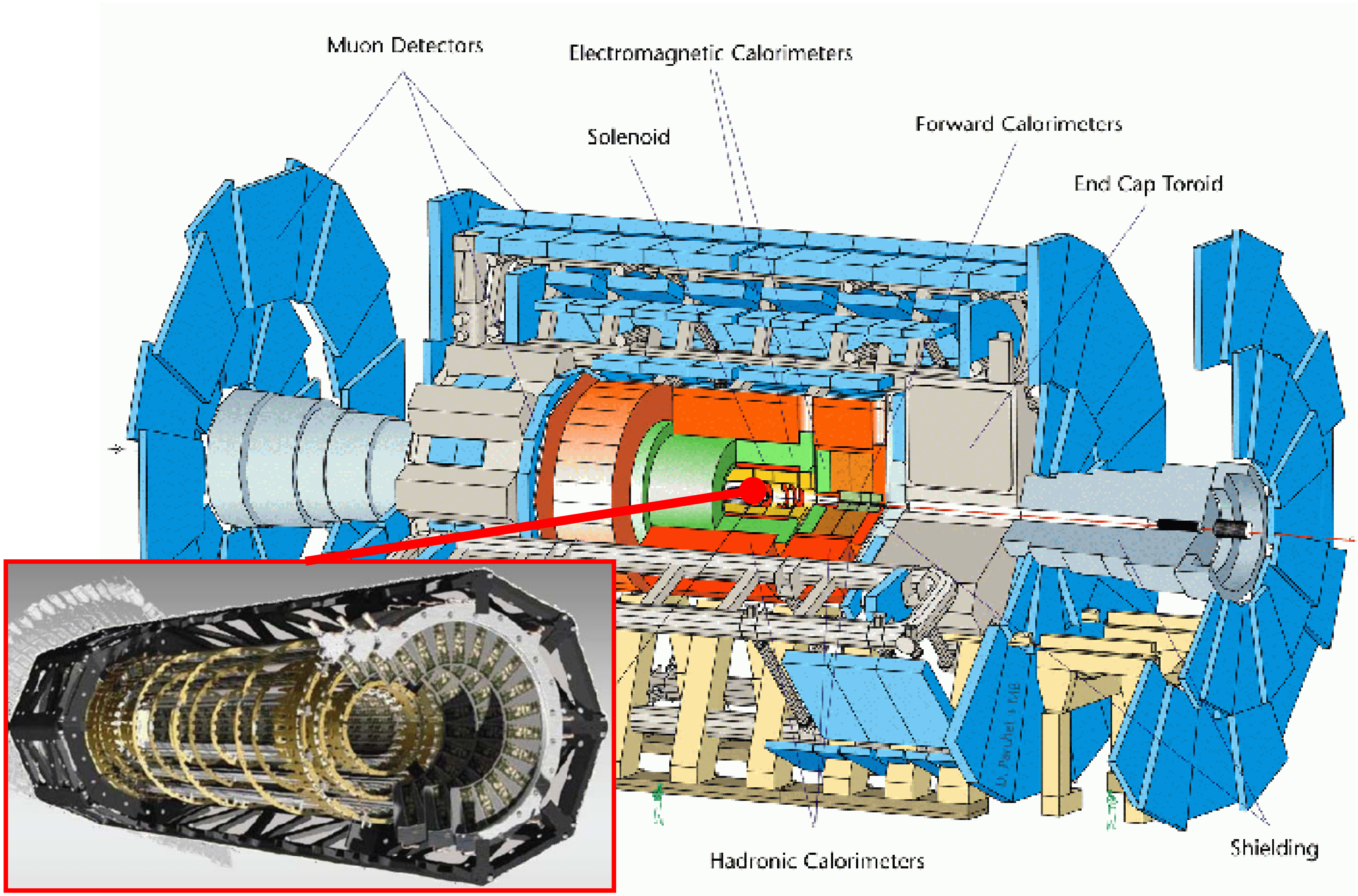
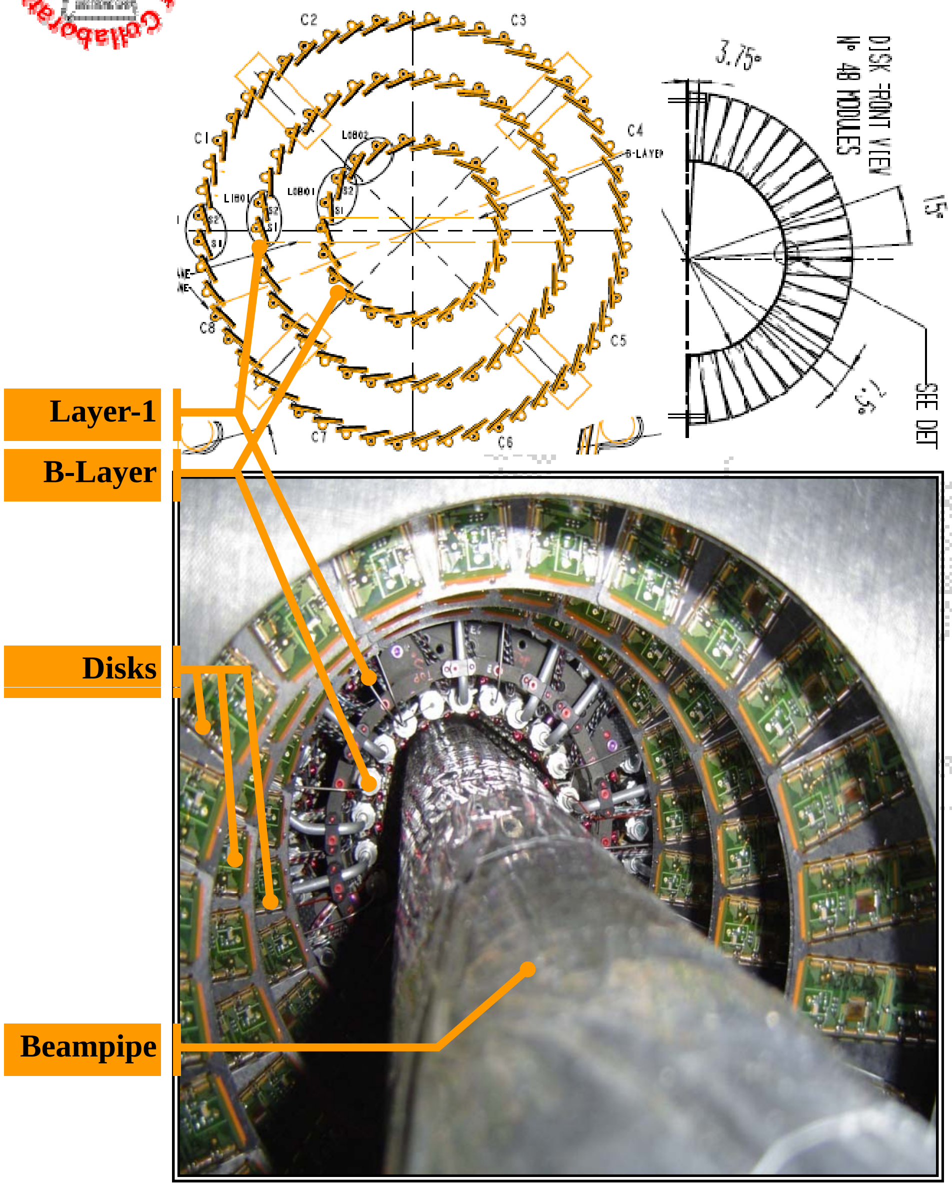
- The LHC environment
- Module structure:
  - sensor, electronics, hybridization
- Production of ATLAS Pixel modules
- Operation:
  - results from test beams and cosmics data

Just some selected topics

A Toroidal LHC ApparatuS



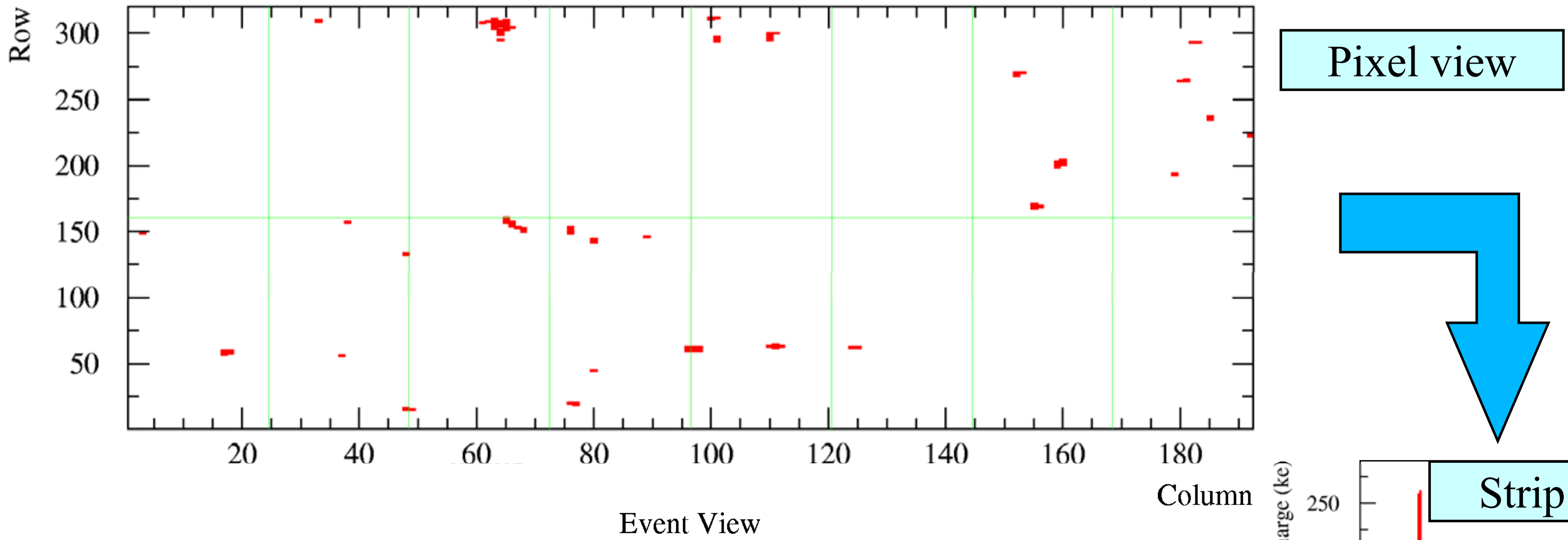
The ATLAS Pixel Detector

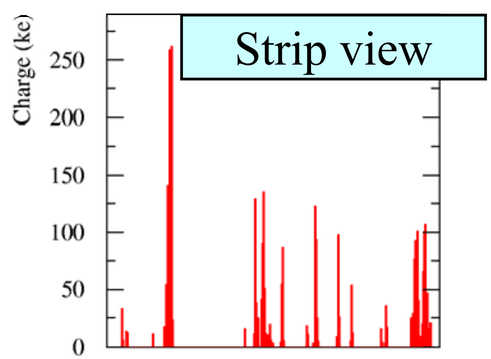


- The Pixel Detector is the vertex detector for the ATLAS experiment.
- It consists of three barrel layers and six disks, covering with three precise measurement points the region up to $|\eta|<2.5$.
- Innermost layer (B-layer) at R=5 cm
- There will be 1456 barrel modules and 288 forward modules, for a total of 80 million channels and a sensitive area of 1.6 m^2.
- Modules will operate in an environment temperature below 0ºC and within a 2T solenoidal magnetic field.
- Barrel module are tilted by 20º in the $R\phi$ plane to overcompensate the Lorentz angle.

Why pixels?

Event in the B-layer at high luminosity

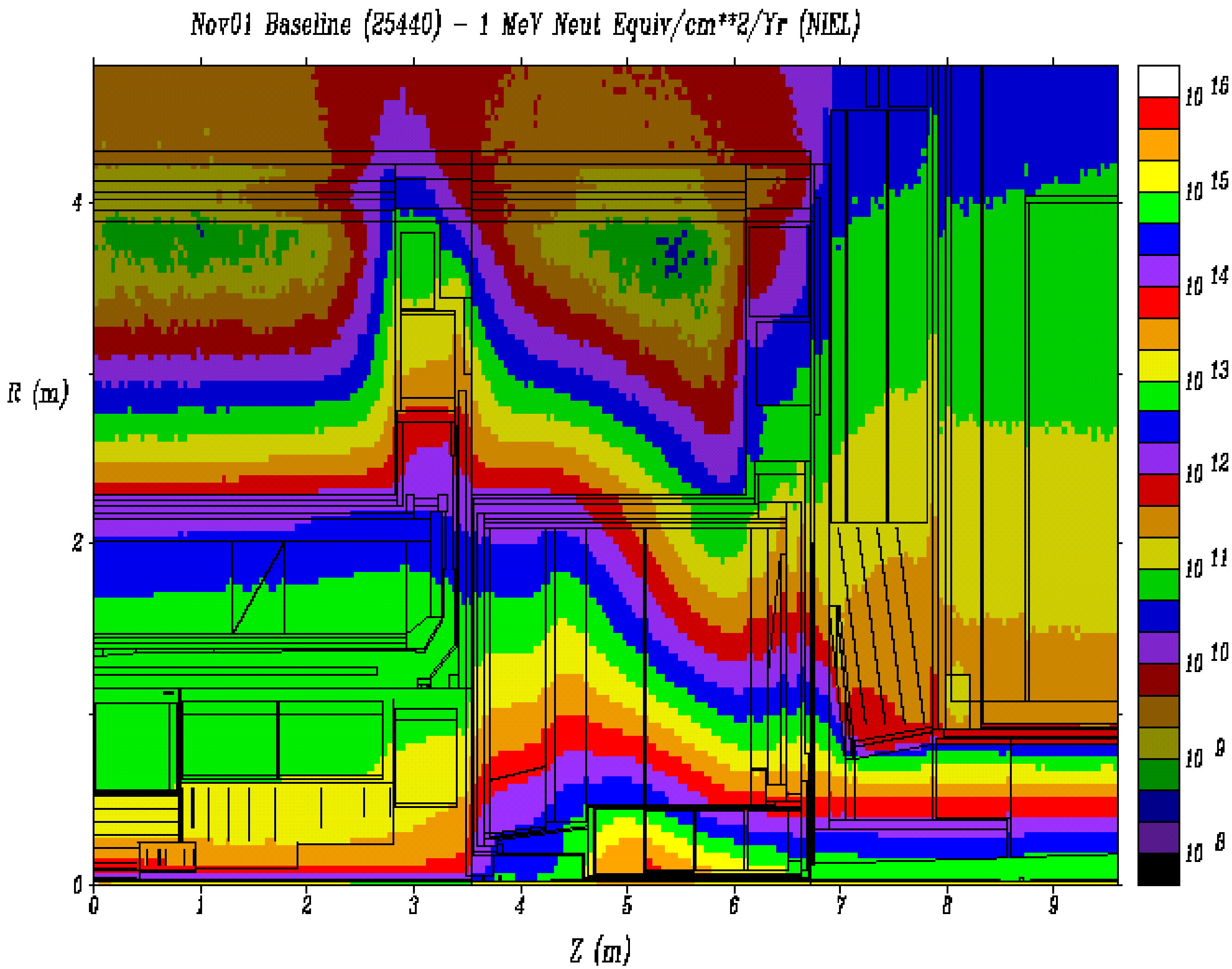




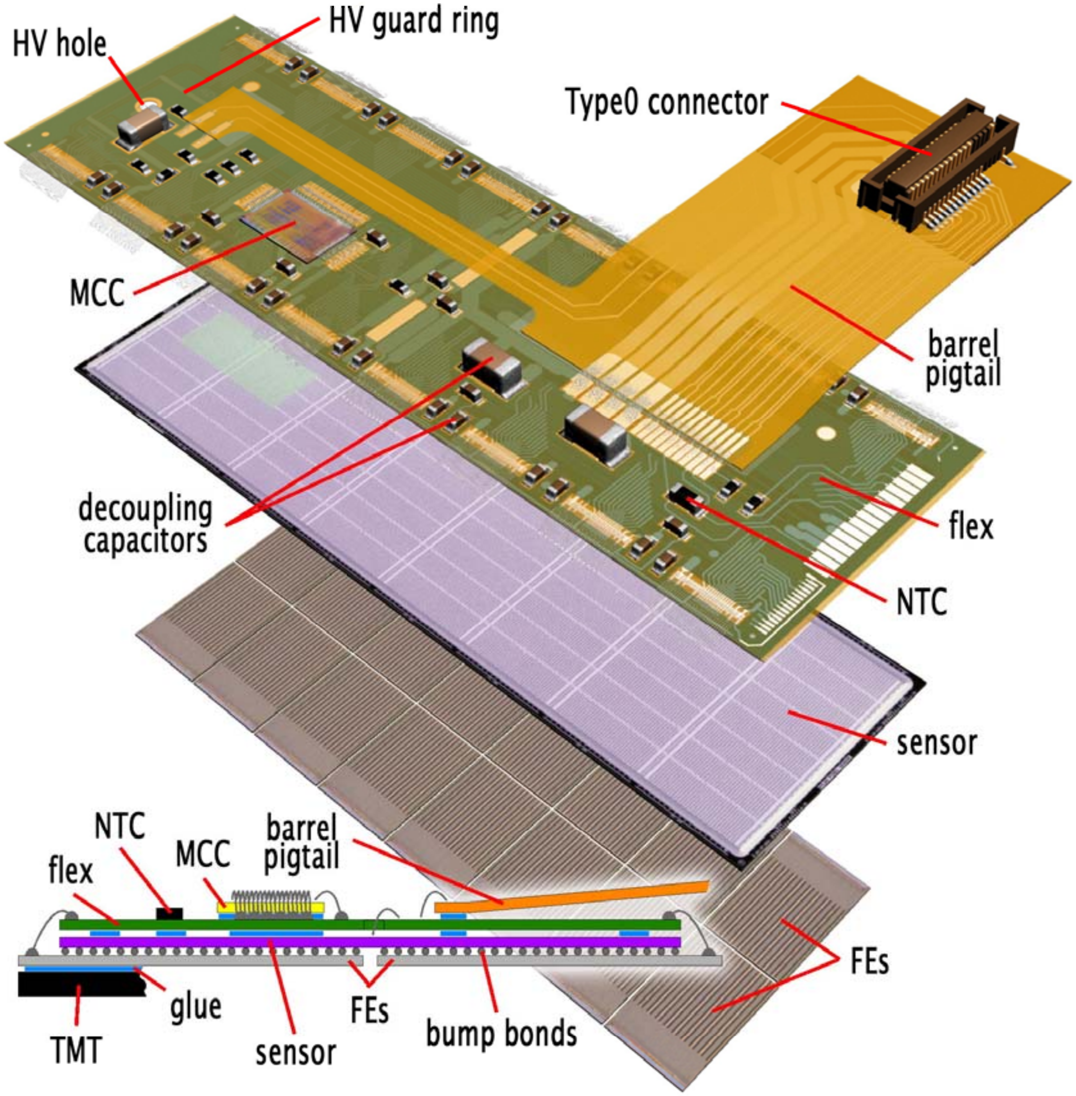
- At 10^{34} $cm^{-2}s^{-1}$ nominal LHC luminosity, there are 23 *p-p* interactions every 25 ns beam crossing:
  - 7×10^{7} particles $cm^{-2}s^{-1}$
  - good granularity and low occupancy are essential for pattern recognition.
  - Precise measurement of *z* for multple vertex separation.

Radiation environment

- External pixel layers will receive a yearly damage from NIEL corresponding to a fluence of 10^{14} n_{eq}/cm^2
- Innermost layer will be a factor two more.
- The requirement is to withstand ten years of operation for the external layers, that is:
  - **NIEL >10^{15} n_{eq}/cm^2**
  - **dose >500 kGy**



Module concept



Self-consistent detector unit.

Sensor (Oxygenated FZ Silicon):

- active area 60.8 × 16.4 mm^2
- 250 μm thickness
- pixel cell 50 μm (RΦ) × 400 μm (Z)
- extended cells (ganged and long pixels) to cover the otherwise dead region between FE chips.

Front-end electronics:

- 16 FE-I3 chips, 0.25 μm IBM technology, with rad-hard design;
- 46080 channels/module

Interconnection by bump-bonding:

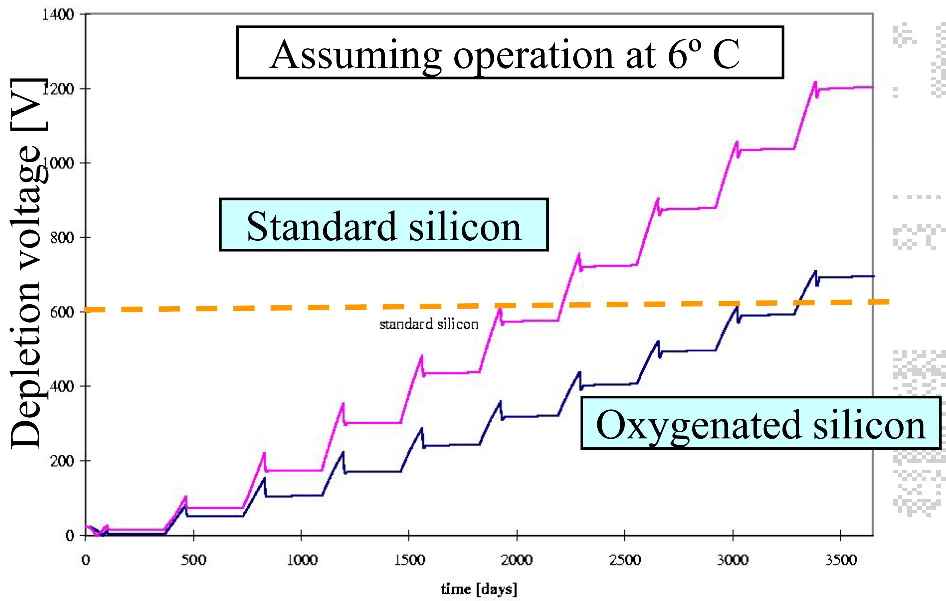
- Solder (IZM, Berlin)
- Indium (Selex, previously AMS, Rome)

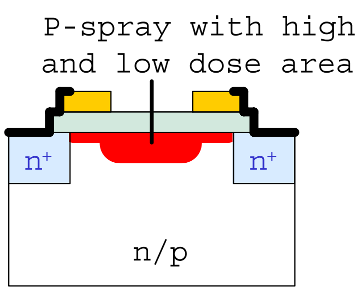
Flex hybrid:

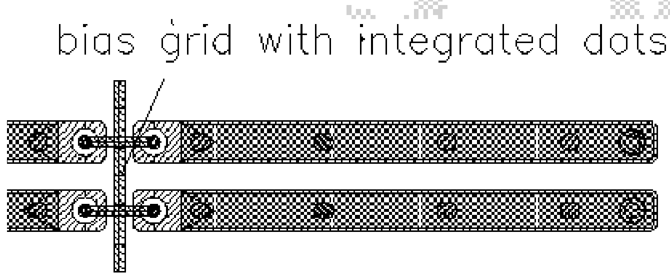
- Module Controller Chip to perform communication and event building;
- local decoupling and temperature monitoring.

The sensor

Rad-hard Sensors

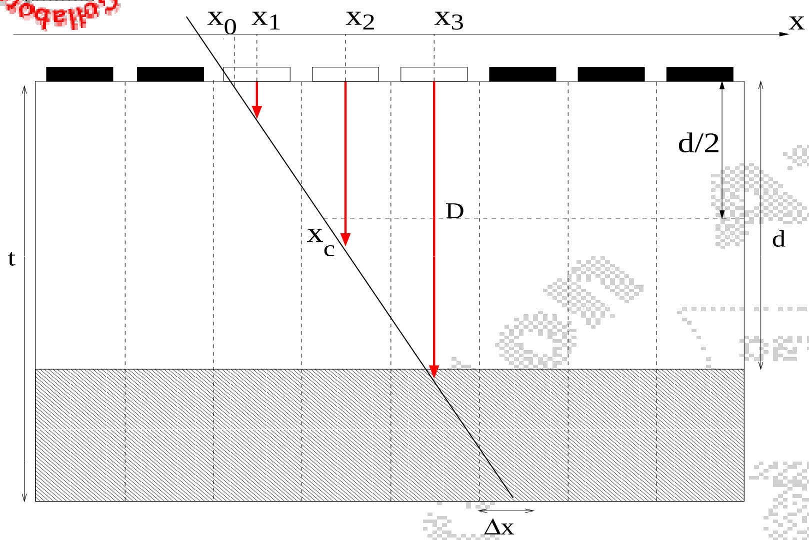




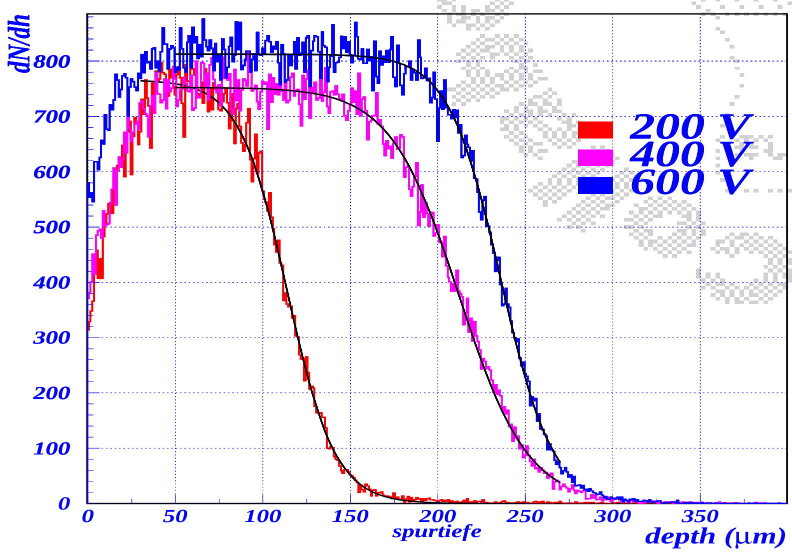


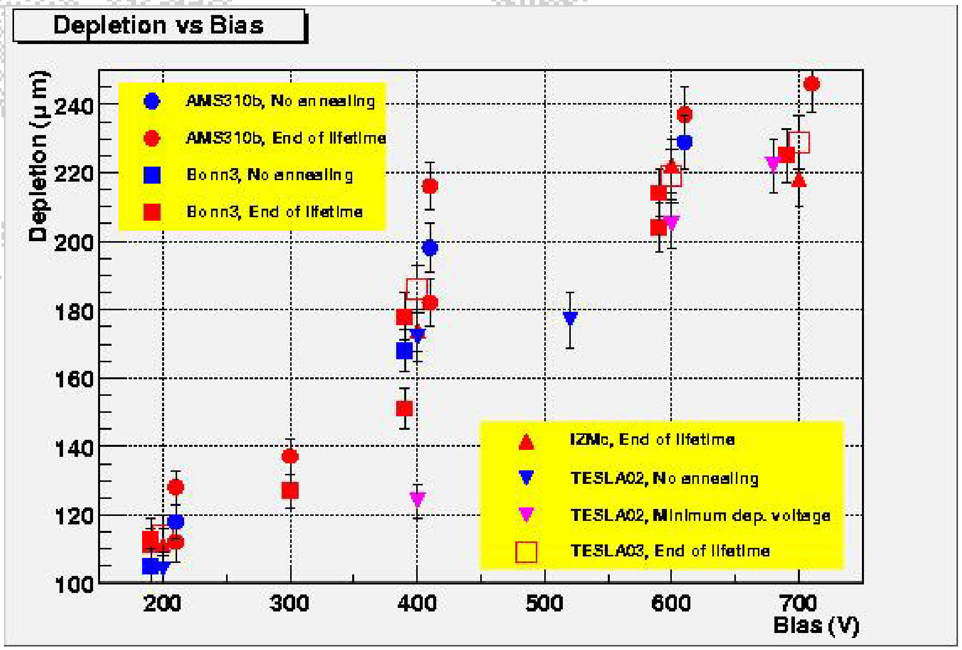
- NIEL damage results in creation of "*p*-type" defects. Substrate will change from low concentration *n*-type to high concentration *p*-type (type inversion):
  - **increased leakage current**
  - **increased depletion voltage**
- The design:
  - ***n*$^+$ over *n*** pixels allow operation under partial depletion after type inversion (max. 600 V to the detector)
  - ***p*-spray** insulation;
  - operation at **low temprature** to keep leakage current at acceptable level;
  - **annealing** during shutdown periods;
  - **oxygenated silicon** is being used, since, according to the results of the ROSE collaboration, it appears to be less sensitive to NIEL damage from charged particles.
  - For sensor testing all pixel can be kept equipotential by a bias grid..
  - Production at **CiS, Germany**, and **ON Semiconductors, Czech Republic.**

Effective depletion depth

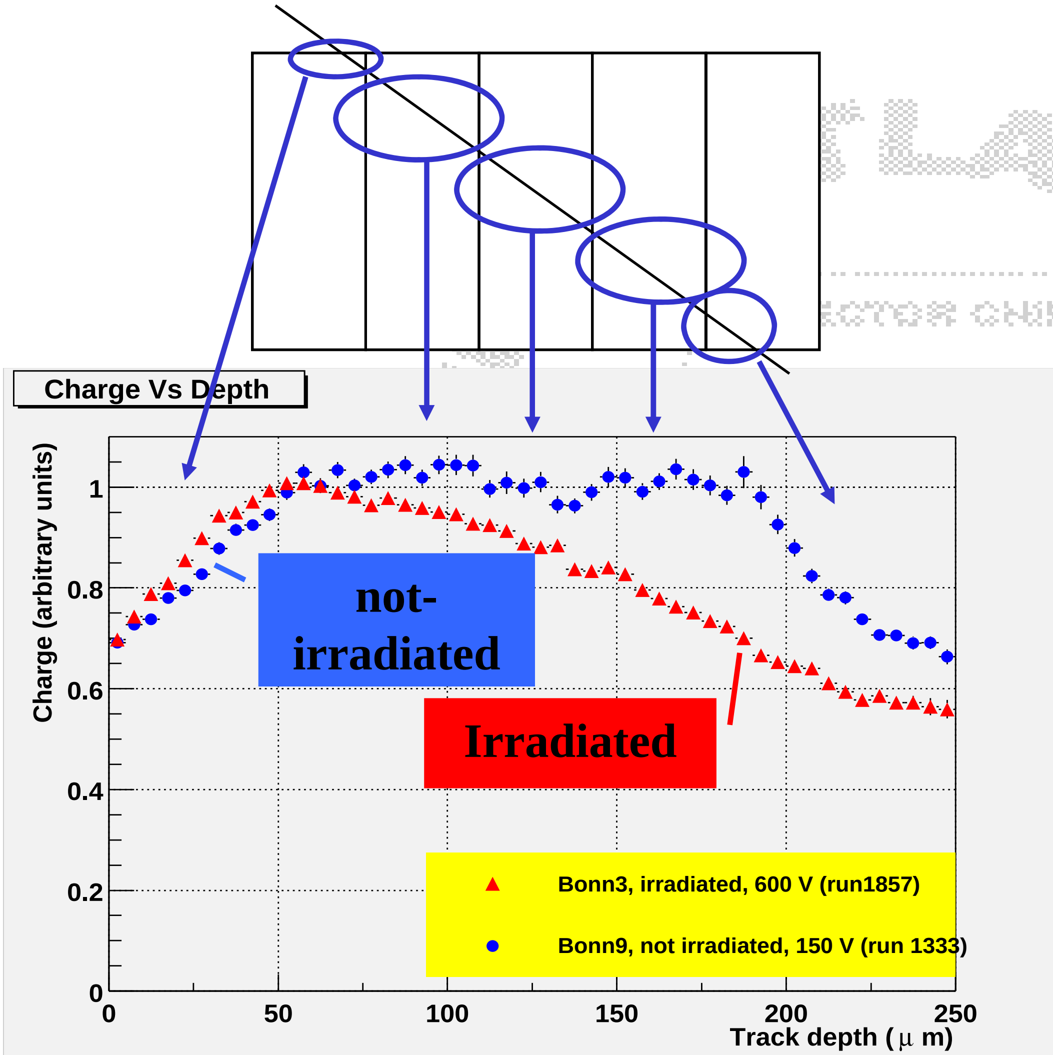


- Tilted tracks cross pixels at different depths.
- The depth of collected hits shows an edge: *effective depletion depth*
  $\Rightarrow$ *depends on the detection threshold.*
- for design radiation damage, **maximum effective depletion depth is reached at 500V**





Trapping



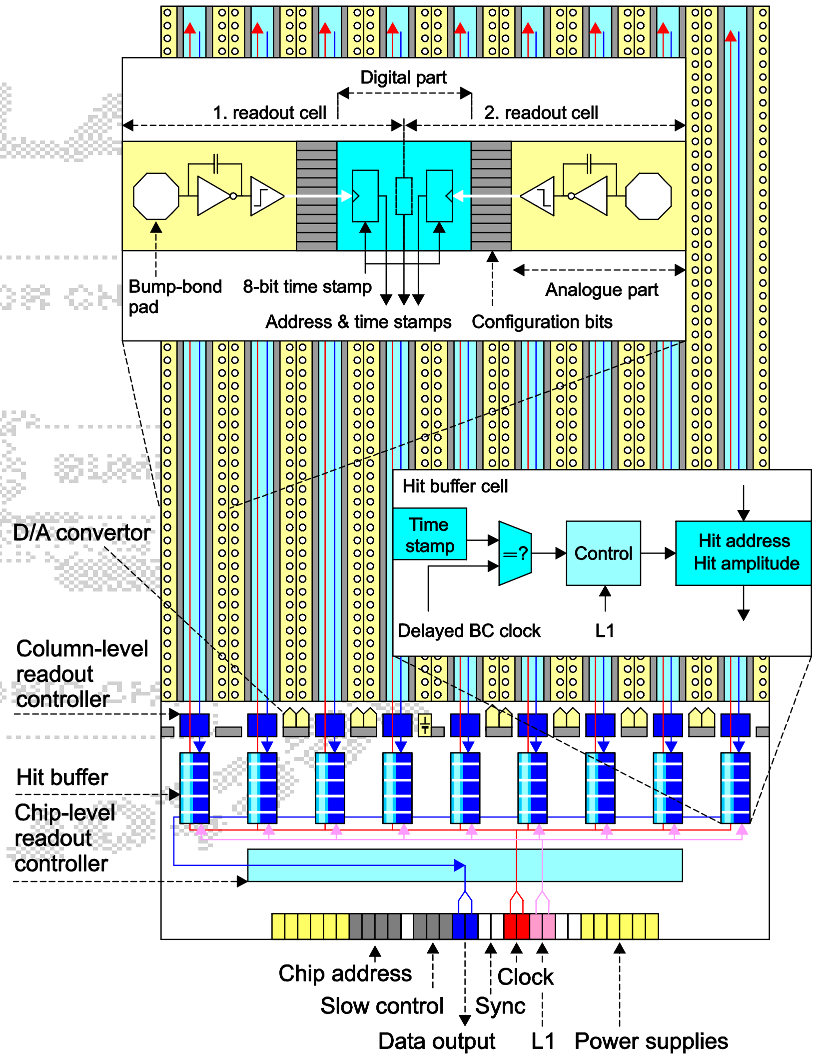
- The same technique of tilted tracks used for the depletion measurement can be applied to measure the trapping of the charge carriers.
- For not irradiated sensors, the collected charge is uniform along the depth.
- For irradiated sensor, the yield as a function of the depth can be translated, via the drift velocity, in a carrier lifetime:
  $\tau_e = 4.1 \pm 0.3 \pm 0.5$ ns
- **80% charge yield after irradiation at nominal dose.**

Read-out electronics

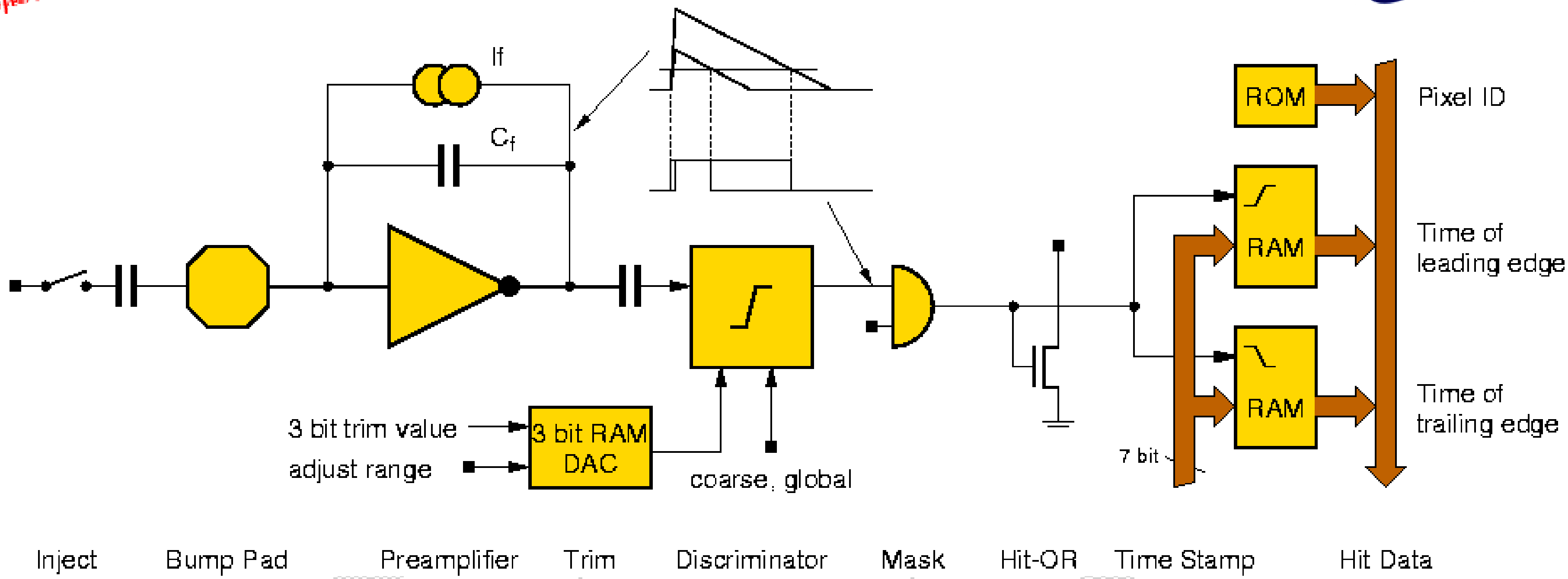
Front-end electronics

- **Front-end** (FE) and **Module Controller** (MCC) chips built in **IBM 0.25 μm** technology, with **6 metal layers**.

- Each front-end contains 18 column of 160 channels
- Readout organized by column pairs:
  - sparse data scan logic
  - 64 memory location for storing hits
  - one serial bus for output to MCC if LVL1 trigger received (~3.2 μs latency)



Front-end electronics: analog cell



- Fast charge amplifier:
  - 15 ns risetime
  - constant current feedback.
  - wide range leackage current compensation (100 nA)
- Fast discriminator with tunable threshold

- Emphasis on **tunability**...:
  - threshold: 7-bit DAC/pixel
  - feedback current: 3-bit DAC/pixel
  - masking individual channel
- ... and **testability**:
  - charge injection circuit
  - self triggering during laboratory tests

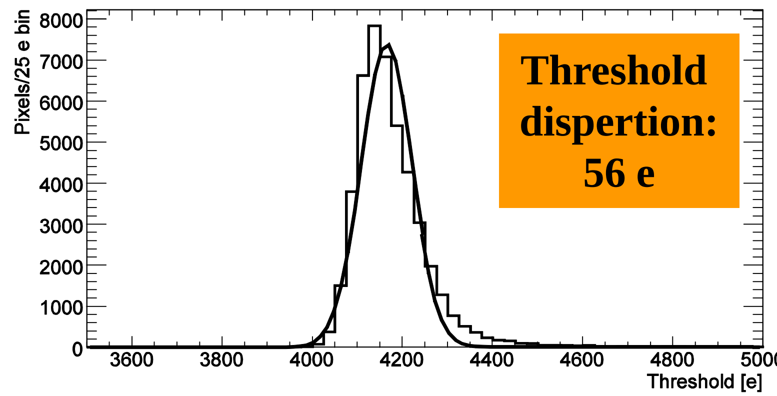
Analog tuning

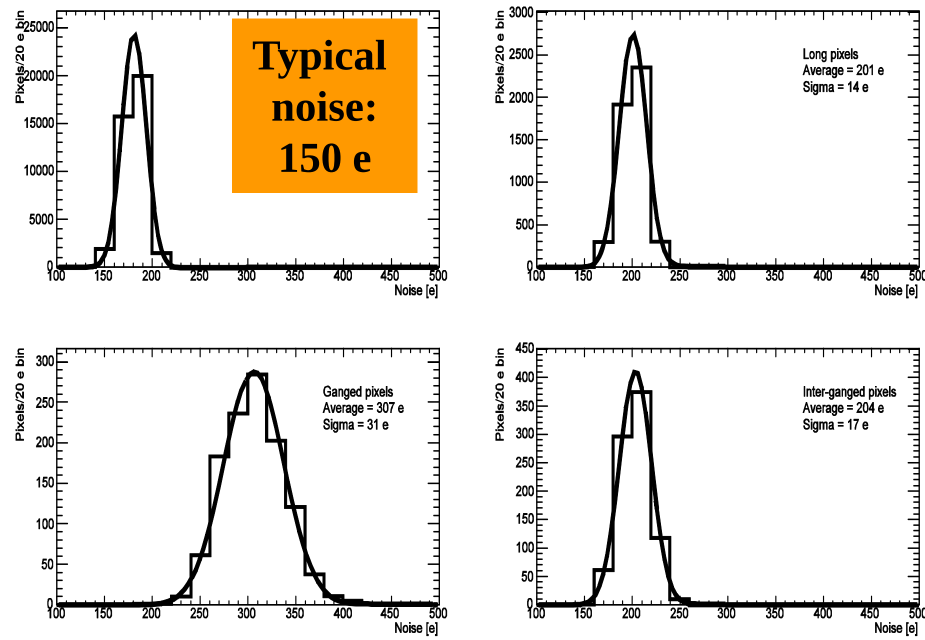
Threshold uniformity is a must:

- uniform efficiency
- no channels with low threshold/noise ratio

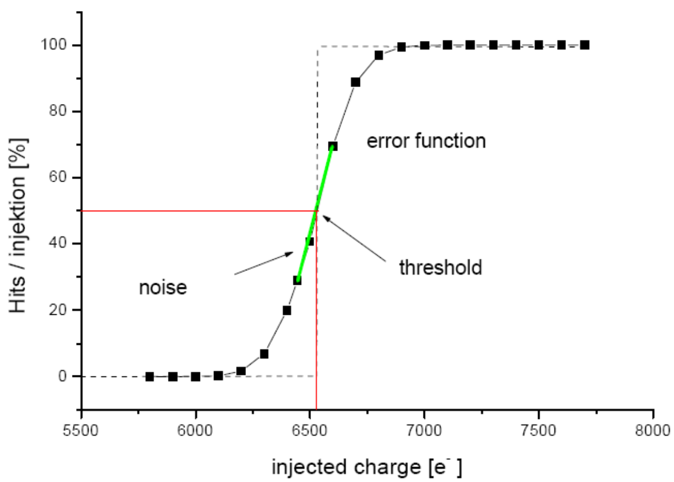
Noise is extremely good:

- does not deteriorate on the whole system
- allows for safe operation down to 3 ke threshold *(maybe better)*
- m.i.p. most probable value is 20 ke



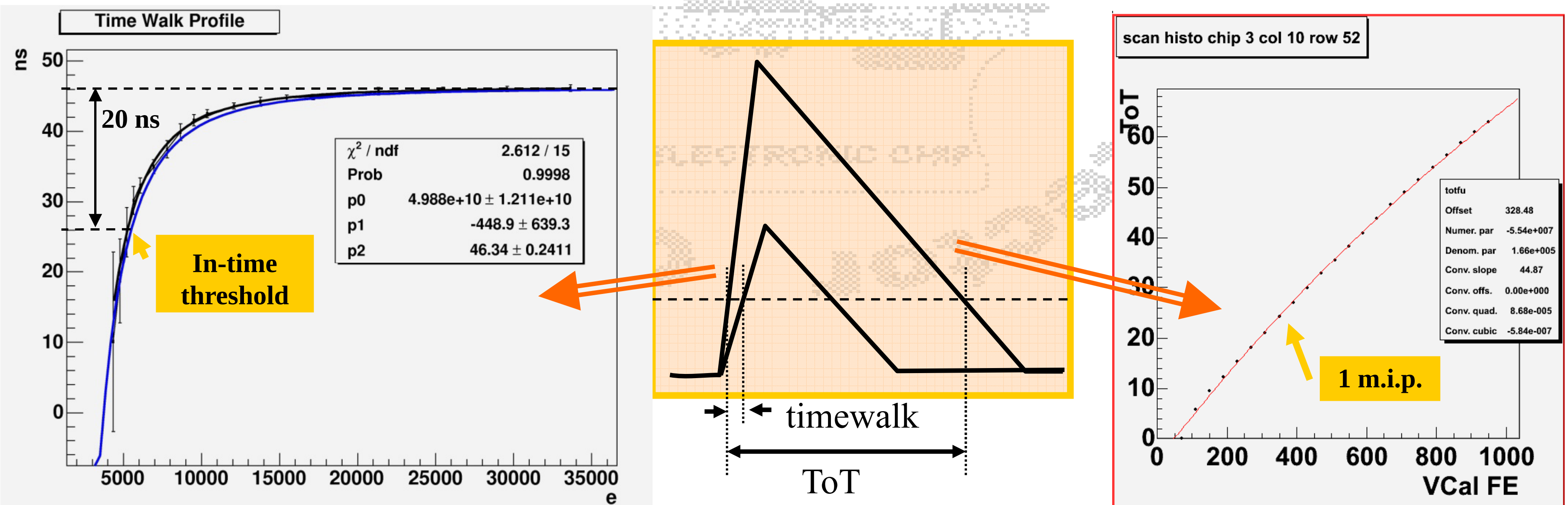


Measurement and tuning from the pixel exitation curve:



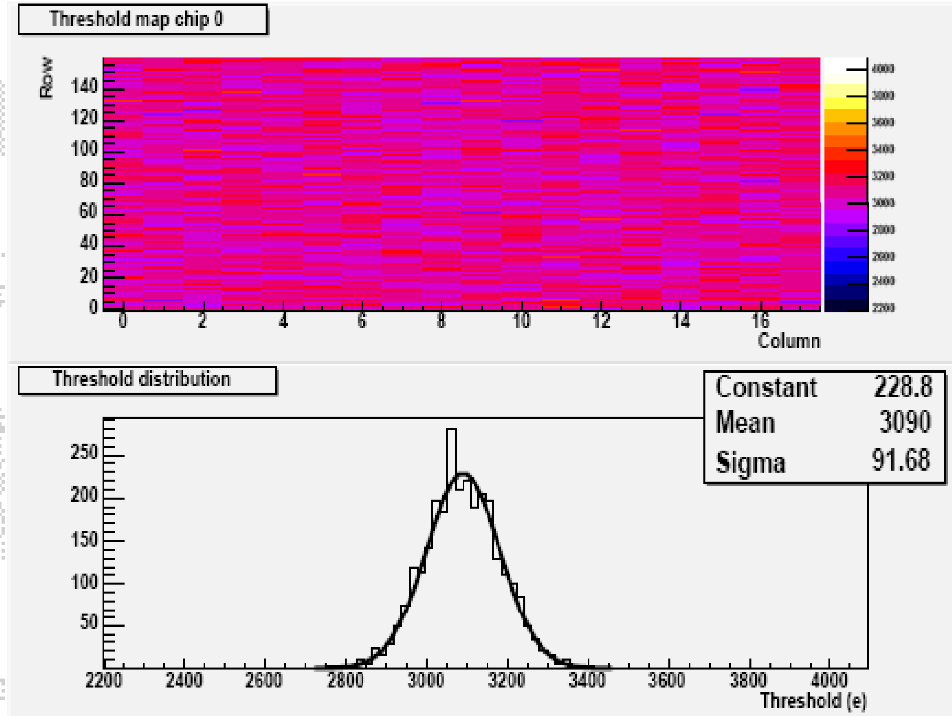
Timing in the pixels electronics

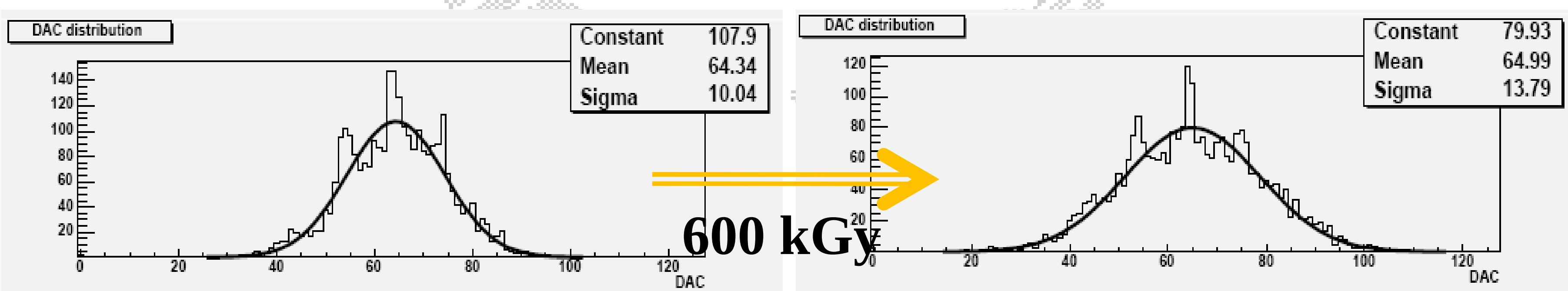
- Ideal pulse shape is almost triangular with fast rise and slow return to baseline.
- Timing of this signal is critical
  1. **Timewalk:**
     - low pulse height signals arrive later than high pulse height;
     - if delay is too high, the pulse is associated to the subsequent bunch crossing.
     - uniform efficiency requires good synchronization.
  2. **Time over Threshold (ToT)** for pulse height measurement
     - used to interpolate position of multi-hit clusters
     - Time over Threshold for a m.i.p. tuned to 30 clock cycles



Electronics irradiation

- All pixel electronics was irradiated to nominal dose with 24 GeV protons.
- Performance are not affected:
  - enough dynamic range to retune after irradiation *(but a reduction of the available TDAC range is visible)*
  - input circuit able to sustain the additional leakage current
  - no loss in timing performance
  - noise increases to ~250 e *(compatible with increased leakage)*

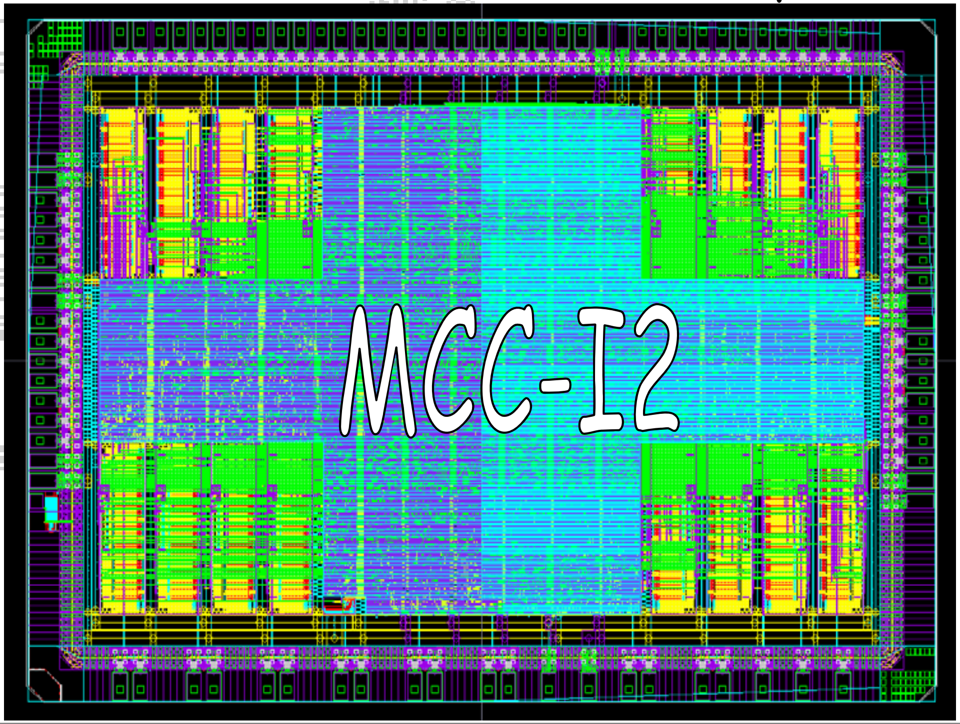




Module Controller Chip

- The Module Controller Chip:
  - distributes clock, commands and trigger signal to the FE
  - collects FE information and performs event building
  - two serial links with maximum speed 80 Mbps each
- Designed to assure resistance to Single Event Upset:
  - all critical registers are tripled and use a majority decision logic;
  - in the FIFO's, where data are stored, a bit-flip safe encoding is used to unambiguously disentangle hits (for which a small corruption rate is acceptable) from event separators (whose loss would cause DAQ misalignment)
- At CERN irradiation facilities MCCs were run for the equivalent **100000 s at the B-layer**, without the need to reconfigure the chip.

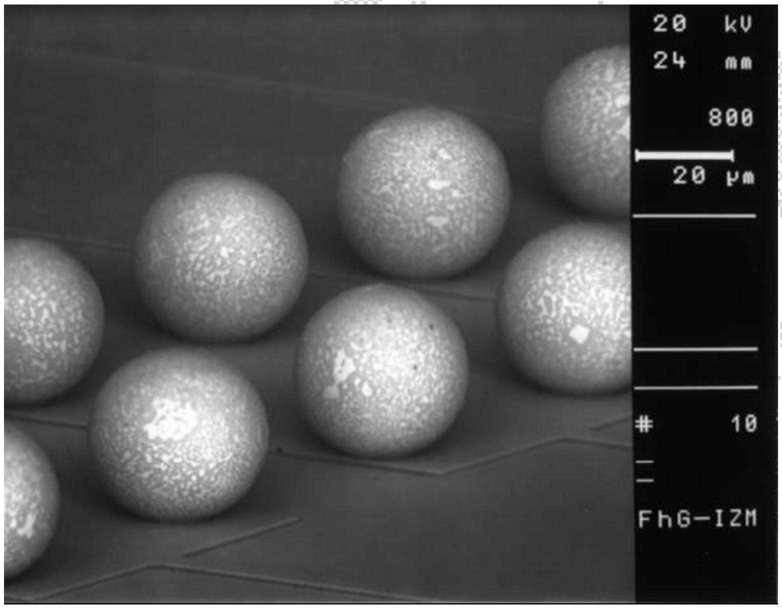
No. of transistors:	880 k
Dimensions:	6840 x 5140 μm^2

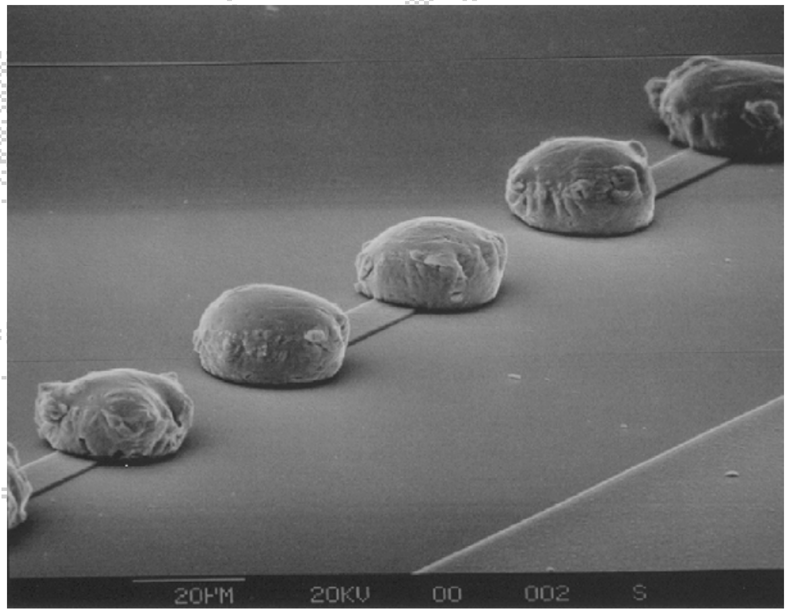


Hybridization

Bump bonding technologies

- **Solder bumps**
  - manufacturer: IZM-Berlin
  - excellent electrical connection
  - very strong, ...but rigid
  - complex metallization process
    → more expensive.
- **Indium bumps**
  - Manufacturer: Selex-Rome (ex Alenia)
  - good electrical connection
  - softer, ...but flexible
  - simple vapour deposition
    → cheaper.





Neither of the firm could guarantee the processing rate needed for full production

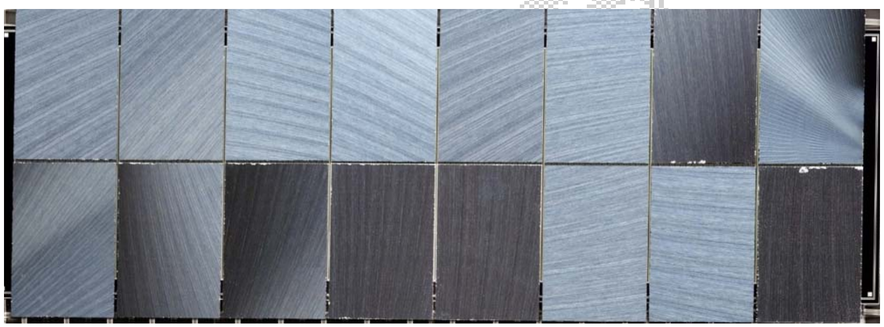
Both techniques have shown an acceptable yield

The flip-chip process

- Bump are deposited on full FE wafer (700 µm thickness)
- They are then covered by photoresist and grinded to 200 µm
- FE chips are singulated and **individually tested**

- Sensor treatment depends on the technology:
  - only under-bump-metallization for solder
  - full bump deposition for indium

- 16 FEs are chip-flipped to one sensor element
- Modules are accepted if **less than 150 bad connections (0.3%)**



Critical step in module production:
• *module efficiency* =
(*chip efficiency*)^{16}
• last time when a repair is possible

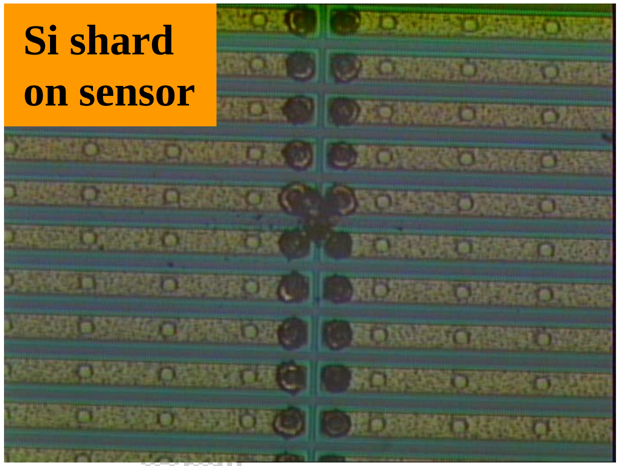
Bumping quality assessment

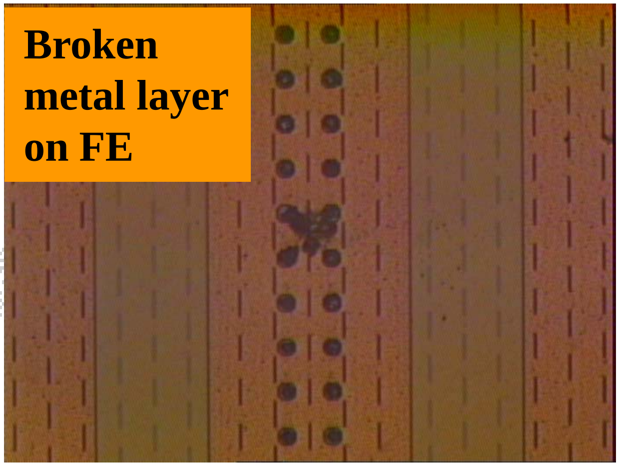
- **Mechanical damage:**
  1. Electrical test of **FE's** basic functionalities:
  2. I-V curve of **sensor**

  due to silicon shards or just bad handling
- **Bump quality:**
  1. X-ray inspection of bumped modules
     - especially useful for solder bumps
  2. Noise measurements
     - **disconnected pixels** do not see the detector load
     - **shorted pixels** have low charge efficiency
     - can be used also on the assembled module to monitor developement of defects during the detector lifetime.
- **No observation of electrostatic damage.**
- Damaged FE lifted off and the module reworked:

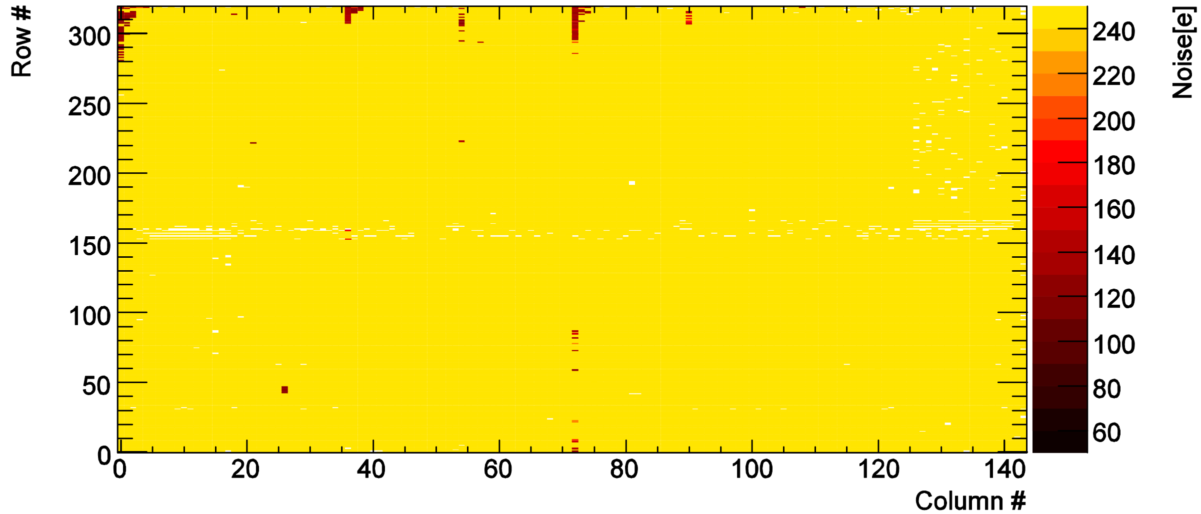
  reworking capability was essential to reach an acceptable yield

  (by the way I have ~100 leftover modules to sell☺)

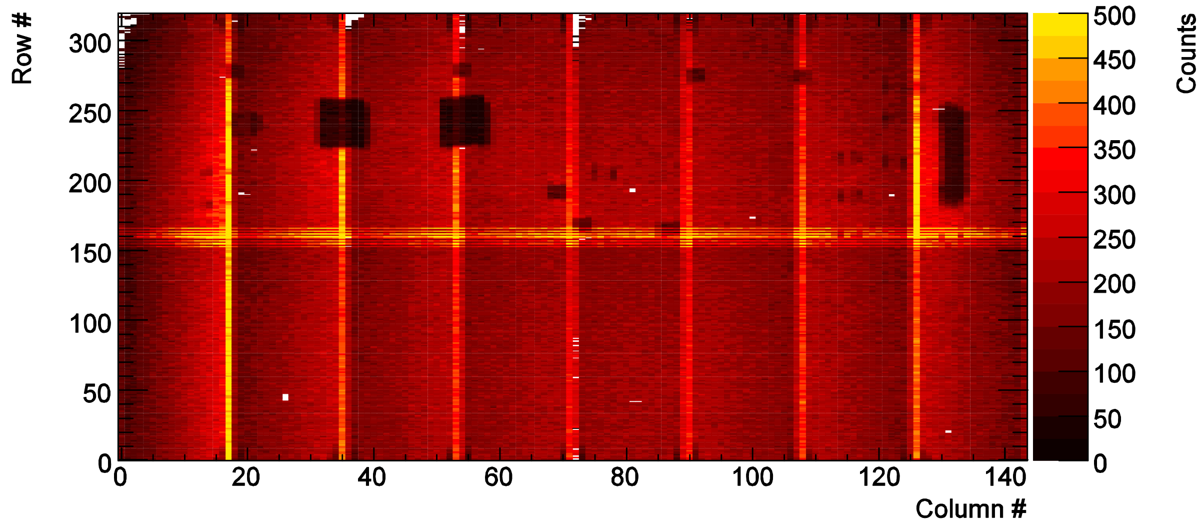




Noise measurements



Noise map
HV off



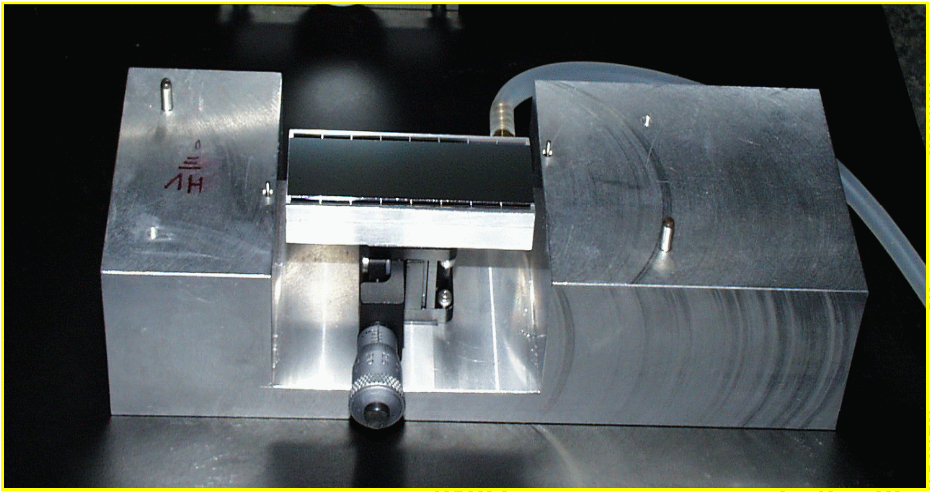
Hitmap
^{241}Am
60 keV X-ray

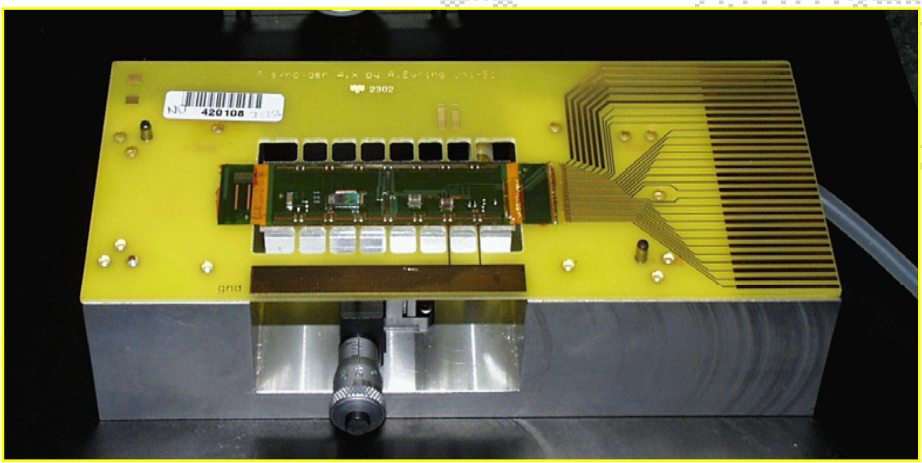
Bumping yield

	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1468		1157		2625	
Rejected	172	11.7%	35	3.0%	207	7.9%
Accepted (total)	1296	88.3%	1122	97.0%	2418	92.1%
Accepted as delivered	1101	75.0%	1035	89.5%	2136	81.4%
Accepted after reworking	195	13.3%	87	7.5%	282	10.7%

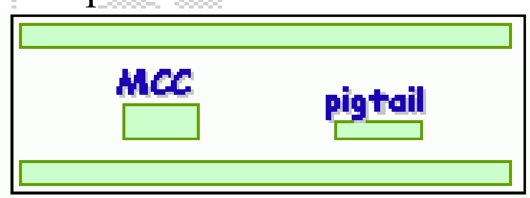
- Sensor damage rate 3% for both technologies
- Indium is more sensitive to the shard contamination:
  - lower bump height
  - pressure applied during the flip-chip process
- If a module is submitted for reworking:
  - **rework efficiency is >95%**
  - **connection quality as good as a not reworked module.**

Hybridization part 2: Flex Hybrid





- The MCC, decoupling capacitors and temperature sensors and resistors needed by the LDVS buffers are mounted on flex hybrid (Dyconex, CH) which is glued on the backside of the sensor.
- A pigtail is later attached to the flex, in order to provide electrical connection to the outside.
- Glue pattern is chosen to:
  - provide a solid substrate for wire bonding,
  - minimize the effect of CTE mismatch between silicon and kapton.

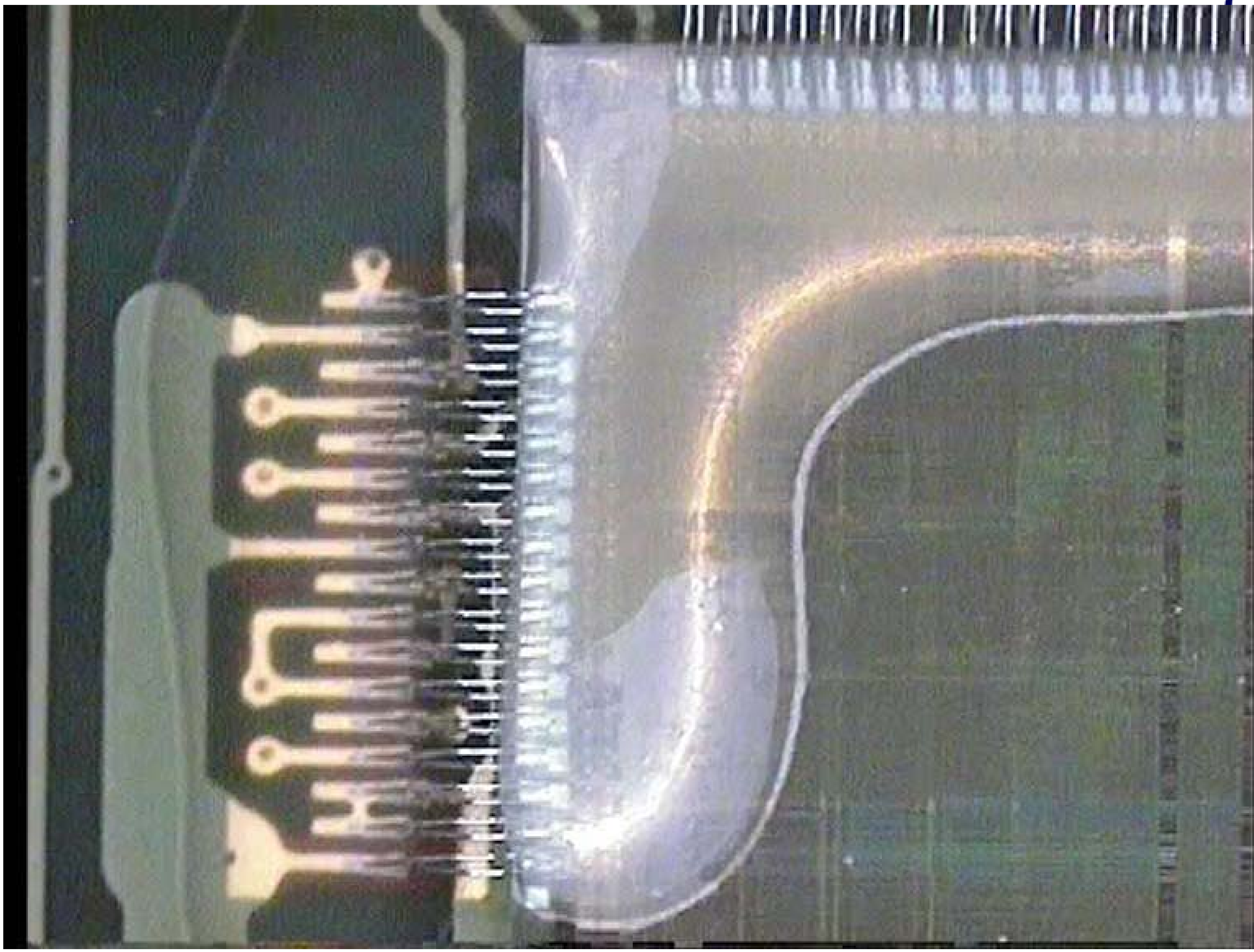


few prototype solder bump modules delaminated because of a too strong connection between the components: flex, module, thermal support

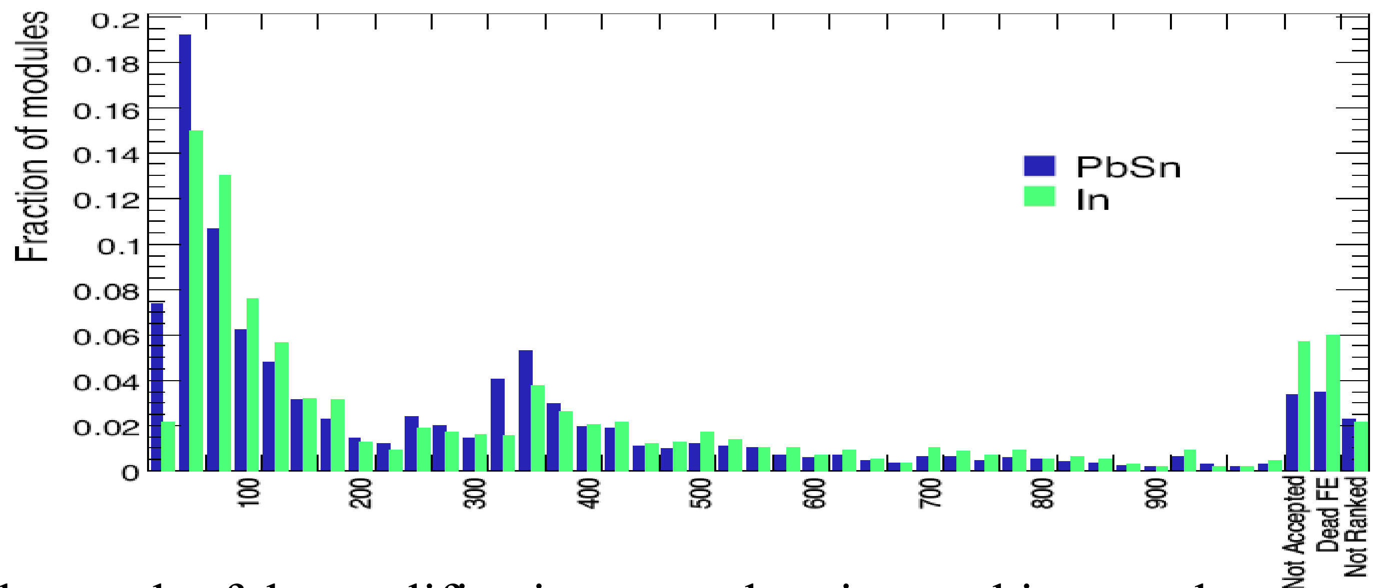
Module qualification

- After the assembly and wire bonding to the flex hybrid module are fully characterized to check their operability in ATLAS:
  - threshold tuning and bad pixel search at room temperature
  - thermal cycles between -30 ºC to 20 ºC:
    - **mechanical stress of the assembly** → ***problems in assembly procedures***
  - check of bad pixels at room temperature
  - full characterization at operating temperature -10 ºC:
    - range of MCC end FE operating voltages
    - threshold and feedback current tuning → ***DAC fingerprint***
    - timewalk and crosstalk measurements
    - data taking with a ^{241}Am source to map noisy and dead channels.
- Characterization procedure requires many hours *(days)* of operation and is a sort of soft burn-in:
  - **no effect of infant mortality seen**

Potting problem on MCC



Module Selection



- The result of the qualification procedure is a ranking number:
  - dead channels
  - weigthed deviation from "normal" behaviour
  - penalty for non conformity, reworking other weaknesses
- **Total fraction of faulty channels in installed detector is 0.2% (0.07% in B-layer)**
- **Module assembly yield >90%**

Module Yield

	Indium		PbSn		Total	
	Modules	Fraction	Modules	Fraction	Modules	Fraction
Assembled	1190		1122		2312	
Accepted	1025	86.1%	1075	95.8%	2100	90.8%
b-layer quality	281	23.6%	445	39.7%	726	31.4%
not b-layer quality	744	62.5%	630	56.1%	1374	59.4%
Not accepted	165	13.9%	47	4.2%	212	9.2%
Ranking > 1000	68	5.7%	10	0.9%	78	3.4%
at least one dead FE	71	6.0%	10	0.9%	81	3.5%
testing not completed	26	2.2%	27	2.4%	53	2.3%

Detector operation (1):
Test beam studies

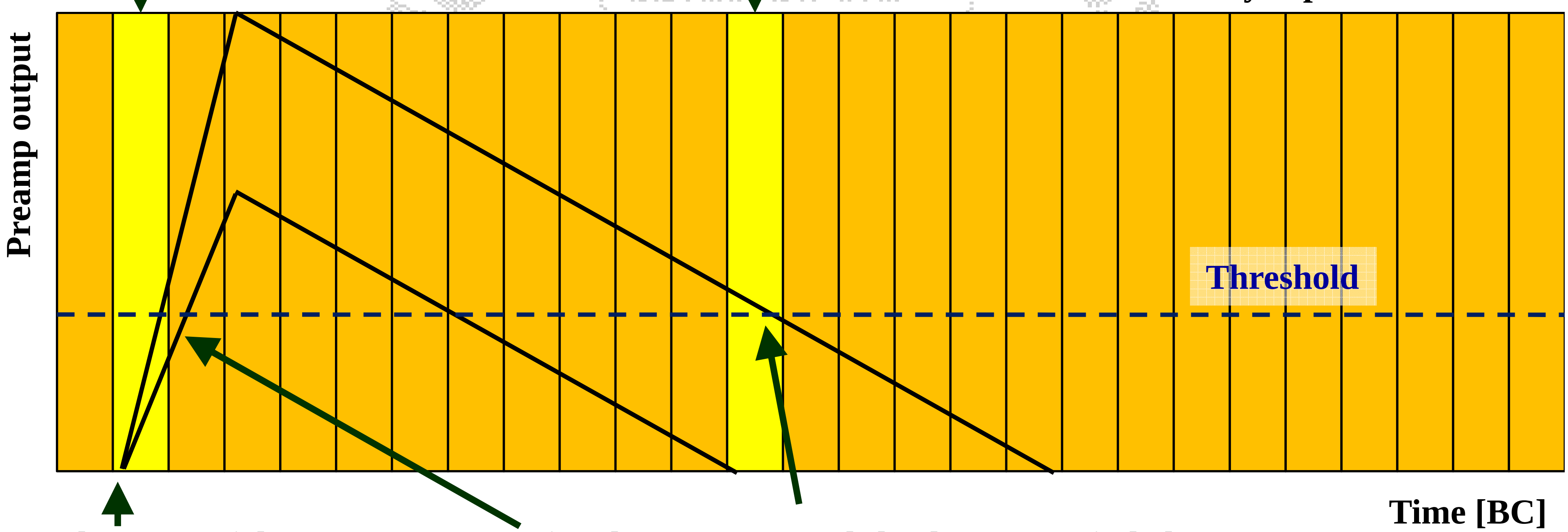
Time: analog vs digital views

The Clock Cycle (≅BC) during which the threshold crossing happens defines the event to which the hit is attributed

The Clock Cycle at which the second threshold crossing defines the pulse height. ONLY NOW THE HIT IS STORED IN THE FE READOUT MEMORY...

Digital view

...where it waits until the LVL1 latency expires



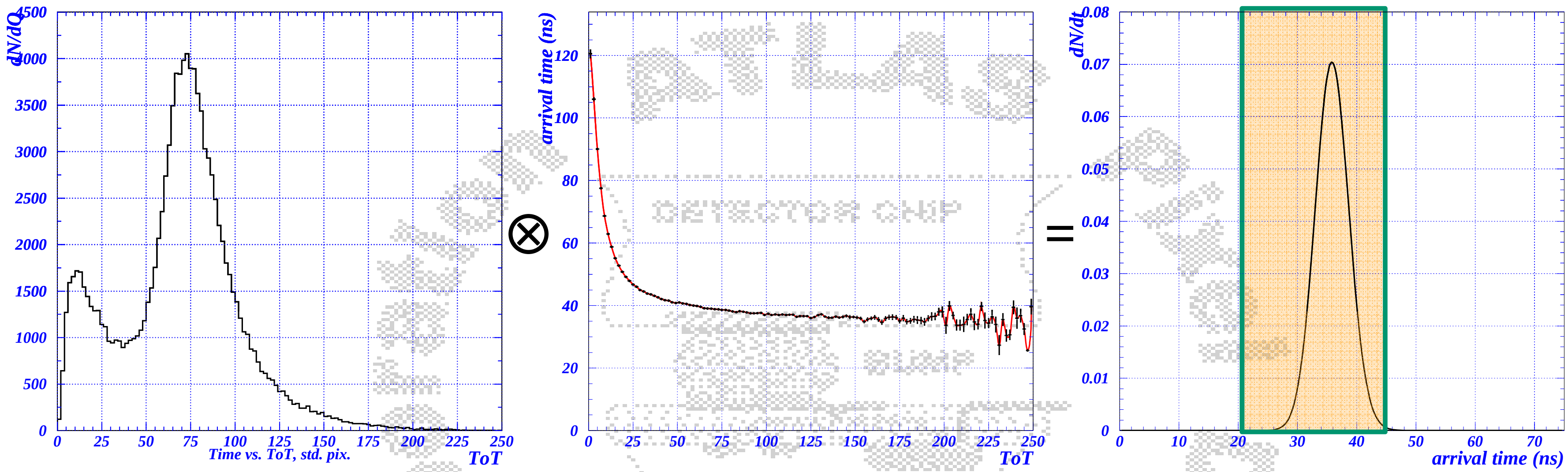
When a particle crosses the detector the signal starts to rise

Some time later (*timewalk*) it reaches the theshold

And slowly goes again below threshold, after a time proportional to pulse height

Analog view

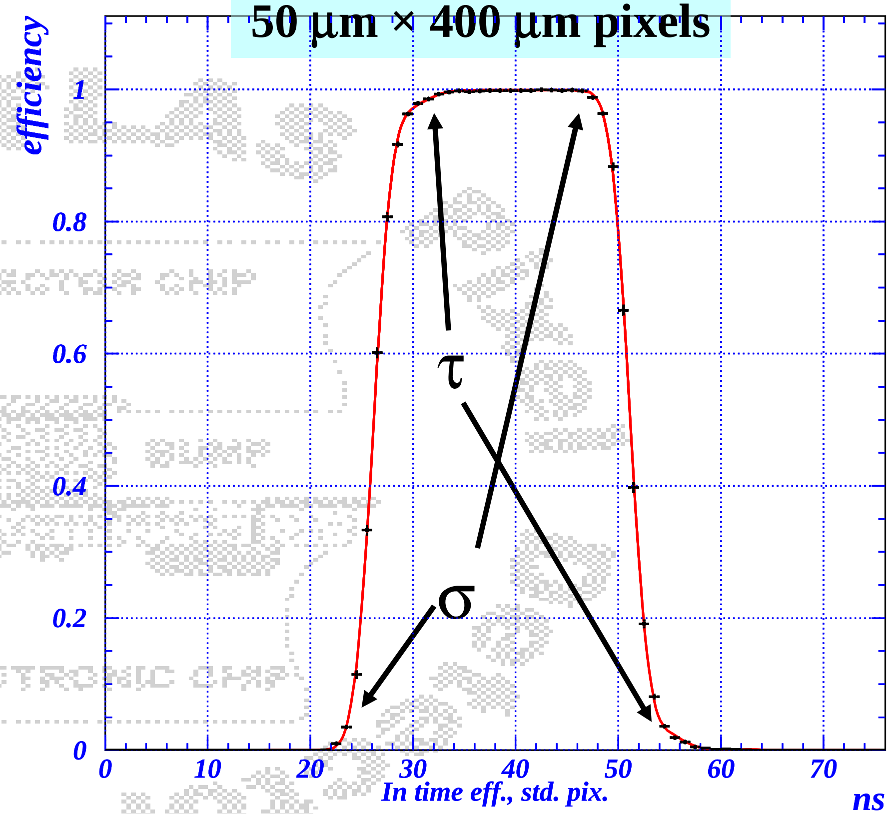
In-time efficiency measurement



- Due to timewalk, it is not enough to quote an absolute efficiency (probability to have a cluster matching the track extrapolation),
- but it is necessary to provide the fraction of clusters which can be collected within one 25 ns level 1 interval.
- In principle that can be computed by making a convolution between the arrival time as a function of the charge and the hit charge distribution and integrating it within a 25 ns box.

- The efficiency as a function of the 25 ns box can be measured directly in test beam.
- The scan to find the position of the interval which maximize the efficiency is simply done by measuring the difference in time between particle crossing and clock edge.
- The fitting function assumes a time distribution given by the convolution of an exponential and a gaussian *(no special reason, it just looks fine…).*
- A most important aspect is the width of the maximum efficiency plateau, which provide the margin of operation at the LHC.

FE-I1 single chip, 50 µm × 400 µm pixels



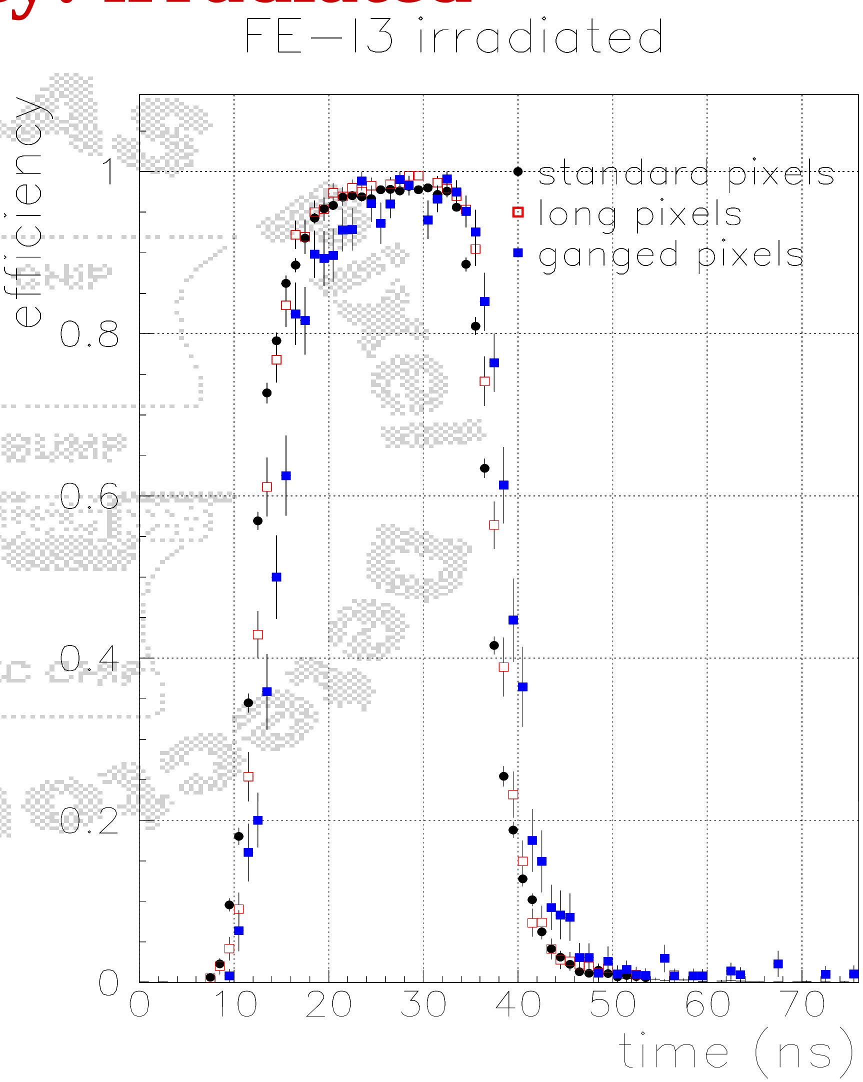
ε [%]	τ [ns]	σ [ns]	0-hit [%]
99.87	0.73	2.09	0.10

In-time efficiency: irradiated

- 7 irradiated production modules have been tested in 2004.

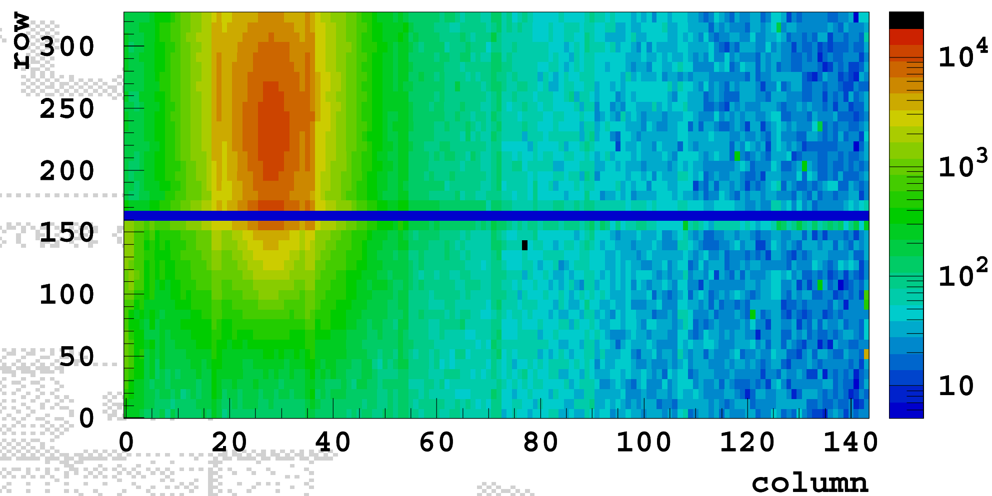
efficiency	97.8	±0.7 %
no hits	1.5	±0.4 %
timewalk losses	0.7	±0.3 %
plateau size	9.7	±1.1 ns
masked	O(10^{-4})	

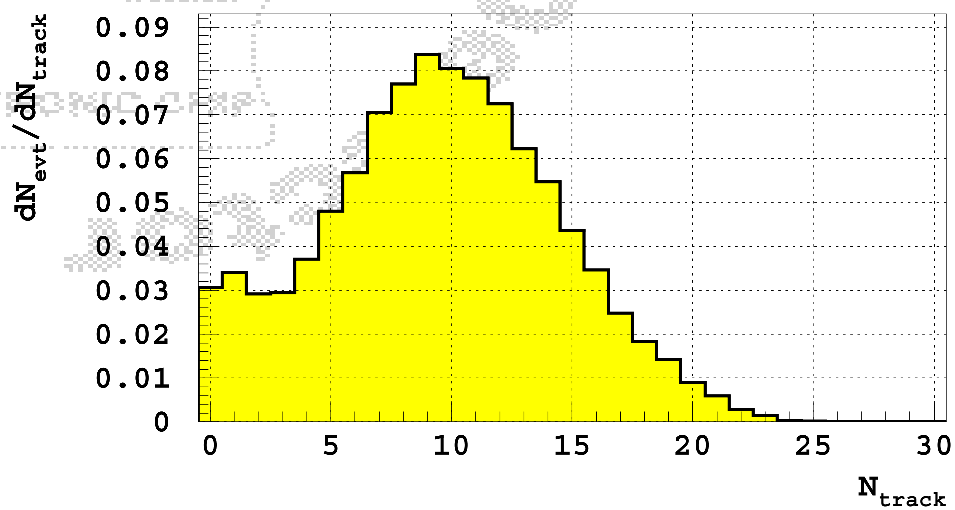
- **Efficiency is above the TDR requirement (97%).**
- **Plateau size is acceptable.**



High intensity operation

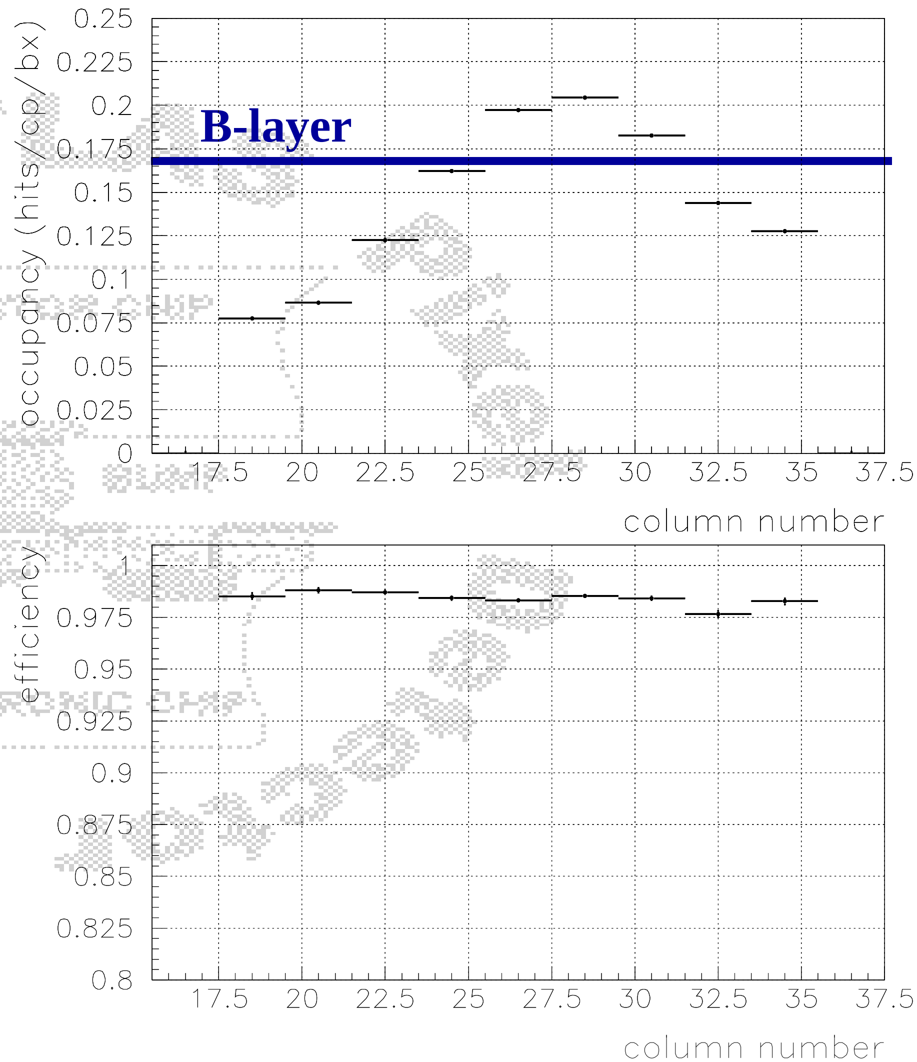
- Single particle tests are not enough to assess real efficiency.
- It depends on the **occupancy:**
  - pixel dead time
  - speed of sparse data scan
  - filling of local memory buffer
- **Special high intensity runs**:
  - CERN SPS H8 beam line
  - local intensity of the ebeam comparable with LHC
  - but limited on a single chip size
  - reconstruction with a telescope of pixels
- Efficiency as a function of the occupancy per column pair per bunch crossing (hits/cp/bx):
  - readout is arranged in column pairs





Efficiency vs. Occupancy

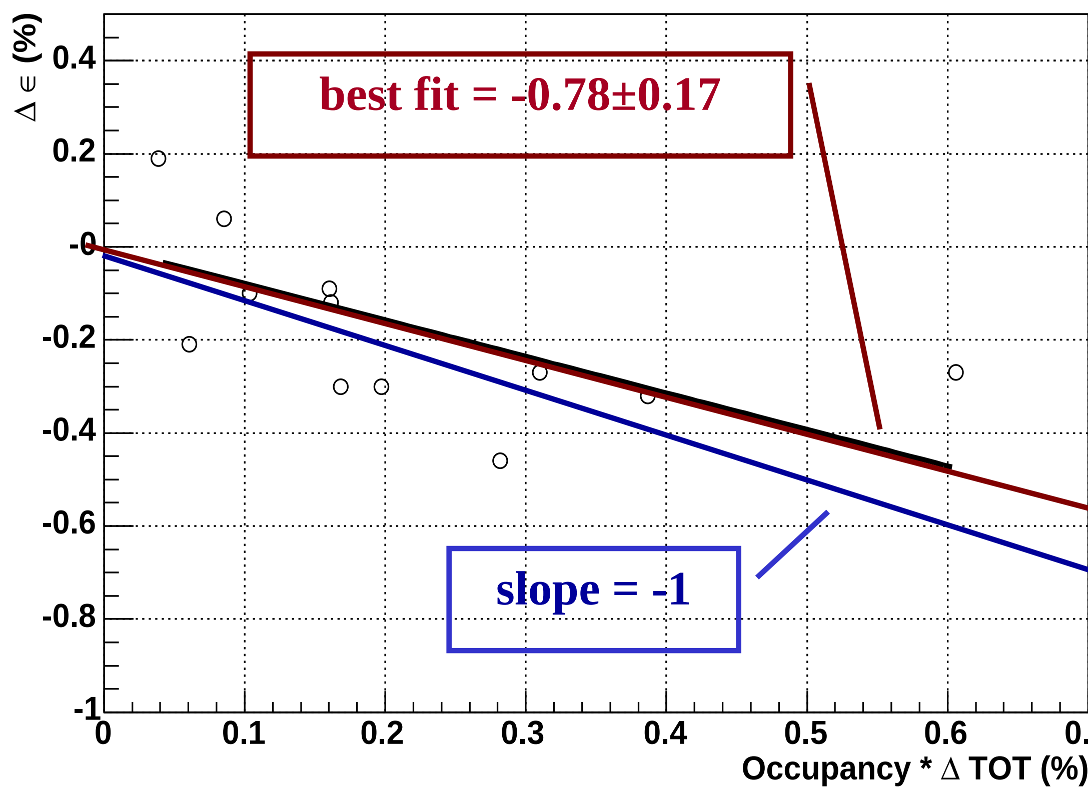
- Default (realistic) running conditions
- Nominal tilt angle of 15 degrees.
- **Max occupancy: 0.20 hits/cp/bx**
- **B-layer at LHC: 0.17 hits/cp/bx**
- **Efficiency (spread over 3 devices): 98.2±3.5%**
  - **consistent with the detection efficiency**
  - **independent on the hit rate.**



- **But how much room is left?**
  - No possibility to increase intensity of SPS beam;
  - Other tricks to stress the system

Dead time losses

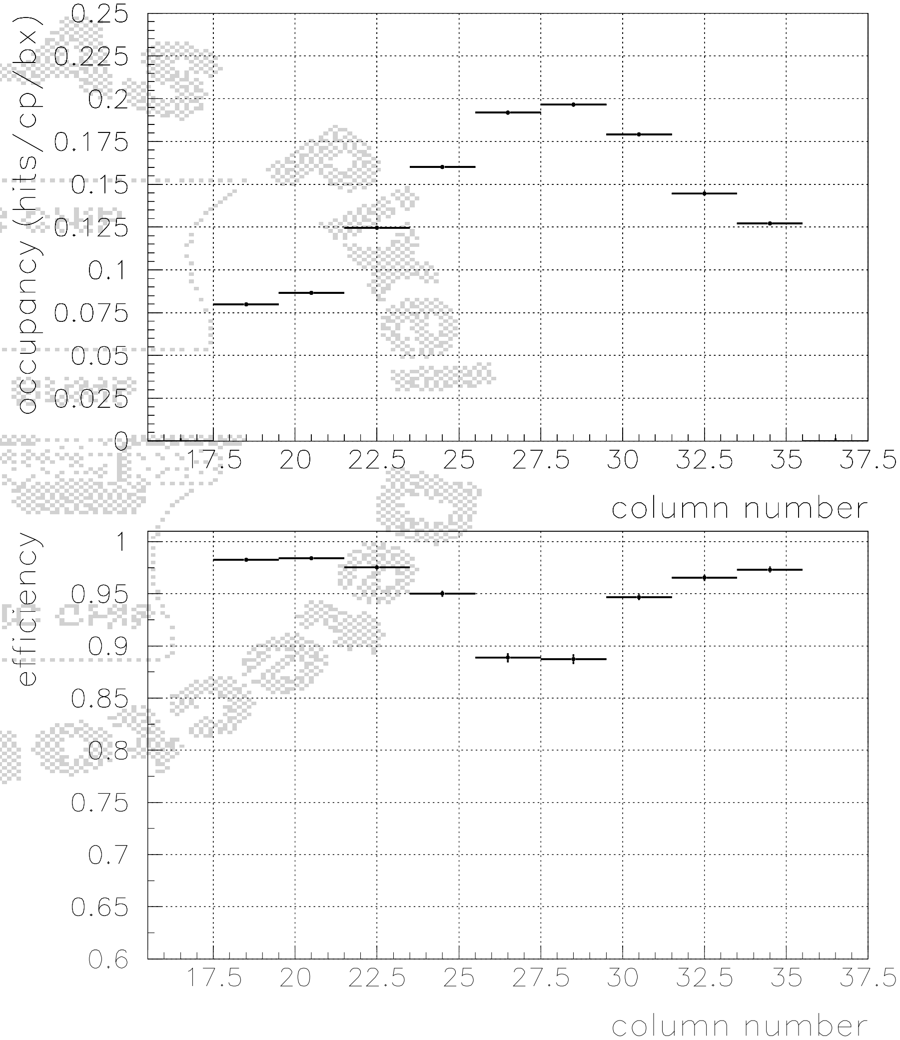
- Losses due to the dead-time of the pixel cell are expected to be:
  pixel occupancy × *<ToT>*
- It can be verified by changing the ToT tuning and checking the efficiency change:
  $\Delta\varepsilon = occupancy \times \Delta\langle ToT\rangle$
- From the spread of the observed point, the best fit line has a slope of
  -0.78±0.17,
  well compatible with the expected slope -1.



- **Even at B-layer occupancies, this effect is below the 1% level.**

Sparse scan losses

- The clock used for the sparse scan may have a frequency reduced with respect to 40 MHz.
- This introduce an additional dead time in the pixel cell due to the increase of transfer time from the cell to the EoC buffers.
- Reducing it to 20 MHz results in an efficiency drop: 98.2% → 91.3%
- losses start at occupancy of 0.14

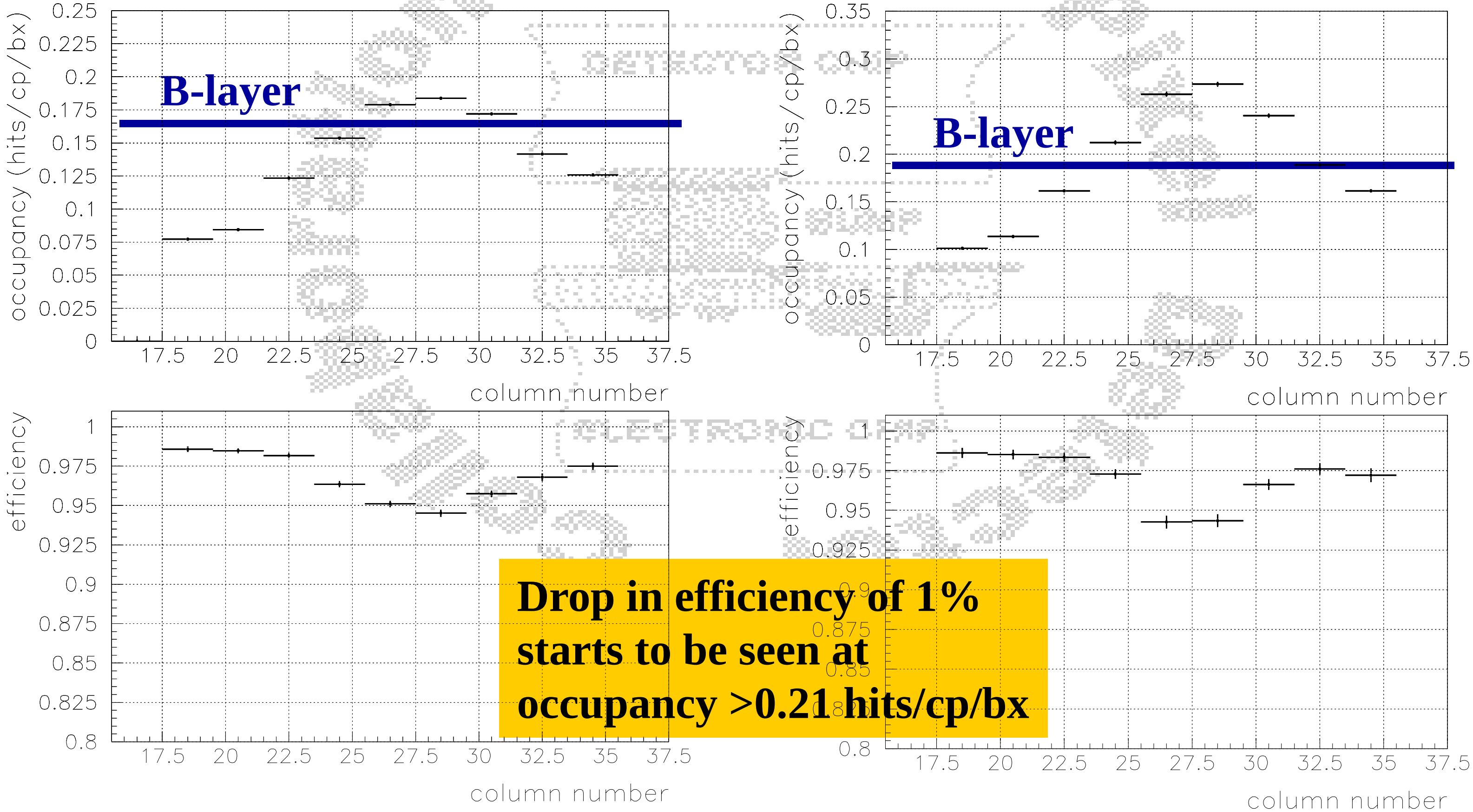


- **At normal readout speed the losses are expected to start at occupancy >0.28 hits/cp/bco.**

Occupation of EoC buffers

- scales with latency.
- Latency 130 bx → 250 bx
- efficiency 98.2% → 95.4%

- can be increased by choosing a high level of hit duplication
- hits/cp/bx 0.20 → 0.28
- efficiency 98.2% → 95.8%

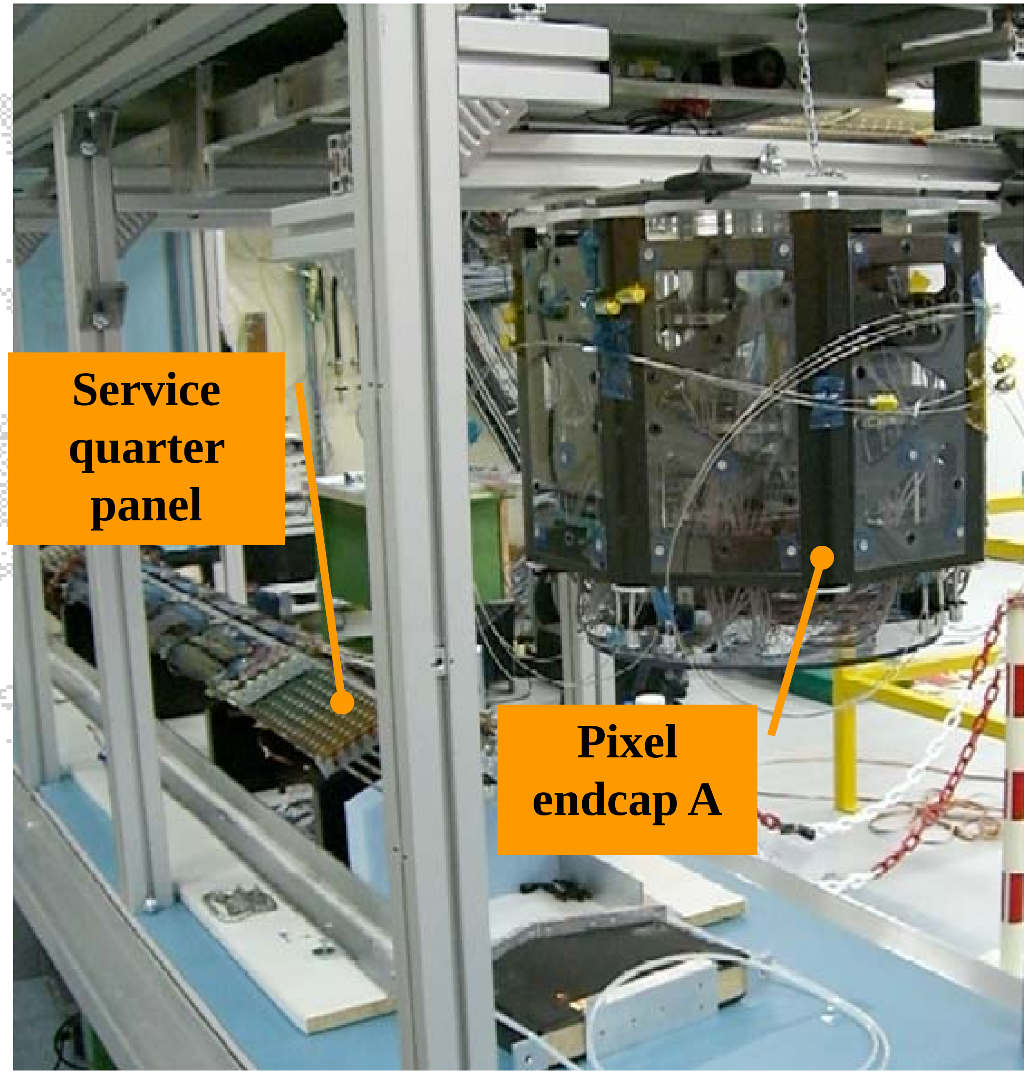


Drop in efficiency of 1% starts to be seen at occupancy >0.21 hits/cp/bx

Detector Operation (2): Cosmics data

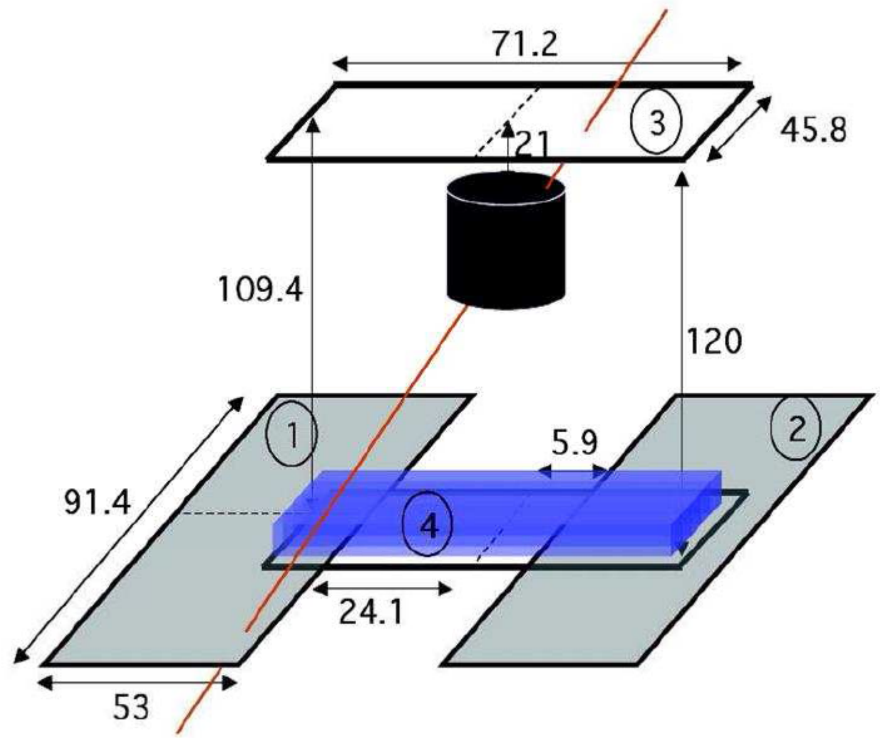
System test setup

- Commissioning of one full pixel detector endcap:
  - 144 modules
- Almost final services:
  - LV supply + rad-tolerant regulation system;
  - operation at -10 ºC, using evaporative cooling;
  - connection to off-detector readout electronics via optical fibres.
- Goals:
  - test of services
  - setting up in-situ calibration tools
  - commissioning of DAQ
  - commissioning of the detector with cosmics ray and noise runs.



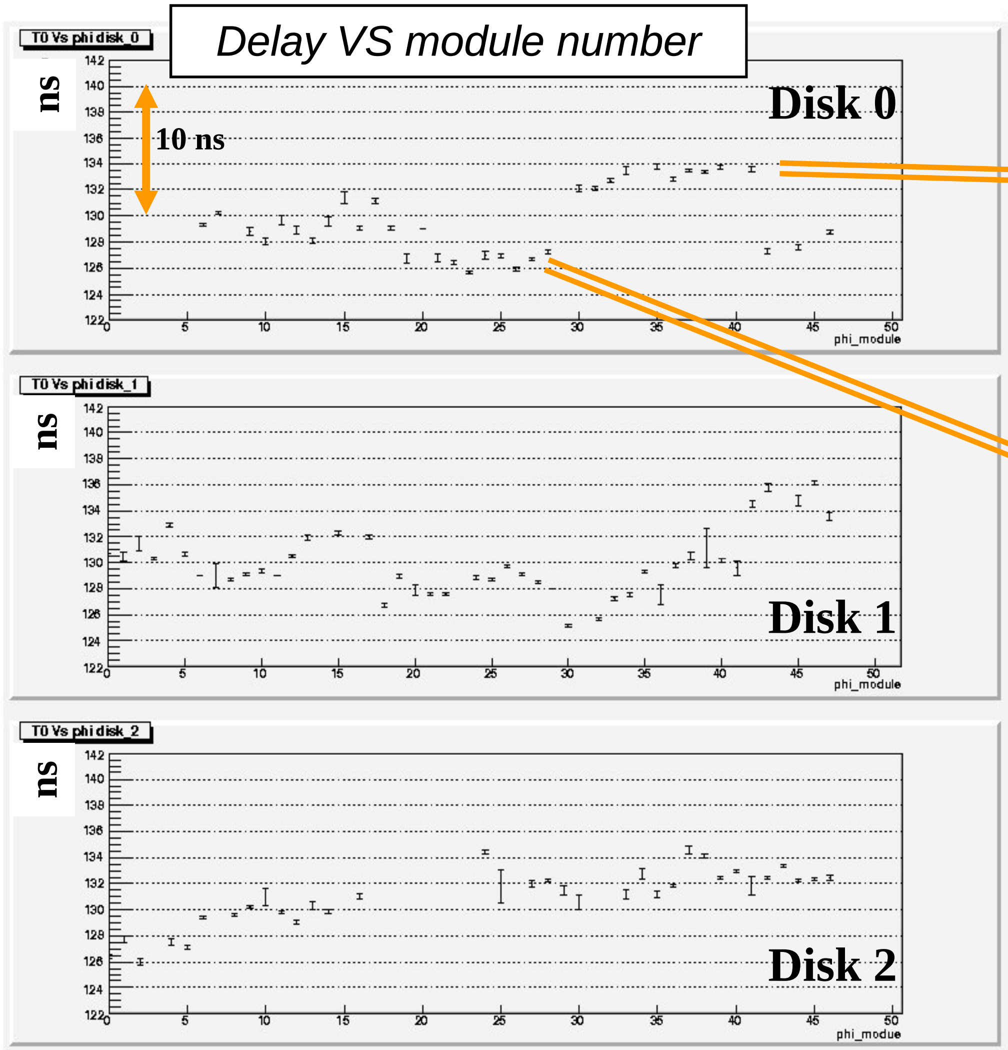
Cosmics data-taking

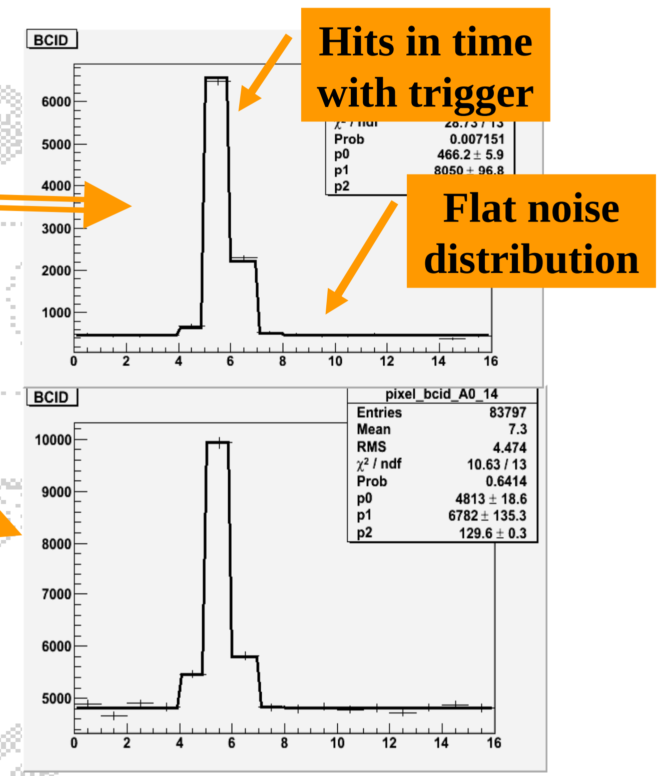
- Standalone running using the system test setup in December 2006:
  - Full Endcap A (144 modules, 112 readout)
  - trigger scintillator system (1 to 4 in the picture): 3 AND (1 OR 2 OR 4)
  - 20 cm iron block to provide a 230 MeV/c momentum cut.



- Huge amount of random trigger data
- About 1 M cosmics trigger
  - 4% with reconstructed tracks through all three disks
- **Reference data for validation of pixel detector understanding**

Cosmics data: module syncronization

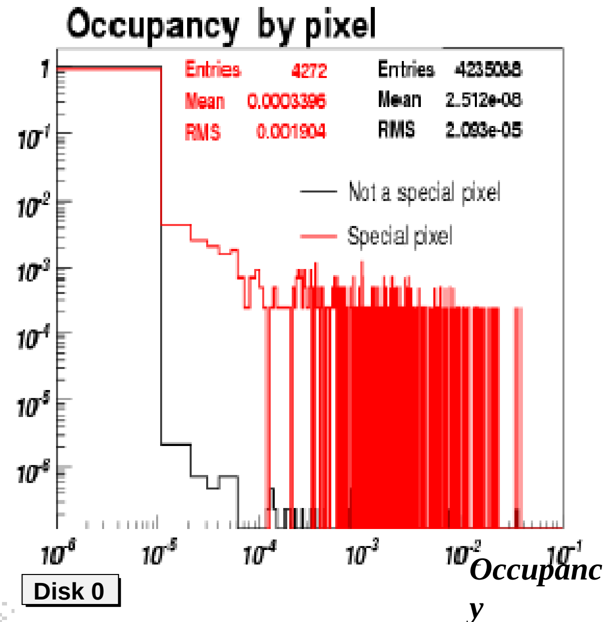


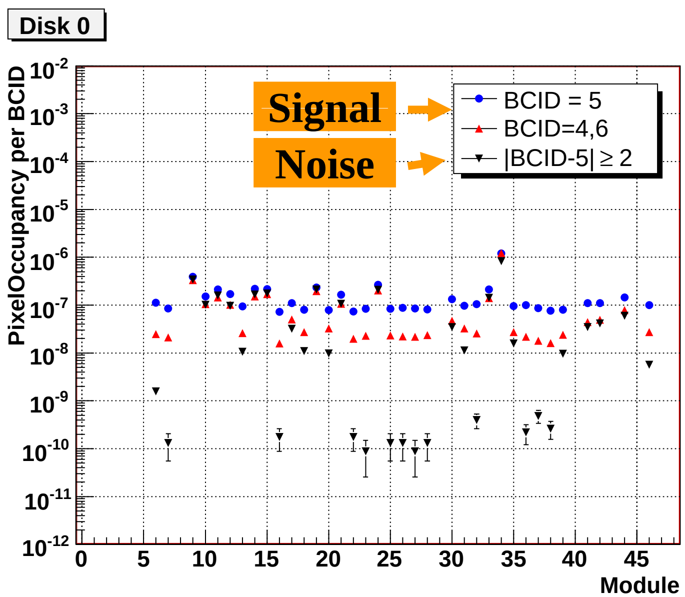


- Timewalk spreads hits through different “bunch crossings”
- This distribution is sensitive to module timing.
- **Checked module synchronization with resolution better than 1 ns.**

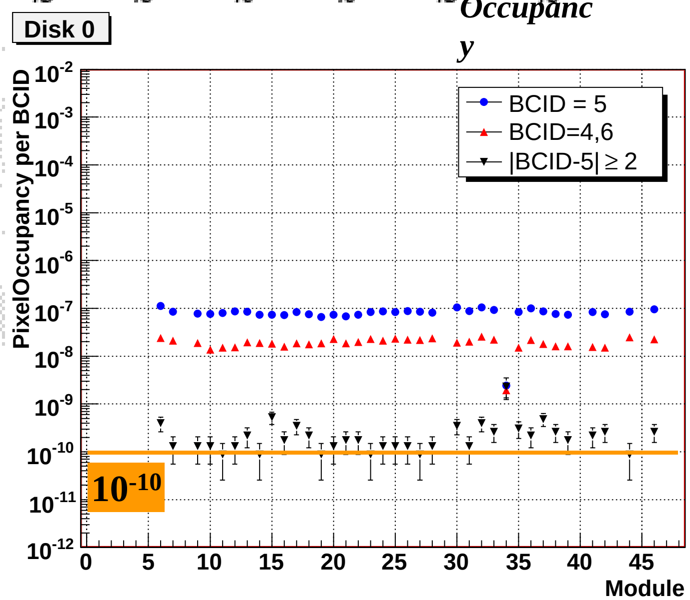
Cosmics data: noise measurements

- Occupancy: hit probability per bunch crossing of a pixel.
- Typical occupancy rate in noise runs is 1-3 10^{-8} per bunch crossing
- **Noise is concentrated on few hot pixels:**
  - ~90% are special pixels, marked during module characterization,
  - remaining can be removed with an additional masking step.
- **True random occupancy is order of 10^{-10}**



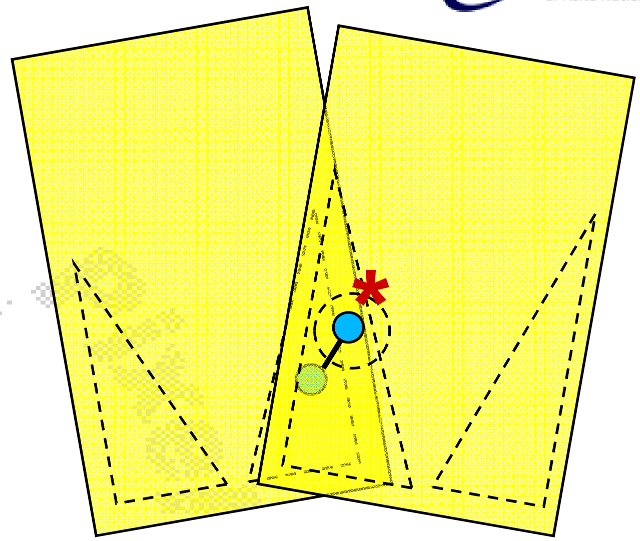


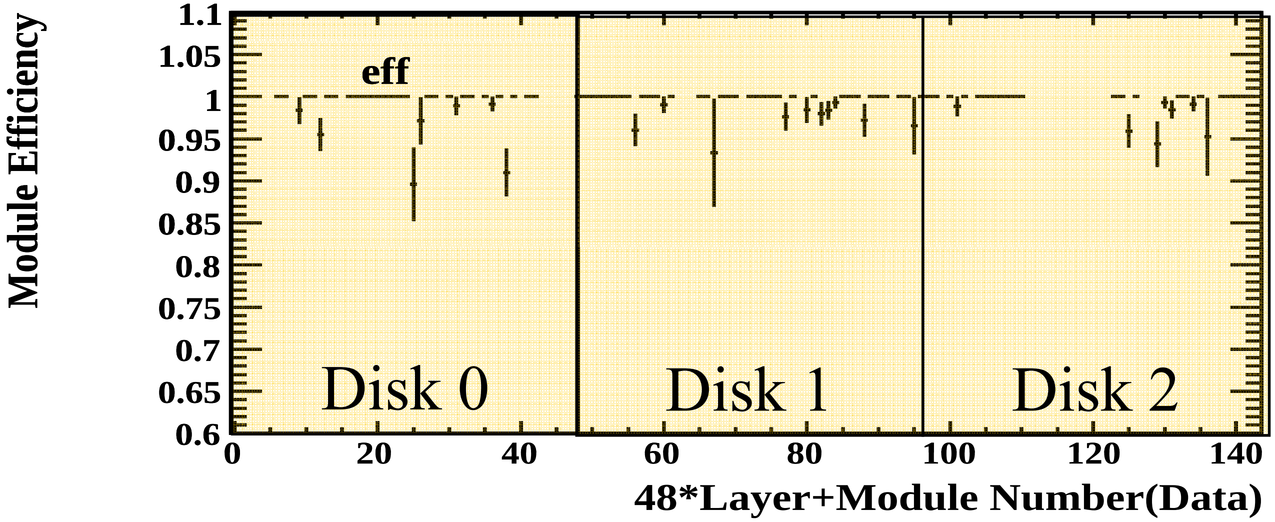
After masking 89 (out of 1.6×10^6) pixels with occupancy greater than 10^{-4}



Cosmics data: efficiency

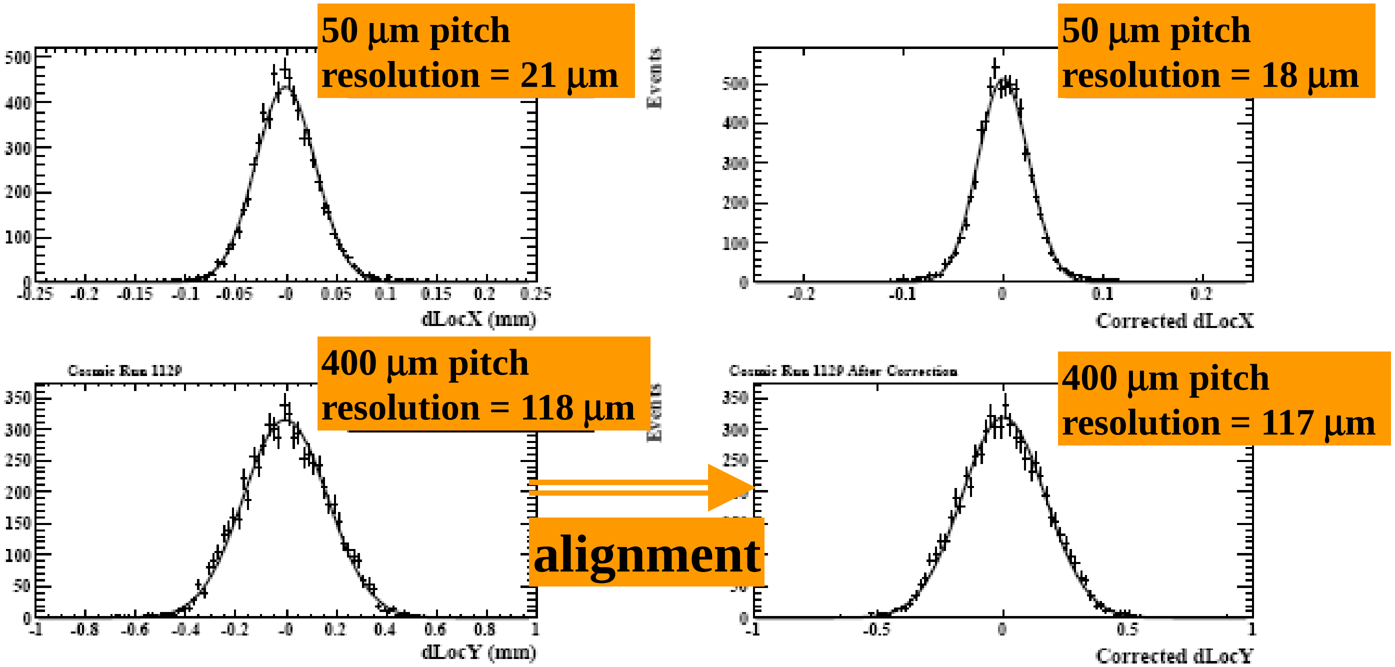
- Efficiency can be computed using particles which crosses overlapping modules in the same disk
  - 24% of tracks
- fiducial cuts on both the initial and overlapping module (remove shallow tracks)
- **Average efficiency ~99%**
- **not enough statistics to provide accurate per module measurement.**





1.1
Efficiency
1.05
effmc
1
0.95

Cosmics data: resolution

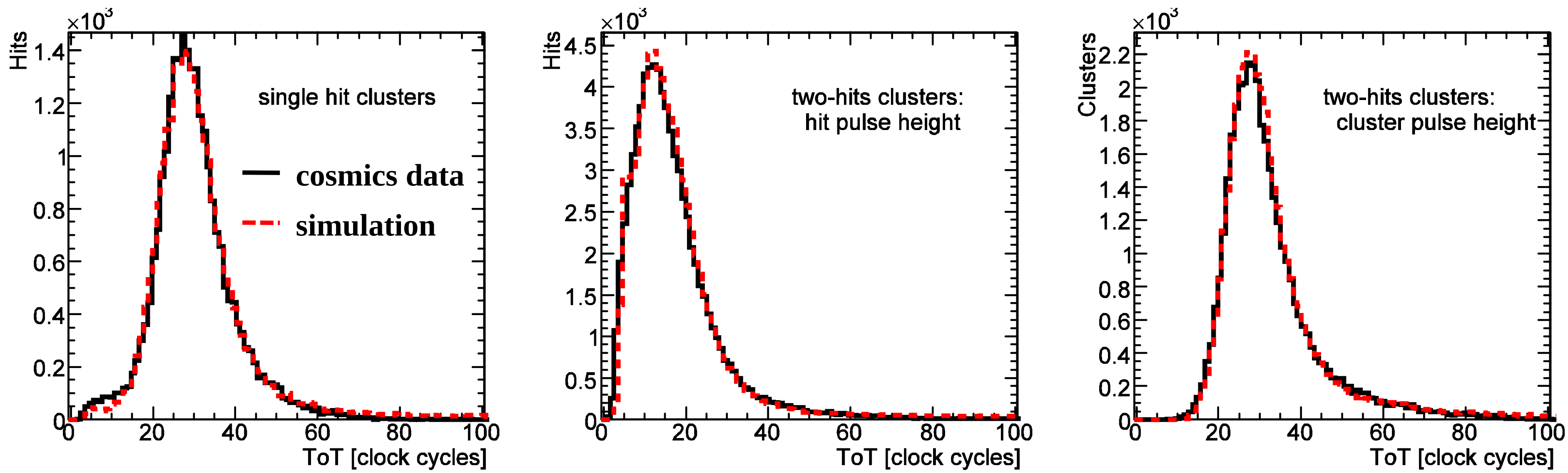


- Due to the low extrapolation distance, overlap residuals are good for testing detector resolution and alignment.
- Low momentum tracks and high incidence angles, results in not-optimal resolution:
  - MC expectation is 16 µm for the precision coordinate (~9 µm for high momentum/normal incidence tracks)
  - **After a simple alignment the observed resolution in data matches well with MC expectation.**

Outlook and conclusions

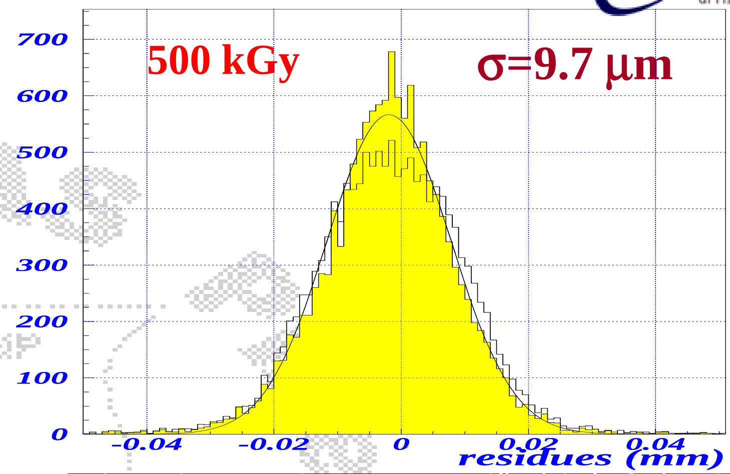
Preparing for data taking

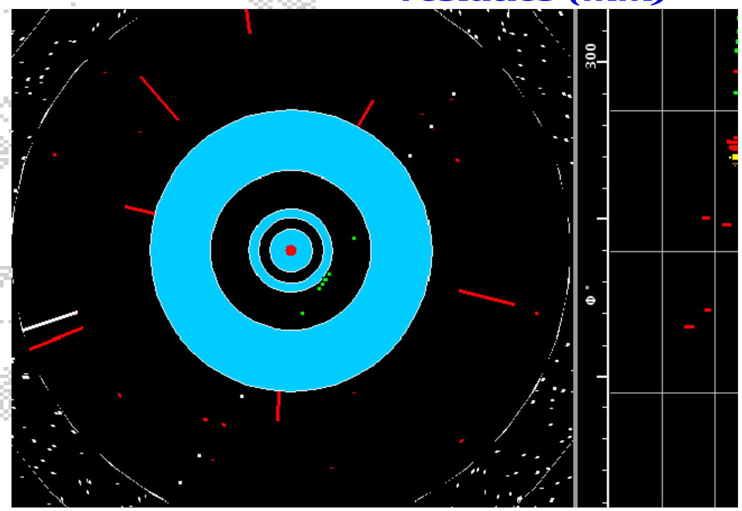
- An enormous knowledge about the detector behaviour has been gathered
  - more than ten years of "testbeam"
  - three year long production
- Tunability is a key factor:
  - stable working point for the whole ATLAS lifetime
  - small number of calibration constants needed for track reconstruction:
    - 80 M channels , but only 1 MB for storing calibration constants
    - and they work!



Preparing for data taking

- The result is a very promising detector:
  - noiseless,
  - >99% efficiency,
  - <10 µm point resolution
  - **rad-hard**
- The pixel detector was inserted in ATLAS in June 2007
- It is finishing connection to the services in these days
- Hope to take first cosmics data in the pit by the end of May
- but what I showed was the easy part:
  - 0.2% of dead channel after production
  - 0.15% of dead areas after integration
  - 0.4% of dead modules after insertion in ATLAS





...so I'll let Danilo go on with the serious problems

Back-up transparencies

Specifications

Radiation hardness:

- NIEL > 10^{15} 1 MeV n_{eq}/cm^2
- 500 kGy

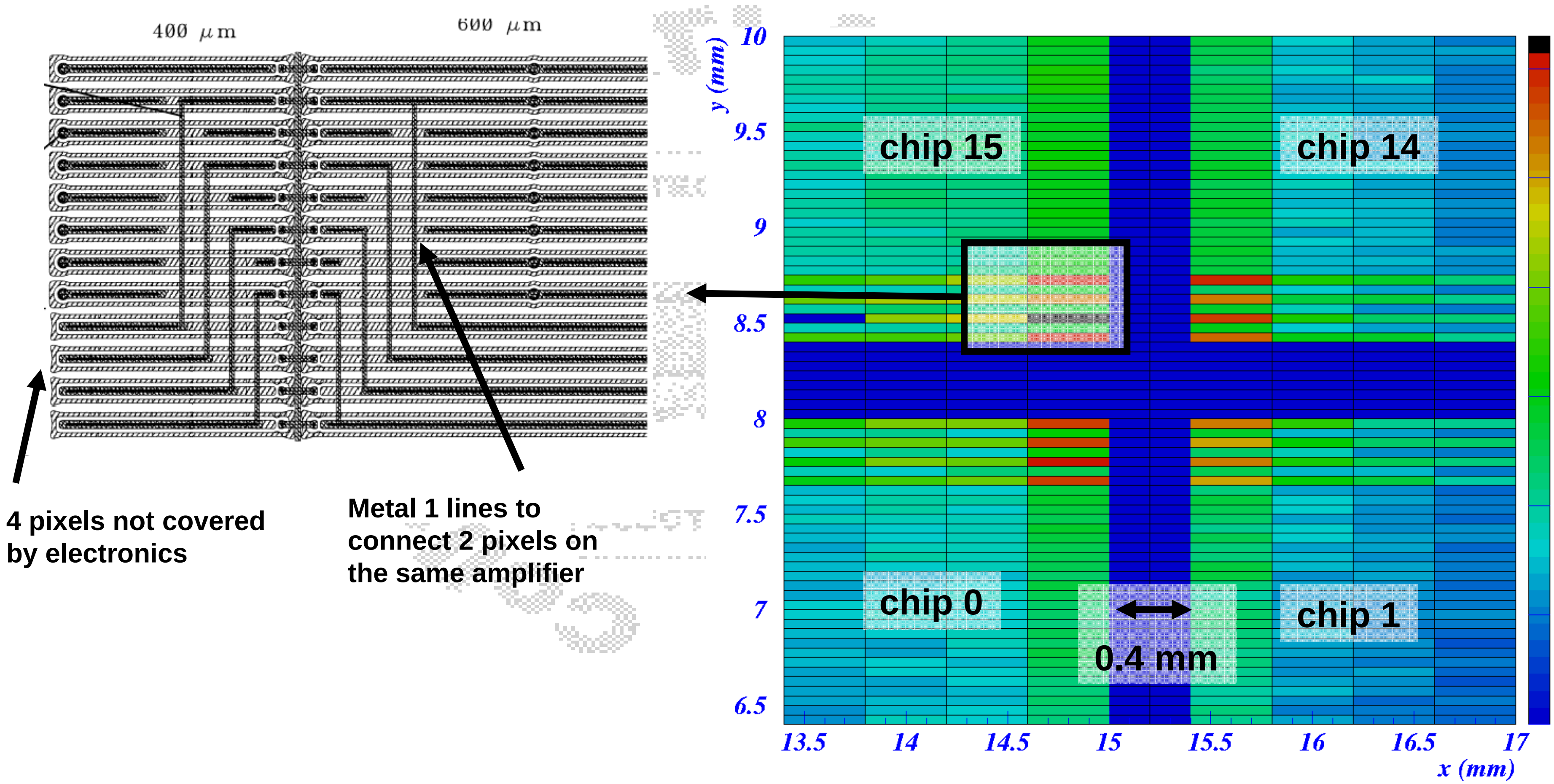
Technical Design Report specification were:

- Rϕ resolution 13 μm,
- efficiency better than 97% at end of lifetime,
- analog information was a high priority option.

Given the 25 ns beam crossing rate at the LHC:

- must be able to assign each hit to the proper bunch crossing;
  (measuremens of timewalk effects on efficiency and resolution)
- must be able to store the hit information during the trigger latency time of ~100 beam crossings.
  (measuremens of rate capability of the readout system with high intensity beam)

Sensor design: inter-chip region



Charge Collection for irradiated assemblies

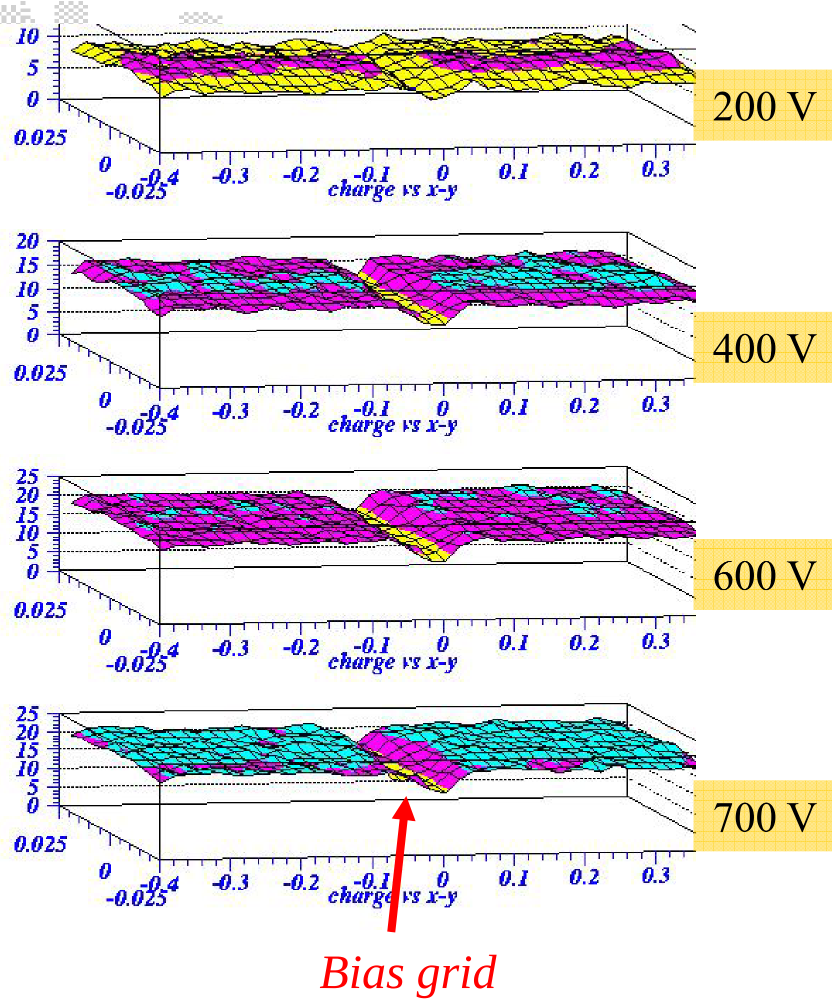
The ATLAS Pixel collaboration has been studying since 1998 silicon detectors irradiated up to the design value.

Oxygenated silicon detectors irradiated up to a fluence of 1.1×10^{15} cm^{-2} 1 MeV neutron equivalent are fully depleted at 600 V (planned maximum operation voltage).

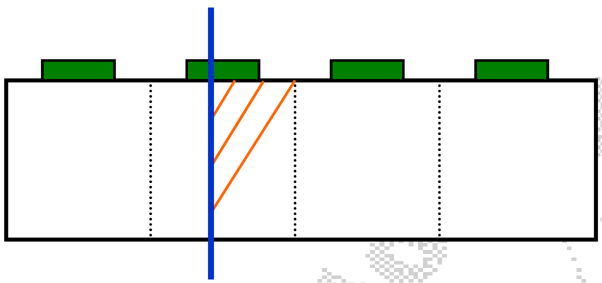
The charge collection efficiency is

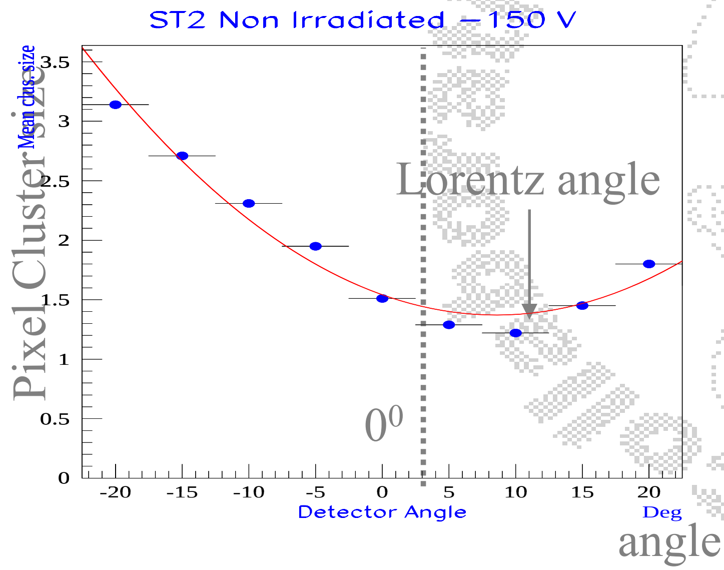
- 72±14 % if no annealing is performed on the sensor
- 87±14 % if a controlled annealing is performed during the LHC shutdown periods (about 2 weeks at room temperature)

Lifetime of charge carriers is in the 4 ns range.

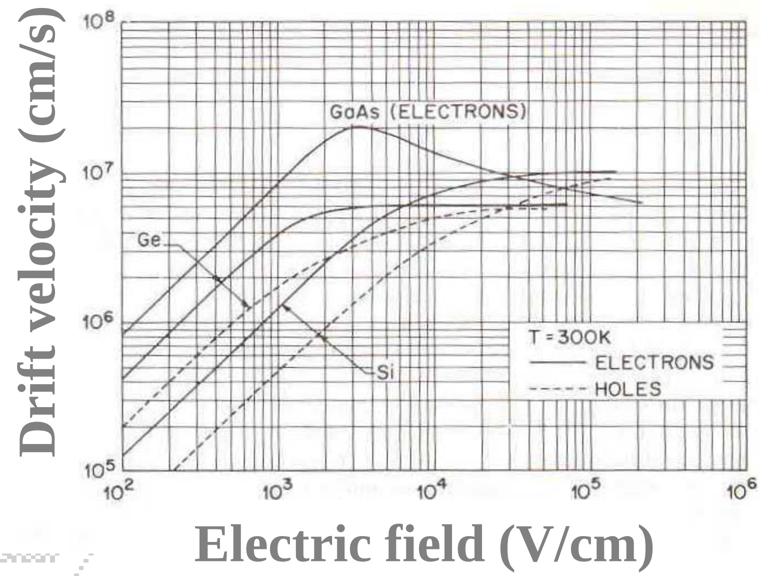


Lorentz angle





Measurement method: number of pixel hits is minimum when incidence angle is equal to the Lorentz angle γ_L.



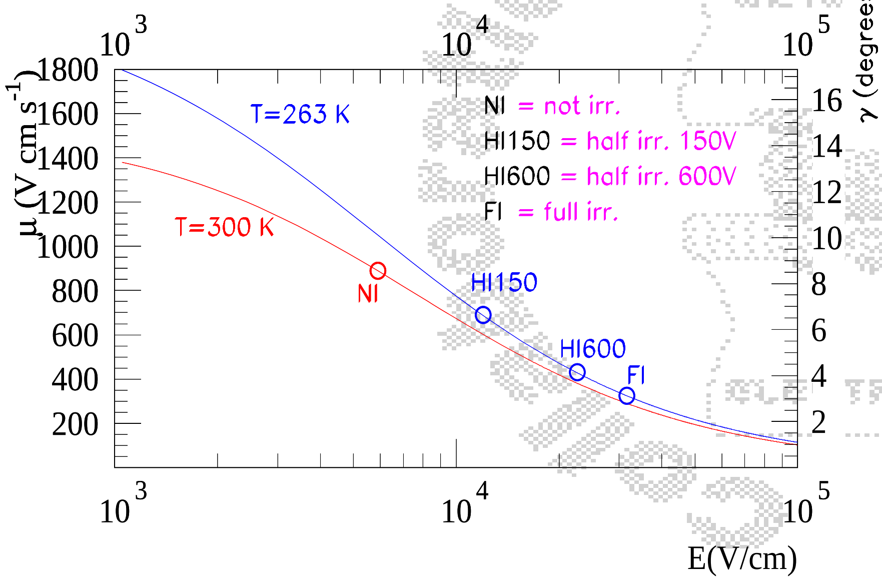
$$\tan\gamma_L \propto \mu_d = \frac{v_s/E_c}{\left[1+\left(E/E_c\right)^{\beta}\right]^{1/\beta}}$$

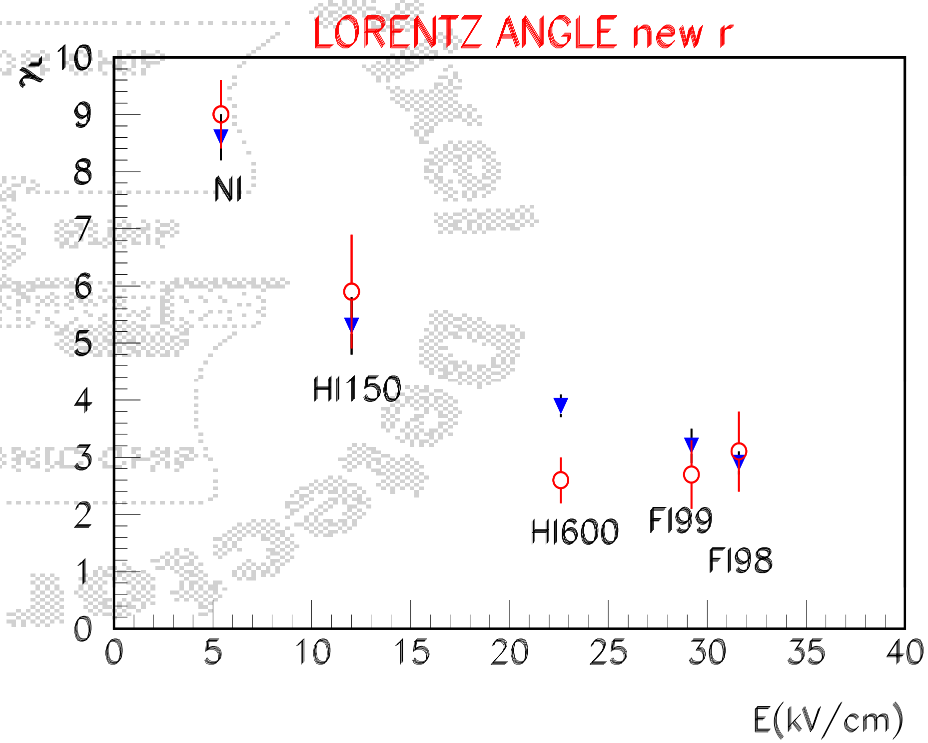
As bias voltage is increased to cope with irradiation, the Lorentz angle decreases:

- **Lorentz angle @2T, 150V = -15^0**
- **Lorentz angle @2T, 600V = -5^0**
- **Pixel modules tilt in ATLAS=20^0**

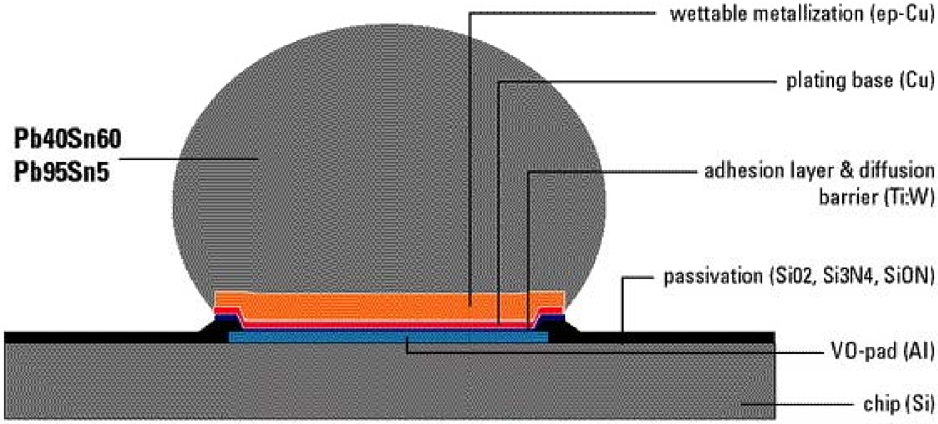
Effective incidence angle = tilt angle + Lorentz angle

Comparison with data





Bump bonding processes



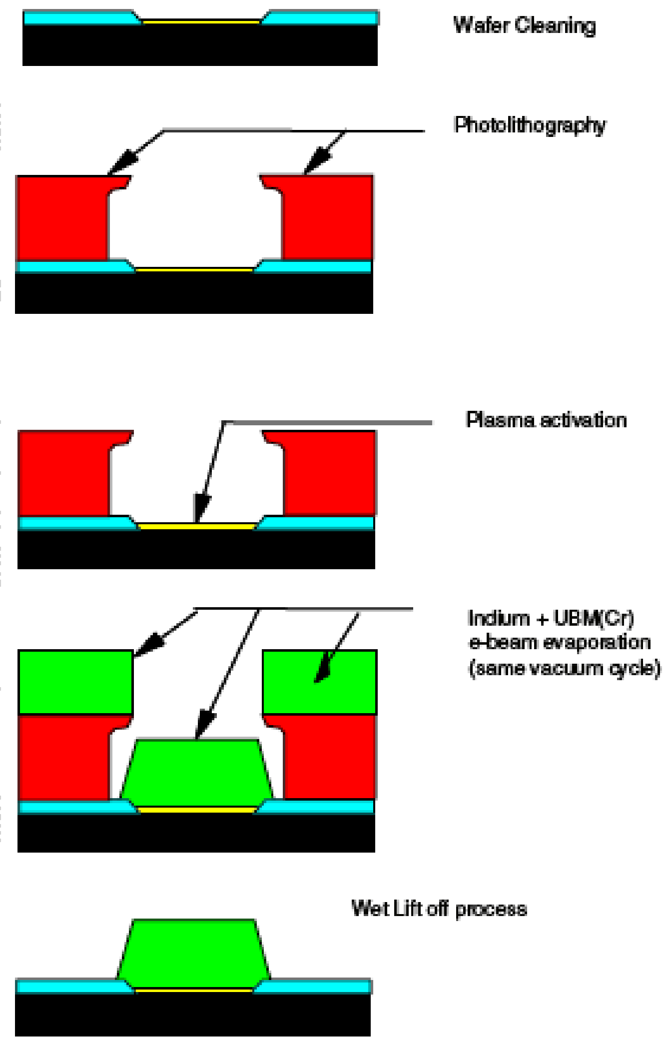
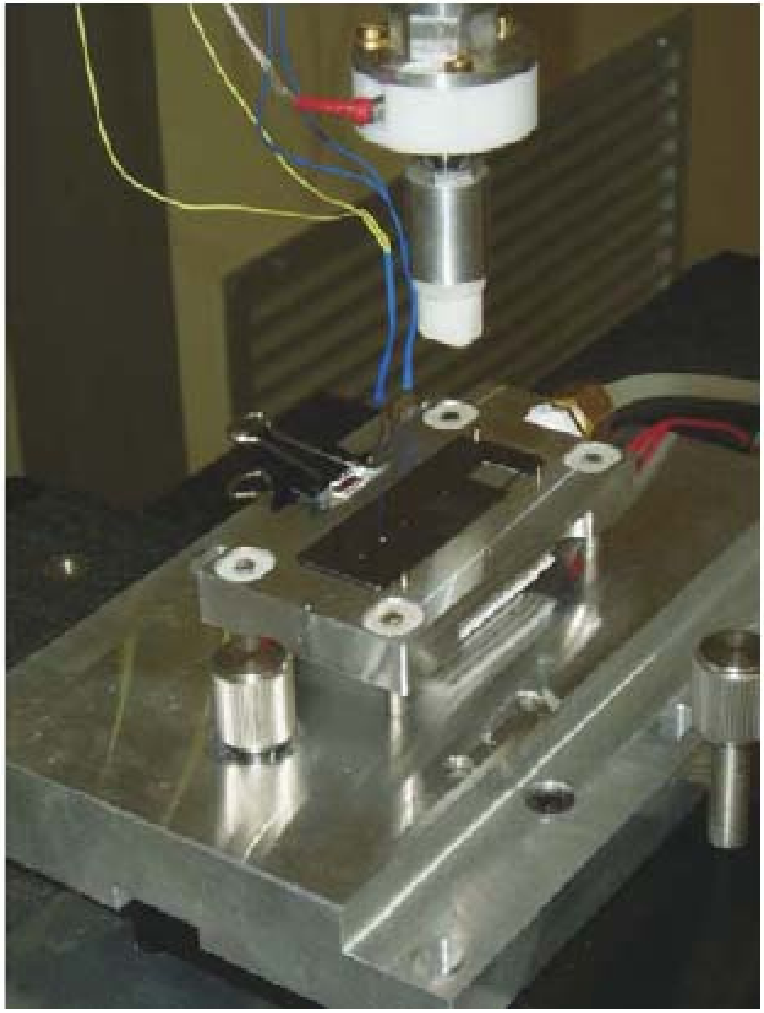


Fig. 1. The In bump deposition process.

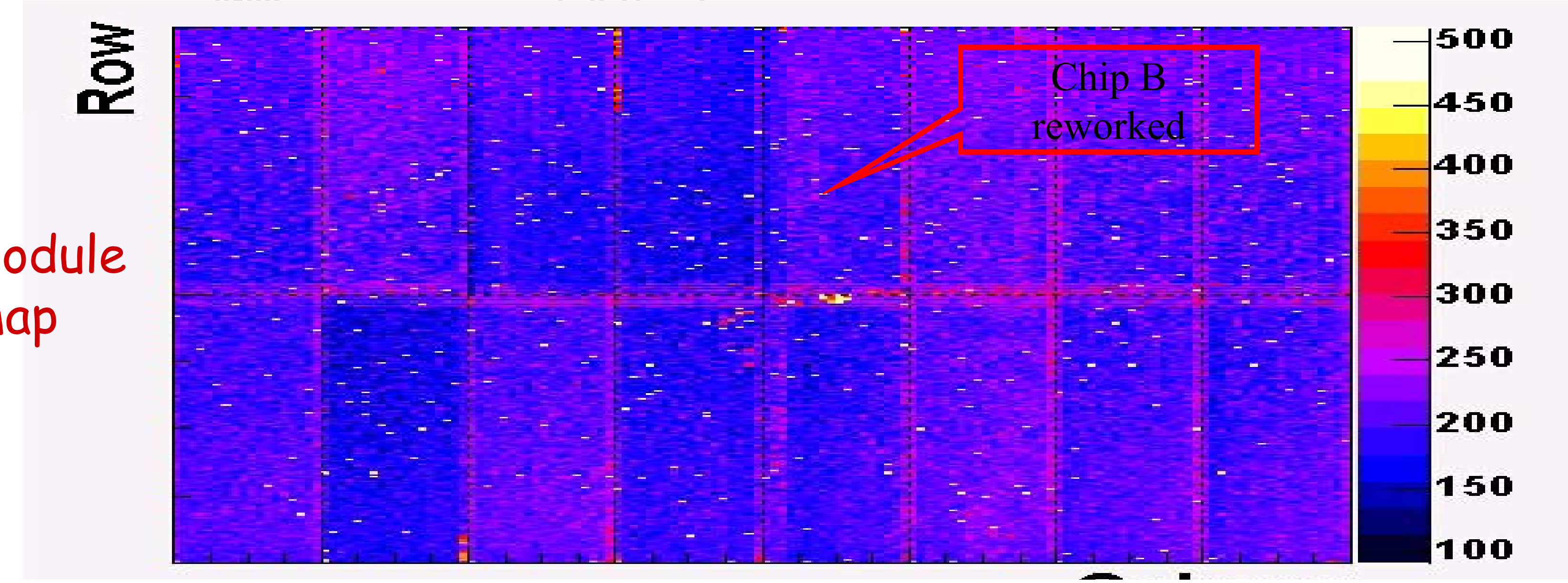
The Milano-Como stripping machine



Re-working

- The flip-chip is one of the most critical operations, since any probability of damage in the operation is multiplied at the 16th power.
- For both bump-bonding technologies, the pixel collaboration and the manufacturers have developed reworking techniques to replace damaged or not conforming FE chips.
- Quality of reworked assemblies is not appreciably worse than standard ones.

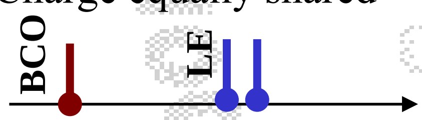
AMS module noise map



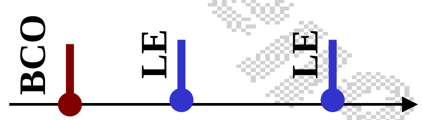
Timing and performances

- Because of timewalk, leading edges reach threshold at different times after the beam crossing.
  Some examples:
  – All charge in one pixel:

  – Charge equally shared

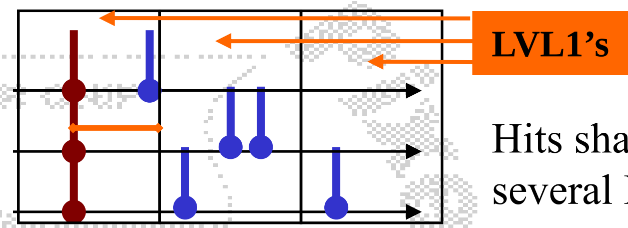


  – Charge unequally shared.

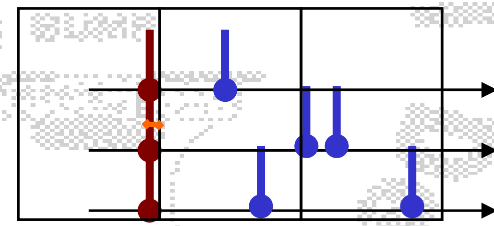


- In test beam setup beam crossing is asynchronous with clock cycle.
- The TDC information is used to retrieve the relative phase between trigger *(=BCO)* and clock edge *(=LVL1)*

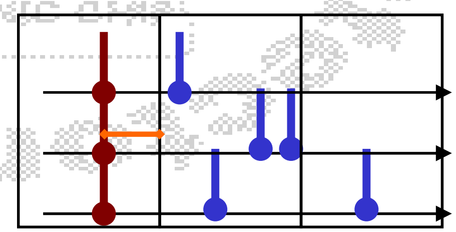
- Classifing events according to TDC reading **(orange bar)** is a scan over BCO-Clock phases:



Hits shared among several LVL1



Some cluster losses

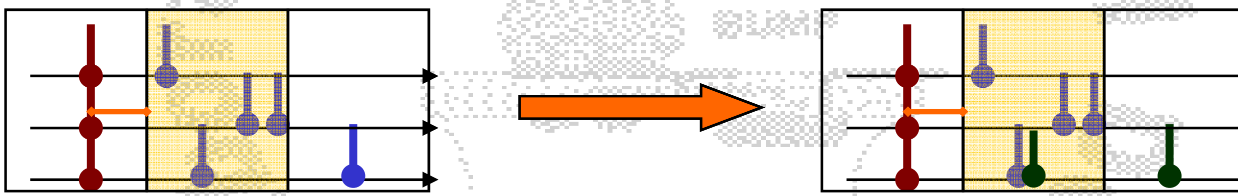


Only some incomplete clusters: full efficiency, but resolution is affected.

- **find optimal conditions;**
- **find stable operation range.**

Hit duplication

- For irradiated modules, which will have a 15° effective incidence angle:
  - lower total collected charge
  - a lot of charge sharing
- it is likely the low charge hit of a cluster will be lost:



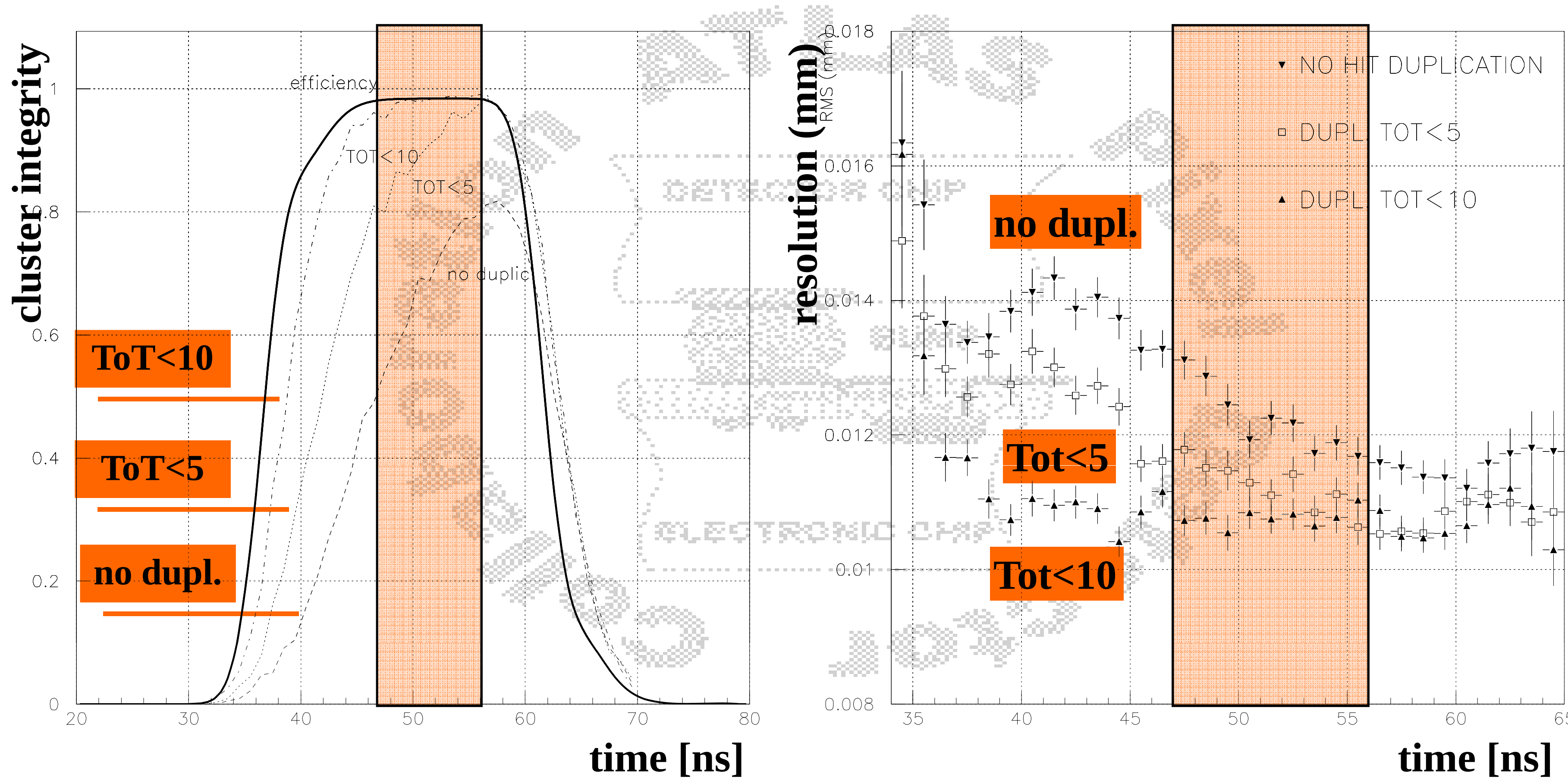
- The cluster is seen anyhow:
  - **no loss of detection efficiency**
- The fraction of cluster to perform charge interpolation is smaller:
  - **loss of resolution**
  - **dependence of resolution on clock phase**

- **FE feature:**

hits below a selectable ToT value can be duplicated in the previous LVL1

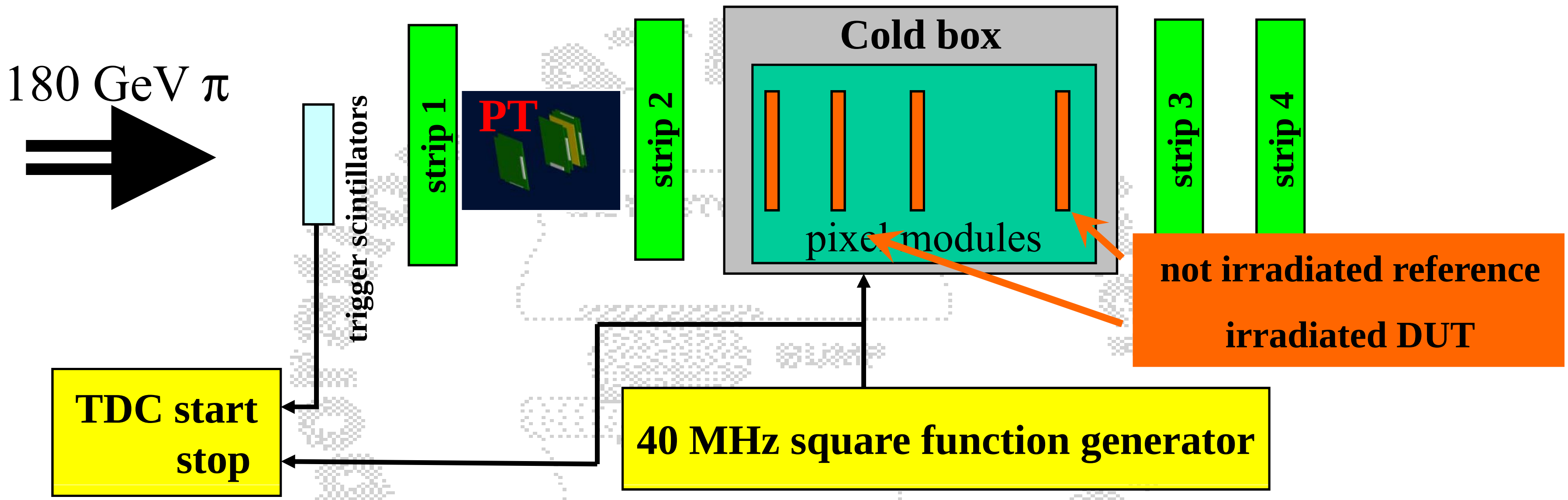
- **restore integrity of clusters for charge interpolation**
- **increase occupancy**

In-time resolution



Almost full resolution can be obtained with duplication at 1/6 of m.i.p. with only 10% occupancy increase

Test beam setup (2)



- In 2003 and 2004 the SPS team delivered to ATLAS a beam with
  - LHC-like intensity
  - ~3 mm gaussian width
- measurement of efficiency dependence upon occupancy in realistic conditions.

- Trigger scintillator not able to cope with the rate:
  ☞ **intensity high enough to use random triggers!**
- Strip detectors not able to cope with the rate:
  ☞ **stand alone pixel telescope!**

System test: optical links

- Connection between on- and off-detector readout electronics is through optical link.
- Each link can be tuned by setting:
  - signal phase
  - threshold
- but size of error free region depends on the bias: one value for 7 channels.
- **Experience from system test operation:**
  - **dynamic range of channels is sensitive to temperature**
  - **matching of the 7 channels is not adequate at the design temperature.**
- **Action:**
  - **install heaters to keep optobards at room temperature.**