Deep N-well 130nm CMOS MAPS for the ILC vertex detector

Valerio Re

C. Andreoli, A. Bulgheroni, C. Cappellini, M. Caccia, L. Gaioni, M. Jastrzab, M. Manghisoni, E. Pozzati, L. Ratti, V. Re, F. Risigo, V. Speziali, G. Traversi

INFN Milano, Pavia, Roma III

University of Bergamo, University of Insubria, University of Pavia, Italy

ILC Vertex Workshop

April 21 – 24, 2008 – Villa Vigoni

Outline

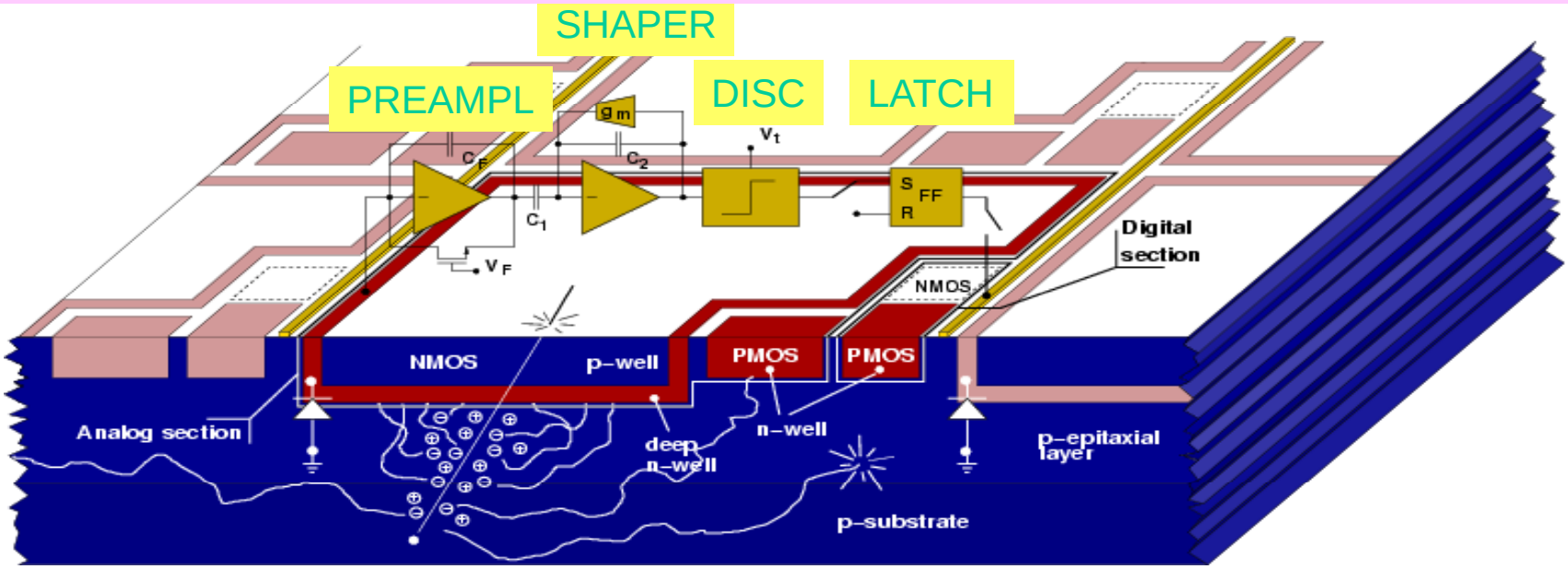
- Deep N-Well Monolithic Active Pixel Sensors in 130nm CMOS technology and ILC Vertex Detector requirements
- **First MAPS generation with pixel-level sparsification and time stamping**
- Pixel analog signal processing, digital section and digital readout architecture
- Experimental results
- Workplan

Why hybrid-pixel-like MAPS

- Modern VLSI CMOS processes (130 nm and below) could be exploited to increase the functionality in the elementary cell → sparsified readout of the pixel matrix.
- Data sparsification could be an important asset at future particle physics experiments (ILC, Super B-Factory) where detectors will have to manage a large data flow
- A readout architecture with data sparsification will be a new feature which could give some advantages with respect to existing MAPS implementations → flexibility in dealing with possible luminosity and background changes during the experiment lifespan, decouple modularity from readout speed
- An ambitious goal is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (sparsification, time stamping)

Deep N-Well (DNW) sensor concept

New approach in CMOS MAPS design compatible with data sparsification architecture to improve the readout speed potential



Classical optimum signal processing chain for capacitive detector can be implemented at pixel level:

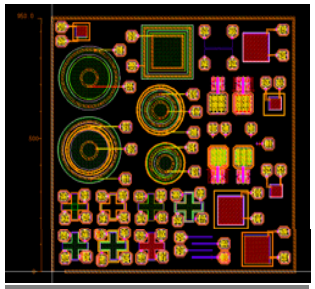
- Charge-to-Voltage conversion done by the charge preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located
- Fill factor = DNW/total n-well area ~90% in the prototype test structures

DNW MAPS 130 nm STM process

IC group contribution:
- Pavia (PV)-Bergamo(BG) analog front-end
- Pisa(PI)-PV-BG in pixel digital logic
- Bologna-PI digital readout architecture

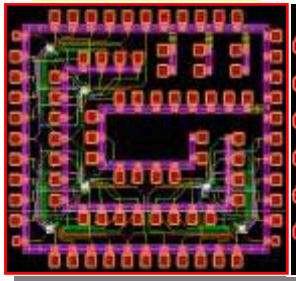
Sub. 12/2004

TEST_STRUCT



ST 130 Process characterization

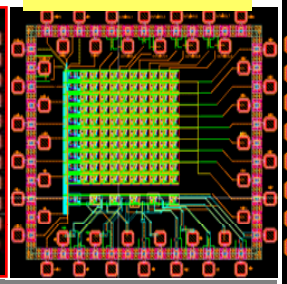
APSEL0



Preamplifier characteriz.

Sub. 8/2005

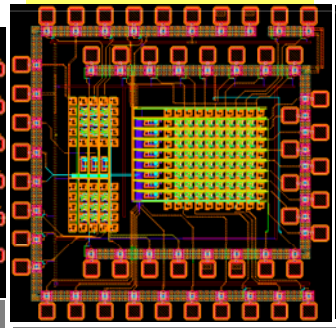
APSEL1



Improved F-E 8x8 Matrix

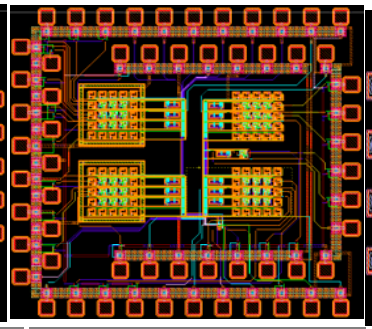
Sub. 8/2006

APSEL2M



Cure thr disp. and induction

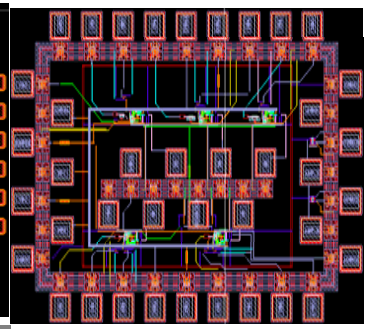
APSEL2T



Accessible pixel Study pix resp.

Sub. 9/2006

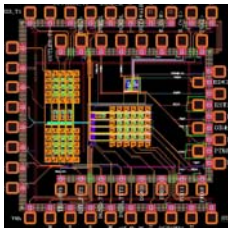
APSEL2_90



ST 90nm characterization

Sub. 11/2006

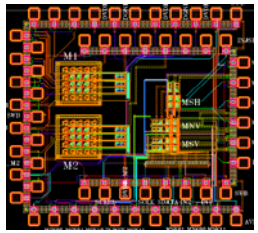
APSEL2D



Test digital RO architecture

Sub. 5/2007

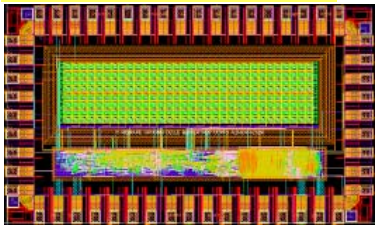
APSEL2_CT



Test chips for shield, xtalk

Sub. 7/2007

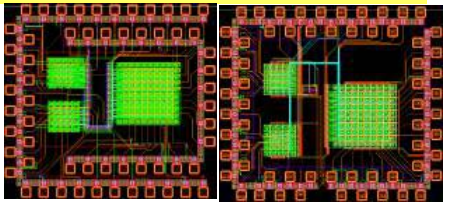
APSEL3D



8x32 matrix. Shielded pixel Data Driven sparsified readout

Sub. 7/2007

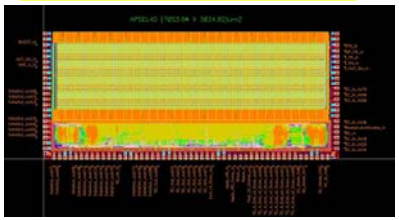
APSEL3_T1, T2



Test chips to optimize pixel and FE layout

Sub. 11/2007

APSEL4D



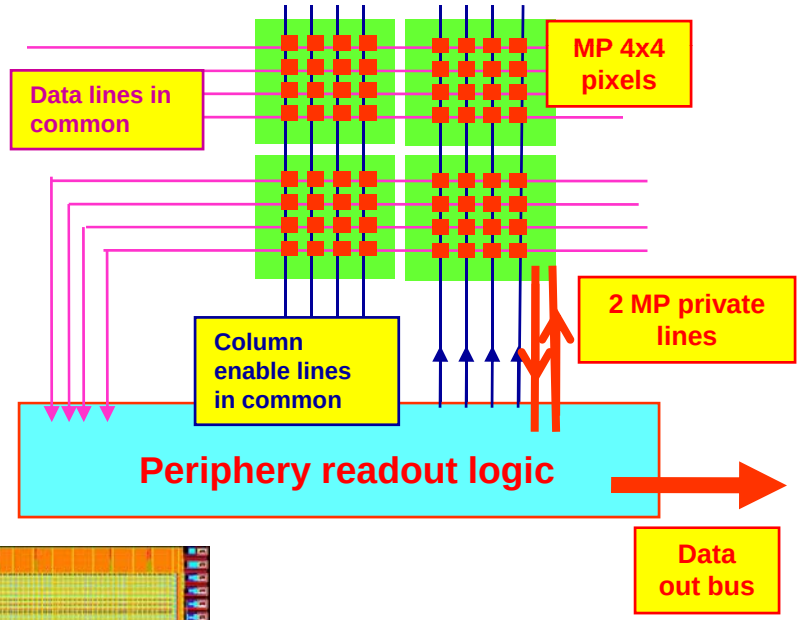
32x128 matrix. Data Driven sparsified readout Beam test Sep. 2008

Fast Readout Architecture for MAPS

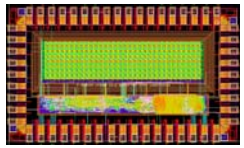
- Data-driven readout architecture with sparsification and timestamp information under development.
- In the active sensor area we need to minimize:
  - the logical blocks with PMOS to minimize the competitive nwell area and preserve the collection efficiency of the DNW sensor.
  - digital lines for point to point connections to allow scalability of the architecture with matrix dimensions and to reduce cross talk with the sensor underneath.

Matrix subdivided in MacroPixel (MP=4x4) with point to point connection to the periphery readout logic:

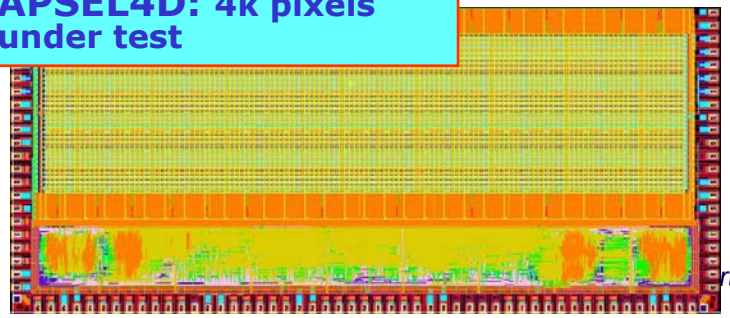
- Register hit MP & store timestamp
- Enable MP readout
- Receive, sparsify, format data to output bus



APSEL3D: 256 pixels under test



APSEL4D: 4k pixels under test



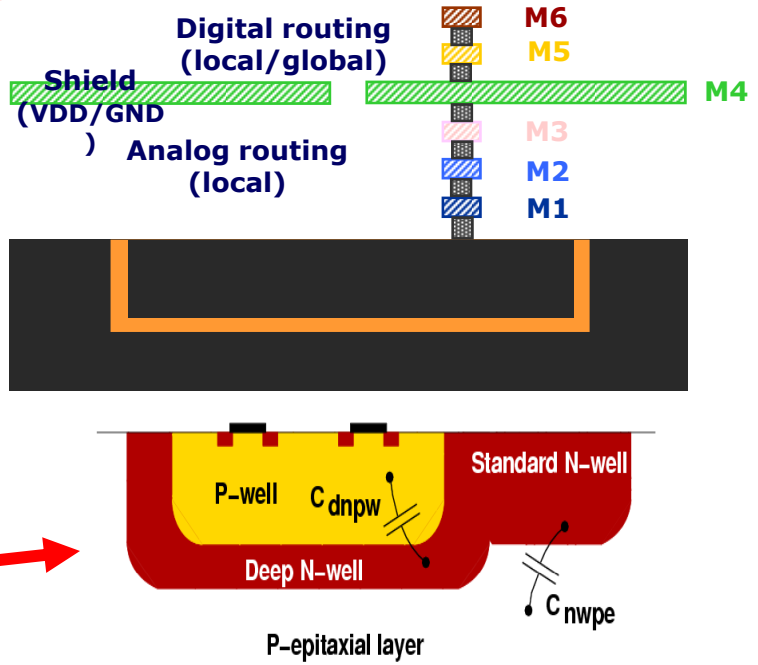
50x50 um pitch

From APSEL2 to APSEL3

APSEL2 issues

- Cross talk between digital lines and substrate
  - Requires aF level parasitic extraction to be modeled
- Relatively small S/N ratio (about 15)
  - Especially important if pixel eff. not 100%
- Power dissipation 60 µW/pixel
  - Creates significant system issues

APSEL3D Digital lines shielding



APSEL3 Redesigned front-end/sensor

Optimize FE Noise/Power:

- Reduce sensor capacitance (from 500 fF to ~300 fF) keeping the same collecting electrode area
  - reduce DNW sensor/analog FE area (DNW large C)
  - Add standard NWELL area (lower C) to collecting electrode.
- New design of the analog part

Optimize sensor geometry for charge collection efficiency using fast simulation developed:

- Locate low efficiency region inside pixel cell
- Add ad hoc "satellite" collecting electrodes

APSEL3 Power=30 µW/pixel: Perfomance

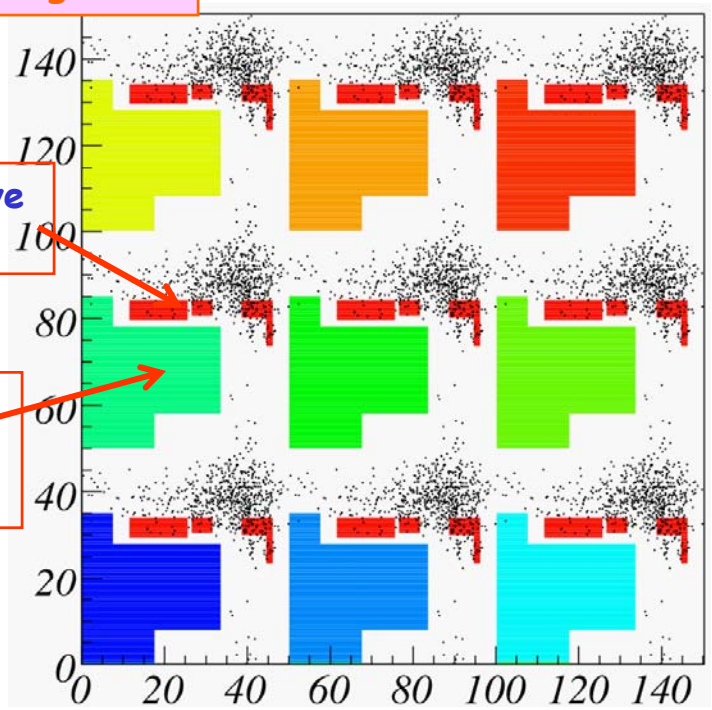
APSEL3 expected performance

FE Version	Geom.	ENC (PLS)	ε(@5σ)	S/N
APSEL2 data	A	50 e-	88.7%	14
APSEL3 Transc.	A	41 e-	93.6%	16
	B	41 e-	99.4%	18
APSEL3 Curr. Mirror	A	31 e-	98.6%	22
	B	31 e-	99.9%	24

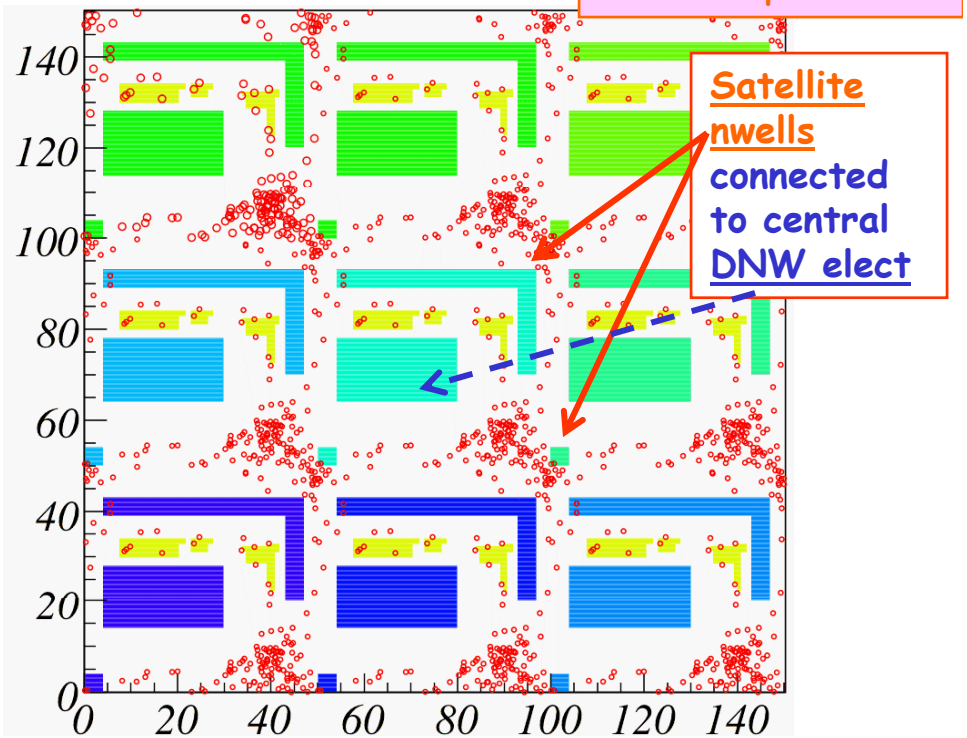
An example of sensor optimization

- With old sensor geometry (left) Efficiency ~ 93.5% from simulation (pixel threshold @ 250 e- = 5xNoise)
- Inefficient regions shown with dots (pixel signal < 250 e-)
- Cell optimized with satellite nwells (right) Efficiency ~ 99.5%

3x3 MATRIX
old sensor geom



3x3 MATRIX
sensor optimized



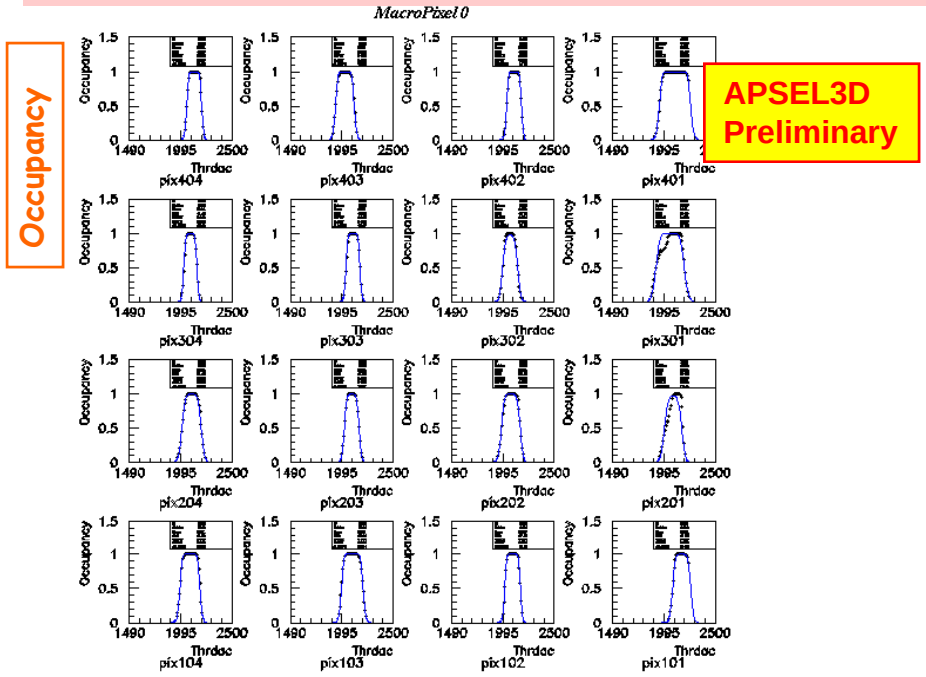
APSEL3 chips now under test

Very preliminary!

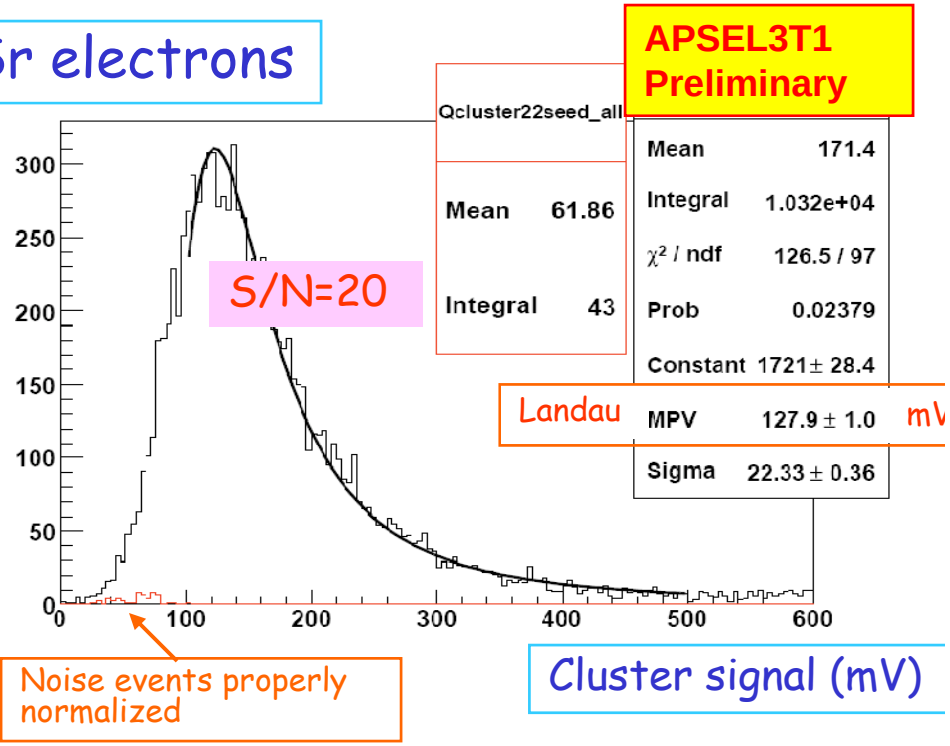
- S/N = 20 for MIP from Sr90
- Absolute calibration of noise and gain still under way

First test on APSEL3D (256 pixels): readout works as expected…with some bugs found!

Noise scan (hit rate vs discriminator threshold) to measure noise and threshold dispersion.



^{90}Sr electrons



→Metal shield effective to reduce crosstalk effects due to digital lines crossing the pixel. This source is now at the level of the pixel noise…

→But some digital crosstalk still present in the APSEL3 series…different source? Power distribution problem?

130nm CMOS DNW MAPS for the ILC vertex detector

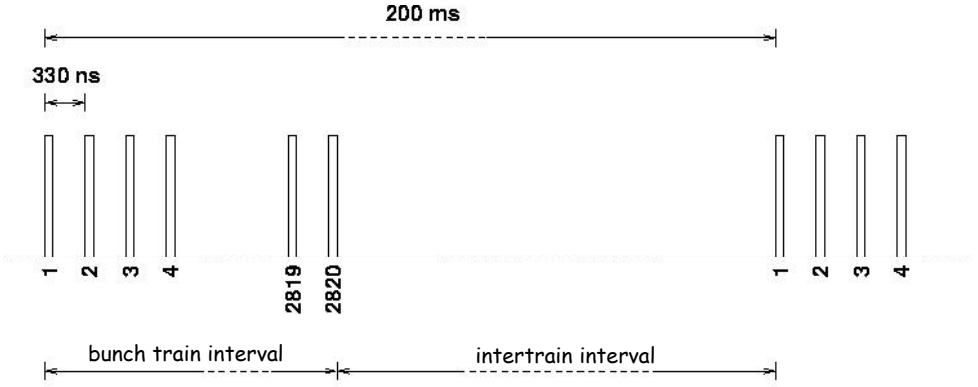
- INFN program started in 2006; design DNW MAPS according to ILC specifications

  (INFN Milano, Pavia, Roma III; University of Bergamo, University of Insubria, University of Pavia)

- Same concept as in the APSEL chips, but reduced pixel pitch and power dissipation
- Digital readout architecture with in-pixel sparsification logic and time stamping, taking into account the beam structure of ILC
- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

Design specifications for the ILC vertex detector

- The beam structure of ILC will feature 2820 crossings in a 1 ms bunch train, with a duty-cycle of 0.5%



  - assuming maximum hit occupancy 0.03 part./Xing/mm^2
  - if 3 pixels fire for every particle hitting → hit rate ≈ 250 hits/train/mm^2
  - if a digital readout is adopted 5μm resolution requires 17.3 μm pixel pitch
  - 15 μm pitch → O_c ≈ 0.056 hits/train → 0.0016 probability of a pixel being hit at least twice in a bunch train period

- A pipeline with a depth of one in each cell should be sufficient to record > 99% of events without ambiguity
- Data can be readout in the intertrain interval → system EMI insensitive

Sparsified readout architecture

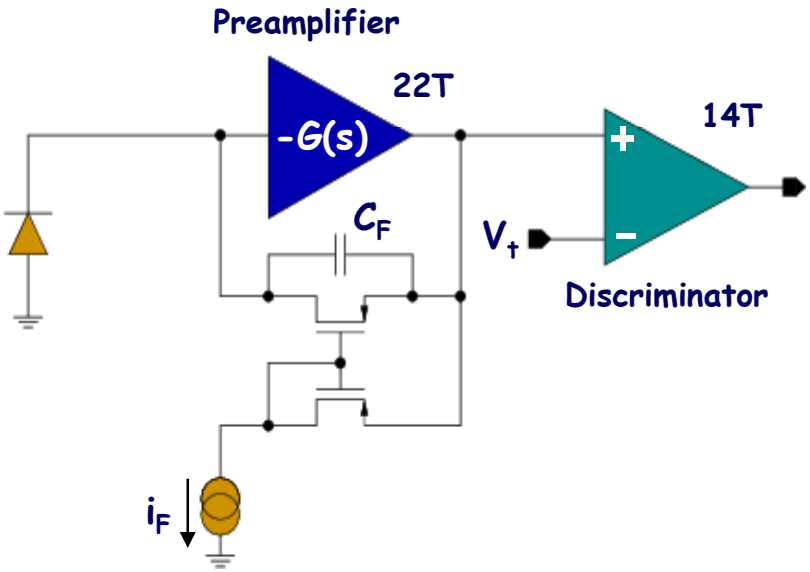
- In DNW MAPS sensors for ILC, sparsification is based on a token passing readout scheme suggested by R. Yarema (FNAL)

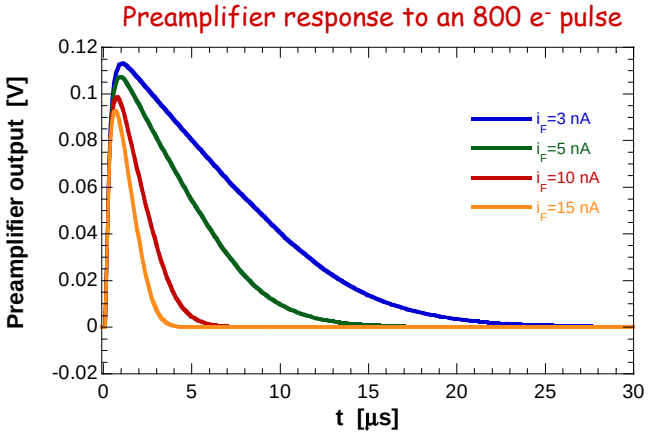
  (R. Yarema, "Fermilab Initiatives in 3D Integrated Circuits and SOI Design for HEP", *ILC VTX Workshop at Ringberg*, May 2006)

- This architecture was first implemented by Fermilab ASIC designers Jim Hoff, Tom Zimmerman and Gregory Deptuch in the VIP1 chip (3-D MIT LL technology, see Fermilab presentation on Wednesday)

- MAPS sensor operation is tailored on the structure of ILC beam
  - Detection phase (corresponding to the bunch train interval)
  - Readout phase (corresponding to the intertrain interval)

Pixel level processor





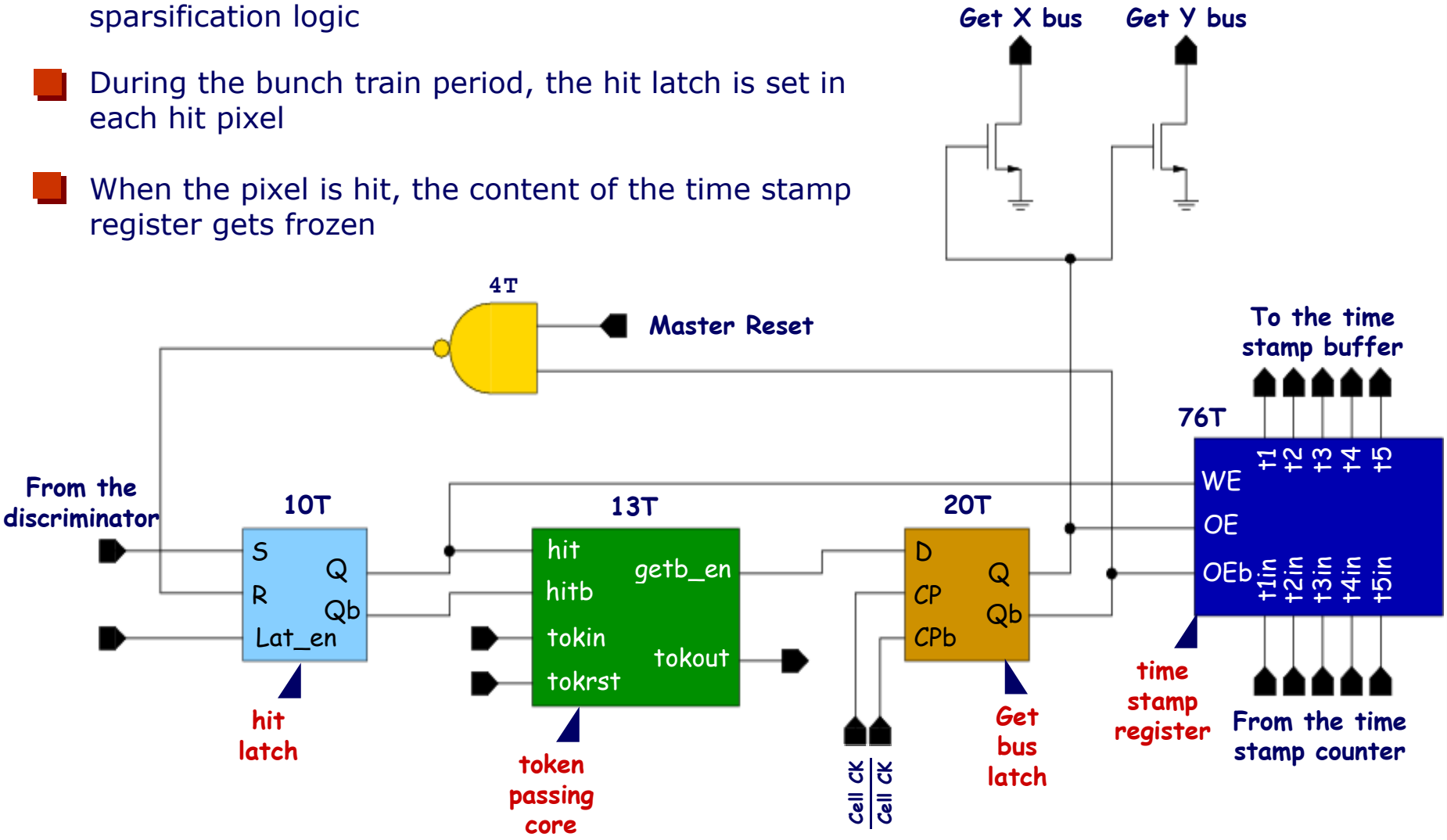
- C_F obtained from the source-drain capacitance
- High frequency noise contribution has been reduced limiting the PA bandwidth

From simulations:

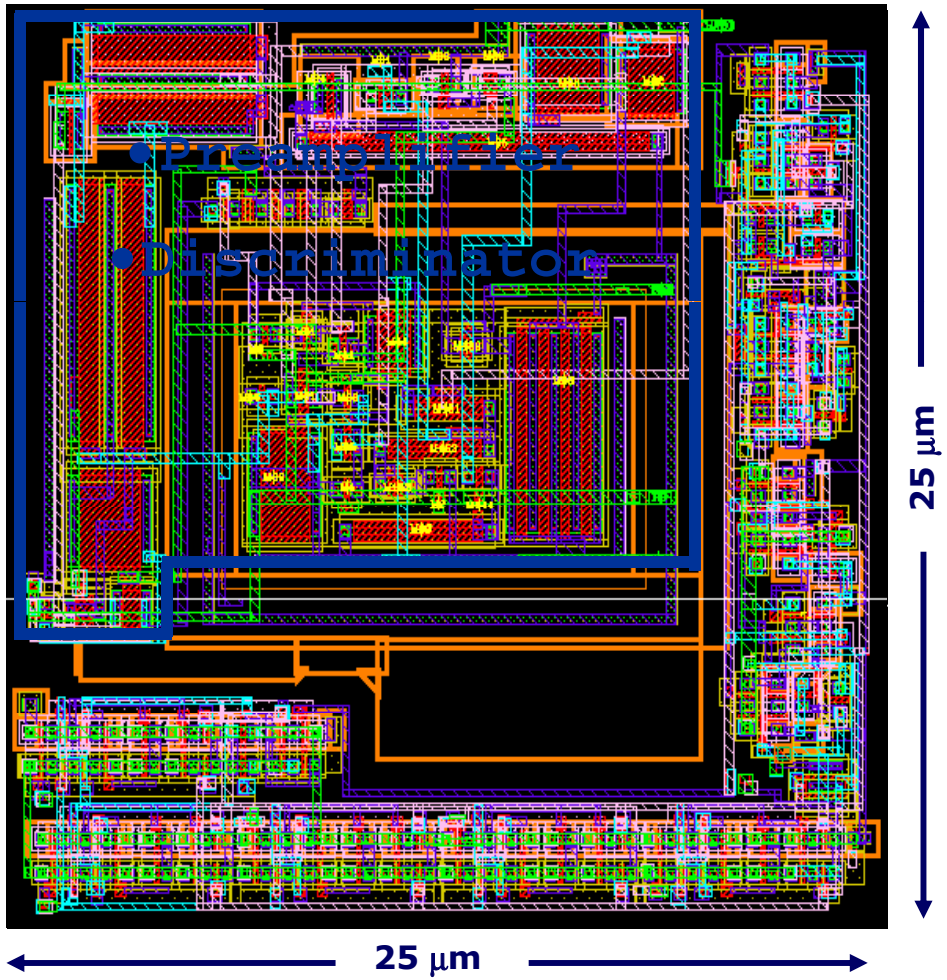
- ENC=**25 e⁻ rms@C_D=100 fF**
- Threshold dispersion ≈ **30 e⁻ rms**
- Power consumption ≈ **5 µW**
- Features power-down capabilities for power saving: the analog section cell can be switched off during the intertrain interval in order to save power (**1% duty-cycle** seems feasible)

Cell digital section

- Includes a 5 bit time stamp register and the data sparsification logic
- During the bunch train period, the hit latch is set in each hit pixel
- When the pixel is hit, the content of the time stamp register gets frozen



ILC DNW elementary cell



analog front-end

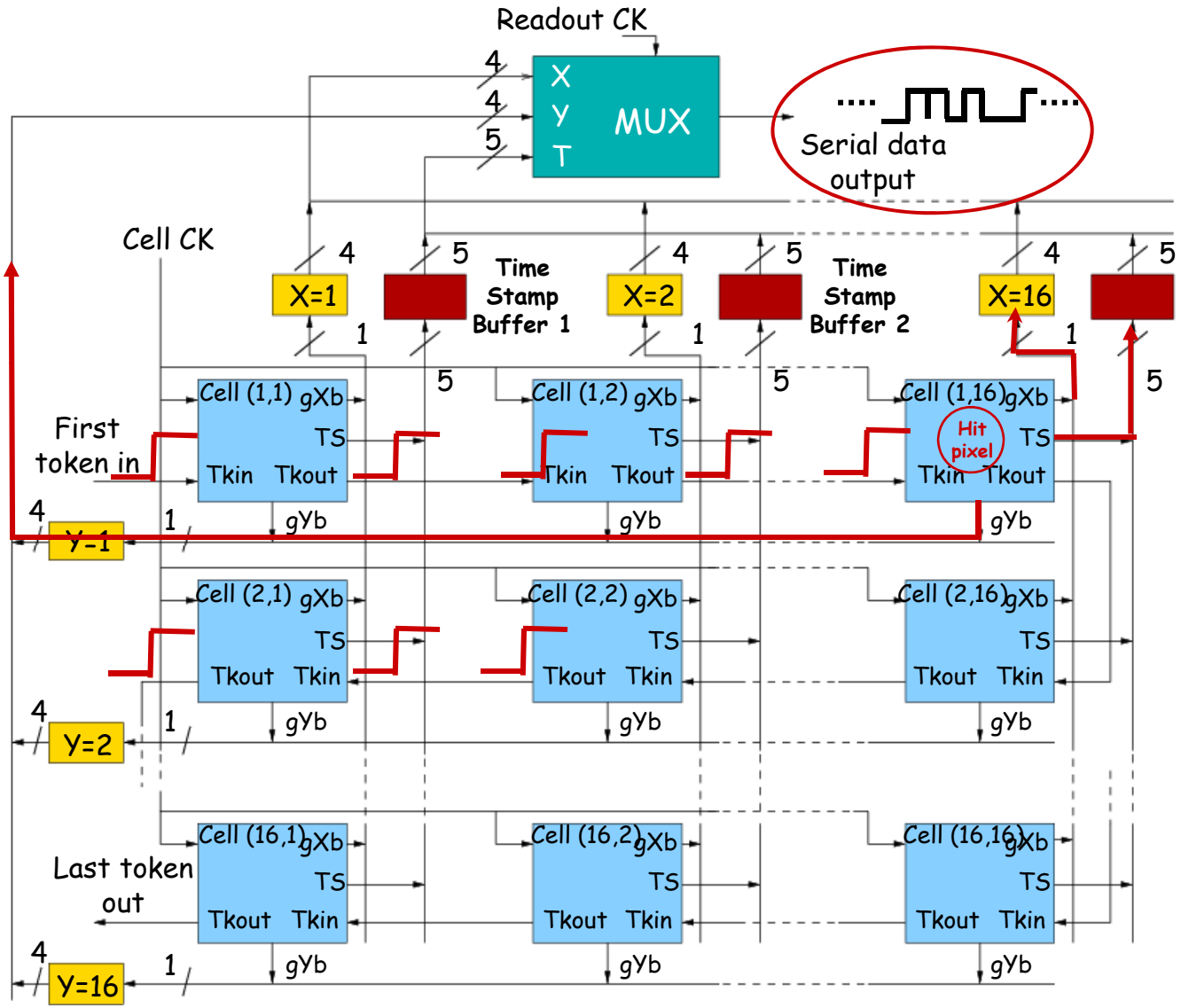
+

digital section

↓

164 transistors

Digital readout scheme



Readout phase:

- token is sent
- token scans the matrix and
- gets caught by the first hit pixel
- the pixel points to the X and Y registers at the periphery and
- sends off the time stamp register content
- data are serialized and token scans ahead

The number of elements may be increased without changing the pixel logic (just larger X- and Y-registers and serializer will be required)

Power dissipation analysis

- Because low material budget is necessary, there is little room for cooling system ⟶ very low power operation
- Analog power: $P_{an,pix} \approx 5\mu W$/pixel (dissipated in the analog PA)
- Digital power: (power in the periphery neglected since it grows as the square root of the number of matrix cells)
  $P_{DC,pix} \approx 7$ nW/pixel (leakage currents of the digital blocks)
  $P_{dyn,pix} \approx 20$ nW/pixel (to charge the input capacitance of the time stamp register blocks during the detection phase)

$$P_{tot} = P_{an,pix} \cdot N \cdot M \cdot \delta_P + P_{DC,pix} \cdot N \cdot M + P_{dyn,pix} \cdot N \cdot M \cdot \delta_P$$

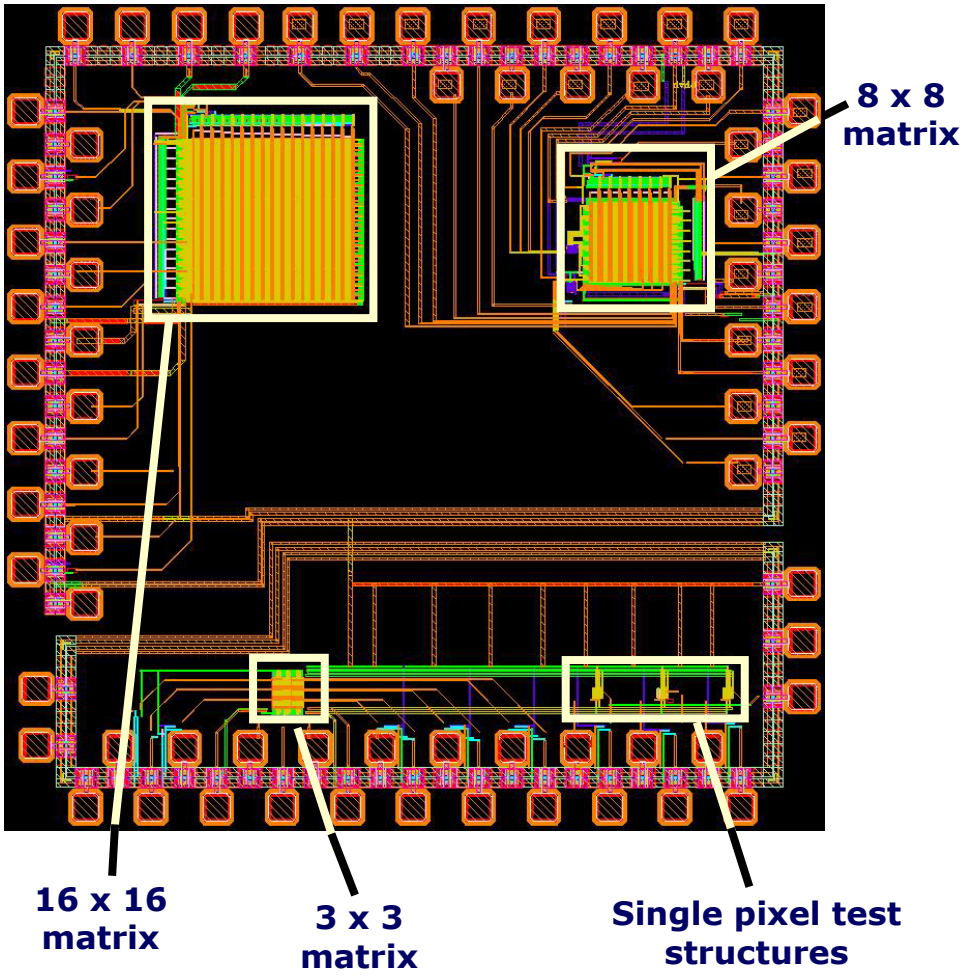
≈ **15.5 W** — **13.6 W** — **1.9 W** — **0.05 W**

Assuming:
- 170000mm^2 total vertex detector area (pixel pitch of 25 μm);
- 1 Mpixel chips;
- δ_P=0.01 power supply duty cycle

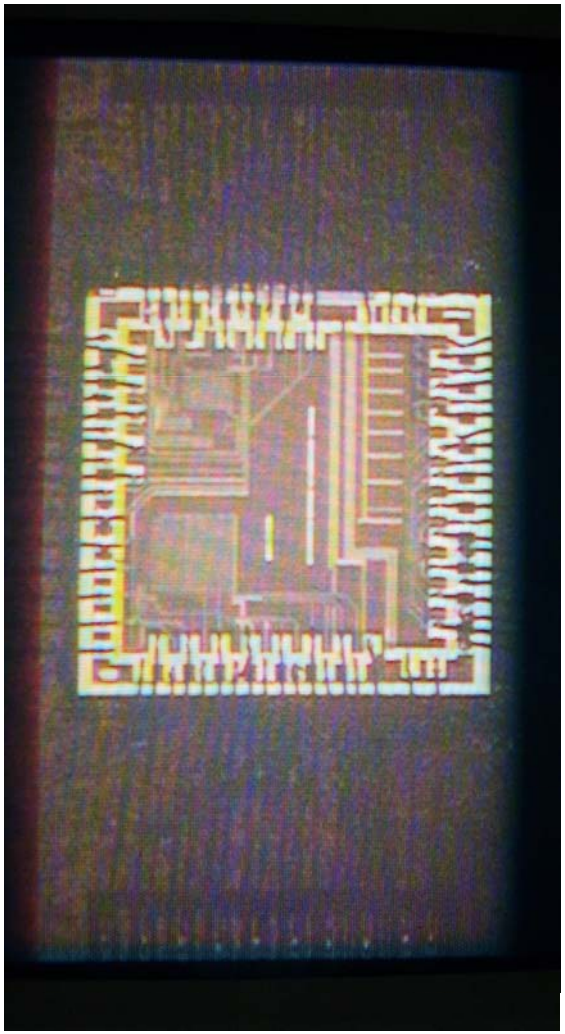
N= number of cell per pixel
M= number of chips composing the detector

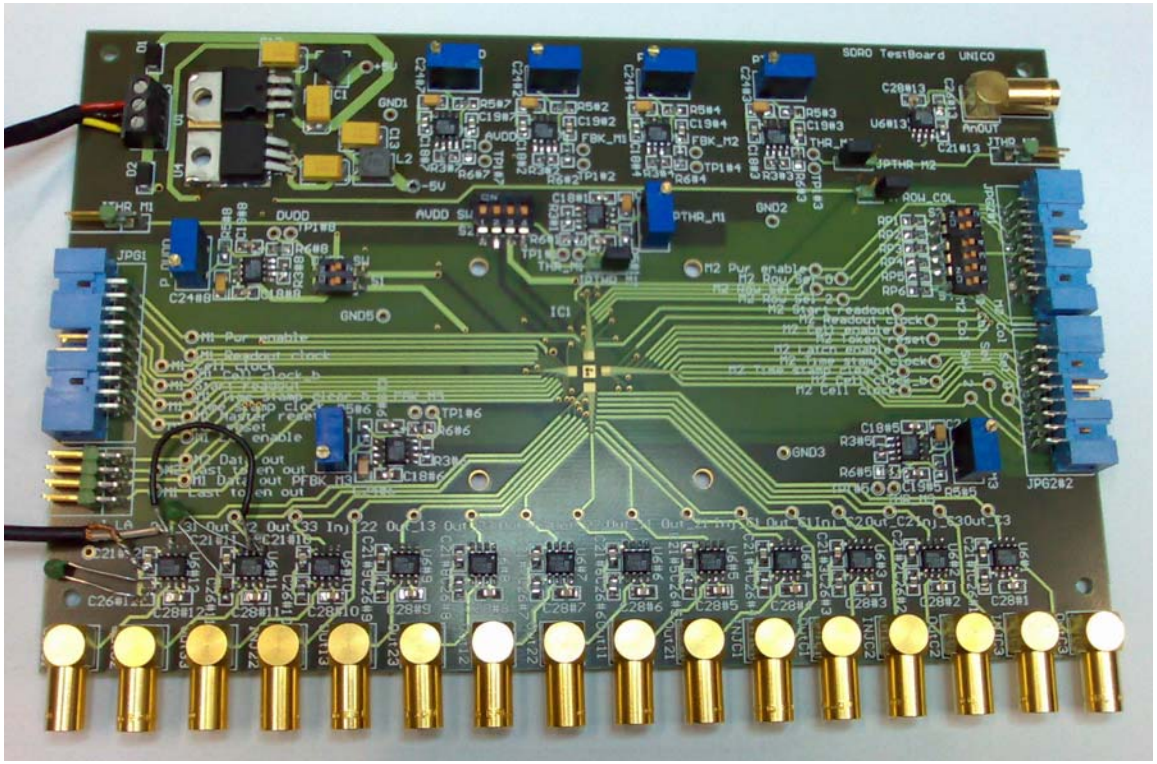
The demonstrator chip (SDR0)

- The chip includes:
  - a 16 by 16 MAPS matrix (25 μm pitch) with digital sparsified readout
  - an 8 by 8 MAPS matrix (25 μm pitch) with digital sparsified readout and selectable access to the output of the PA in each cell
  - a 3 by 3 MAPS matrix (25 μm pitch) with all of the PA output accessible at the same time
  - 3 standalone readout channels with different C_D (detector simulating capacitance)
- Delivered end of July 2007



SDRO chip and test board



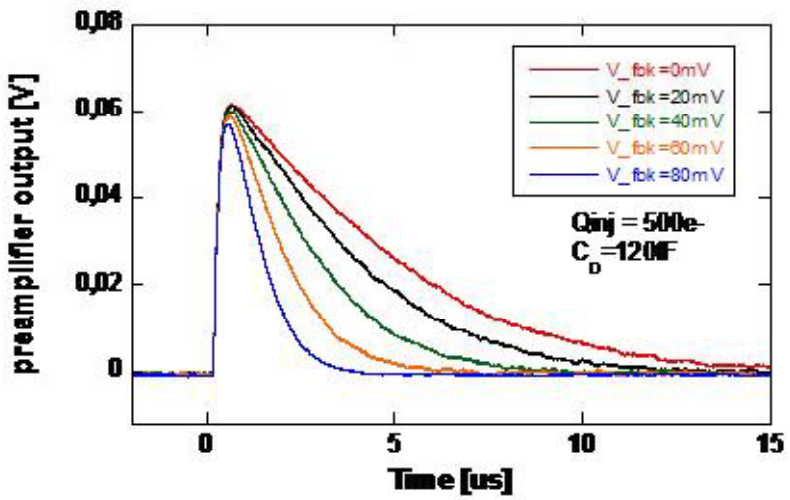


Test board designed by Marcin Jastrzab
University of Science and Technology, Cracow (Poland) and University of Insubria, Como (Italy)

Credit: Fabio Risigo University of Insubria, Como (Italy)

SDRO experimental results

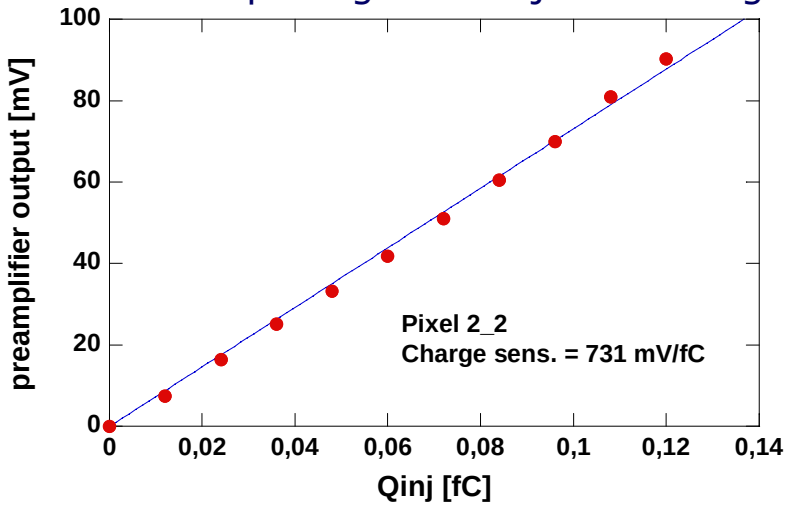
Preamplifier response
to an external calibration signal



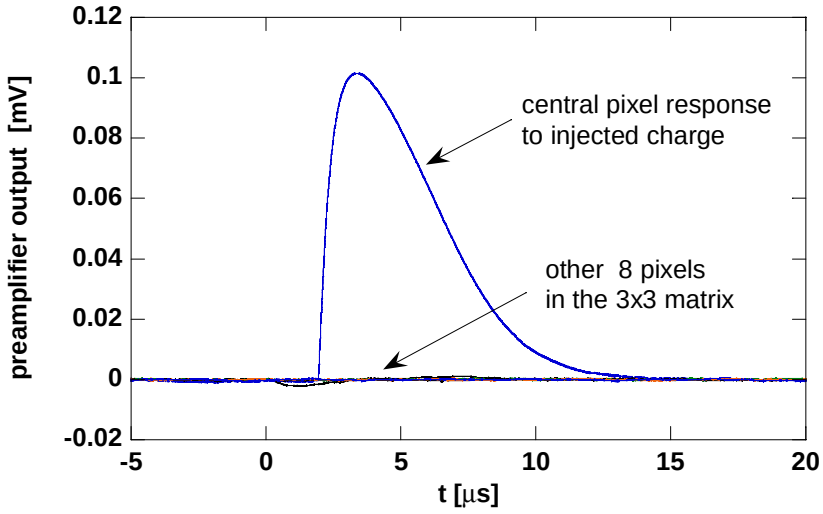
- Average **charge sensitivity ≈ 0.7 V/fC**
- ENC = **40 e rms @ C_D=120 fF**

  (preamplifier input device: I_D = 1 μA, W/L = 22/0.25)
- **Threshold dispersion ≈ 60 e** (in 8x8 matrix)

Pixel output signal vs injected charge

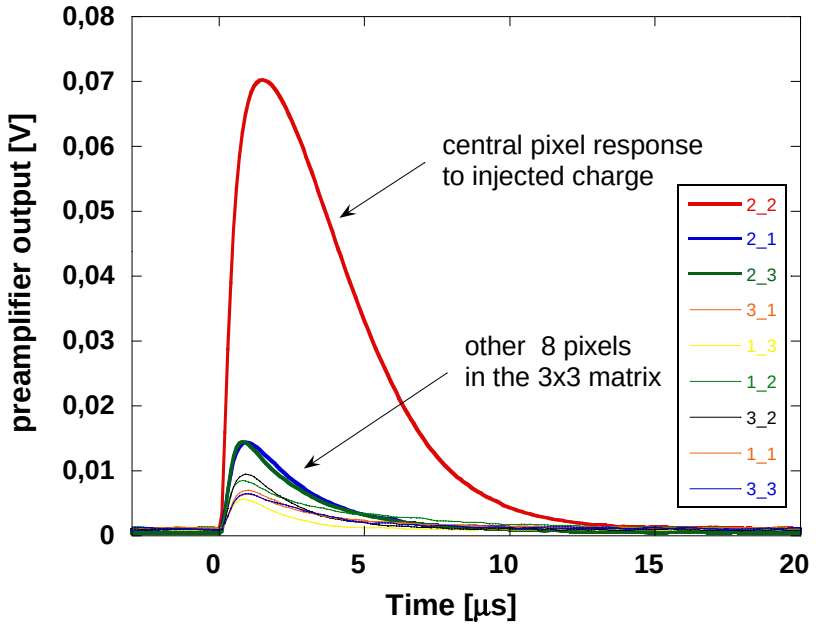


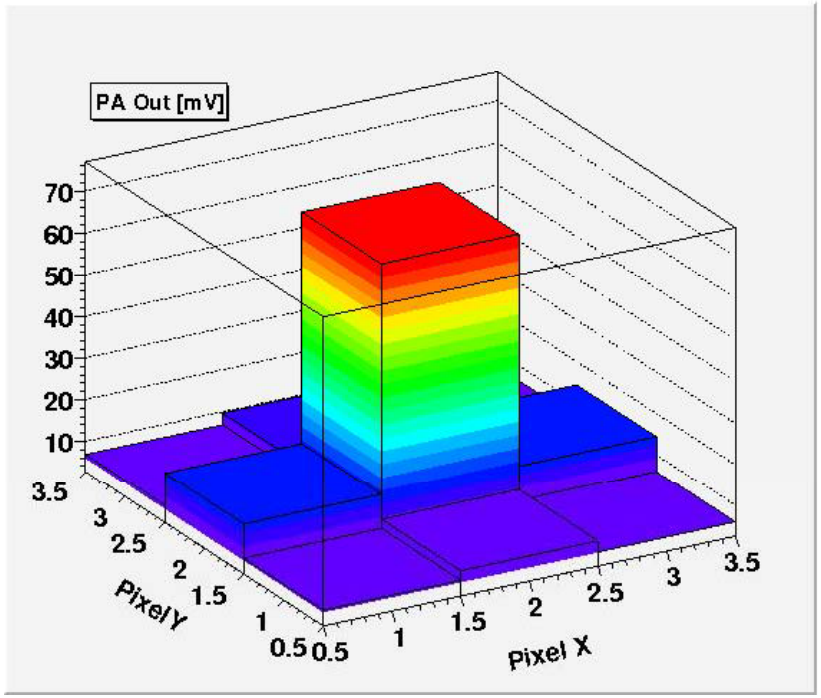
No crosstalk between pixels,
no correlated noise



SDRO experimental results

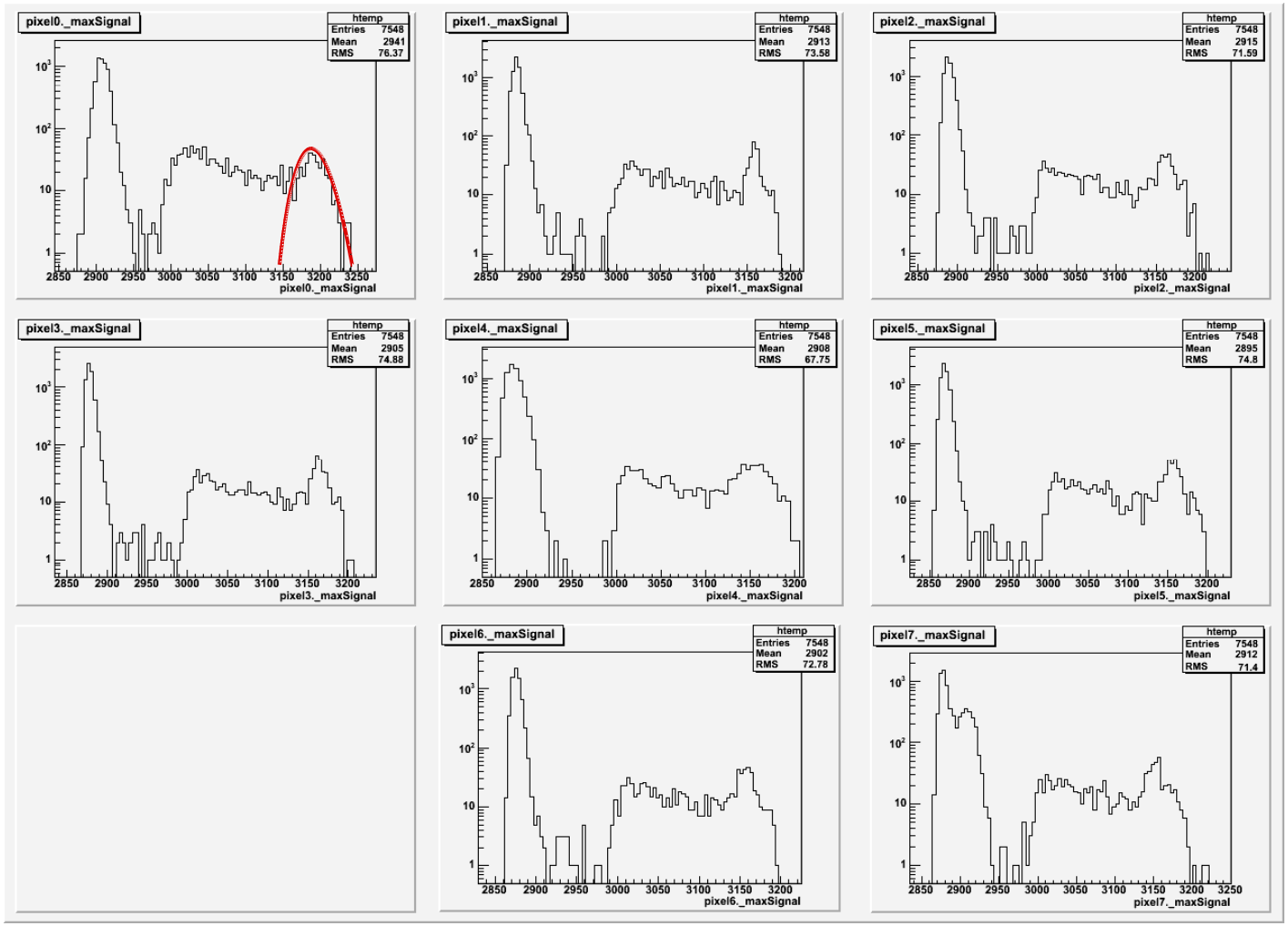
3x3 matrix response to infrared laser





SDRO experimental results

3x3 matrix response to ^{55}Fe source



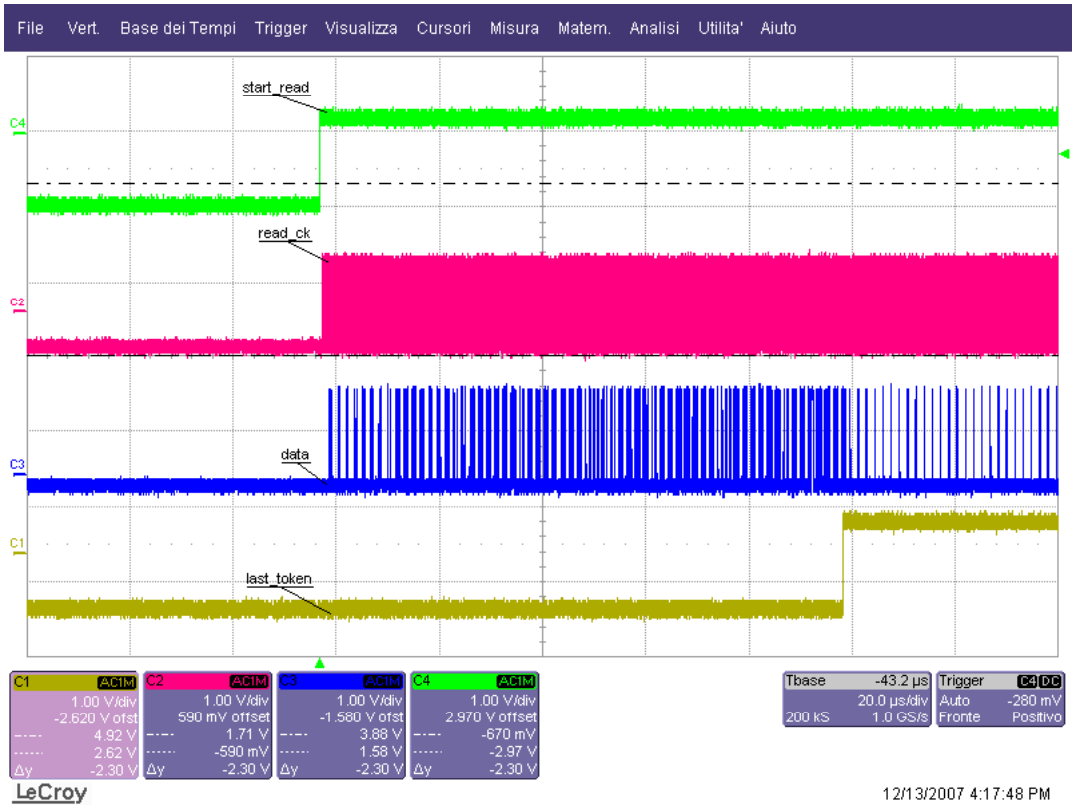
^{55}Fe data confirm pixel gain calibration

SDRO experimental results

Digital readout: pixel address (8x8 matrix)

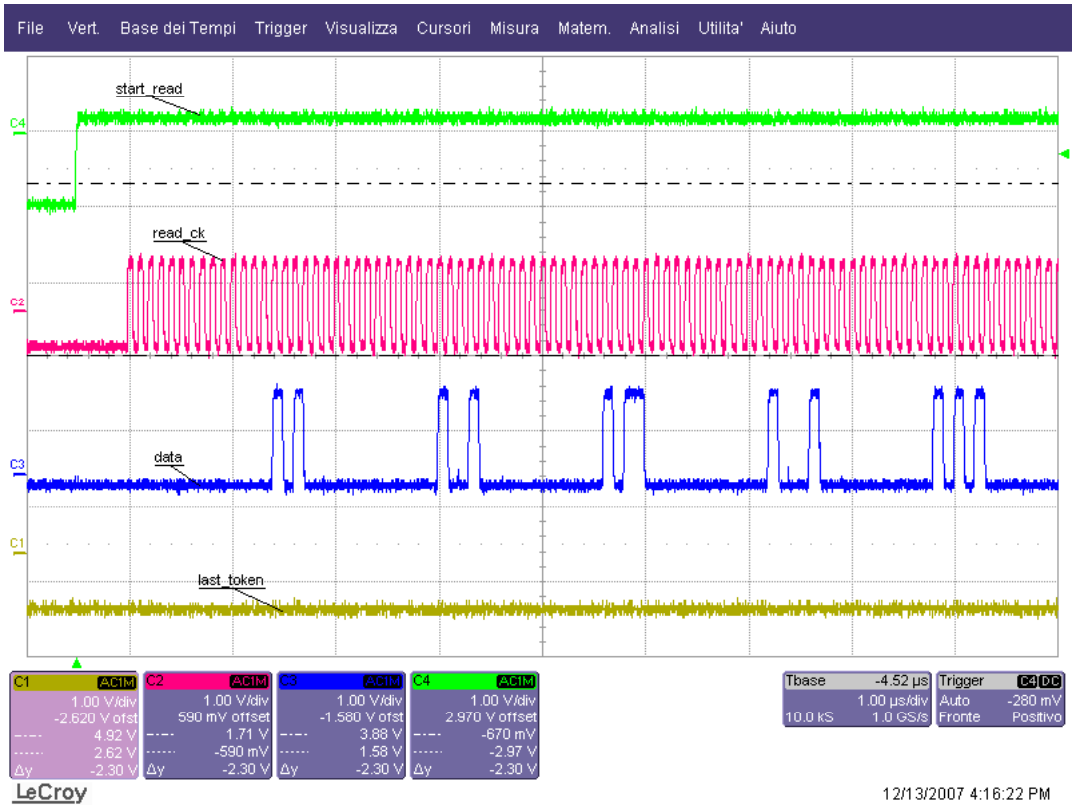
SDRO experimental results

Digital readout: pixel address (8x8 matrix)



SDRO experimental results

Digital readout: pixel address (8x8 matrix)

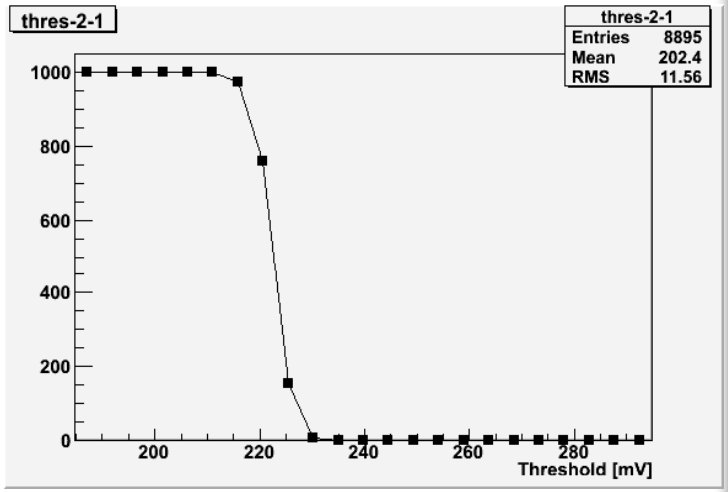


SDRO experimental results

Digital readout: pixel address (8x8 matrix)

SDRO experimental results

Digital readout: threshold scan (8x8 matrix)



SDRO experimental results

Digital readout: time stamp (8x8 matrix)

Notepad++ - C:\Documents and Settings\Utente\Desktop\slim215.txt

File Modifica Cerca Visualizza Formato Linguaggio Configurazione Macro Esegui Plugins ?

slim215.txt

		Data_bit		
592	0	0	synchro	
593	0	1	synchro	
594	0	0	synchro	
595	0	1	x0	
596	0	1	x1	X=7
597	0	1	x2	
598	0	0	x3	
599	0	0	y0	
600	0	1	y1	
601	0	1	y2	Y=6
602	0	0	y3	
603	0	1	ts0	
604	0	1	ts1	
605	0	0	ts2	TS=2
606	0	0	ts3	
607	0	0	ts4	
608	0	0	synchro	
609	0	1	synchro	
610	0	0	synchro	
611	0	1	x0	
612	0	0	x1	X=1
613	0	0	x2	
614	0	0	x3	
615	0	1	y0	
616	0	1	y1	Y=7
617	0	1	y2	
618	0	0	y3	
619	0	0	ts0	
620	0	0	ts1	
621	0	0	ts2	TS=0
622	0	0	ts3	
623	0	0	ts4	
624	0	0	synchro	
625	0	1	synchro	
626	0	0	synchro	
627	0	0		
628	0	1		

Normal text file

Notepad++ - C:\Documents and Settings\Utente\Desktop\slim215.txt

File Modifica Cerca Visualizza Formato Linguaggio Configurazione Macro Esegui Plugins ?

slim215.txt

		Data_bit		
640	0	0	synchro	
641	0	1	synchro	
642	0	0	synchro	
643	0	1	x0	
644	0	1	x1	X=3
645	0	0	x2	
646	0	0	x3	
647	0	1	y0	
648	0	1	y1	
649	0	1	y2	Y=7
650	0	0	y3	
651	0	0	ts0	
652	0	0	ts1	
653	0	0	ts2	TS=0
654	0	0	ts3	
655	0	0	ts4	
656	0	0	synchro	
657	0	1	synchro	
658	0	0	synchro	
659	0	0	x0	
660	0	0	x1	X=4
661	0	1	x2	
662	0	0	x3	
663	0	1	y0	
664	0	1	y1	Y=7
665	0	1	y2	
666	0	0	y3	
667	0	1	ts0	
668	0	0	ts1	
669	0	0	ts2	TS=14
670	0	1	ts3	
671	0	0	ts4	
672	0	0	synchro	
673	0	1	synchro	
674	0	0	synchro	

Explore more advanced technological solutions: Vertical Integration

- Vertical integration between two layers of 130nm CMOS chips.

  The first layer may include a MAPS device with analog readout, and the second layer the digital readout circuits

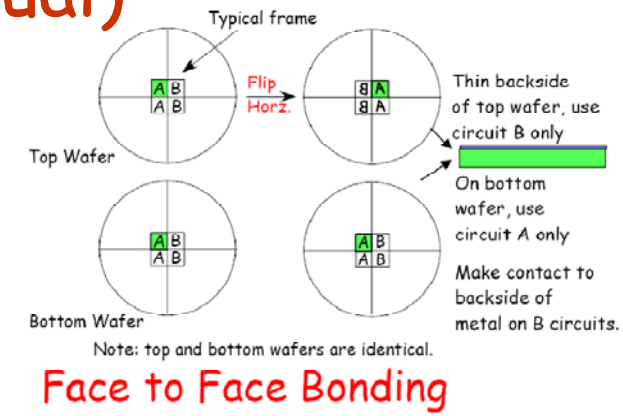
  (from an idea of Ray Yarema)

- Overcome limitations typically associated to "conventional" and DNW CMOS MAPS:
  - Reduced pixel pitch
  - 100 % fill factor (few or no PMOS in the sensor layer)
  - Better S/N vs power dissipation performance (smaller sensor capacitance)
  - Reduction of possible analog-to-digital interferences
  - Increased pixel functionalities (multiple hit handling, analog information)

3D vertical integration based on DNW MAPS (conceptual)

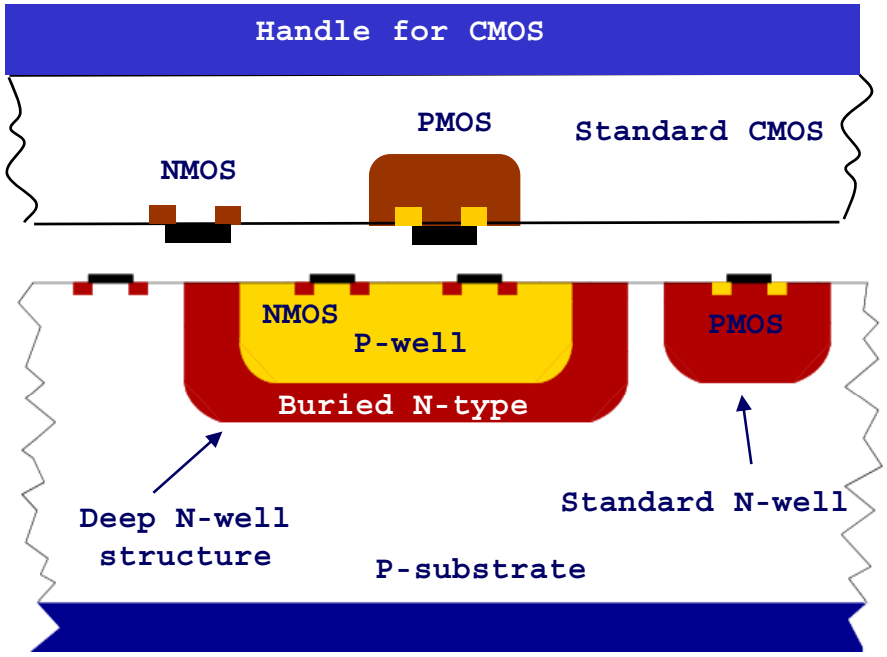
Use vertical integration technology to interconnect two 130nm CMOS layers

(R. Yarema)



Mostly digital CMOS tier
Tier interconnection and vias with industrial technique

Analog and sensor CMOS (mostly NMOS) tier



Conclusions

- INFN R&D program aims at developing 130nm CMOS MAPS with sparsified readout and time stamping for the ILC vertex detector
- DNW MAPS structures have been fabricated in a 130 nm, triple well CMOS technology; **for the first time ever we have MAPS with pixel-level sparsification and time stamping**
- Several issues have to be addressed to meet ILC specifications (pixel pitch, detection efficiency)

  Binary readout: ILC VTX demands a pixel pitch < 20 μm.

- Plans for the future:
  - Tests of SDR0 structures with ^{90}Sr and in a beam
  - Design of a 256 x 256 matrix for beam test (2008)
  - Evaluation of microelectronic technologies with higher integration density (90 nm CMOS, 3D Vertical Integration)

Acknowledgments

I want to thank the ILC pixel R&D group at Fermilab for the very useful discussions that helped us to choose the SDR0 chip architecture.

Backup slides

Design specifications for the ILC vertex detector

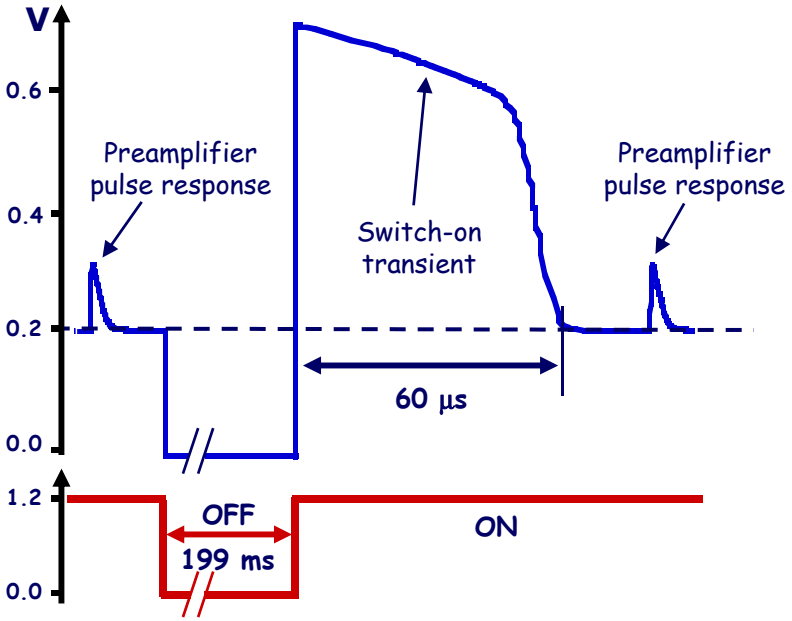
SDR0 prototype

Hit rate [particles/bco/mm^2]	Detector pitch [μm]					
	5	10	15	20	25	30
0.03	99.99%	99.97%	99.84%	99.52%	98.87%	97.76%
0.06	99.99%	99.87%	99.39%	98.20%	95.91%	92.26%
0.09	99.98%	99.72%	98.69%	96.20%	91.70%	84.93%
0.12	99.97%	99.52%	97.76%	93.68%	86.66%	76.75%
0.15	99.95%	99.26%	96.62%	90.75%	81.13%	68.36%

Detection efficiency for different sensor pitch and hit rate values

Power cycling simulations

- Power cycling can be used to reduce average dissipated power by switching the chip off when no events are expected
- Example:
  - ✓ILC bunch structure: ~330 ns spacing, ~3000 bunches, 5Hz pulse
- The analog section in the elementary cell can be switched off during the intertrain interval in order to save power (analog power is supposed to be predominant over digital)



- Based on circuit simulations, power cycling with at least **1% duty-cycle** seems feasible