Optimising CMOS Pixel Sensors for the ILC Micro-Vertex Detector

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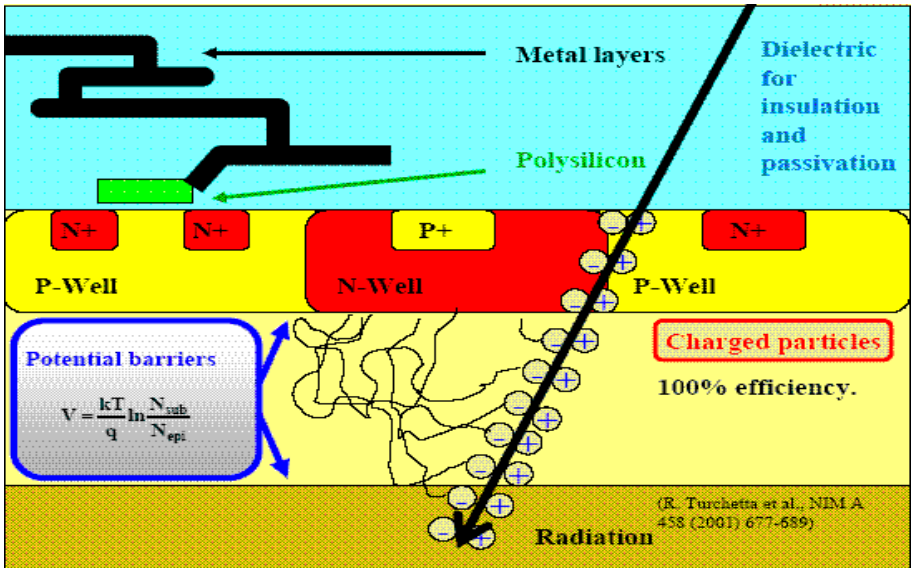
▷ **More information on IPHC Web site:** **http://wwwires.in2p3.fr/ires/web2/rubrique.php3?id_rubrique=63**

OUTLINE

- **Reminder on CMOS sensors:** *Specific advantages* *Specific limitations*
- **Achieved performances with analog output sensors** **(AMS-0.35 OPTO fab. process) :**
  - *Detection efficiency* *Spatial resolution* *Operating temperature* *Radiation tolerance*
  - *Thinning* *Ladder design* *Current applications (telescopes)*
- **Fast read-out architecture:** *State of the art* *Plans until 2009/10*
- **Summary – Outlook**

Main Features and Advantages of CMOS Sensors

- p-type low-resistivity Si hosting n-type "charge collectors"
  - signal created in epitaxial layer (low doping):
    $Q \sim 80$ e-h / $\mu m \mapsto$ signal $\lesssim 1000\ e^-$
  - charge sensing through n-well/p-epi junction
  - excess carriers propagate (thermally) to diode
    with help of reflection on boundaries
    with p-well and substrate (high doping)



- Specific advantages of CMOS sensors:
  - ◇ Signal processing μcircuits integrated on sensor substrate (system-on-chip) $\mapsto$ compact, flexible
  - ◇ Sensitive volume ($\sim$ epitaxial layer) is $\sim$ 10–15 μm thick $\longrightarrow$ thinning to $\sim$ 30–40 μm permitted
  - ◇ Standard, massive production, fabrication technology $\longrightarrow$ cheap, fast turn-over
  - ◇ Room temperature operation
  - ◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation

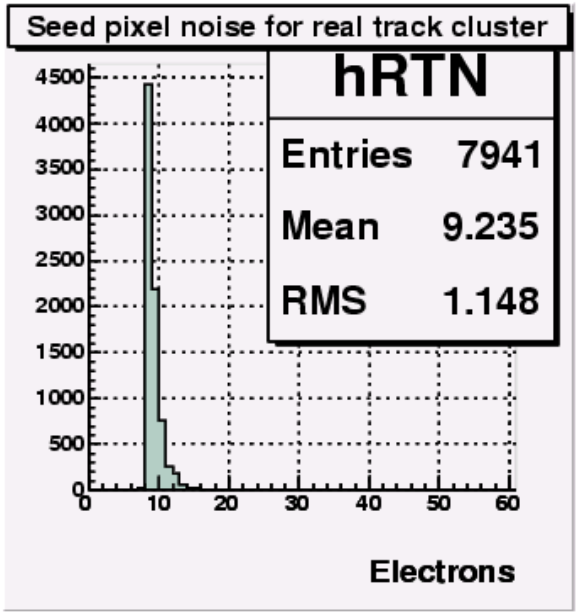
- **BUT :**
  - ⋈ Very thin sensitive volume $\rightarrowtail$ impact on signal magnitude (mV !)
  - ⋈ Sensitive volume almost undepleted $\rightarrowtail$ impact on radiation tolerance & speed
  - ⋈ Commercial fabrication (parameters) $\rightarrowtail$ impact on sensing performances & radiation tolerance
  - ⋈ NWELLS used for charge coll. $\rightarrowtail$ restricted use of PMOS transistors

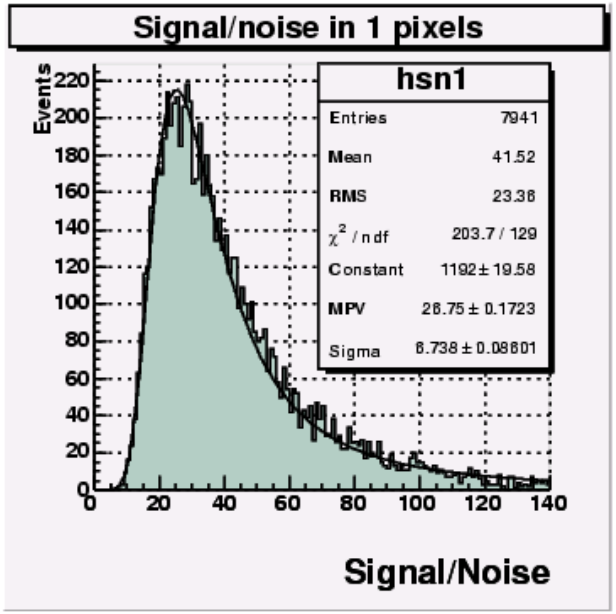
Achieved Performances

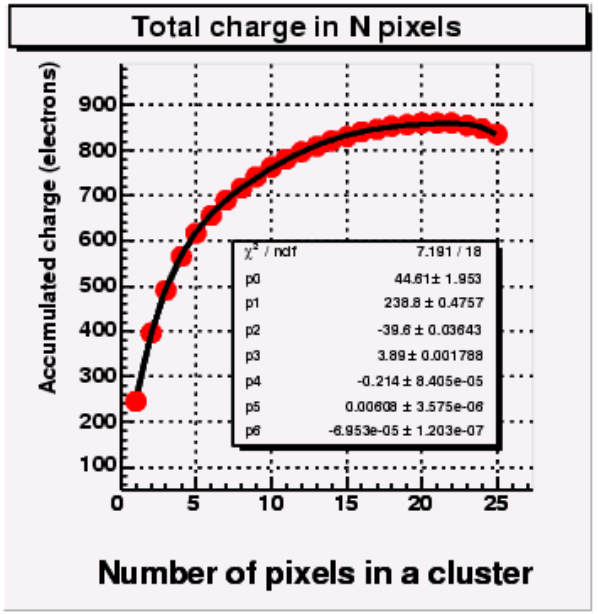
with Analog Output Sensors

M.I.P. Detection with CMOS Sensors

- *$\sim$ 100 chips (M1, M2, M4, **M5**, M8, M9, M11, M14, M15, M16, **M17**, **M18**) tested on H.E. beams since 2001 at CERN-SPS & DESY, mounted on Si-strip telescope (calibrated with ^{55}Fe) $\mapsto$ well established perfo. (analog output):*
  - *Best performing technology: AMS 0.35 μm OPTO $\rightarrowtail$ $\sim$ 11 & 15 μm epitaxy (called epi-14 and epi-20)*
  - *$N \sim 10\ e^-$ ENC $\mapsto$ S/N $\gtrsim$ 20 – 30 (MPV) at room Temperature*





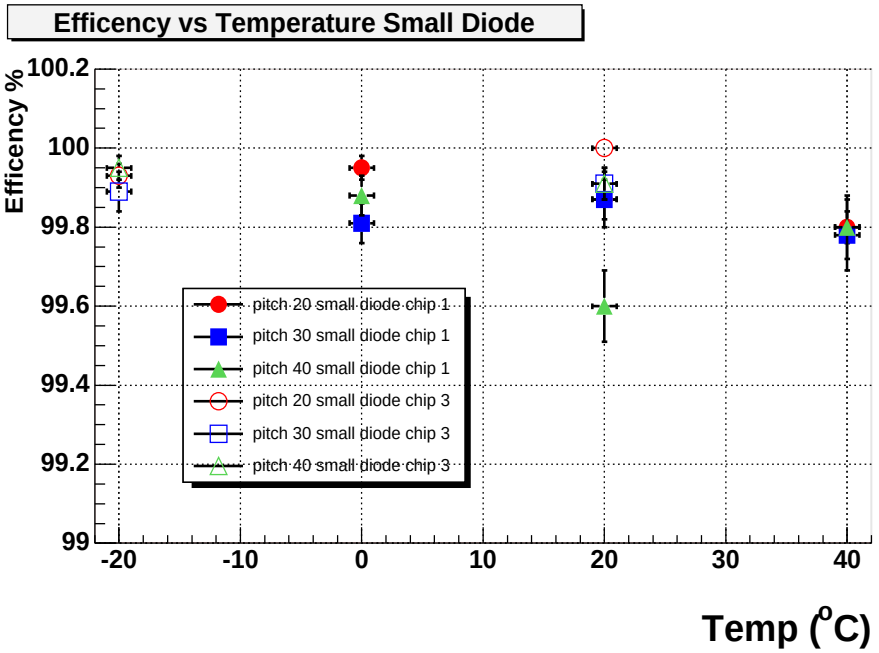


- *Technology without epitaxy also performing well : very high S/N but large clusters (hit separation $\searrow$)*
- *Macroscopic sensors : MIMOSA-5 ($\sim$ 1.7x1.7 cm^2; 1 Mpix) ; MIMOSA-20 (1x2 cm^2; 200 kpix) ; MIMOSA-17 (0.76x0.76 cm^2; 65 kpix) ; MIMOSA-18 (0.55x0.55 cm^2; 256 kpix)*

Detection Efficiency & Spatial Resolution

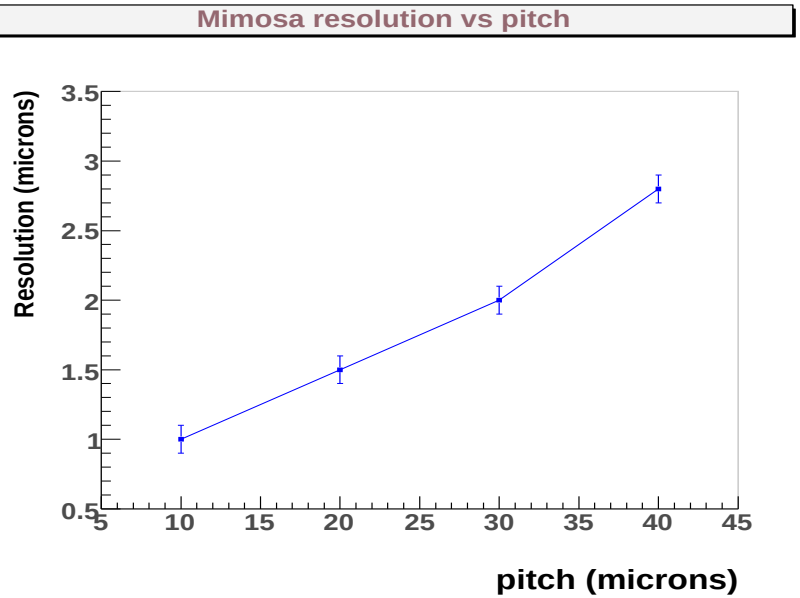
Detection efficiency:

- *Ex: MIMOSA-9 data (20, 30 & 40 μm pitch)*
- $\epsilon_{det} \gtrsim$ *99.5–99.9 % repeatedly observed at room temperature (fake rate* $\sim 10^{-5}$*)*
- $T_{oper.} \gtrsim 40\,^{\circ}C$



Single point resolution versus pixel pitch:

- *clusters reconstructed with eta-function, exploiting charge sharing between pixels (12-bit ADC)*
- $\sigma_{\mathbf{sp}} \sim \mathbf{1}\ \mu\mathbf{m}$ *(10* μm *pitch)* $\rightarrowtail \lesssim \mathbf{3}\ \mu\mathbf{m}$ *(40* μm *pitch)*
- *4-bit ADC simul.* $\Rrightarrow \sigma_{\mathbf{sp}} \lesssim \mathbf{2.}\ \mu\mathbf{m}$ *(20* μm *pitch)*



Radiation Tolerance: Summary of AMS-0.35 OPTO Evaluation

Requirements:

- **beamstrahlung (**GuineaPig X 3 **) :** $\lesssim 10^3$ **e**$^{\pm}_{BS}$**/cm**^{2}**/25** μs $\longrightarrow$ $\lesssim 2{\cdot}10^{12}$**e**$^{\pm}_{BS}$**/cm**^{2}**/yr**
  $\hookrightarrow$ **O(100) kRad/yr – O(10**^{11}**)** n_{eq}**/cm**^{2}**/yr (**NIEL $\sim$ 1/30**)**
- **neutron gas:** $\lesssim 10^{10}$ n_{eq}**/cm**^{2}**/yr (**MC X 10 **)**

Non-ionising radiation tolerance (20 μm pitch):

- **MIMOSA-15 irradiated with O(1 MeV) neutrons tested on DESY e**$^-$ **beams : Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 700\ \mu s$
  - **5.8·10**^{12} n_{eq}**/cm**^{2} **values derived with standard and with soft cuts**

Fluence	0	0.47	2.1	5.8 (5/2)	5.8 (4/2)
S/N (MPV)	27.8 $\pm$ 0.5	21.8 $\pm$ 0.5	14.7 $\pm$ 0.3	8.7 $\pm$ 2.	7.5 $\pm$ 2.
Det. Eff. (%)	100.	99.9 $\pm$ 0.1	99.3 $\pm$ 0.2	77. $\pm$ 2	84. $\pm$ 2.

Ionising radiation tolerance:

- **Pixels modified against hole accumulations (thick oxide) and leakage current increase (guard ring)**
- **MIMOSA-15 tested with $\sim$ 5 GeV e**$^-$ **at DESY after 1 MRad (10 keV X-Ray) exposure : Preliminary results**
  - T = - 20°C, $t_{r.o.} \sim 180\ \mu s$
  - $t_{r.o.} << 1$ms crucial at T_{room}

Integ. Dose	Noise	S/N (MPV)	Detection Efficiency
0	9.0 $\pm$ 1.1	27.8 $\pm$ 0.5	100 %
1 MRad	10.7 $\pm$ 0.9	19.5 $\pm$ 0.2	99.96 $\pm$ 0.04 %

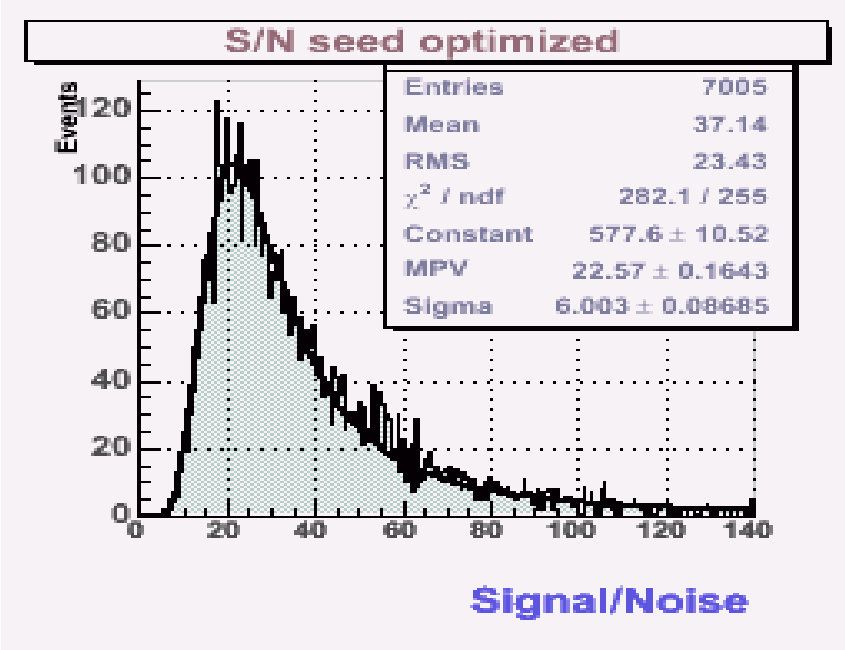
Provisional conclusion:

- **at least 3 years of running viable at T_{room} (or close to), more if T $\lesssim 0^\circ$C**
- **further assessment needed (also with $\sim$ 10 MeV e**$^-$**) : sensors with integ. CDS, ADC, ...**

Radiation Tolerance : Low Energy Electrons

Investigation of sensitivity to $\sim$ 10 MeV electrons (NIEL factor $\sim$ 1/30)

$\hookrightarrow$ **similar to beamstrahlung $e^{\pm}$ in 4 T field at 15 mm radius**



1) **MIMOSA-9 exposed to $10^{13} e^-_{9.4MeV}$/cm^2 in Darmstadt : equivalent to $\lesssim$ 300 kRad/cm^2 and $\sim 3 \cdot 10^{11} n_{eq}$/cm^2**

2) **Irradiated chip tested with $\sim$ 6 GeV e^- at DESY**

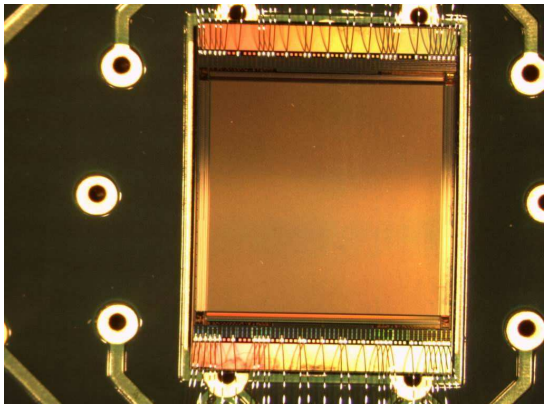
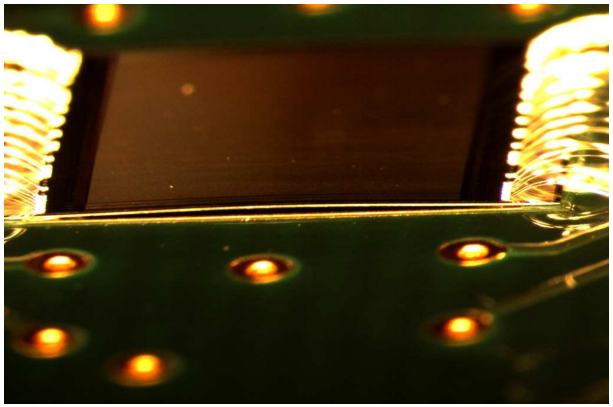
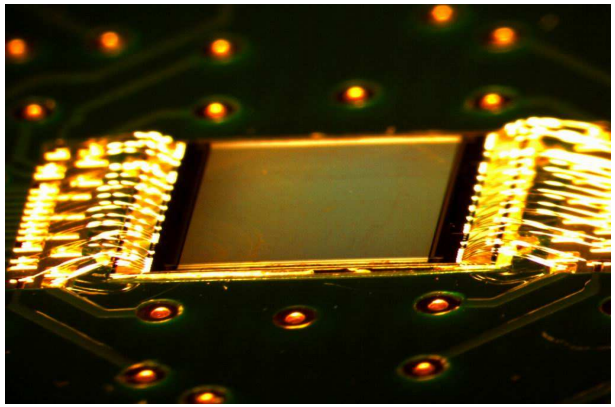
$\hookrightarrow$ **Test result at -20°C : S/N $\sim$ 23 $\rightarrowtail \epsilon_{det} > 99.3\%$**

(before irradiation: S/N $\sim$ 28 and ϵ_{det} = 99.93 $\pm$ 0.03 %)

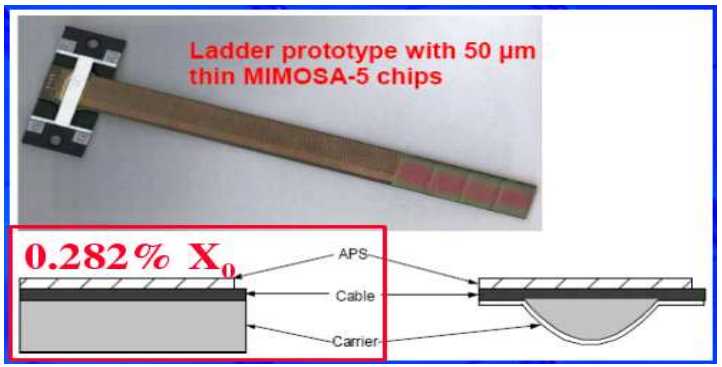
$\triangleright$ **Sensors may need to be also evaluated at room temperature (compatible with very light cooling system)**

System Integration

- **Industrial thinning (via STAR coll. at LBL)** $\rightarrowtail$ *MIMOSA-18 (5.5×5.5 mm^2 thinned to 50 μm)*

- **Devt of ladder equipped with MIMOSA chips (coll. with LBL) :** *STAR ladder ($\lesssim$ 0.3 % X_0)* $\rightarrowtail$ *ILC ($<$ 0.2 % X_0)*

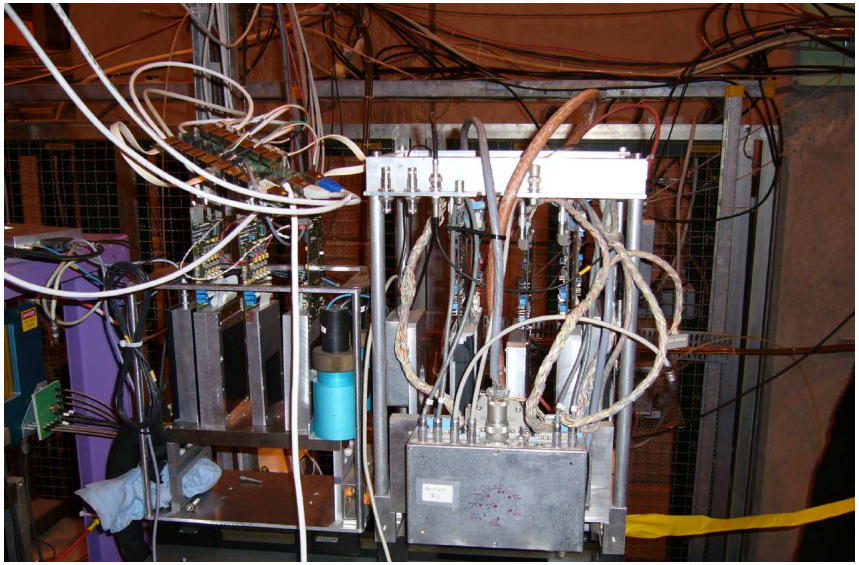


- **High precision packaging technologies :** $\rightarrowtail$ *mount & connect $\lesssim$ 5 MIMOSA-18, thinned to 50 μm, on support made of industrial diamond, thinned to 50–100 μm and aluminised $\equiv$ mecha. support & heat extractor & cable*

$\hookrightarrow$ *project started in 2007: diamond (50–100 μm) fabricated* $\rightarrowtail$ *assembly of MIMOSA-18 sensors under way*

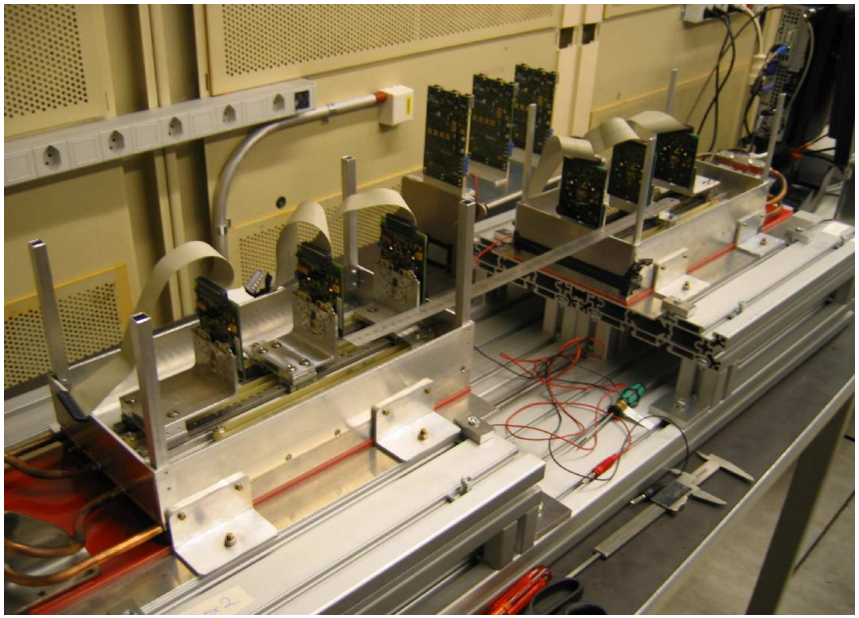
Applications of Sensors with Analog Output

- **Pixel telescope of IPHC (T.A.P.I.):**
  - *$\leq$ 4 MIMOSA-17 and/or -18 sensors*
  - *commissionned in June 2007 at DESY*
  - *data taking campaign in Sept. & Nov. '07 at CERN-SPS*
  - *read-out freq. $\sim$ 10 (M-18) or 25 frames/s (M-17)*
  - *installed in front of standard Si-strip telescope ▷▷▷▷▷*



- **STAR(RHIC) : telescope (3 MIMO-14) inside exp. apparatus (2007)** $\rightarrowtail$ *BG meast, no pick-up !*

- **Beam telescope of the FP6 project EUDET**
  - *2 arms of 3 planes (plus 1 high resolution plane)*
  - *$\sigma_{extrapol.} \lesssim 1\ \mu m$ with e^- (3 GeV, DESY)*
  - *2 steps :*
    - ◇ *2007: sensors with analog output*
      $\hookrightarrow$ *operationnal facility ($<$ 1 kframe/s)*
    - ◇ *end 2008: sensor with digital output and integrated $\emptyset$*
      $\hookrightarrow$ *read-out time $\sim$ 100 μs*

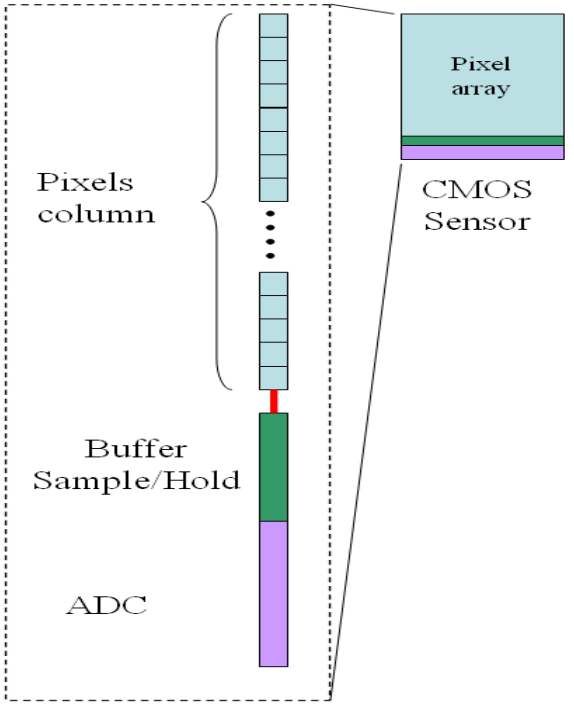


Achieved Performances an Present R&D

with Digital Output Sensors

Fast Read-Out Architecture

- **Parallel development of 3 components (analog, mixed, digital):**
  - **column // arrays with CDS/pixel & discriminated outputs**
  - **4-5 bit ADCs intended to replace discriminators**
  - **$\varnothing$ μcircuits & output memories**



- **2 stage approach :**

  1) Develop sensors for mid-term (2009) applications

  $\hookrightarrow$ less severe requirements, almost suited to 3 outer layers:

  - **EUDET: 1x2 cm^2, t$_{r.o.}$ $\sim$ 100 μs, discri. binary charge encoding (no ADC);**
  - **STAR: 2x2 cm^2, t$_{r.o.}$ $\sim$ 200 μs, discri. binary charge encoding (no ADC);**

  $\hookrightarrow$ will be operated in real experimental conditions by 2009/2010

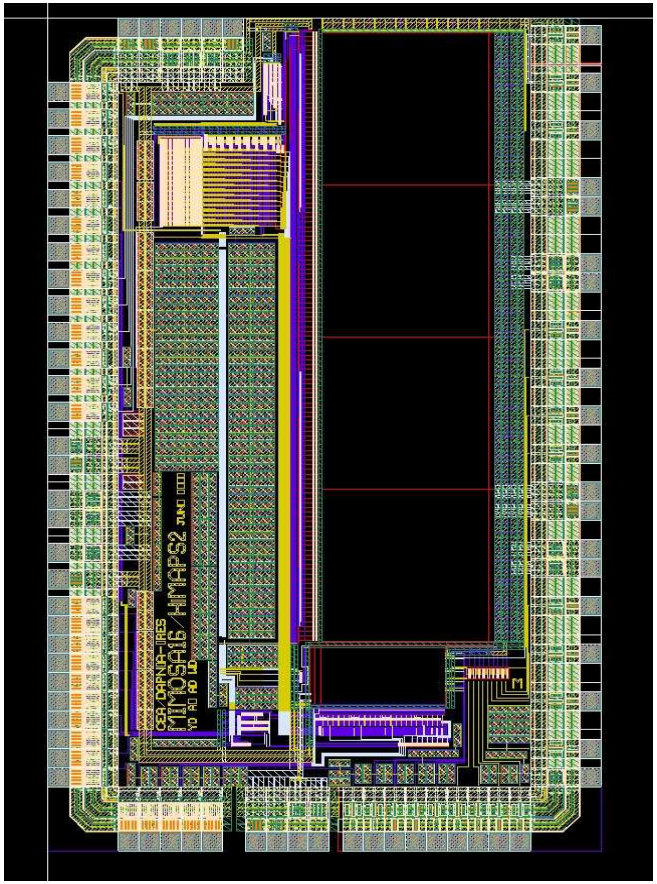
  2) Develop ILC sensors (mainly for inner layers) extrapolating from EUDET & STAR:

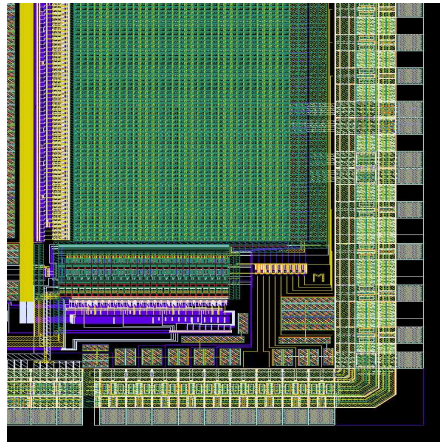
  - **increase row read-out frequency by $\sim$ 50 %**
  - **replace discriminators with ADCs**

High R.-O. Speed Architecture : 2nd Prototype = MIMOSA-16

MIMOSA-16 design features :

- AMS-0.35 OPTO translation of MIMOSA-8
  $\hookrightarrow \sim$ 11–15 μm epitaxy instead of $\lesssim$ 7 μm
- 32 // columns of 128 pixels (pitch: 25 μm)
- on-pixel CDS (DS at end of each column)
- 24 columns ended with discriminator
- 4 sub-arrays :
  - S1 : like MIMOSA-8 (1.7x1.7 μm^2 diode)
  - S2 : like MIMOSA-8 (2.4x2.4 μm^2 diode)
  - S3 : S2 with ionising radiation tol. pixels
  - S4 : with enhanced in-pixel amplification
    (against noise of read-out chain)





Tests of analog part (”20” & ”14” μm epitaxy) :

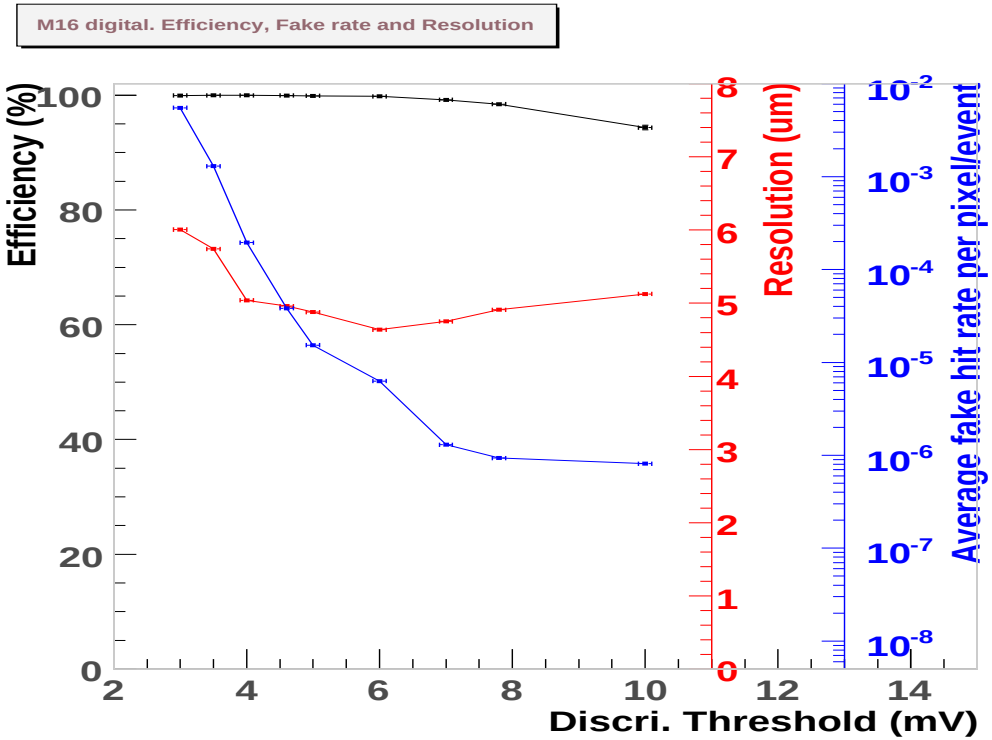
- sensors illuminated with ^{55}Fe source and $F_{r.o.}$ varied up to $\gtrsim$ 150 MHz
- measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs $F_{r.o.}$

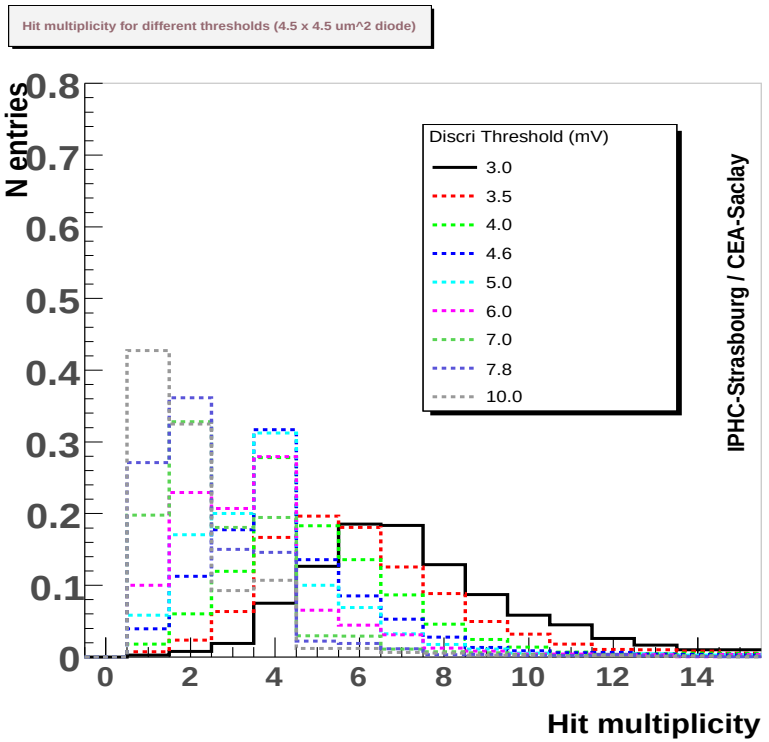
M.i.p. detection with Si-stip telescope studied at CERN in Sept. ’07 $\longrightarrow$ characterisation of digital response :

- π^- beam of $\sim$ 180 GeV/c
- measurements of SNR, det. efficiency, fake rate, cluster characteristics, spatial resolution vs discri. threshold

MIMOSA-16 Beam Test Results (Digital Part)

- **CERN-SPS ($\sim$ 180 GeV π^-) $\longmapsto$ results of S4 ("14 μm" epitaxy)**
- **Read-out time $\sim$ 50 μs** *($\sim$ 1/4 of max. freq. due to DAS limitations)*





- **Pixel architecture validated for next steps : S4 (SNR $\sim$ 16)**

Discri. Threshold	*det. efficiency*	*fake rate*	*sgle pt resolution*
4 m V	*99.96 $\pm$ 0.03 (stat) %*	*$\sim 2{\cdot}10^{-4}$*	*$\sim$ 4.8–5.0 μm*
6 m V	*99.88 $\pm$ 0.05 (stat) %*	*$<10^{-5}$*	*$\sim$ 4.6 μm*

Main Characteristics of the MIMOSA-22 Sensor

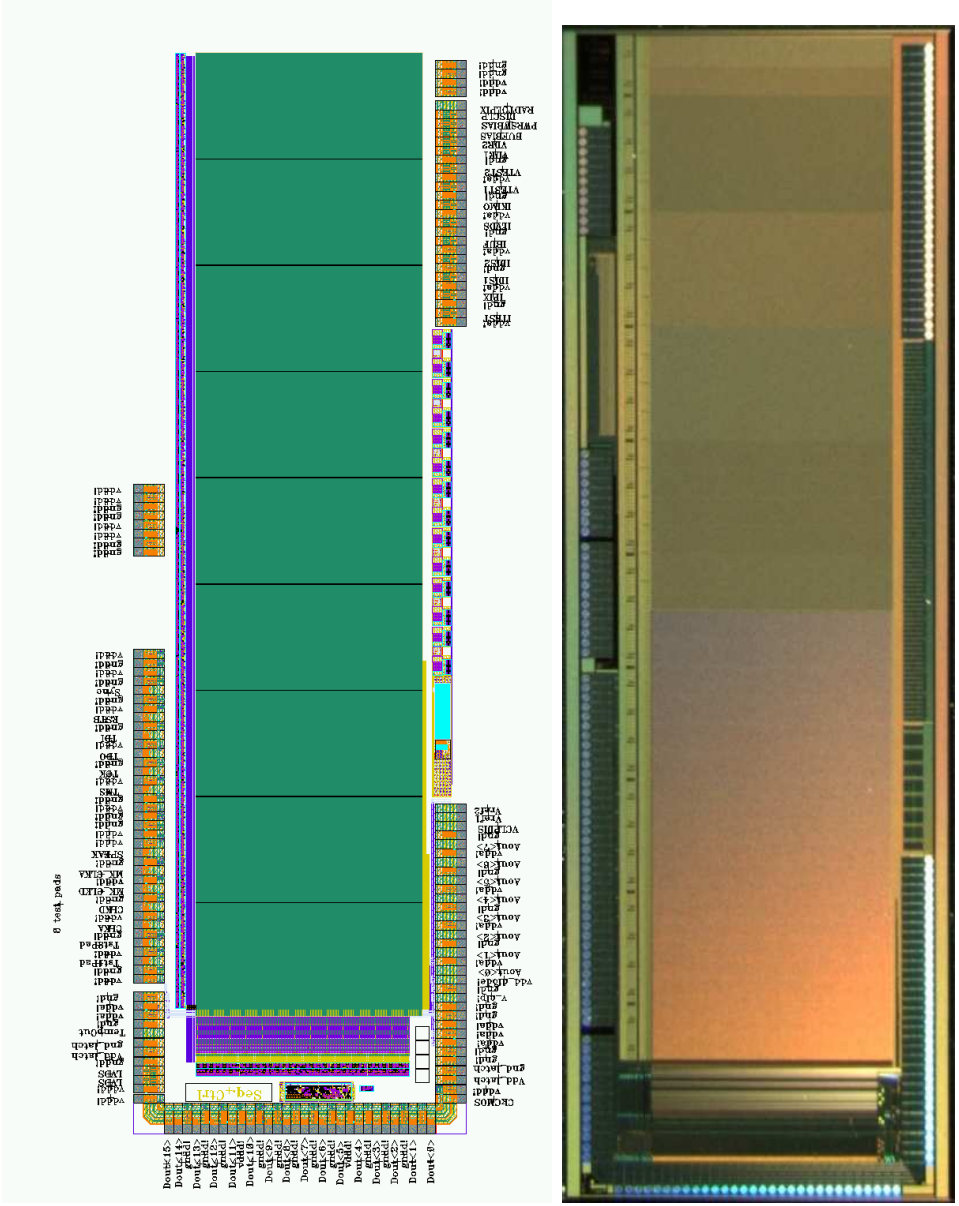
♣ **Extension of MIMOSA-16 ⟼ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

■ Pixel characteristics (*optimal charge coll. diode size ?*) :

- ※ pitch : 18.4 μm (compromise resolution/pixel layout)
- ※ diode surface : $\sim$ 10–15 μm^2 to optimise charge coll. & gain
- ※ 128 columns ended with discriminator
- ※ 8 columns with analog output for test purposes
- ※ 9 sub-matrices of 64 rows :
  - 17 pixel designs w/o ionising rad. tol. diode
  - ⟹ active digital area : 128 x 576 pixels ($\sim$ 25 mm^2)
- ※ read-out time $\sim$ 100 μs

■ Testability :

- ※ JTAG + bias DAC ⟼ programmable chip steering
- ※ 2 additionnal DC voltages to emulate pixel's output
  - for independent discriminator performance assessment
- ※ output frequency $\leq$ 40 MHz

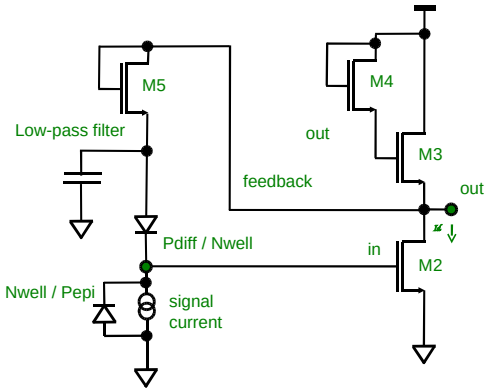


MIMOSA-22 Lab Tests : Analog Output Results (1/2)

Best performing pixels (rad. tol. design) :

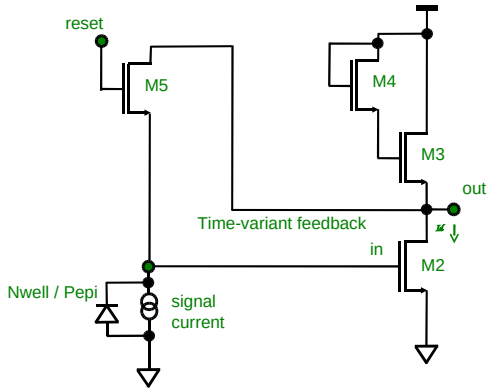
- *self-biased feedback diode (improved gain)*

Amplifier schematics (3): improved common source + continuously biased from feedback (self-biased)



- *reset diode (improved gain)*

Amplifier schematics (4): improved common source + reset from feedback (time-variant feedback)



Main results obtained with exposure to ^{55}Fe source :

- *Chip-4 ; $F_{r.o.}$ = 100 MHz ($t_{r.o.}$ = 92.5 μs) ; $T \simeq 15\,^{\circ}C$ (coolant) / $20\,^{\circ}C$ (chip) ;*

Pixel	diode	Noise (ENC)	CCE (4 pix)	CCE (9 pix)	CEE (25 pix)	comment
S6	14.6 μm^2	12.4 e^-	57 %	73 %	84 %	rad.tol. – self-bias – high gain
S7	14.6 μm^2	11.4 e^-	58 %	75 %	85 %	stand. – self-bias – high gain
S8	19.4 μm^2	12.8 e^-	65 %	82 %	90 %	stand. – self-bias – high gain
S9	11.6 μm^2	10.5 e^-	54 %	72 %	83 %	stand. – self-bias – high gain
S10	15.2 μm^2	13.3 e^-	60 %	77 %	86 %	rad.tol. – feedback reset – high gain
S12	15.2 μm^2	11.8 e^-	58 %	75 %	84 %	stand. – feedback reset – high gain

Dispersion between chips (rad. tol. pixels, with high gain) :

Pixel	chip	Noise (ENC)	CCE (4 pix)	CCE (9 pix)	CEE (25 pix)
S6	4	12.4 e^-	57 %	73 %	84 %
	3	12.7 e^-	59 %	76 %	86 %
	1	12.6 e^-	58 %	74 %	85 %
S10	4	13.3 e^-	60 %	77 %	86 %
	3	12.8 e^-	58 %	75 %	85 %
	1	13.5 e^-	59 %	76 %	86 %

Sensitivity to operating temperature (rad. tol. pixels, with high gain) :

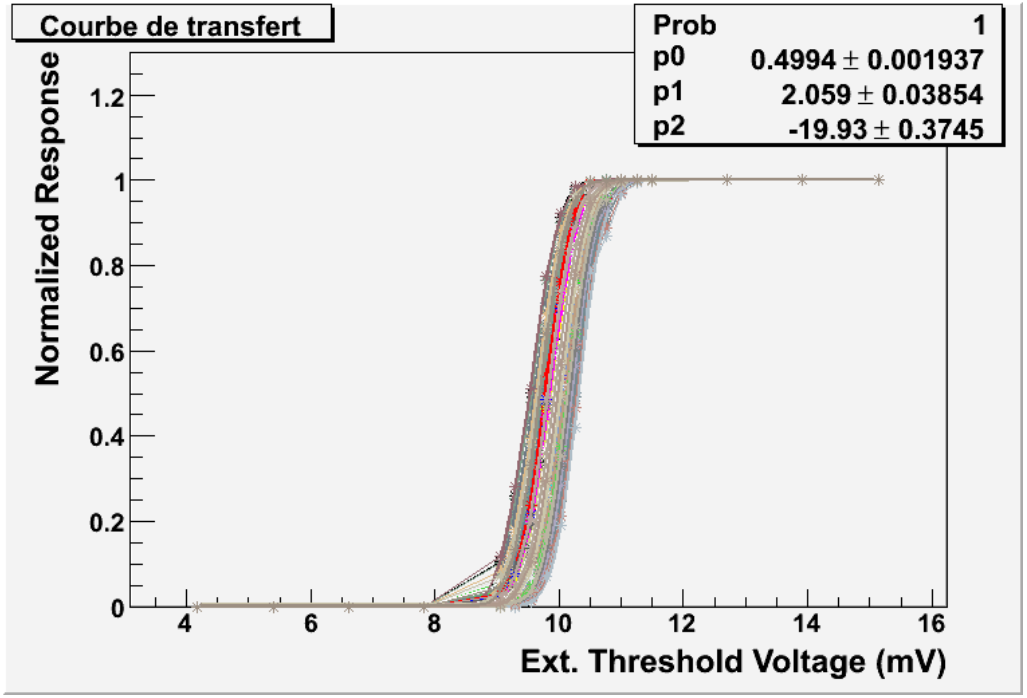
Pixel	T ($^\circ$C)	Noise (ENC)	CCE (4 pix)	CCE (9 pix)	CEE (25 pix)
S6	0 / 10	12.5 e^-	58 %	75 %	85 %
	10 / 15	12.6 e^-	58 %	74%	85%
	30 / 35	13.0 e^-	59 %	76 %	80 %
S10	0 / 10	12.8 e^-	59 %	77 %	84 %
	10 / 15	13.5 e^-	59 %	76 %	86 %
	30 / 35	14.2 e^-	60 %	76 %	86 %

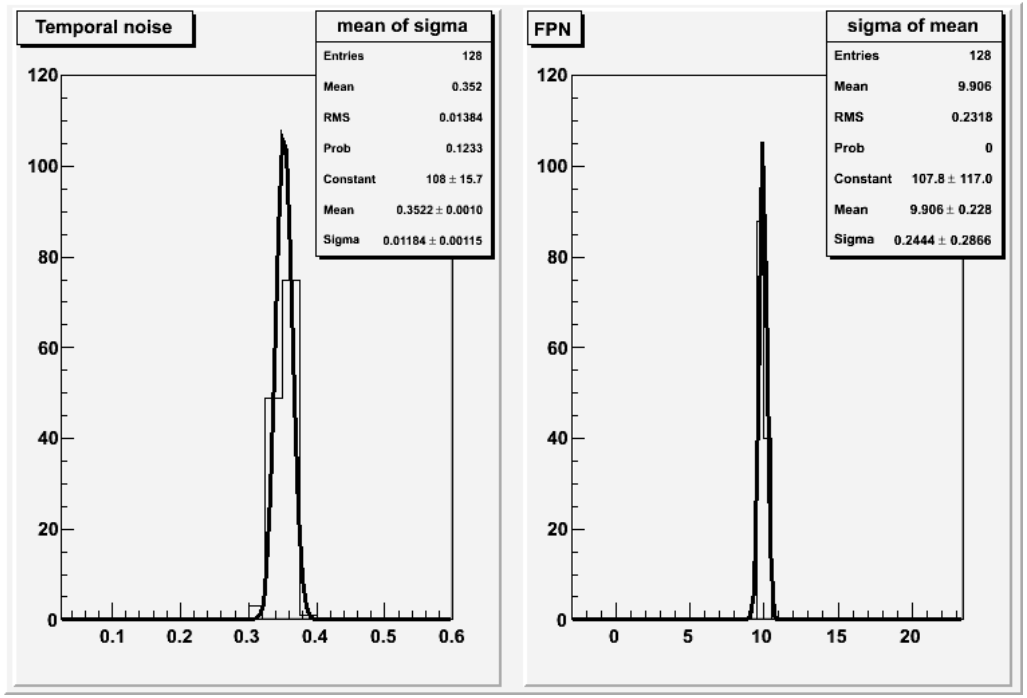
Conclusions :

- *Pixel array operationnal at nominal frequency and room temperature*
- *Rad. tol. pixel exhibits rather moderate noise (12.5–13.5 e^- ENC), $\sim$ +1 e^- ENC w.r.t. standard diode*
- *Self-bias pixel seems slightly less noisy than reset pixel $\longmapsto$ assess ionising rad. tol. before chosing*

MIMOSA-22 Lab Tests : Digital Output Results (1/2)

■ **Uniform voltage (0 ⟶ 10 mV) injected in discri. ⟶ transfer functions of all 128 discriminators :**





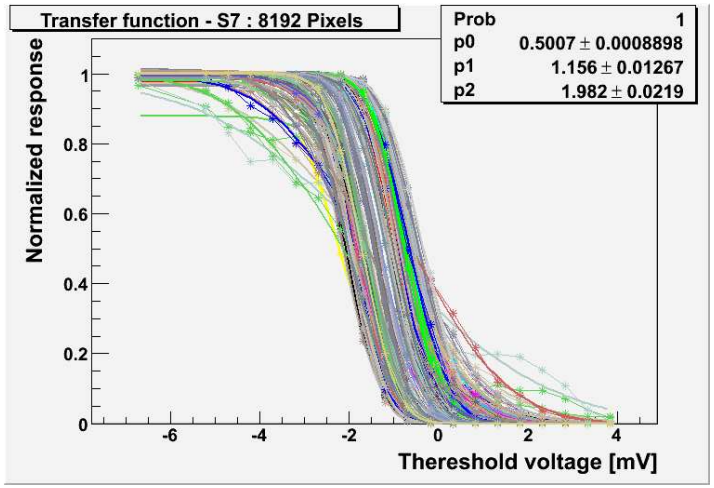
■ **Noise performances for F_{clock} = 100 MHz, T ∼ 15 / 20°C**

- ⁂ *Temporal noise ≃ 0.35 mV* ✓
- ⁂ *Fixed Pattern Noise ≃ 0.25 mV* ✓

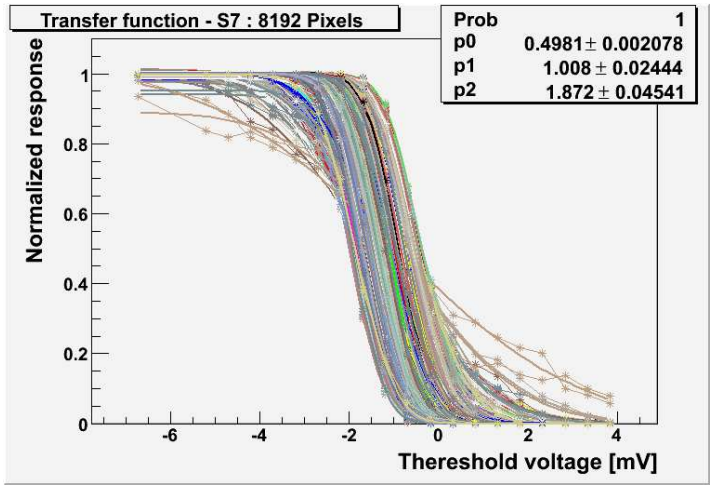
MIMOSA-22 Lab Tests : Digital Output Results (2/2)

■ **Threshold scan of pixel noise from S6 & S7** *(self-biased feedback with high gain)* **:**

※ *rad. tol. diode (S6)*



※ *standard diode (S7)*

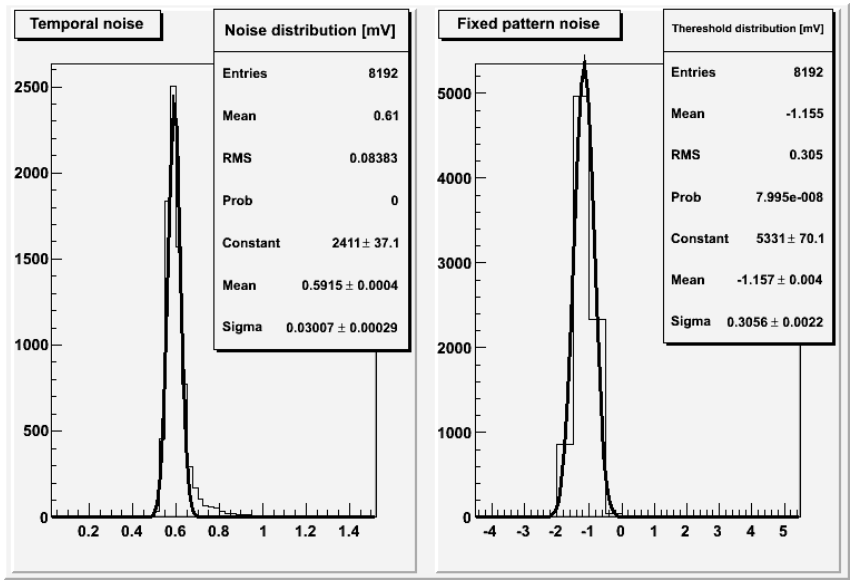


■ **Noise derived from scan of S6 (CVC $\simeq$ 50 $\mu V/e^-$) :**

※ *Running conditions : 100 MHz, T $\sim$ 25°C*

※ *Pixel noise $\simeq$ 0.6 mV* ✓

※ *Fixed Pattern Noise $\simeq$ 0.3 mV ($\equiv$ MIMOSA-16)* ✓



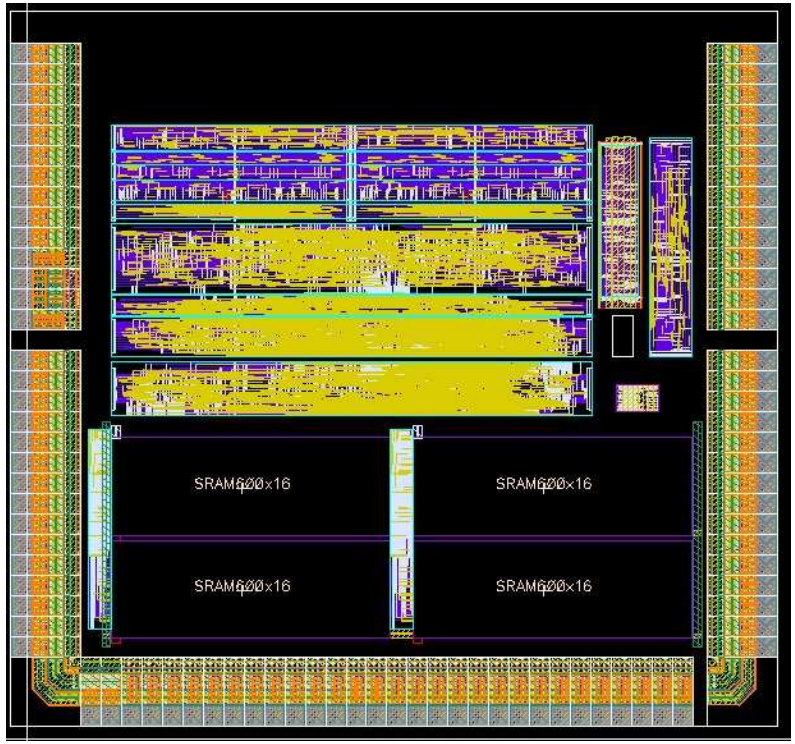
⇒ **Requirements satisfied**

■ **Next steps:**

※ *complete lab tests* ※ *check radiation tol.* ※ *check m.i.p. detection perfo. (SPS in August)*

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- *2 step, raw by raw, logic :*
  - ◇ *step-1 (inside blocks of 64 columns) :*
    identify up to 6 series of $\leq$ 4 neighbour pixels per raw
    delivering signal $>$ discriminator threshold
  - ◇ *step-2 : read-out outcome of step-1 in all blocks*
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- *4 output memories (512x16 bits) taken from AMS I.P. lib.*
- *surface $\sim$ 3.9 $\times$ 3.6 mm^2*



Test results summary :

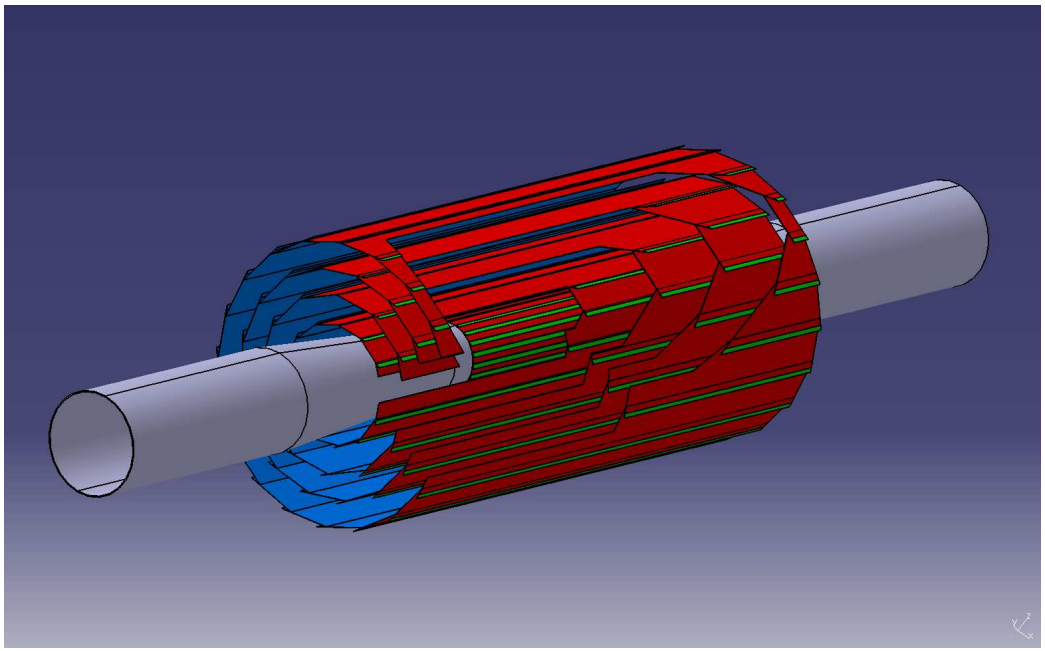
- *back from foundry end of Sept. '07 $\longmapsto$ (lab) tests completed*
- *design performances reproduced up to 1.15 $\times$ design read-out frequency (T_{room}) :*
  - ▷ *noise values as predicted, no pattern encoding error*

Still to do : *evaluate radiation tolerance of ouput memories*

Example of Basic Vertex Detector Design features

- *ILD geometry: $\geq$ 5 cylind. layers (R = 15–60 mm), $\|cos\theta\| \leq$ 0.90 – 0.97*
- *L0 and L1 : optimised against occupancy*
- *L2, L3 and L4 : optimised against power dissipation*
- *Pixel pitch varied from $\sim$ 20 μm (L0–L1) to $\gtrsim$ 30 μm (L2–L4) $\rightarrowtail$ minimise P_{diss}*

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	*15*	20	25	20	25	$<$100	$<$*5*
L1	$\leq$ *25*	25	50	$\leq$26	$\leq$ 65	$<$130	$<$*7*
L2	*37*	33	$\sim$100	24	50	$<$90	$<$*5*
L3	*48*	33	$\sim$100	32	80	$<$120	$<$*6*
L4	*60*	33	$\sim$100	40	150	$<$125	$<$*8*
Total				142	**330**	$<$600	**3–30**



- *Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; $\lesssim$ 40 μm thin sensors)*
- *Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)*
- *Fake hit rate $\lesssim 10^{-5} \rightarrowtail$ whole detector $\cong$ close to 1 GB/s (mainly from $e^{\pm}_{BS}$)*

SUMMARY – OUTLOOK

- **1st generation of CMOS sensors with digital (binary) output almost completed :**
  - *performances suited to ILC-VD outer layers*
  - *equip EUDET beam telescope in 2009 (binary with $\emptyset$)*
  - *equip 3 sectors of STAR-HFT in 2009 (binary without $\emptyset$) $\longmapsto$ D^0 physics in 2010*

- **2nd generation (faster, integrated ADCs) :**
  - *aim for performances suited for the ILC-VD inner layers*
  - *1st (small) pixel matrix with integrated ADCs to be fabricated in 2008*

    $\Rrightarrow$ *1st real scale prototype in 2010 ?*
  - *in parallel : explore alternatives to AMS-0.35 Opto : 0.18 Opto ?, customised substrate, 3DIT*

- **System integration :**
  - *50 μm thinning $\sim$ under control*
  - *edgeless dicing under study*
  - *1st prototype ladder (extrapolated from STAR-HFT) in 2010/11 ?*