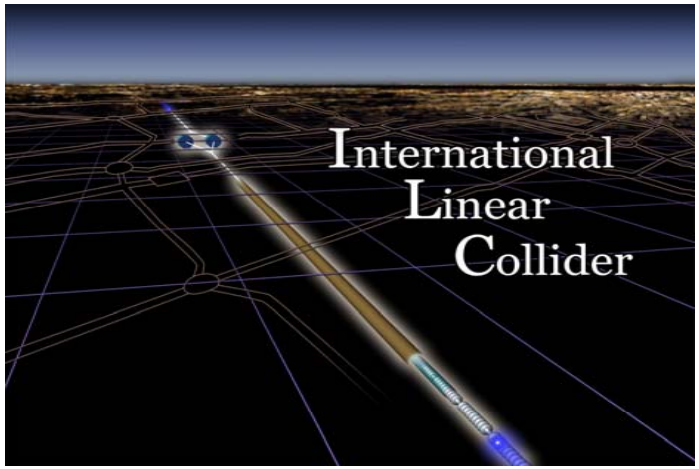
ILC Vertex Workshop 21-24 April 2008 Villa Vigoni

On pixel sparsification architecture in 130nm STM technology

Eleuterio Spiriti (INFN RomaTre)

1. **Our (RomeTre group) experience on MAPS**
   - **Mimoroma1 chip: brief description and some results**
2. **The Mimoroma2 chip**
   - **Main goals and constrains**
   - **Pixel noise simulation**
   - **Readout architecture**
   - **Pixel architecture**
   - **Simulation of sparsified pixel**
   - **Autozero simulation**
3. **Conclusions**

Monolithic pixels in vertex detector for future accelerator

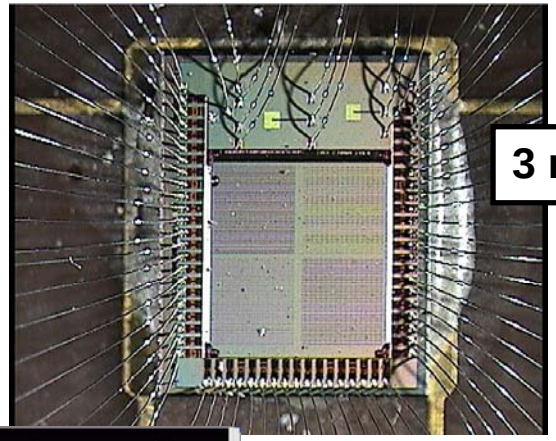


	Super-B	ILC
Spatial resolution	10 μm	2.5 μm
Multiple scattering	$0.05\% * X_0$	$0.1\% * X_0$
Duty cycle	100 %	0.5 %
Occupancy	~1%	~1%

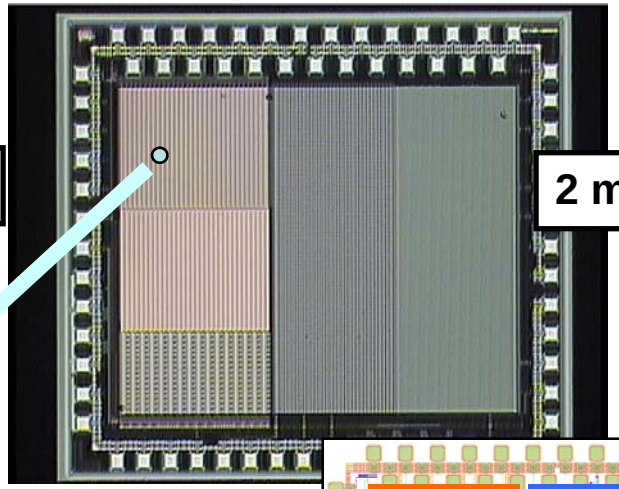
Our (short) experience on MAPS at RomeTre INFN group

Chip mimoroma1
(TSMC 250nm technology)

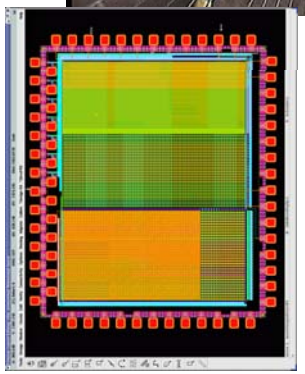
Chip mimoroma2
(STMicroelectronics 130nm technology)

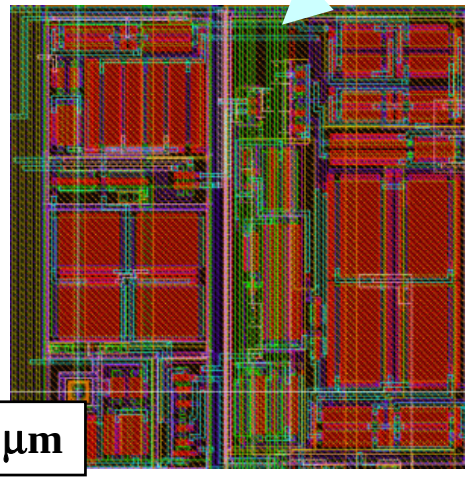


3 mm x 4 mm



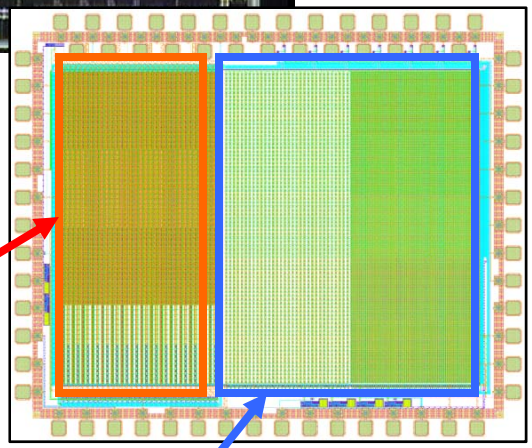
2 mm x 3 mm





25 μm x 25 μm

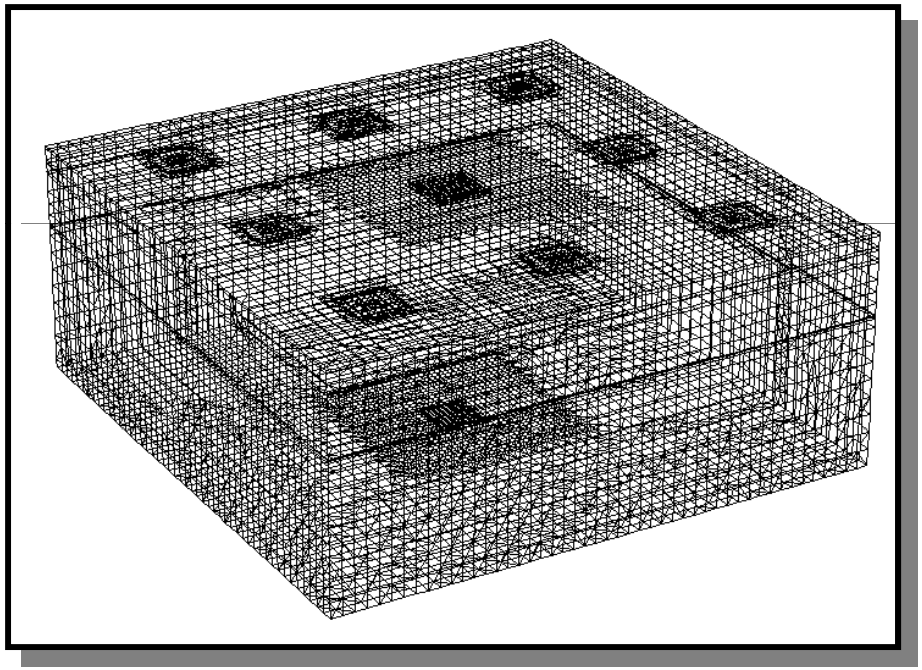
Sparsified side



Non sparsified side

Monolithic Pixel physical simulation

MIMOSA ISE/TCAD simulation

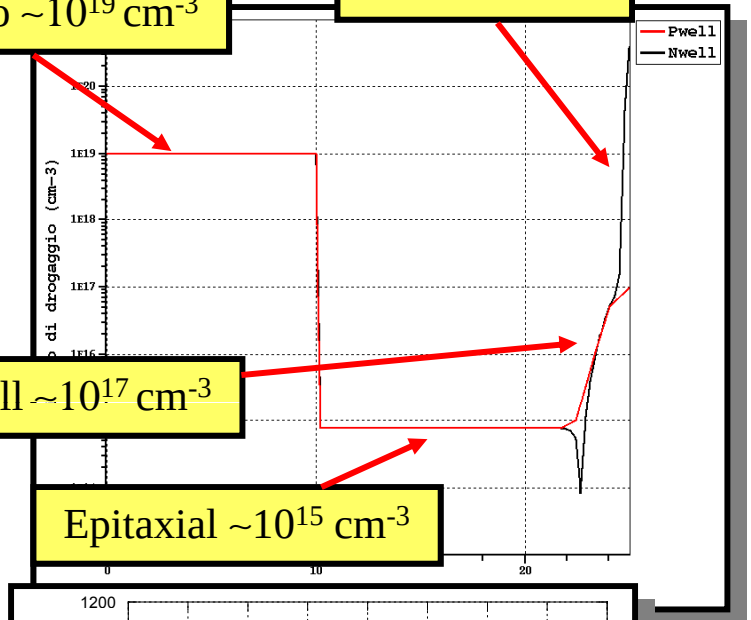


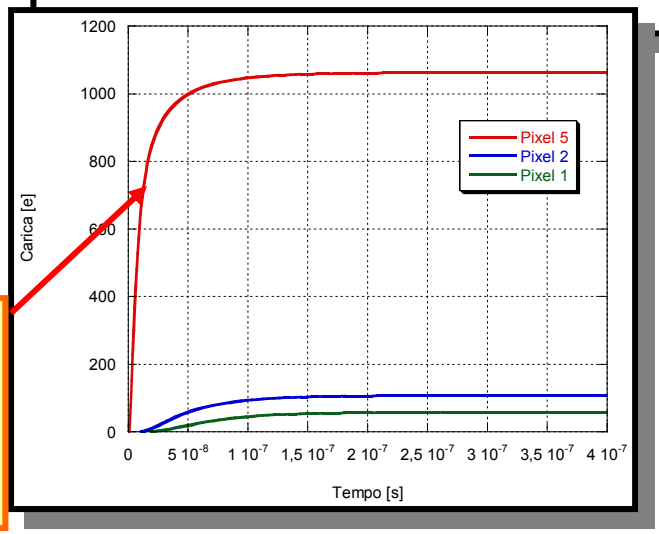
Substrato ~10^{19} cm^{-3}

n+ ~10^{20} cm^{-3}

pwell ~10^{17} cm^{-3}

Epitaxial ~10^{15} cm^{-3}

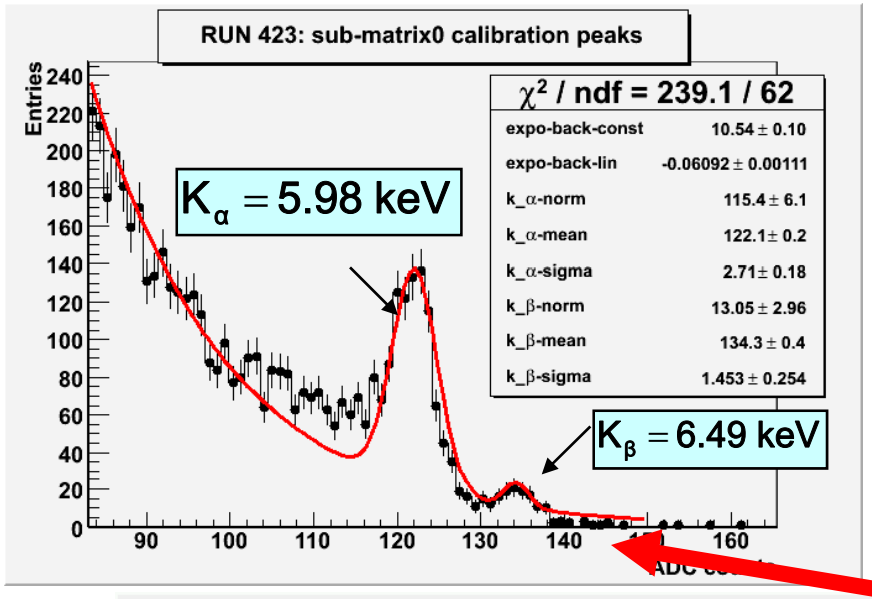




Pitch = 20 µm
Nwell diode 3x3 µm
~ 90000 vertex

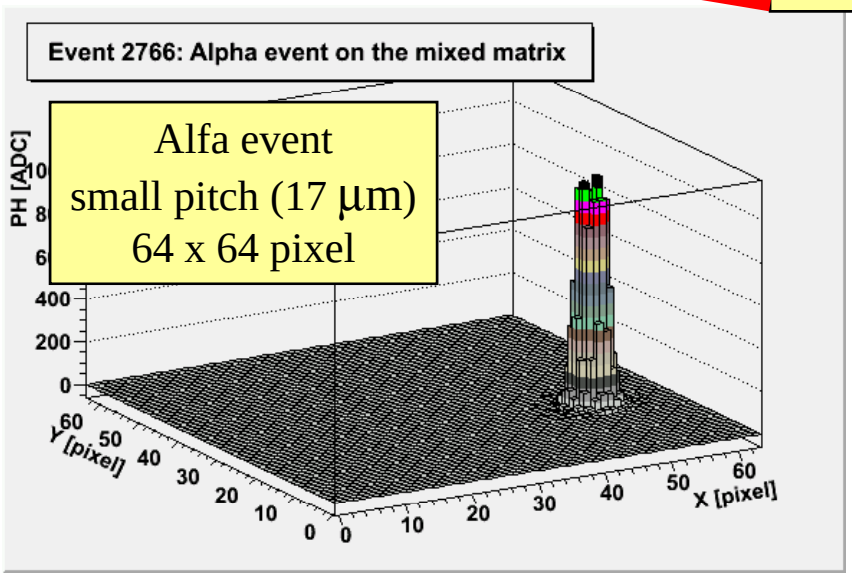
Collection time
~ 100 ns

Mimoroma1 chip measurement results

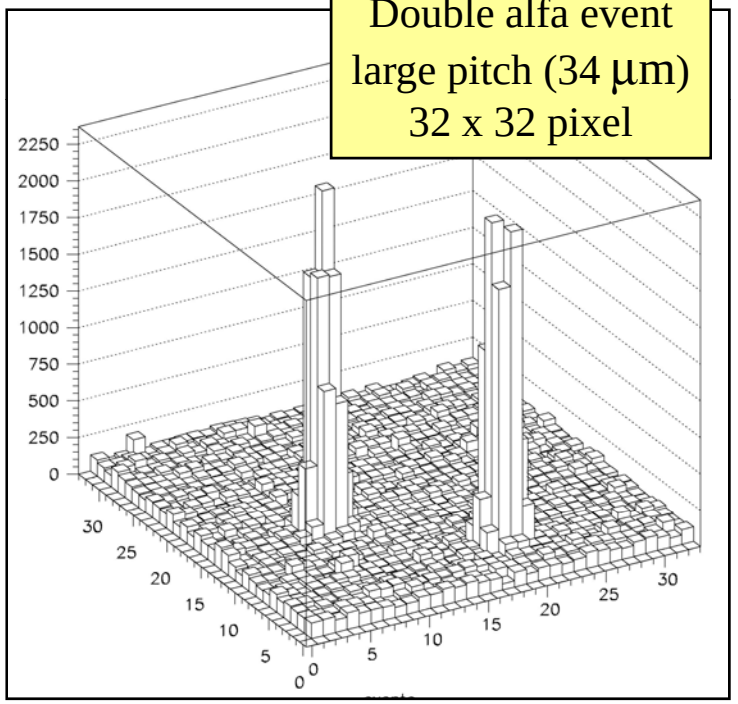


mimoroma1 chip (first MAPS designed at INFN RomaTre)

Fe55 X X ray source



Alfa event
small pitch (17 μm)
64 x 64 pixel



Double alfa event
large pitch (34 μm)
32 x 32 pixel

Mimoroma2 chip: main goals and constrains

- Characterization of the signal (epitaxial thickness and quality) level provided by the STM 0.13 μm technology
- Implementation of an on-pixel sparsification architecture
  - digital and analog output

1. **Only NMOS transistors: no competing n-wells**
2. **Small available area (pitch 20-25 μm)**
3. **Common threshold for all pixels in a chip**
4. **Threshold voltage and curren mismatch in submicron CMOS**
5. **Noise:**
   - ❑ **Temporal noise**
   - ❑ **White and 1/f noise**
   - ❑ **Charge injection**
   - ❑ **Digital to analog cross-talk**

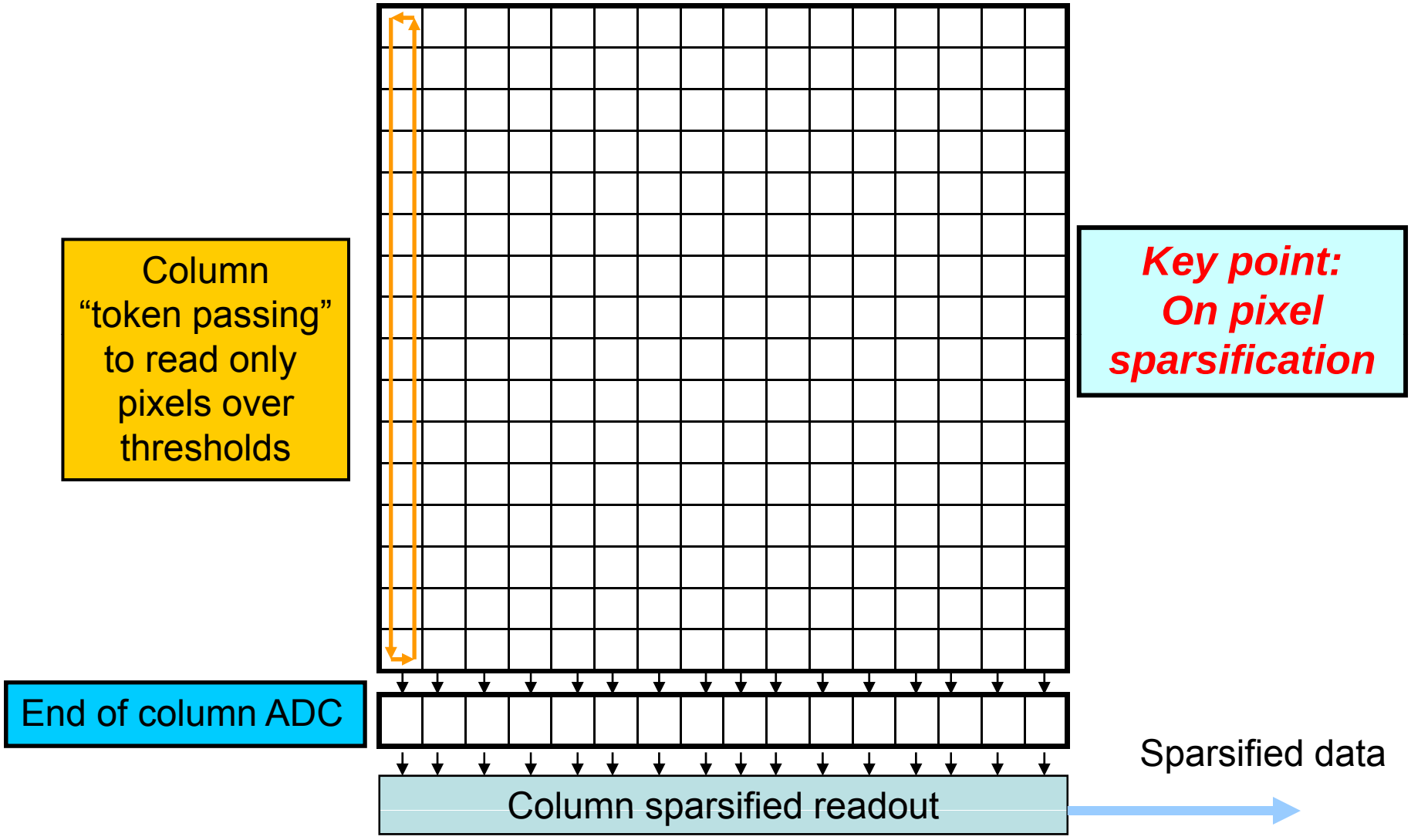
Technology characterization from the signal collection point of view
Different parameters for the non sparsified part of the chip

Ten different matrix implemented

- ✓ **Five 32x16 pixels arrays with 20x20 μm size**
- ✓ **Five 64x32 pixels arrays with 10x10 μm size**

Parameter	Value 1	Value 2
Pixel structure	3T	SB
Pitch	20 μm	10 μm
Diode dimension	1 μm x 1 μm	1.5 μm x 1.5 μm
SF transistor size	Small gain	Large gain
Power supply	2.5 V	1.2 V

Proposed MAPS readout architecture



Paper submitted at the "IEEE Custum Integrated Circuit Conference" http://www.ieee-cicc.org/ September 2008, San Jose, California (under review)

On Pixel Signal Processing for MAPS Sparsified Readout Implemented in CMOS Technology

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Abstract-The paper presents on pixel signal processing for data sparsification in MAPS detector for High Energy Physics application. It includes correlated double sampling, signal discrimination and analog information storing on each single pixel. A chip with the described architecture was submitted for fabrication in ST Microelectronics 130 nm CMOS technology.

I. Introduction

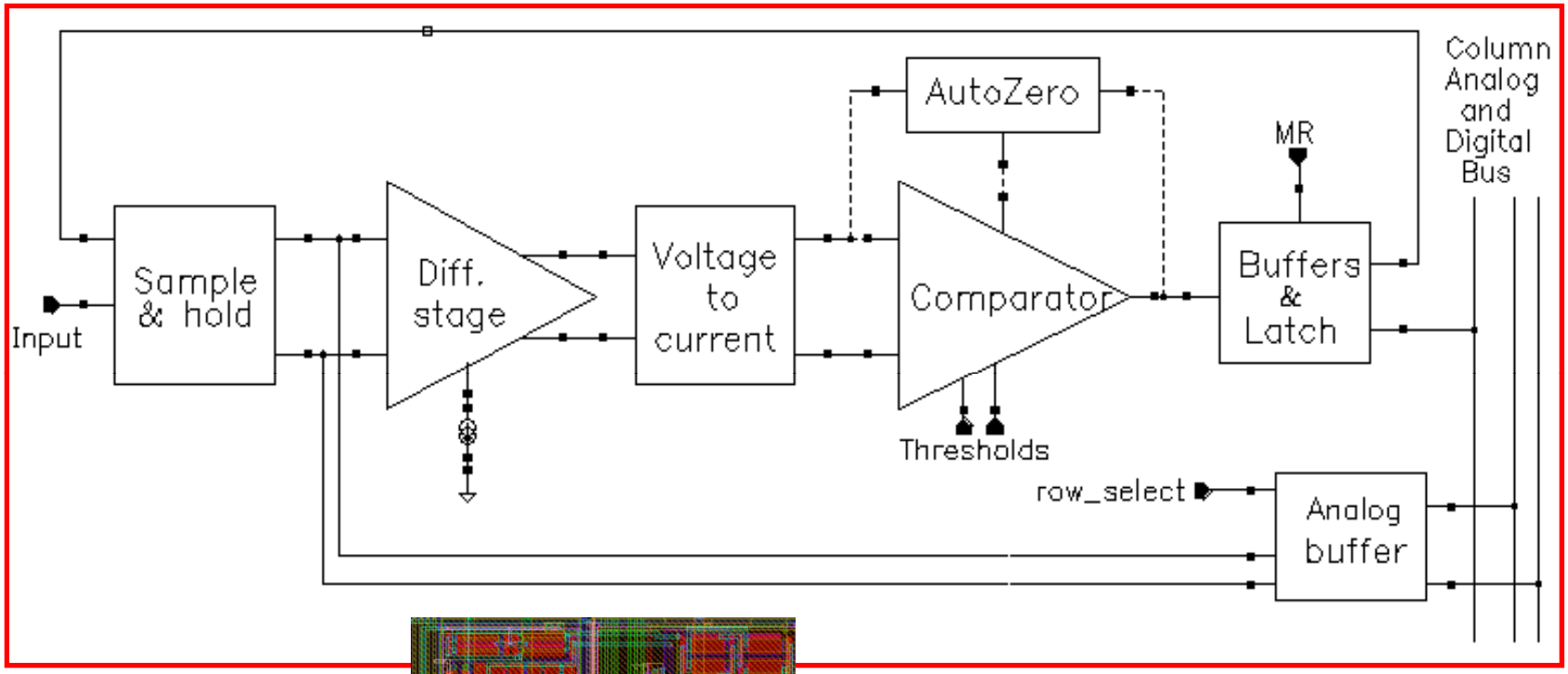
Monolithic Active Pixel Sensors (MAPS), originally used for visible light detection [1], have been proposed for particle tracking detection in the High Energy Physics field [2]. An

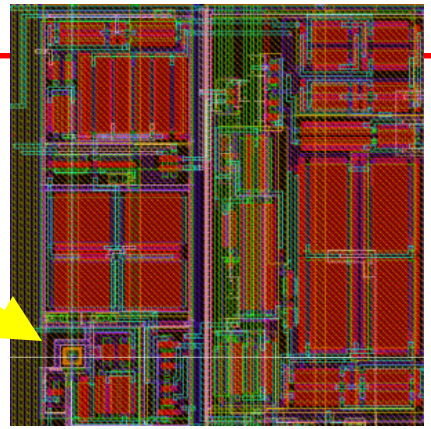
Main constrains we had to deal with are:

1) Only NMOS transistors allowed in the design: any other n-well, to house PMOS transistors, except the one collecting the signal, would drain part of the charge produced in the epi-layer.
2) Highly limited pixel area (25 m x 25 m): small pitch is essential for a good space resolution.
3) Common threshold for entire chip i.e. for each pixel: having in mind the number of pixels and their small area it is impossible to imagine a threshold setting specific to each pixel.

Detailed description of the sparsified pixel circuitry

Pixel architecture

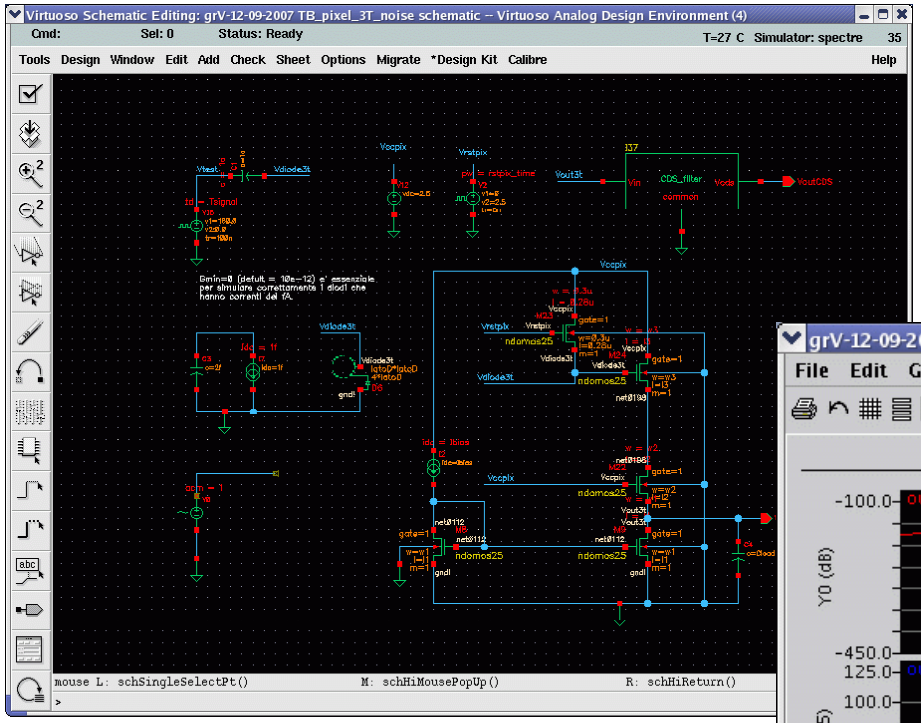




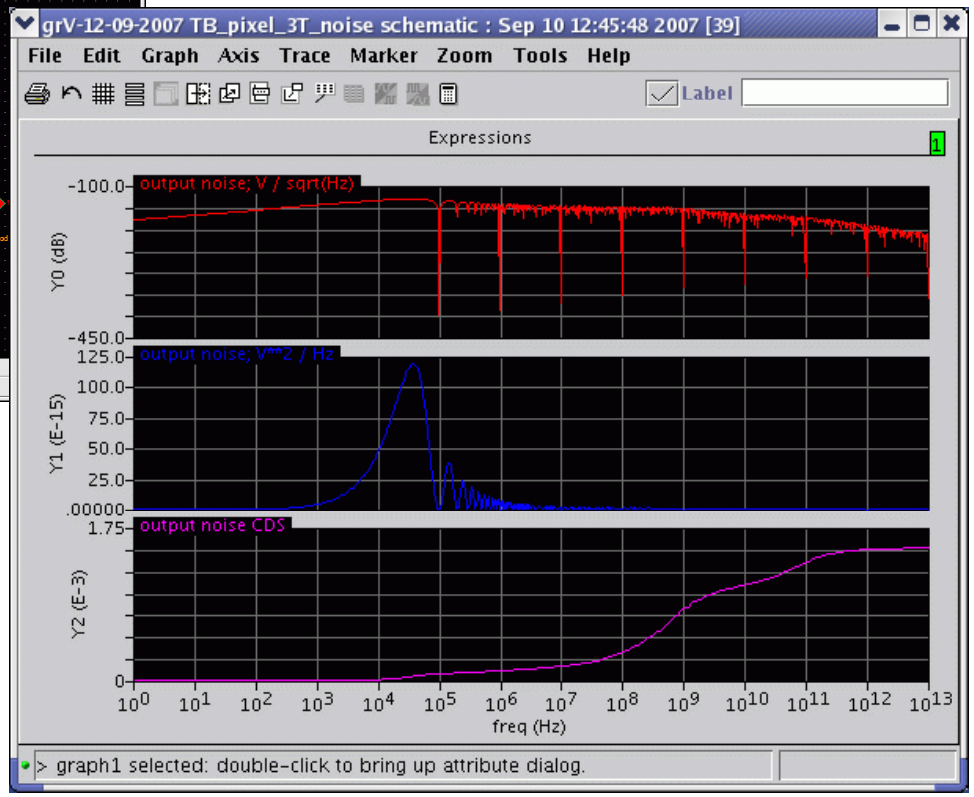
Sensing diode

Size 25 μm x 25 μm
~ 70 transistors

Pixel 3T noise simulation

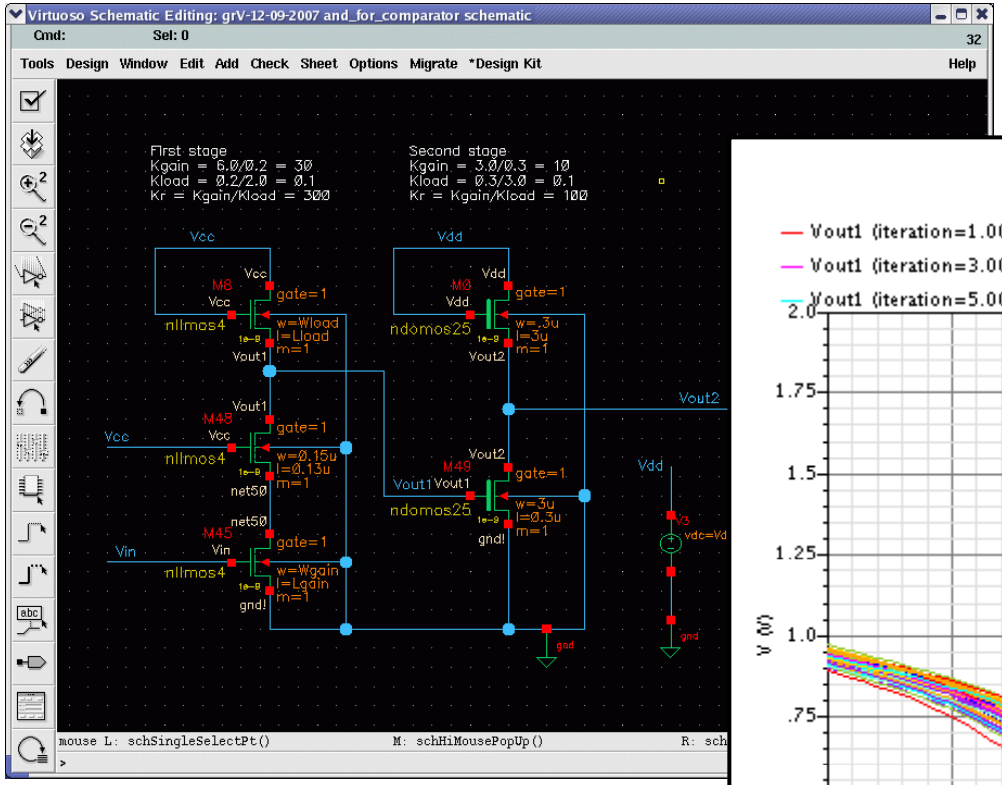


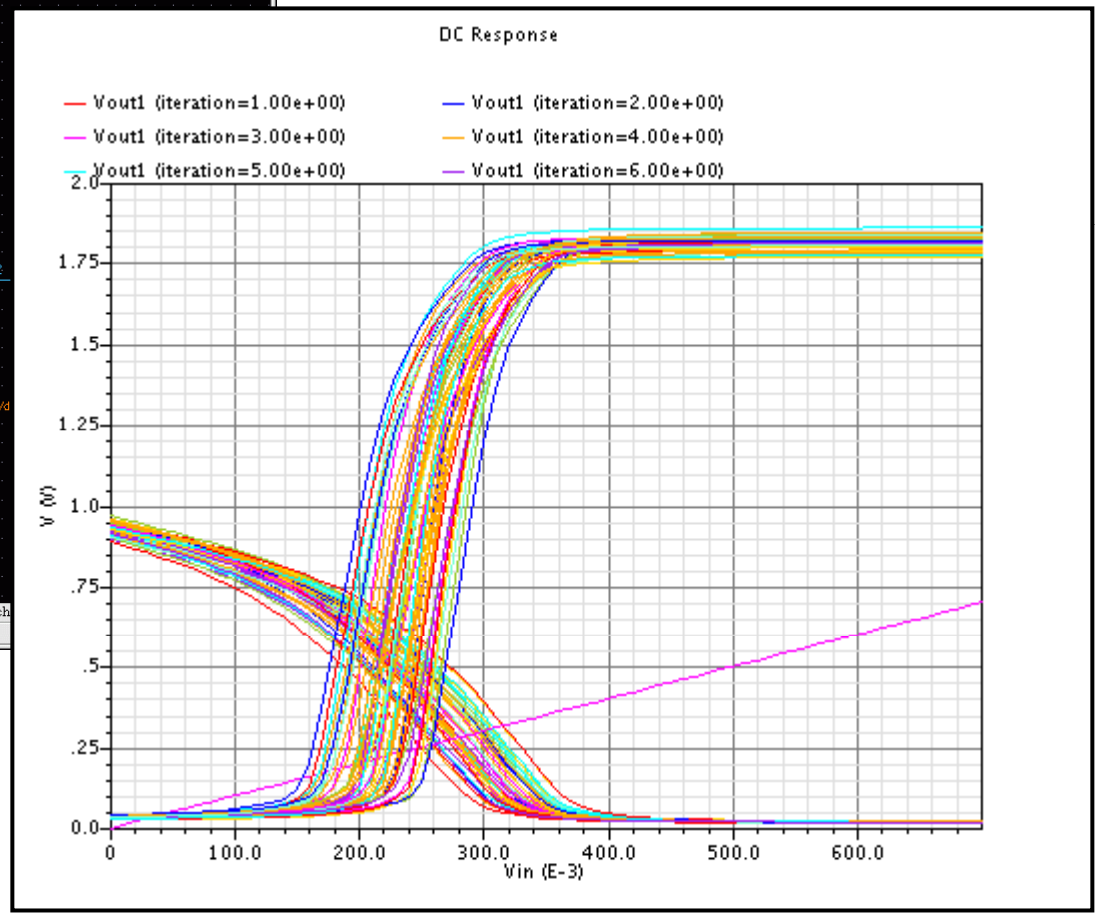
Noise level after CDS
(1Hz-10THz)
~ 1.5 mV - ~ 25 elec.



N-well/p-epi sensing diode model → level-0.
leakage current/white noise?

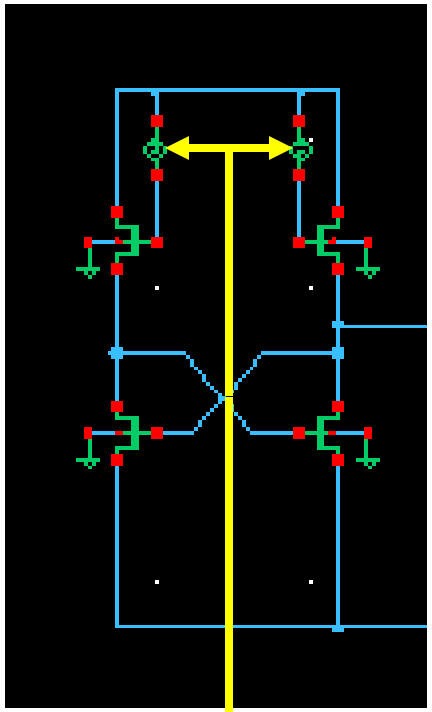
NAND logic Montecarlo simulation. (used inside the Pixel)



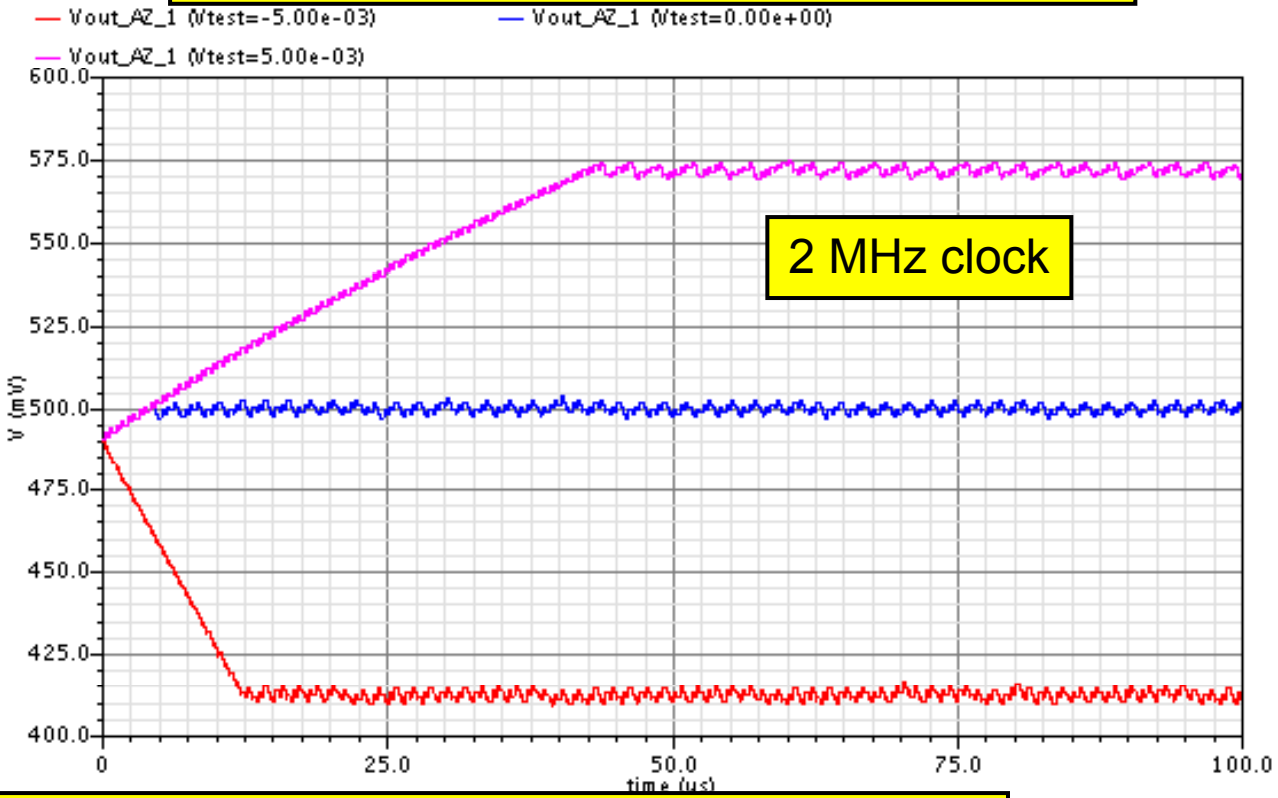


Process and mismatch fluctuations included.

Autozero correction voltage simulation.



Autozero correction voltage versus external bias autozero voltage fixed at 500 mV.



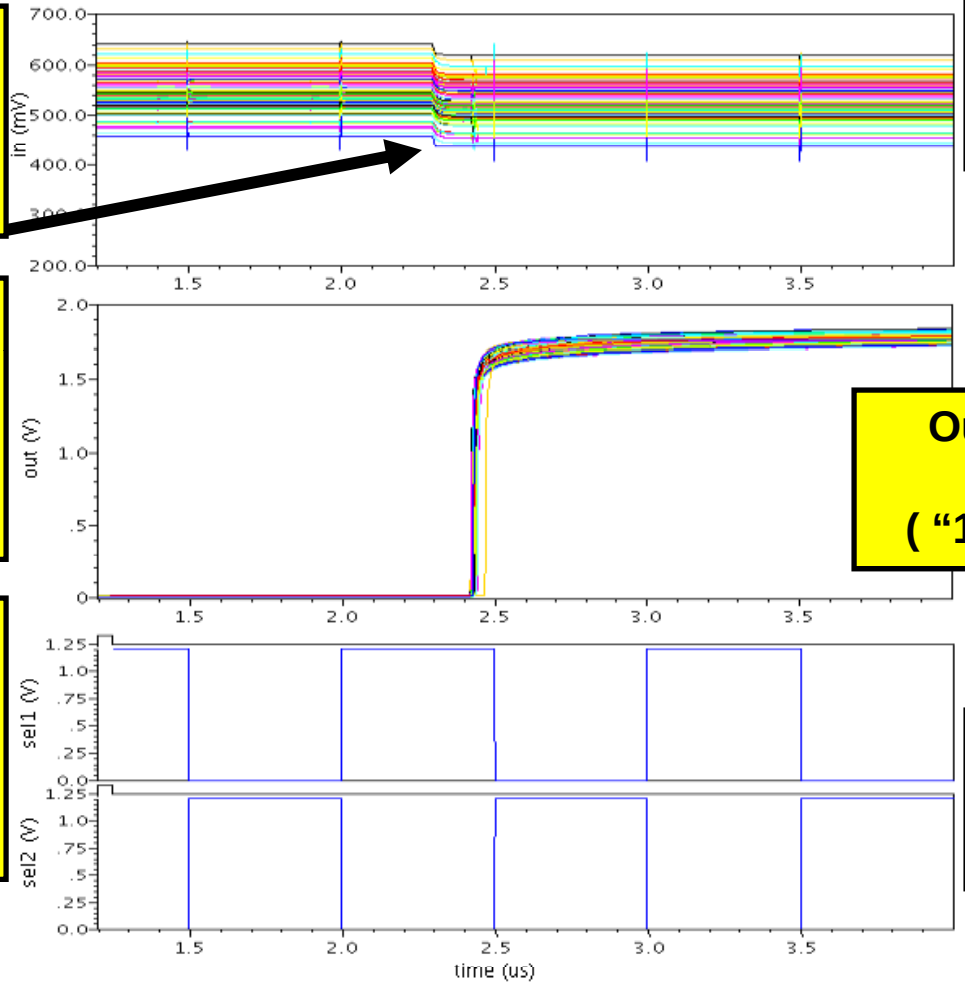
Autozero correction voltage and external bias autozero voltage produce a correction differential current to the discriminator to compensate the two unbalancing voltage generators

Sparsification logic Montecarlo simulation (100 runs)

Input signal injected on sensing diode ~22 mV (~ 350 e)

~ 350 electron is a rough estimation of seed pixel charge in STM 0.13 μm

Treshold at the minimum value needed to have zero false trigger ("100% purity")



Mismatch spread on sensing diode ~182mV (~ 2900 e)

Output signal after discrimination ("100 % efficiency")

Sample and hold timing (integration time)

Conclusions

- Design effort was driven by the highly demanding performances required by the vertex detectors for future colliders
- The proposed architecture for the on-line data sparsification was designed and simulated
- Simulation results of the on-pixel signal processing seems promising, considering that this will be the first run in ST 0.13um technology. We had many unknows and we tried to be prepared for the worst case
  - Large room for improvements expected after feedback from measurements.
- The autozero correction technique could be a key point.
- Chip submitted through CMP Service November 2007, testing will start next week