LCFI Report

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for LCFI collaboration

ILC VD Workshop, Menaggio, 23 April 2008

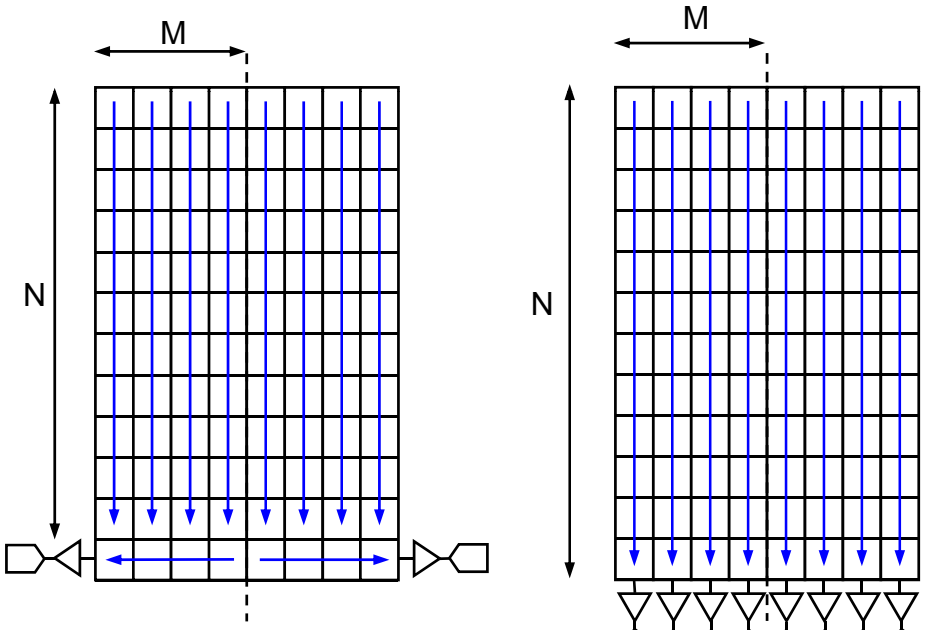
Outline

- CCD-based sensors
  - Column Parallel CCD
  - ISIS
- Driver and Readout chips for CPCCD

- Physics studies
- Mechanics

The Column Parallel CCD

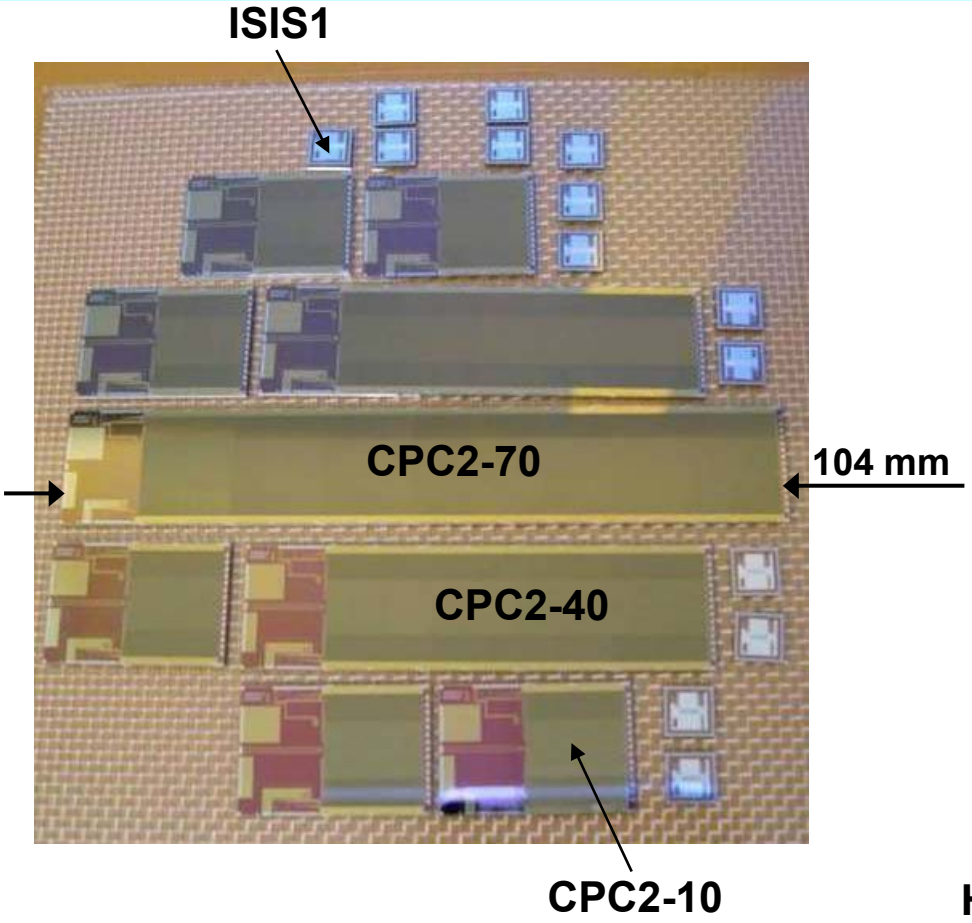
- **Every column has its own amplifier and ADC**
- **Readout time shortened by ~3 orders of magnitude**
- **All of the image area is clocked, complicated by the large gate capacitance**
- **Optimised for low voltage clocks to reduce power dissipation**



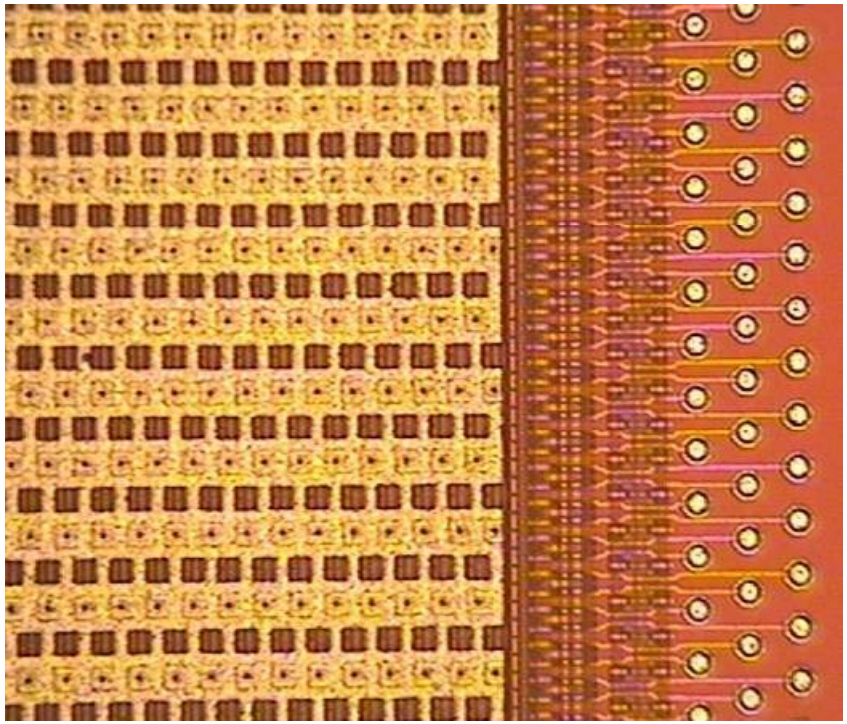
"Classic CCD"
Readout time ≈ $N \times M/f_{out}$

Column Parallel CCD
Readout time = N/f_{out}

Our Second Generation CPCCD : CPC2



Busline-free CPC2



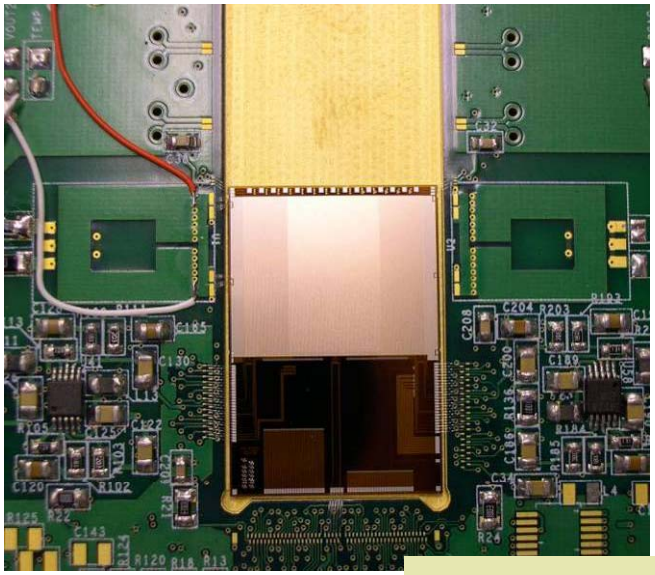
- CPC2 wafer (100 Ω.cm/25 µm epi and 1.5kΩ.cm/50 µm epi)
- Low speed (single level metallisation) and high speed versions

High speed (busline-free) devices with 2-level metal clock distribution:

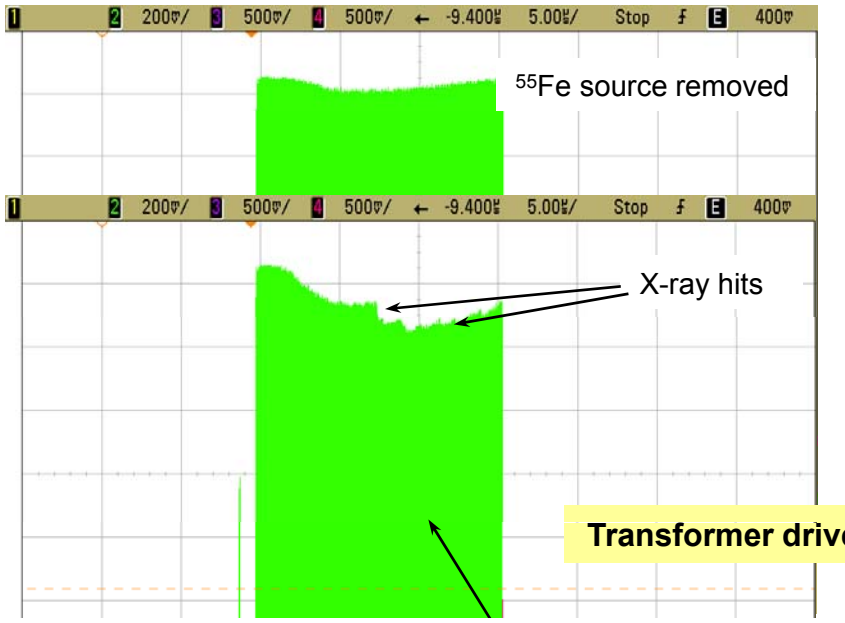
❖ The whole image area serves as a distributed busline

❖ Designed to reach 50 MHz operation (needed to keep the occupancy < 1% in L1)

CPC2 – High Speed in Stand-alone Mode

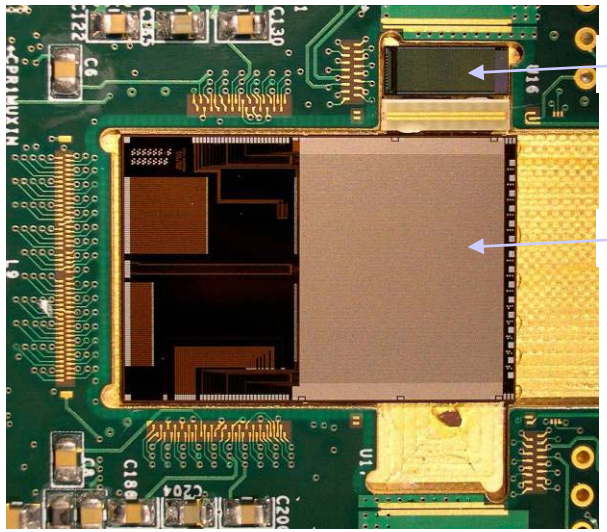


K.Stefanov, RAL
B.Hawes, Oxford



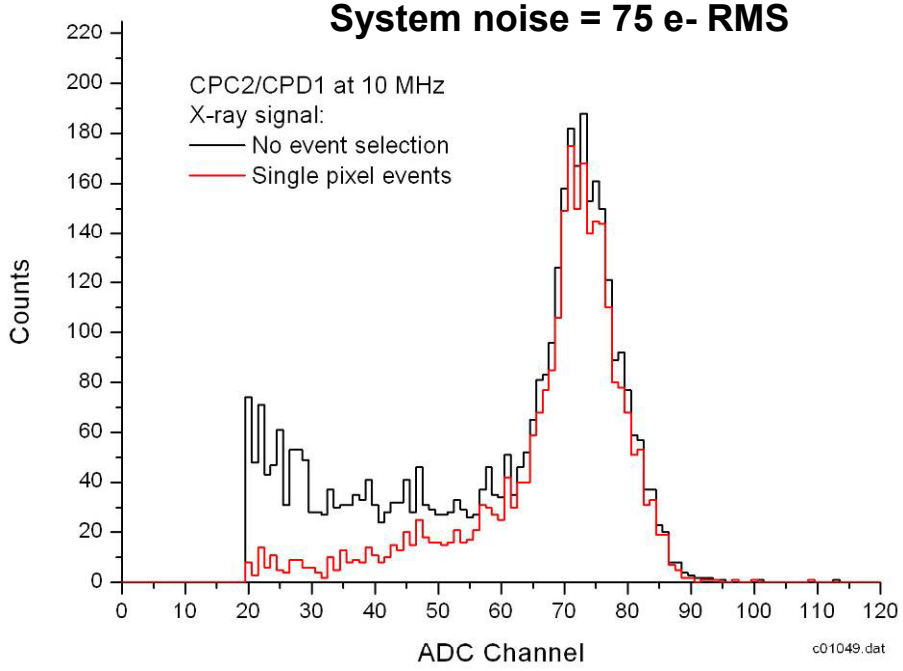
CCD output (2-stage source follower), ≈ 2 V_{pk-pk} clocks

- **First tests with a PCB transformer and a RF amplifier for clocking**
- **Busline-free CPC2-10 working at 45 MHz, important milestone**
- **Numerous parasitics diminish overall performance, high noise from the RF amplifier**
- **CMOS driver chip used as well**

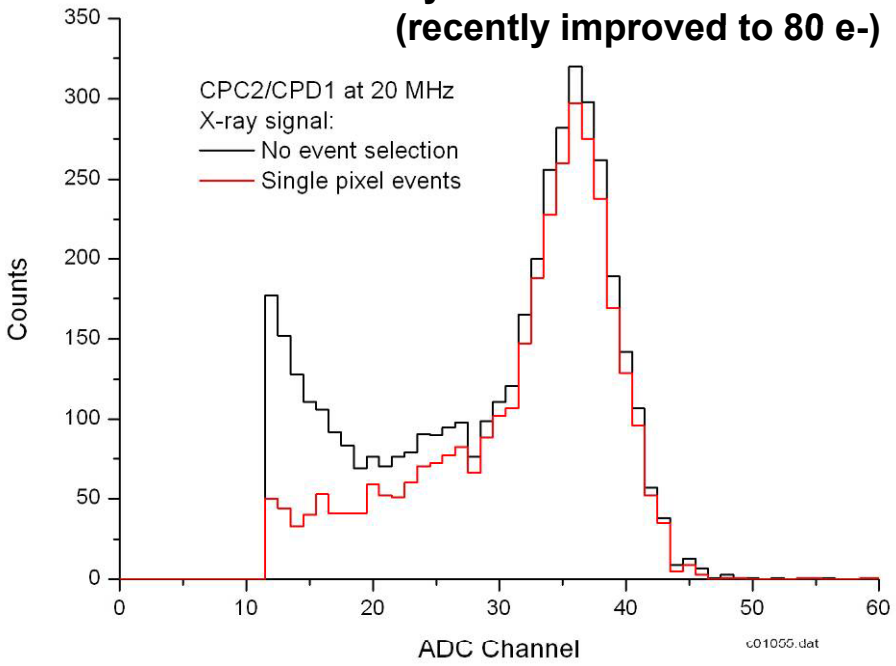


CPC2-10 BLF with CPD1 Clocking

10 MHz
System noise = 75 e- RMS



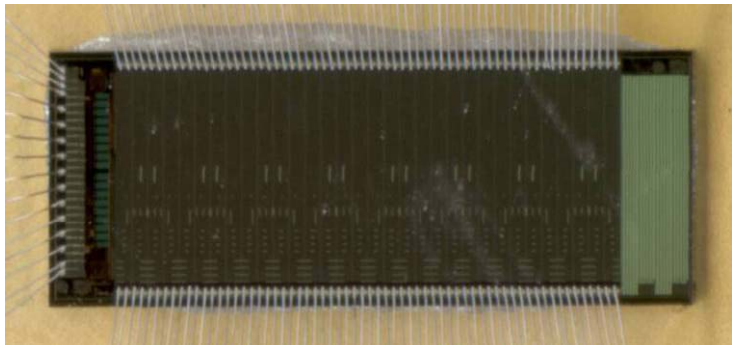
20 MHz
System noise = 110 e- RMS
(recently improved to 80 e-)



- **Stand-alone 2-stage source follower outputs**
- **^{55}Fe signal (1620 electrons, MIP-like)**
- **CPD1 producing clocks in the range 3.3 V to 1.2 V**
- **Noise reduced from 200e- (with transformer drive) to 75 e- (CMOS driver)**
- **CPC2 works with clock amplitude down to 1.35 Vpp**
- **Tests are continuing – pushing up frequency, using 50 mm long sensor**

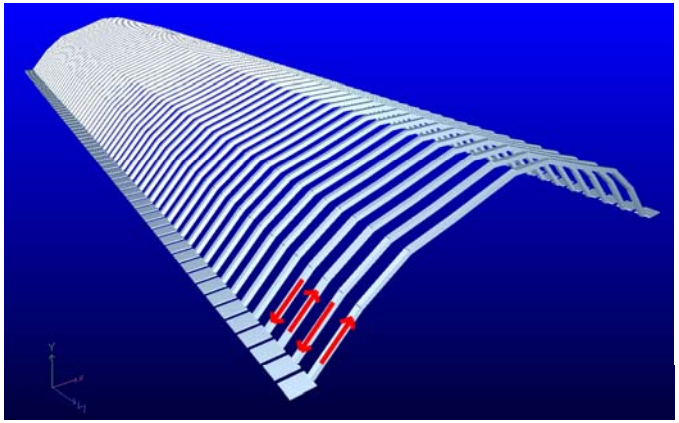
K.Stefanov

Clock Driver for CPC2: CPD1

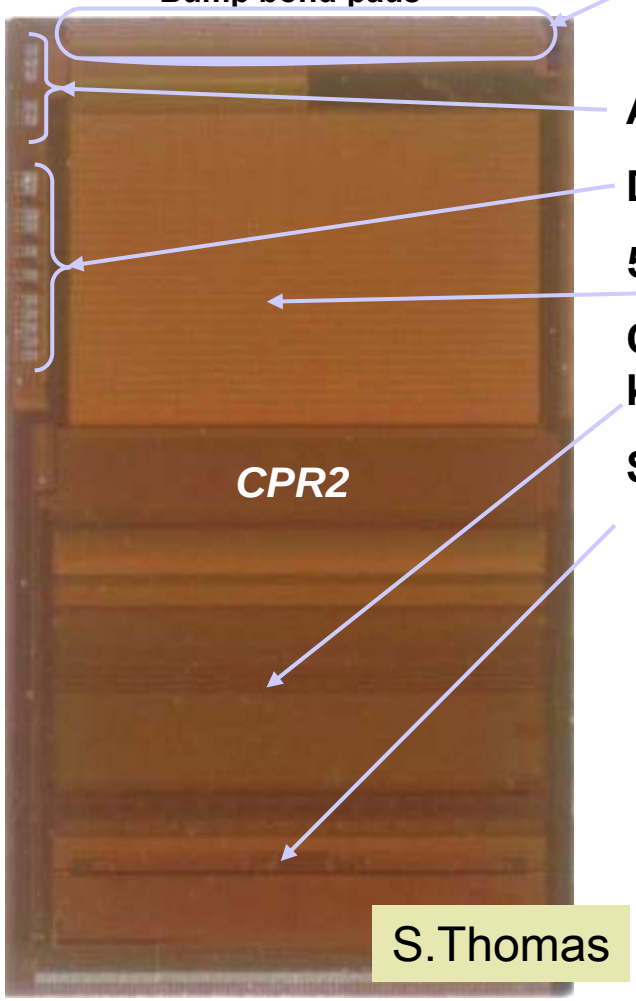


S.Thomas
P.Murray, RAL

- Designed to drive:
  - Outer layer CCDs (127 nF/phase) at 25 MHz
  - L1 CCD (40 nF/phase) at 50 MHz
  - CPC2 requires ~21 Amps/phase @ 2 V_{pp}
- One chip drives 2 phases, up to 3.3 V clock swing
- 0.35 µm CMOS process, chip size 3×8 mm^2
- 8 independent clock sections
- Careful layout on- and off-chip to cancel inductance, bump-bondable
- Internal 2 nF load capacitor to one section
- Works well up to 50 MHz



Readout Chips – CPR1 and CPR2



Voltage and charge amplifiers 125 channels each

Analogue test I/O

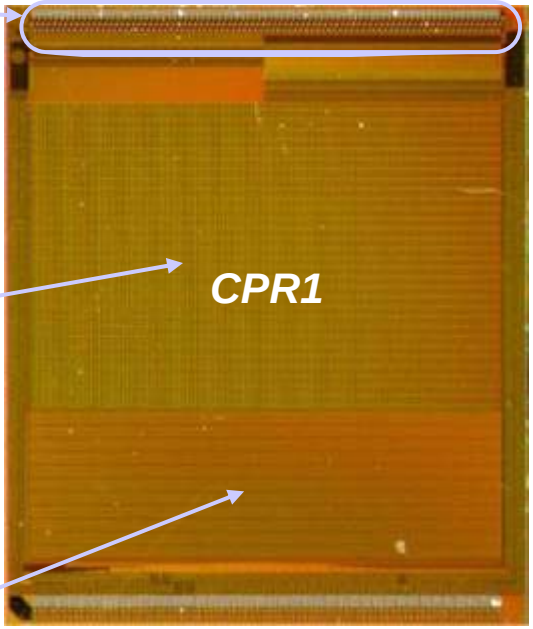
Digital test I/O

5-bit flash ADCs on 20 μm pitch

Cluster finding logic (2×2 kernel)

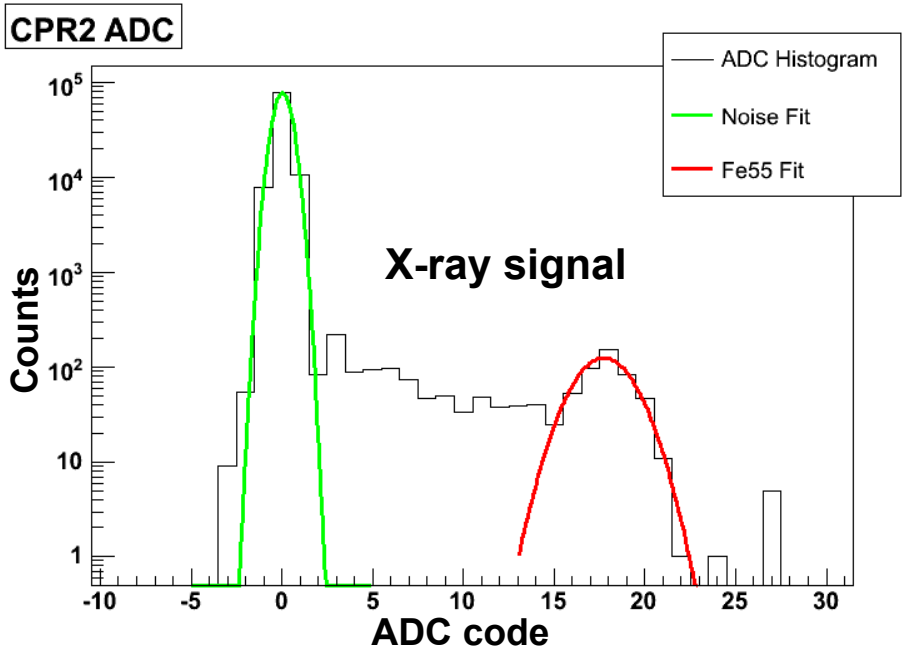
Sparse readout circuitry

FIFO

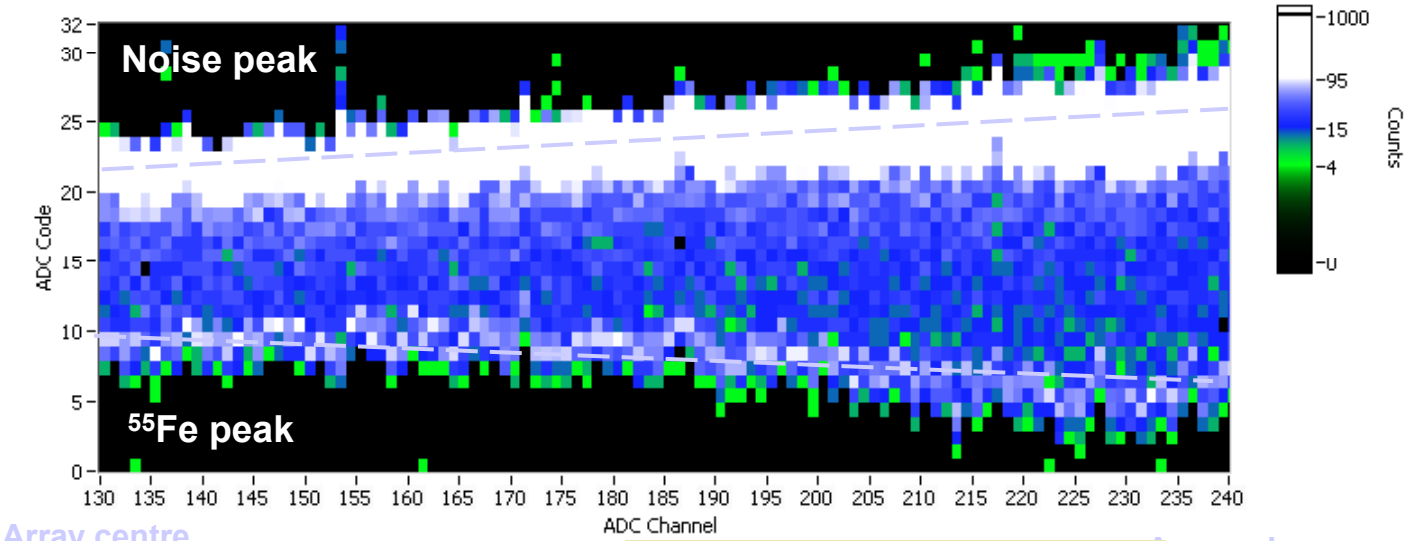


- Both chips made on 0.25 μm CMOS process (IBM)
- Front-end amplifiers matched to the CCD outputs
- CPR1 can be bump-bonded to CPC1 and CPC2, also has 1-in-3 wire bondable pads
- CPR2 can only be bump-bonded to CPC2
- Additional test features in CPR2

CPR2: Analogue Performance (1)



- Signals from all voltage channels observed (here at 2 MHz, 300 mV ADC range)
- Bump bond yield appears to be 100%
- Charge channels did not work – possibly swamped by digital crosstalk from the ADCs
  - ❖ Complex mixed signal chip, difficult to design and simulate
- Gain decreases by 50% away from the chip edges (as in CPR1), under investigation
- Noise around 60 e-

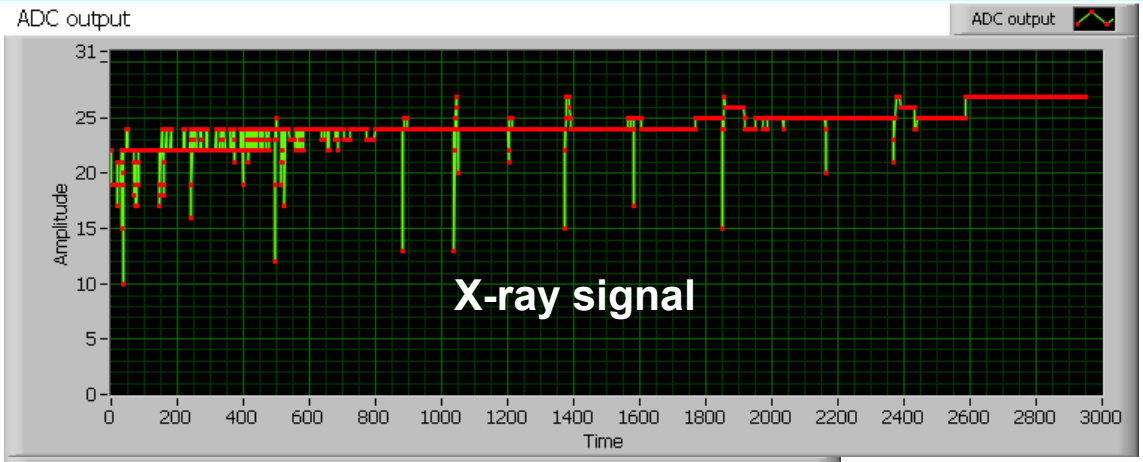


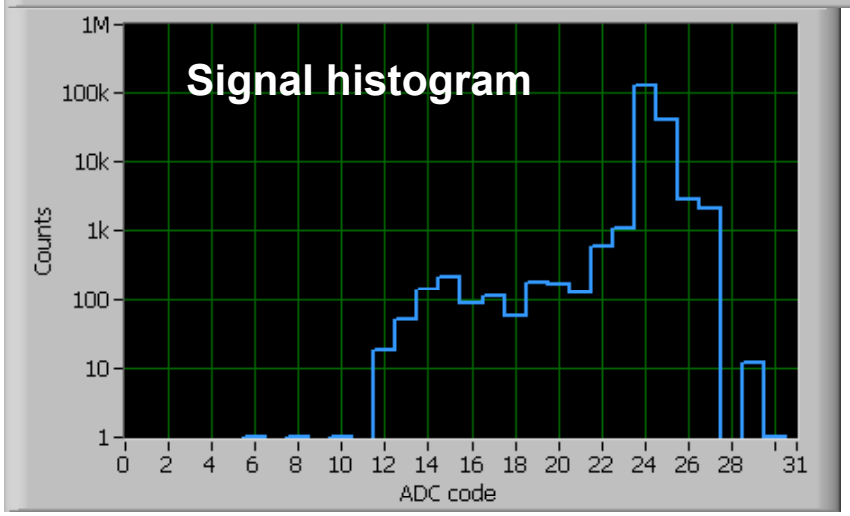
Array centre

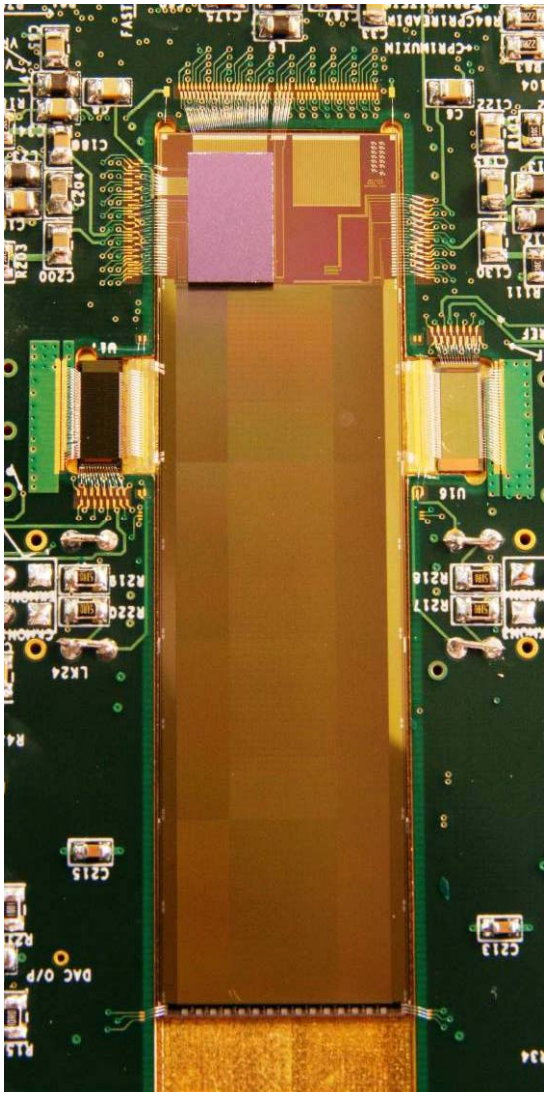
Array edge

T.Wooliscroft, Liverpool

CPR2: Analogue Performance (2)







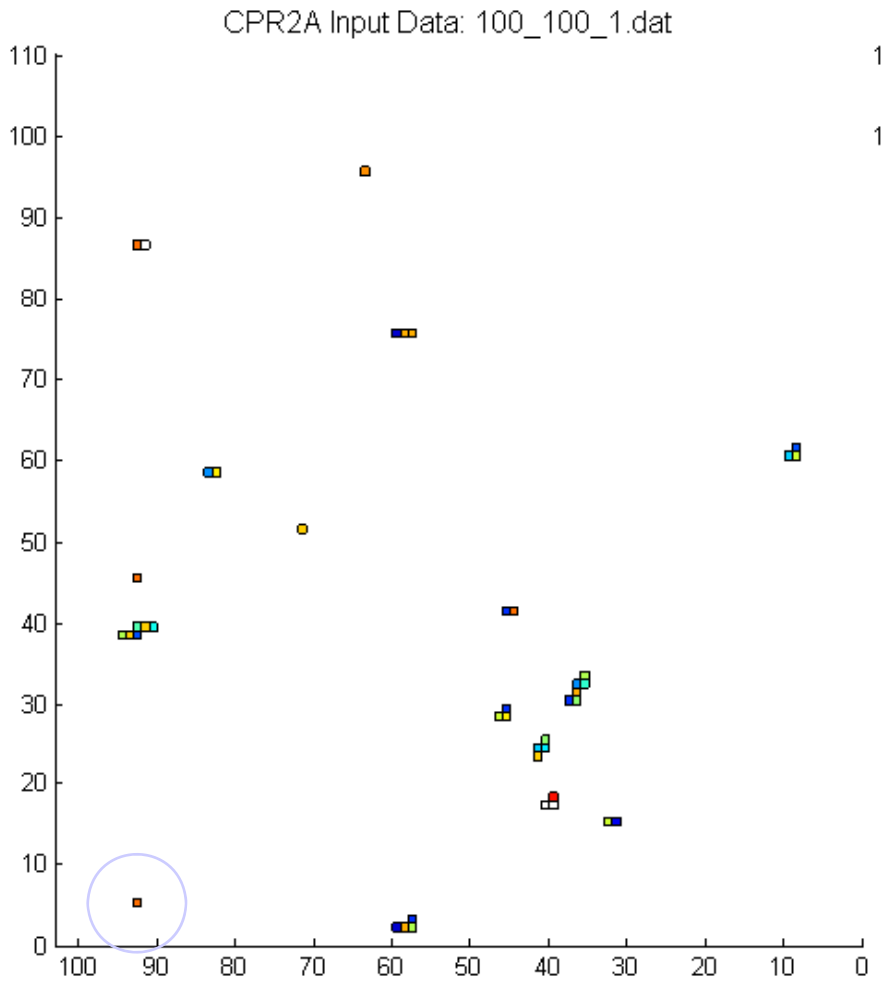
- Bump-bonded CPC2/CPR2 driven by two CPD1 chips
- Works up to 9 MHz

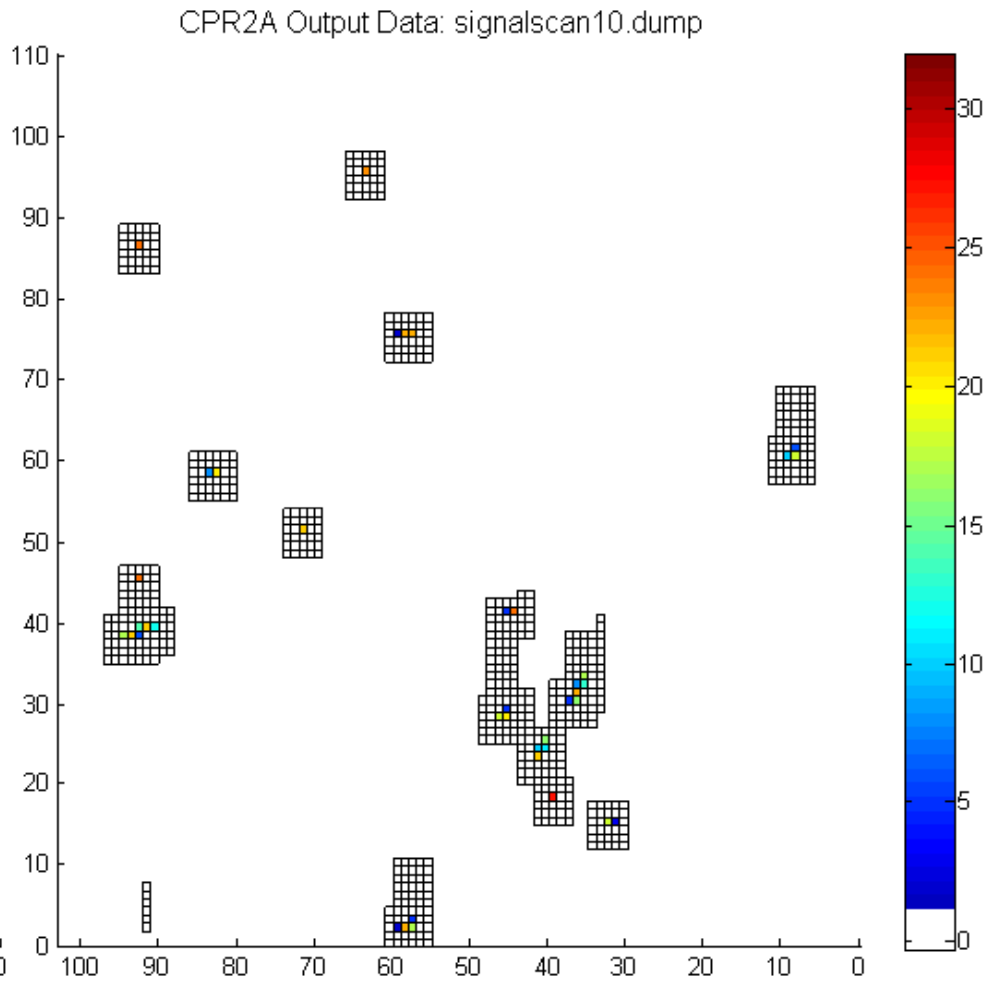
New Features in CPR2A

- A range of improvements being implemented in the next generation chip CPR2A:
  - ❖ Cluster size reduced to 4×6
  - ❖ 3-fold increase in the column memory buffer (can store up to 3 clusters) to reduce dead time and a new state machine
  - ❖ Individual column threshold – corrects for gain variations
  - ❖ Analogue calibration circuit – the chip can be partially tested without bump bonding to a CCD
  - ❖ Improvements to the analogue circuitry: gain matching, reduced differential non-linearity in the ADC, new clock distribution
  - ❖ Digital crosstalk to the charge amplifiers will be minimized
  - ❖ Code-dependent current in the ADC will be reduced

- CPR2A received a week ago, being diced now – tests will start soon

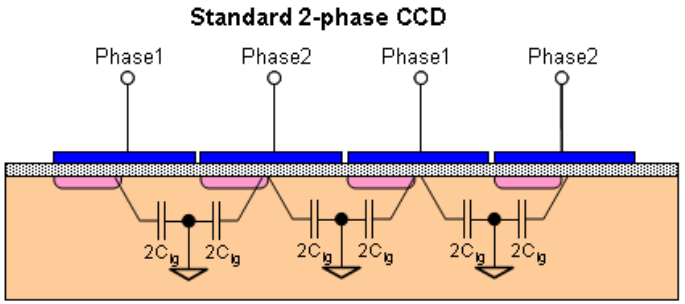
Sparsification with Realistic Data in CPR2A

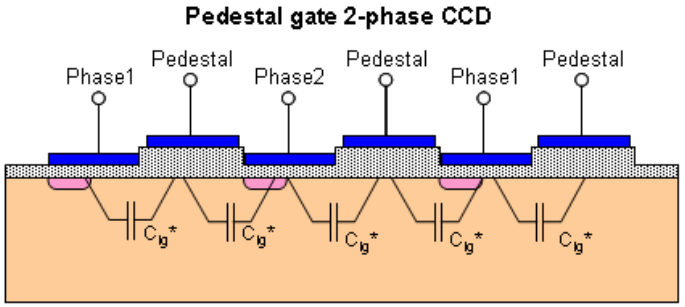




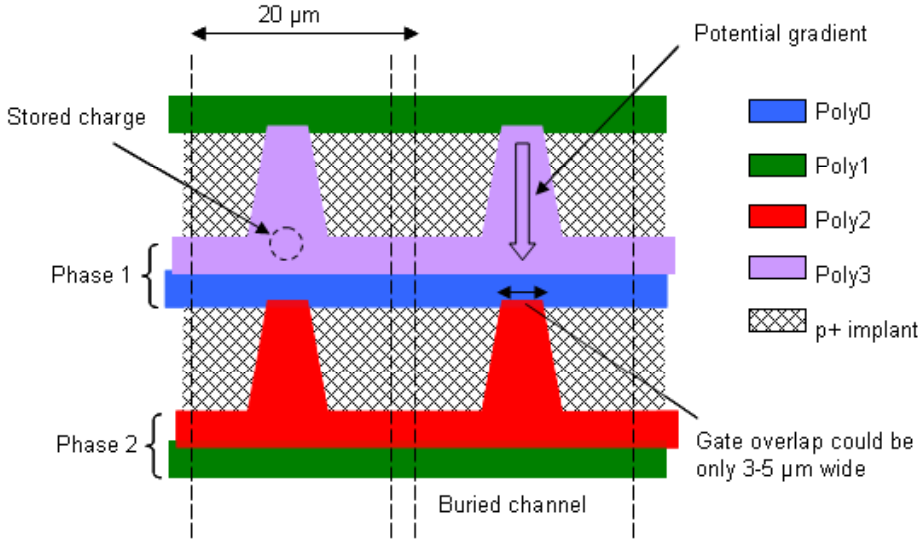
- ❖ **Near-perfect readout over 100 time steps (44 hit pixels, occupancy 0.44%)**
- ❖ **One missing data point in the output (channel 92, time stamp 4)**

CPC-T

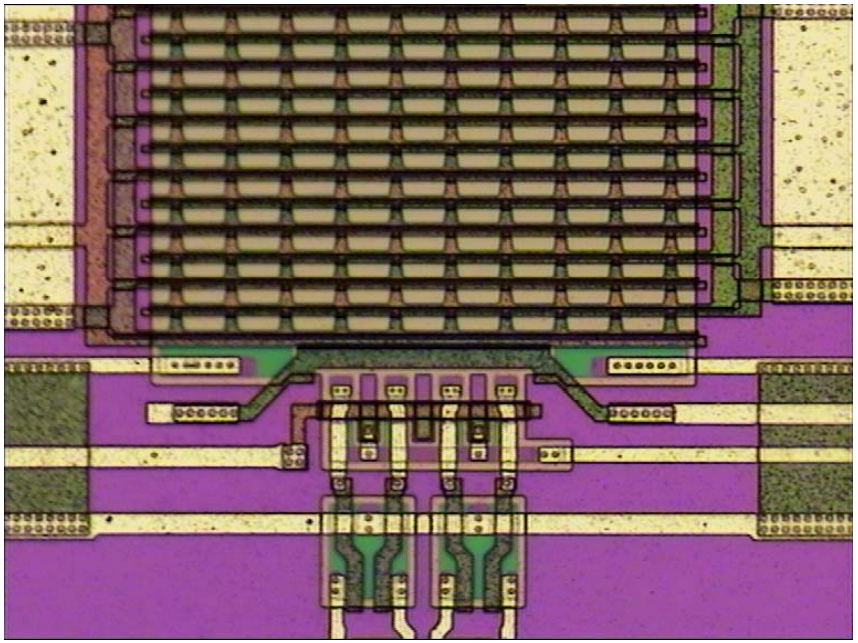


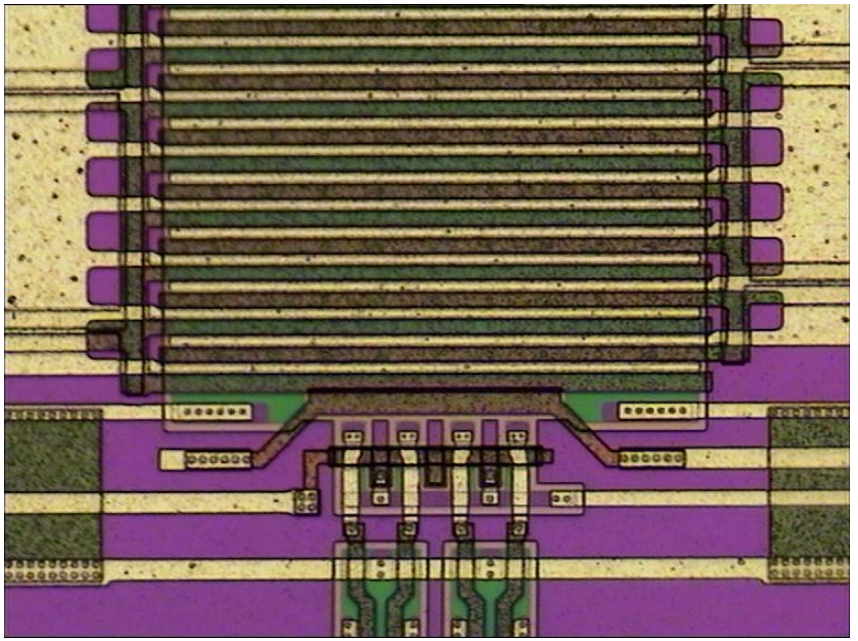


- **Two-fold goal : lower V and lower C**
- **Two designs based on CPC2 to study very low inter-gate barriers and clock amplitudes**
- **Six designs for reduction of the inter-gate capacitance:**
  - **Pedestal CCD (on 20 μm and 24 μm pitch)**
  - **Shaped Channel CCD (variant of the Pedestal CCD), on 20 μm and 24 μm pitch**
  - **Open Phase CCD**
  - **"Inter-channel gap" CCD**
- **Pedestal designs could reduce Cig by a factor of**



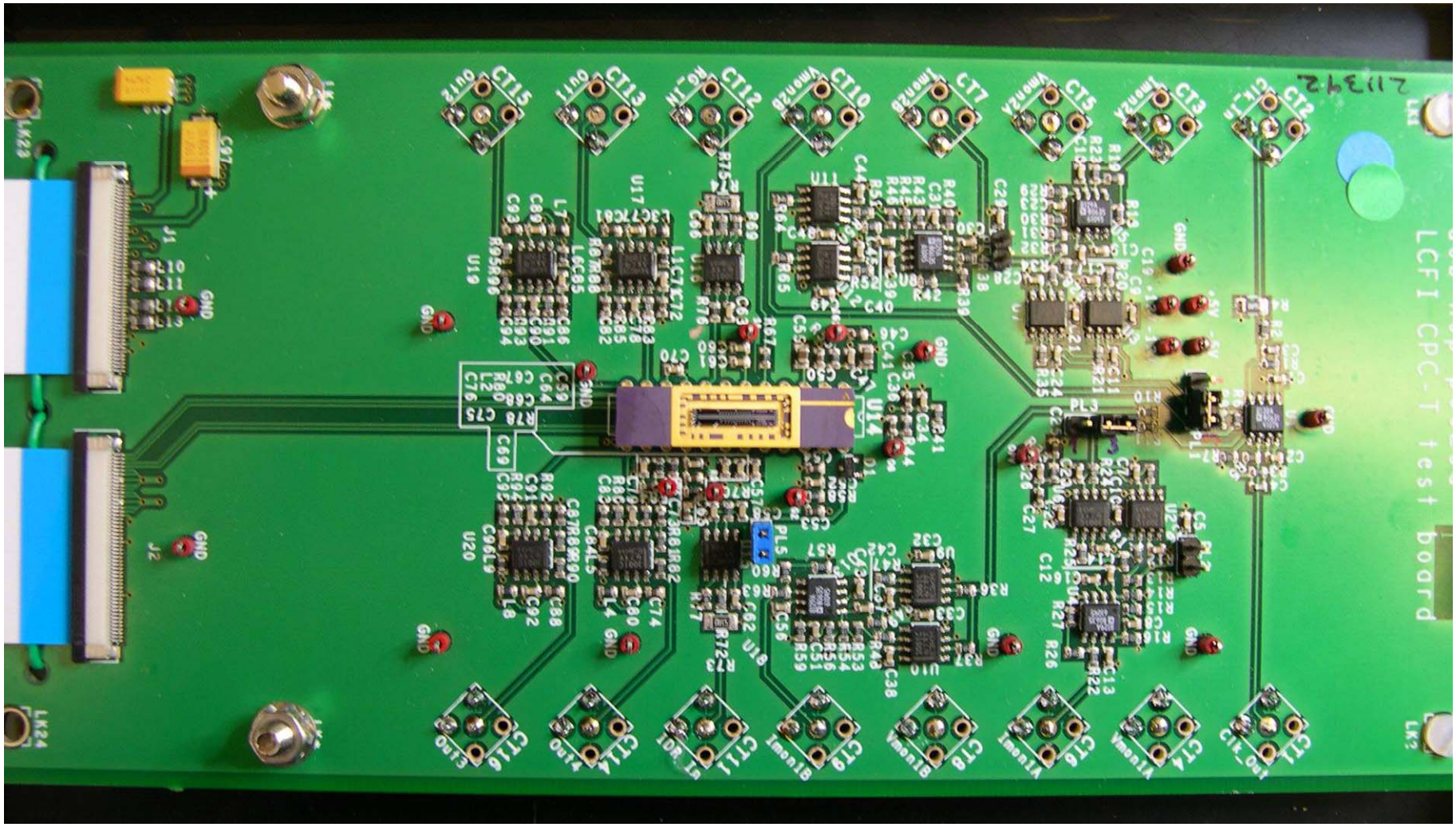
CPC-T





- 6 CPC-T wafers delivered, one of each type
- One type (stepped nitride barrier) failed the complete wafer
- Tests started at RAL and Oxford – the chip works!

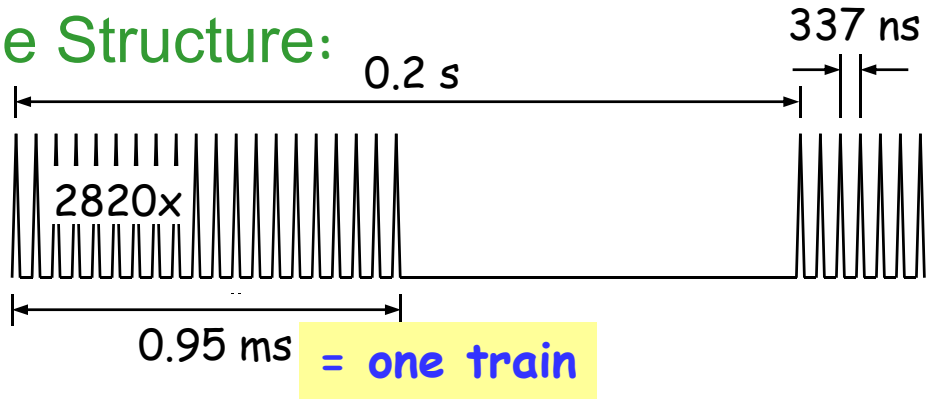
CPC-T in its board



D.Cussans, Bristol

Readout for ILC

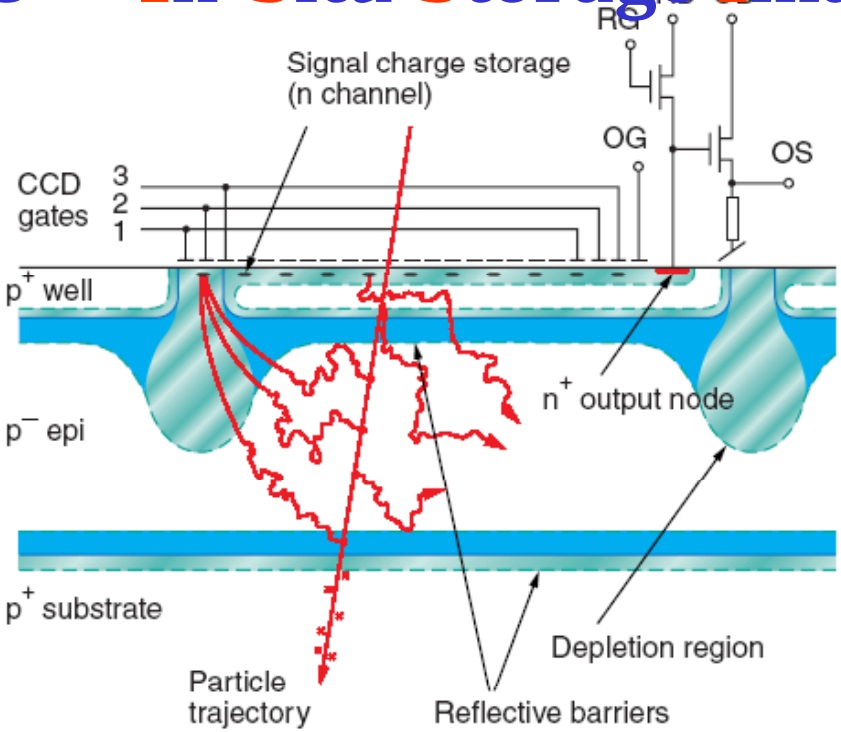
LC Beam Time Structure:



- Massive e^+e^- background from beamstrahlung : pairs radiated in intense EM fields of bunches
- Need to read out pixels in vertex detector once occupancy = 1%
  - 20 times per train

- **Main idea: Each pixel has a 20-cell storage**
  - Charge is stored INSIDE the pixel during collisions and read out during quiet time

ISIS – In-Situ Storage Image Sensor

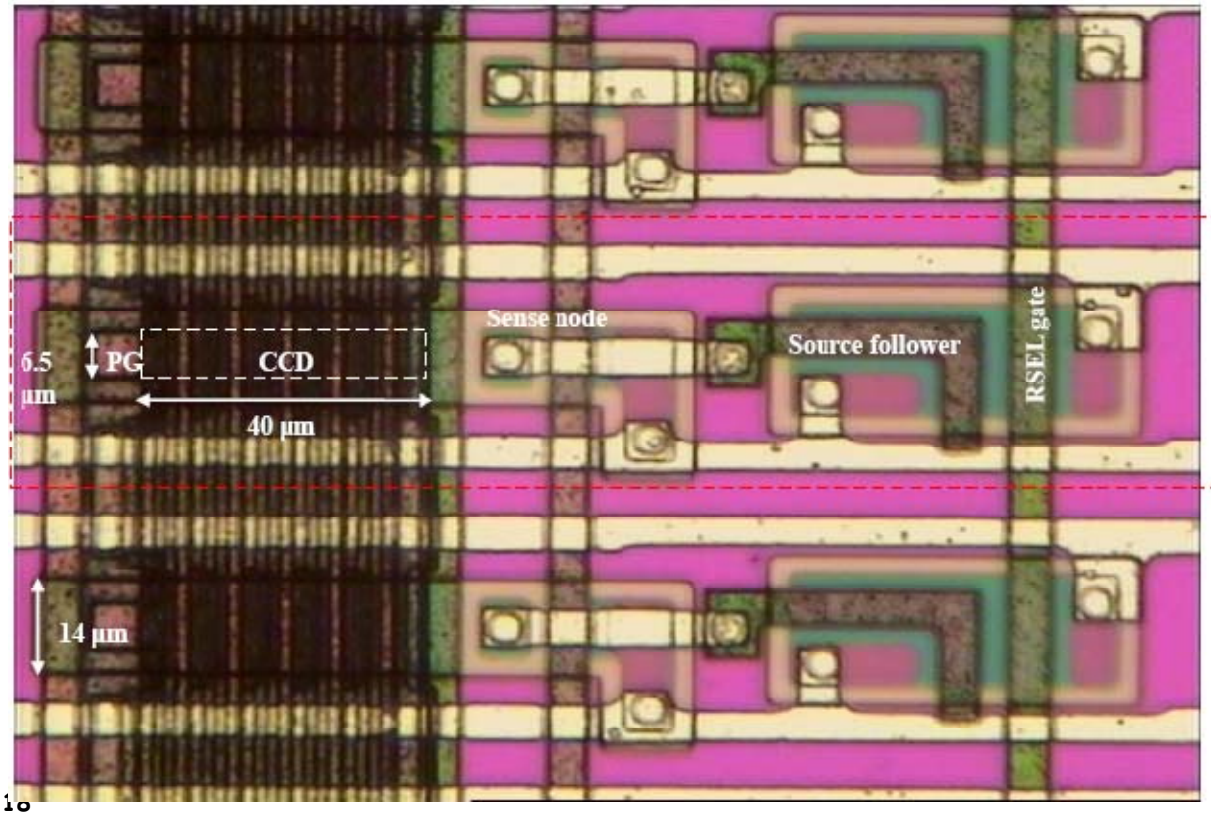


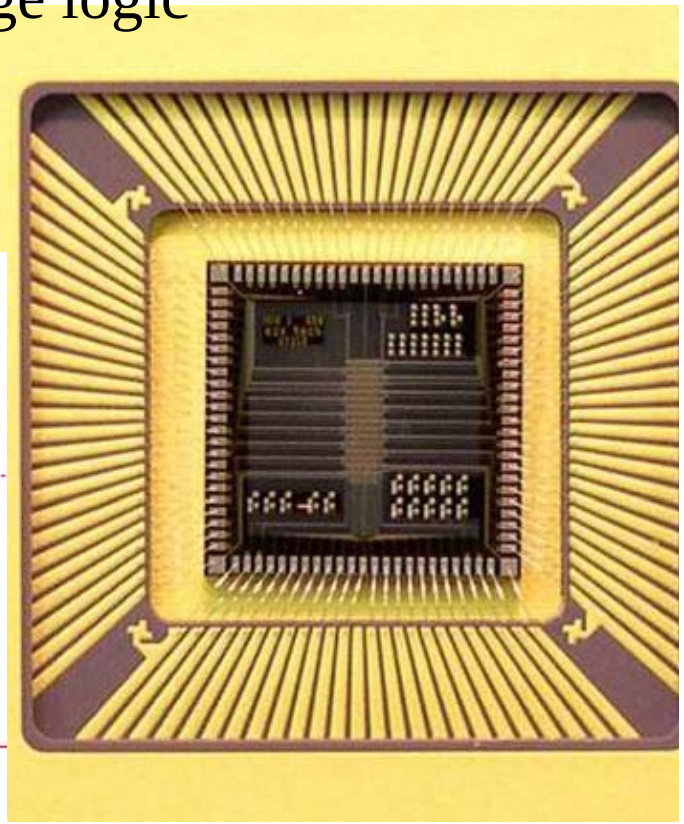
Ch.Damerell

- Each pixel has internal memory implemented as CCD register
  - Charge collected under a photogate
  - Charge is transferred to 20-pixel storage CCD in situ
  - Conversion to voltage and readout in the 200 ms-long quiet period after collisions
- Visible light imagers based on the ISIS principle are available off-the-shelf (ex. DALSA, 100 MHz camera with 16 storage cells)

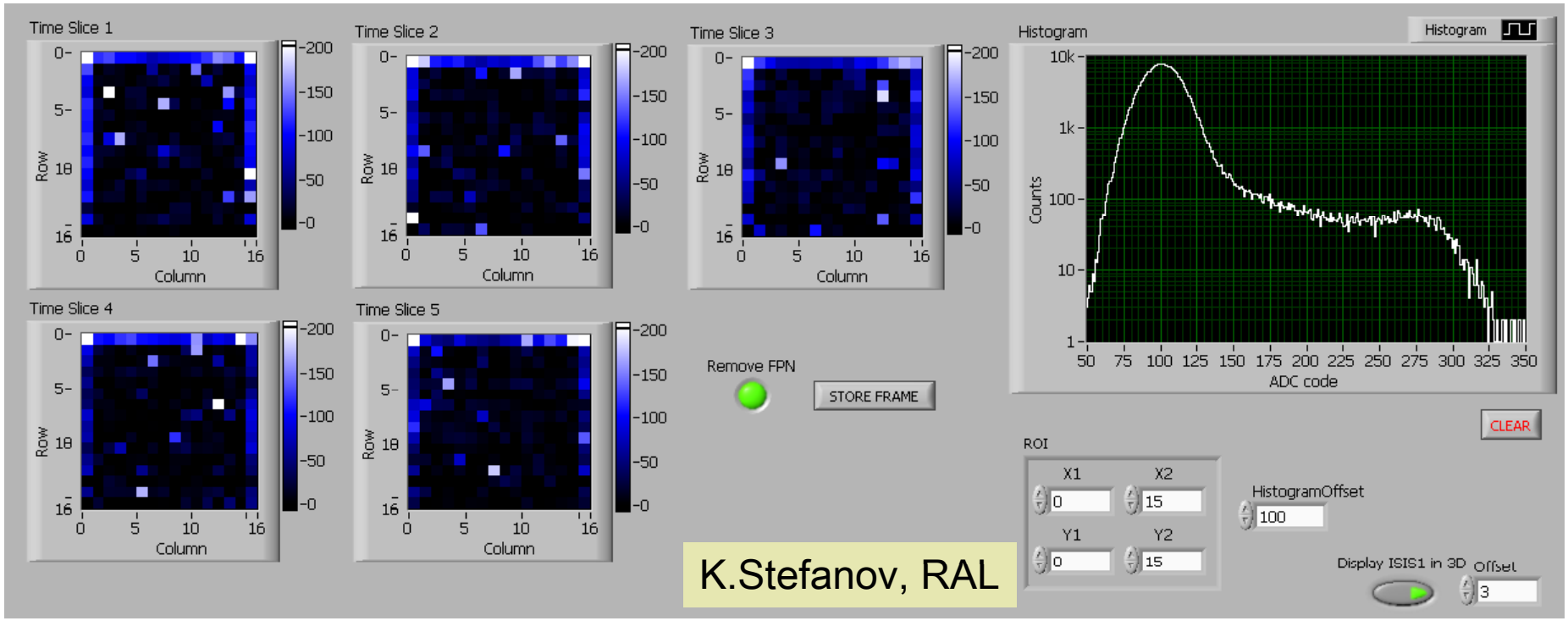
The ISIS1

- 16x16 pixels, each 140x60 μm^2
- Five storage cells for pixel
- Direct access to pixels by Row Select, no edge logic
- Two variants : with and without p-well
- Produced by e2V in UK
  - e2V had to rerun the p-well variant





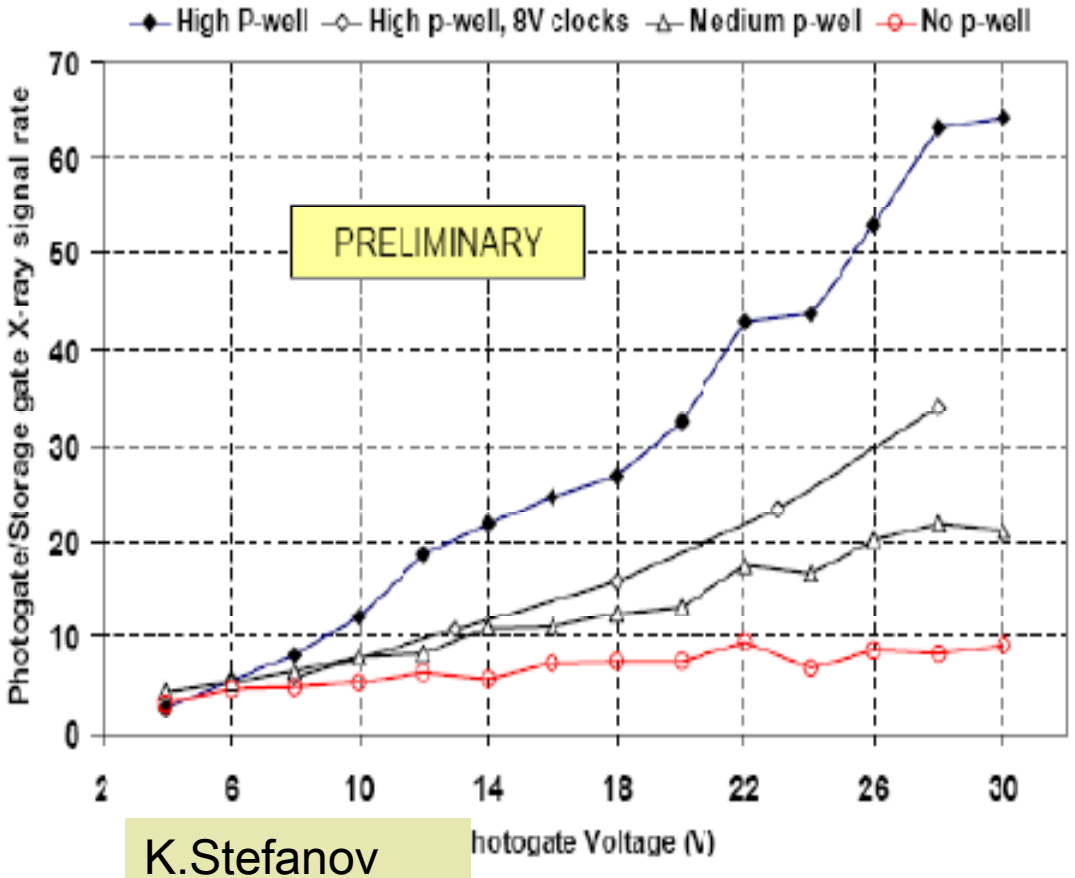
ISIS Proof of Principle



- Tests with ^{55}Fe X-ray source
  - Demonstrated correct charge storage in 5 time slices and consequent readout

ISIS1 with p-well

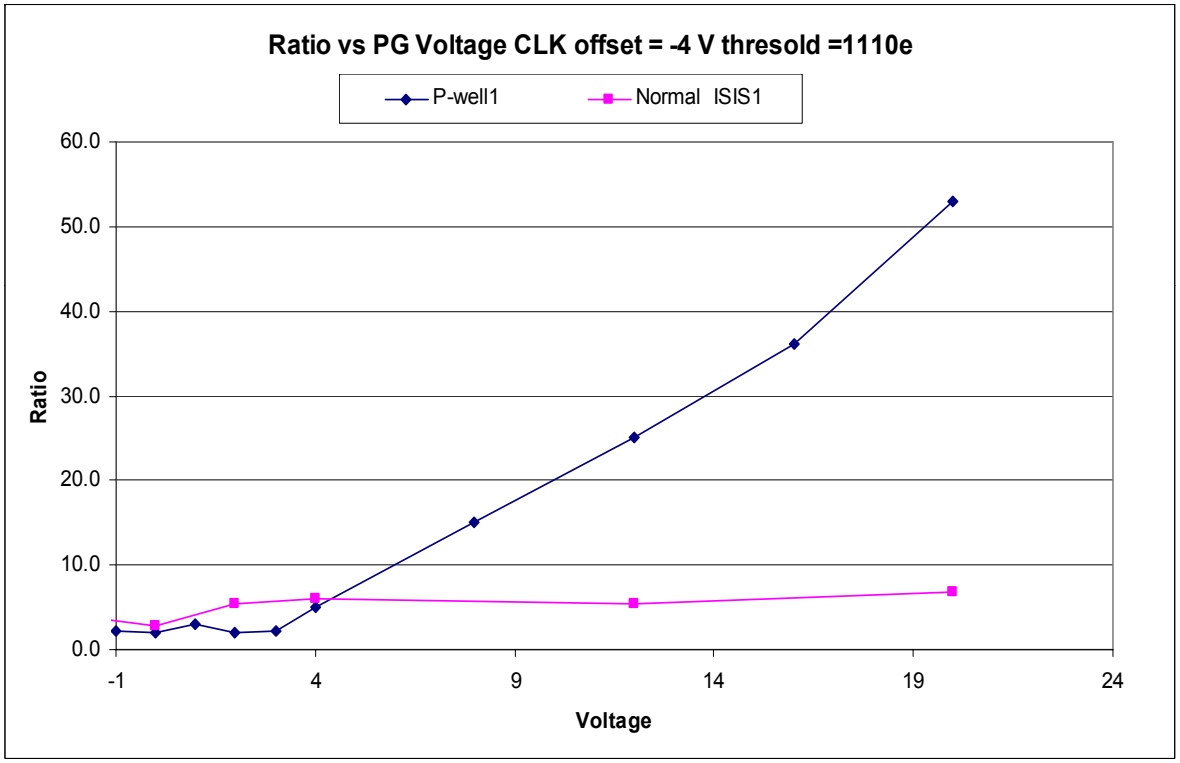
- High p-well doping protect storage register
- Look at ratio R of charge collected at photogate to charge collected at storage pixel
  - From ^{55}Fe (1640 e-)
- If increase clock voltage, get punchthrough under in-pixel CCD, R drops
- Lower p-well doping, charge reflection decreases
- No p-well, R ~ 7
  - dependent on gate geometry and voltages



K.Stefanov
G.Zhang, RAL

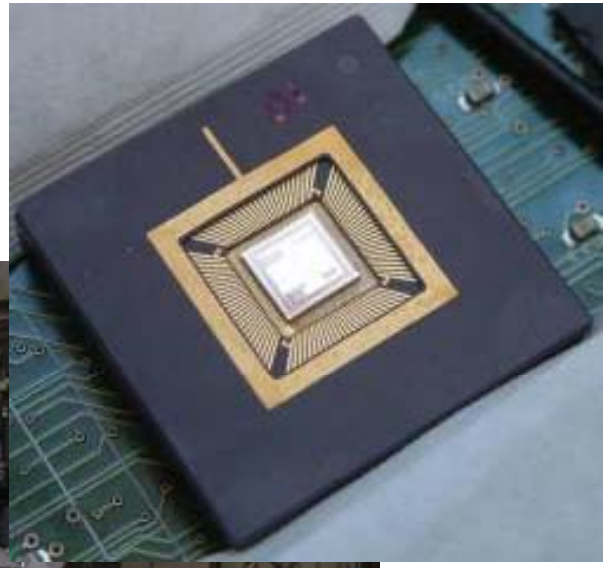
ISIS1 (p-well)

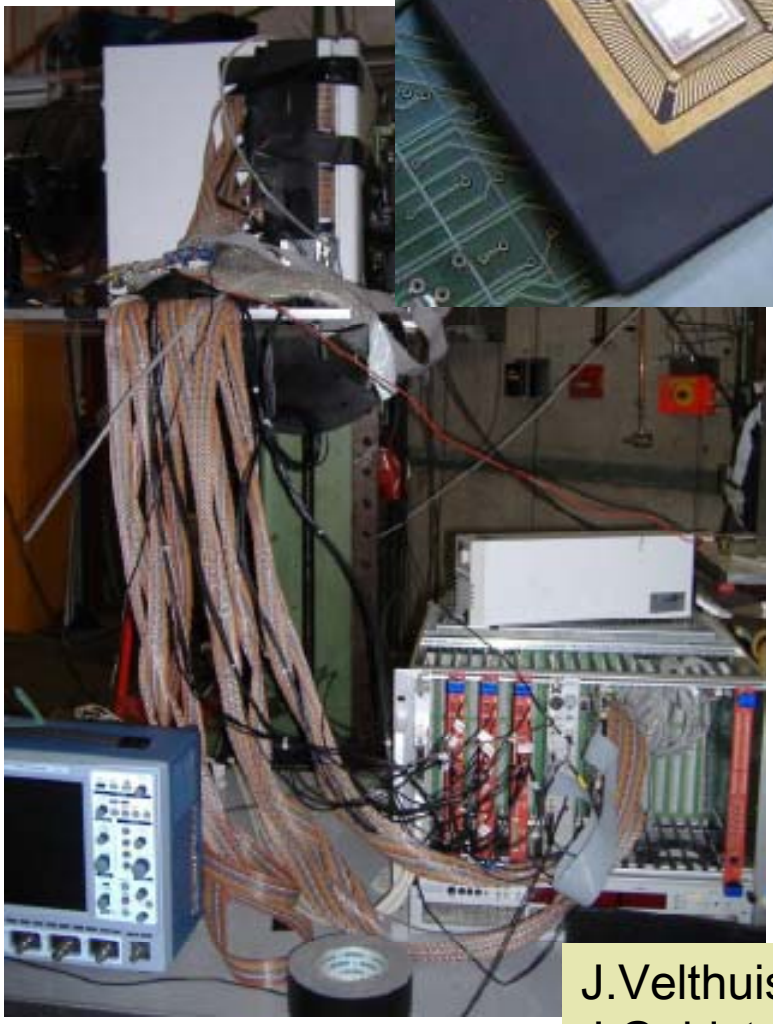
- **Direct punch-through observed too (below):**



ISIS1 Testbeam

- Constructed telescope with five ISIS1 chips
  - No p-well
- Active area 0.56 x 2.22 mm^2
  - Accurate alignment required
- Tests performed at DESY 1-6 GeV electron beam in Nov 2007
- Readout speed 2.5 MHz
  - ILC needs 1 MHz



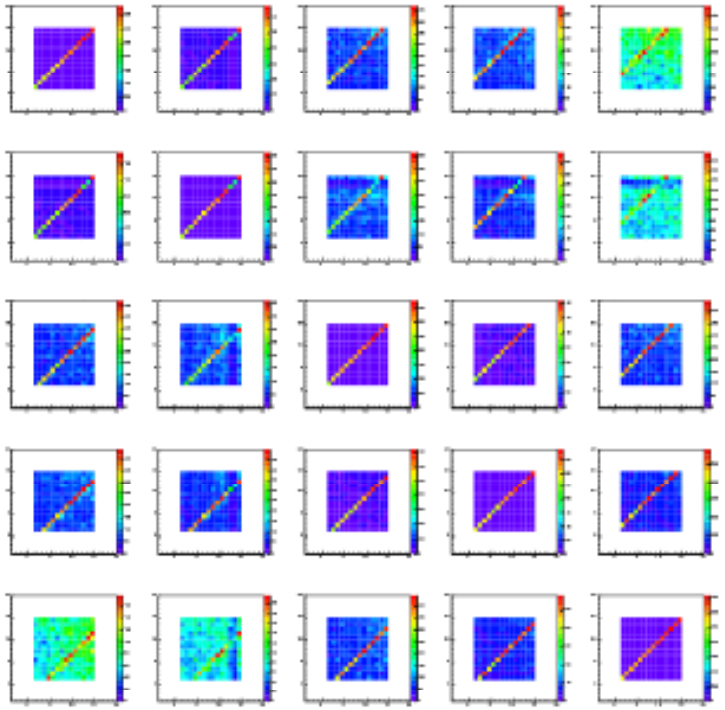


J.Velthuis
J.Goldstein
S.Mandry, Bristol

Test Beam First Results

- S/N = 37
- Position resolution in x-direction 10.8 μm
  - Pitch 60 μm → some charge sharing
  - Included large multiple scattering
- Little charge sharing in y-direction (140 μm across pixel)
- Next testbeam in August at CERN
  - Large beam energy and EUDET telescope
- Will test ISIS1 with p-well

- x versus x ("short" direction).

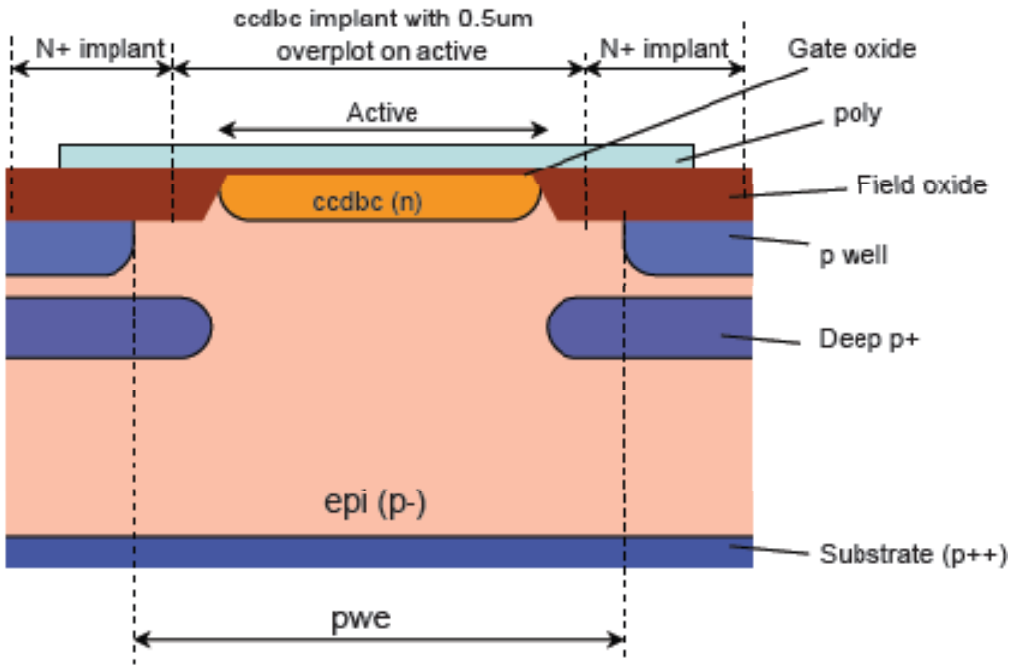


Correlation between measured and predicted position

J.Velthuis, Bristol

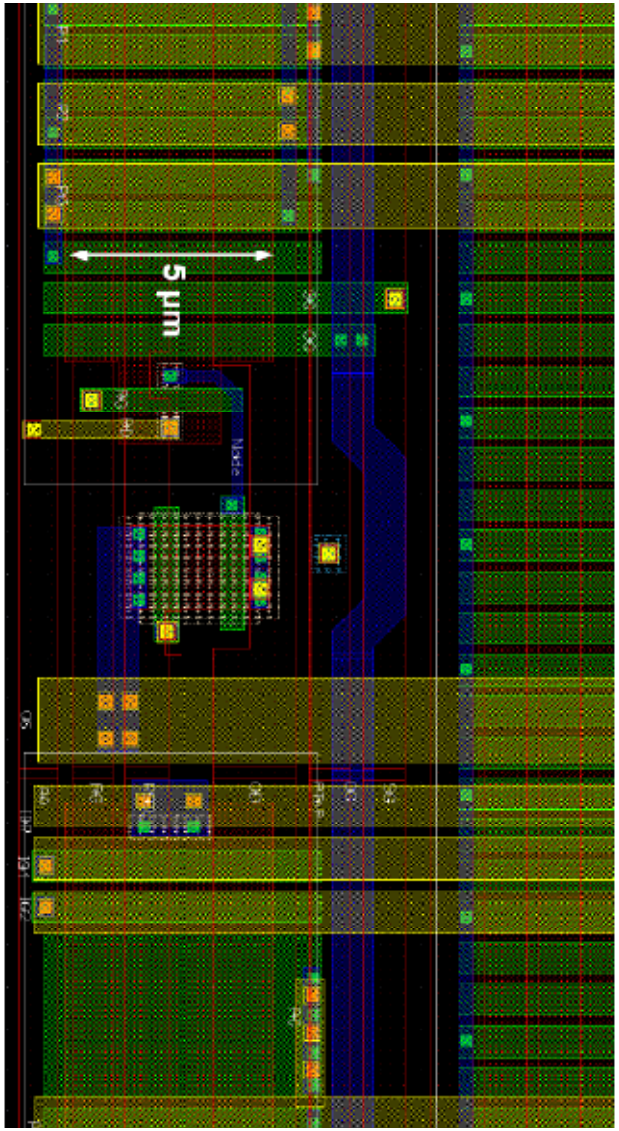
Next generation ISIS: ISIS2

- Jazz Semiconductor will manufacture ISIS2
  - Process: 0.18 µm with dual gate oxide → possible voltages 1.8V and 5 V
  - p++ wafers with 25 µm epi layer ρ > 100 Ohm cm
  - Area 1 cm^2 (four 5x5 mm^2 tiles)
- Will develop buried channel and deep p+ implant
  - Buried channel is necessary for CCD
  - Non-overlapping gates
  - Deep p+ is beneficial to decouple buried channel from p-well, no need for punchthrough, was absent in ISIS1
- Cross section under Photogate:



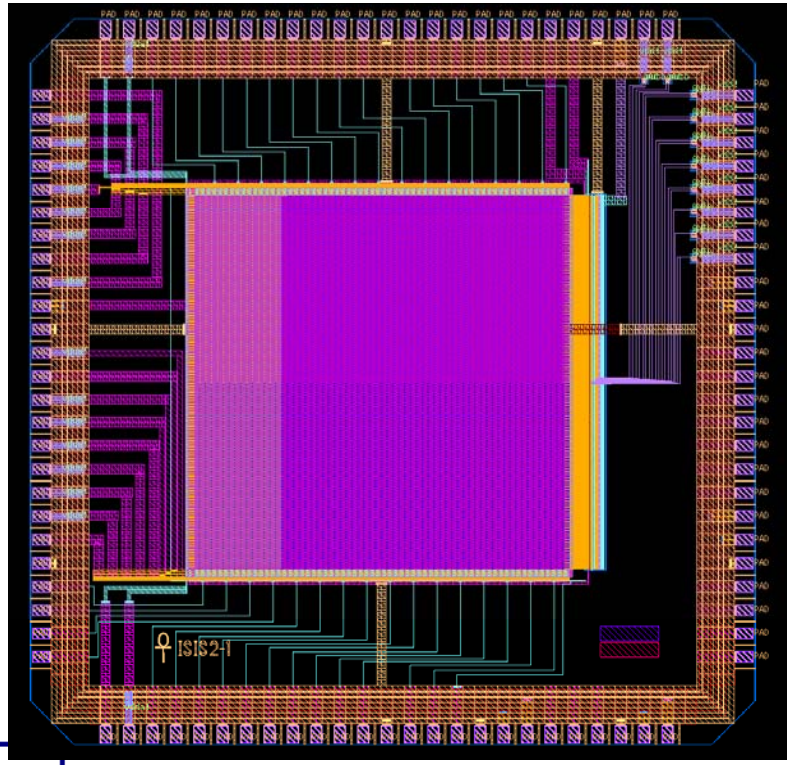
ISIS2 Design

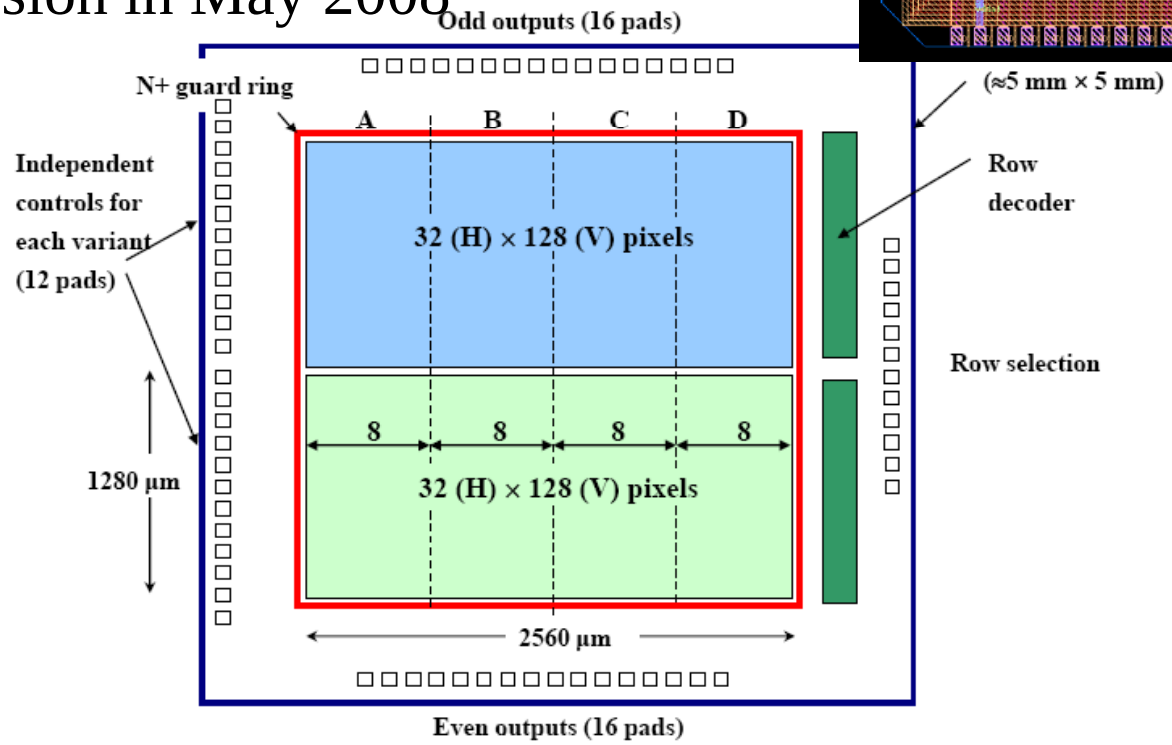
- Pixels 80 x 10 μm^2
- Buried channel 5 µm wide
- 3 metal layers
- CCD gates: doped polysilicon
- Logic, source follows use 5V custom logic gates



ISIS2 Design

- One chip will have several variants of ISIS2
  - Each has independent control
- Row select and decoder edge logic
- Will have several test structures
- Submission in May 2008

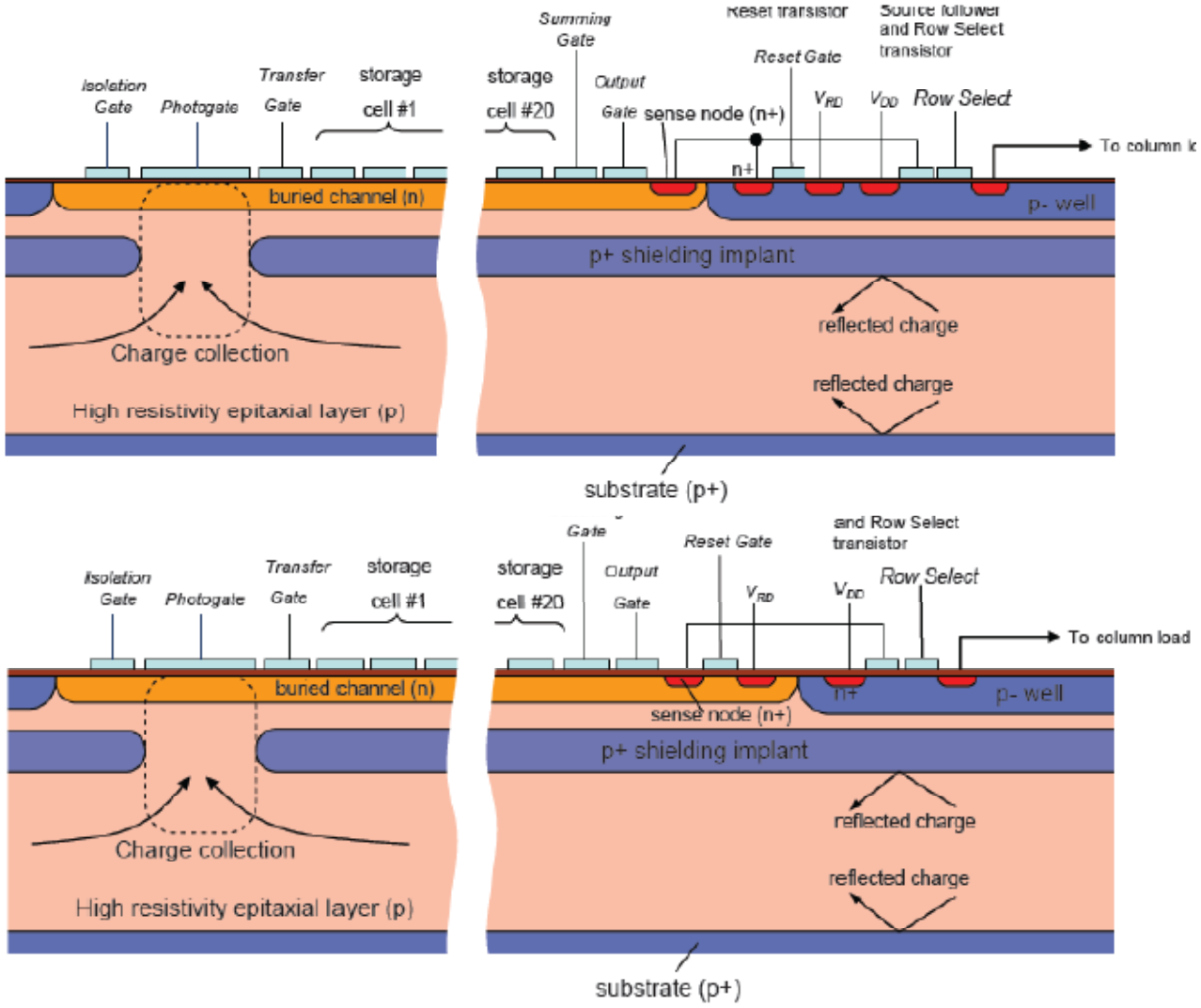




K.Stefanov
P.Murray, RAL

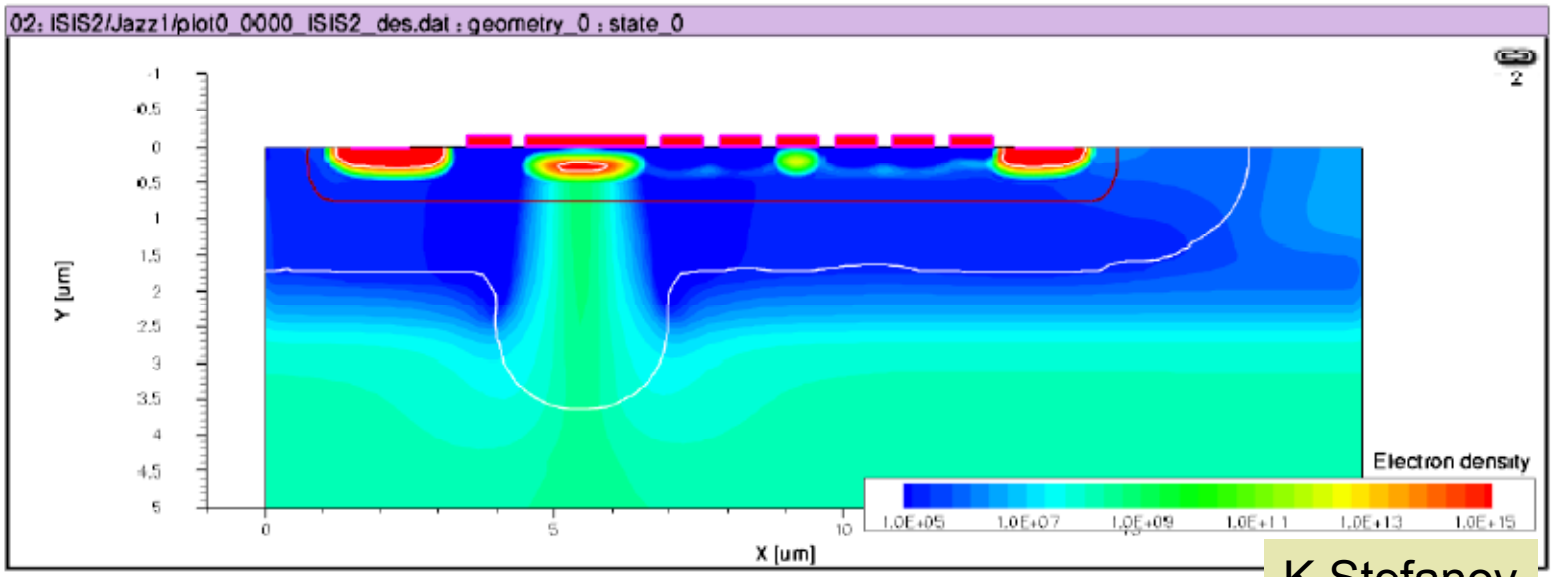
ISIS2 Variations

- Reset transistor
  - Surface
  - Buried channel
- Deep p+
  - With deep p+
  - Without deep p+
  - With deep p+ but no charge collection hole
  - Change in dopant concentrations of ~20%
- CCD gate width



Charge Collection

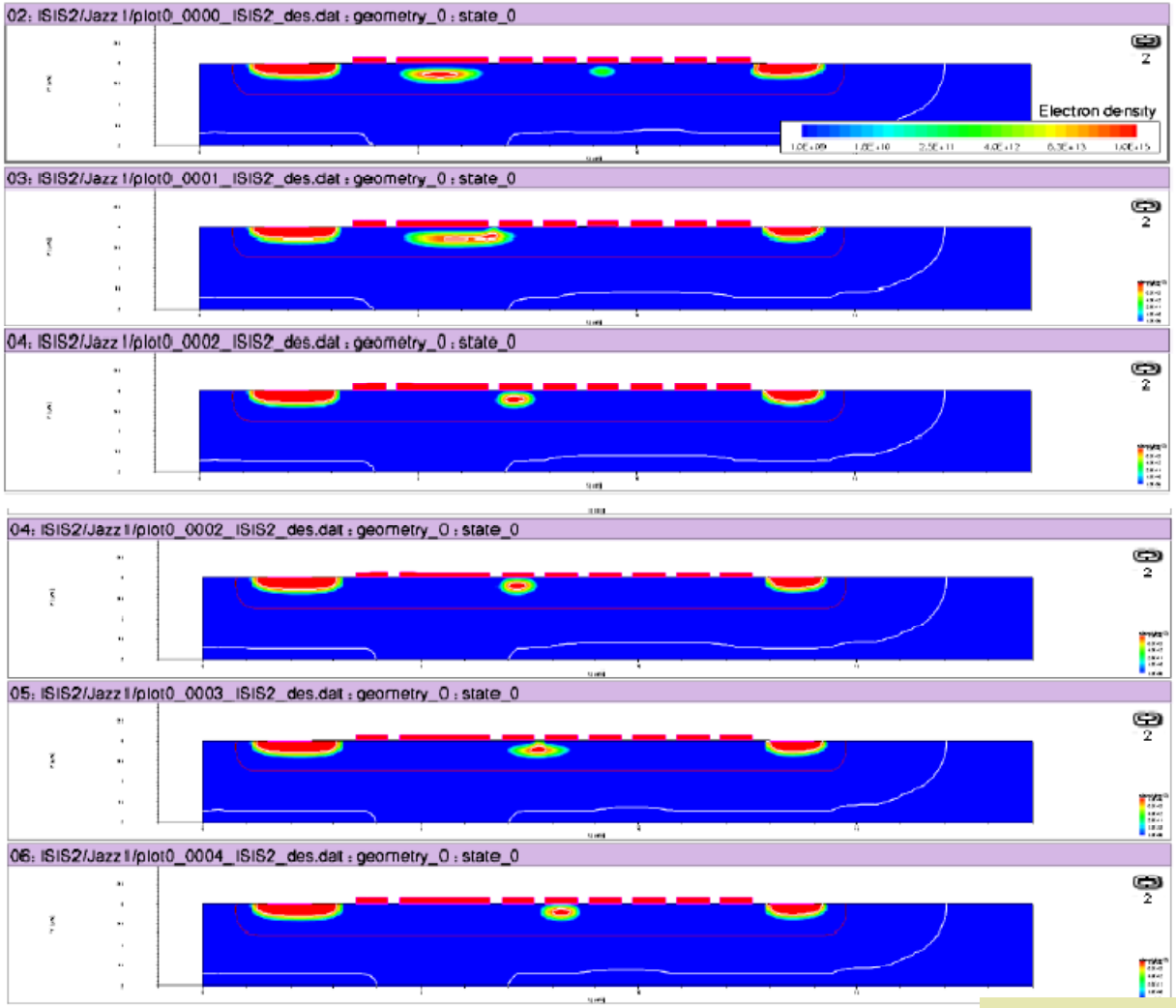
- Performance extensively simulated
- Charge collection:



K.Stefanov

Charge transfer

- Simulated charge transfer to photogate and to storage cells – all function with high efficiency



K.Stefanov

Physics Studies

- LCFI vertexing package is actively used by all ILC detector concepts
- LCFI has strong participation is the ILC and SiD benchmarking studies
- Physics processes
  - ttbar
  - ZHH
  - ZH→ cc νν; cc qq; ee X
  - ee→bb; cc
  - Sbottom → soft b jets

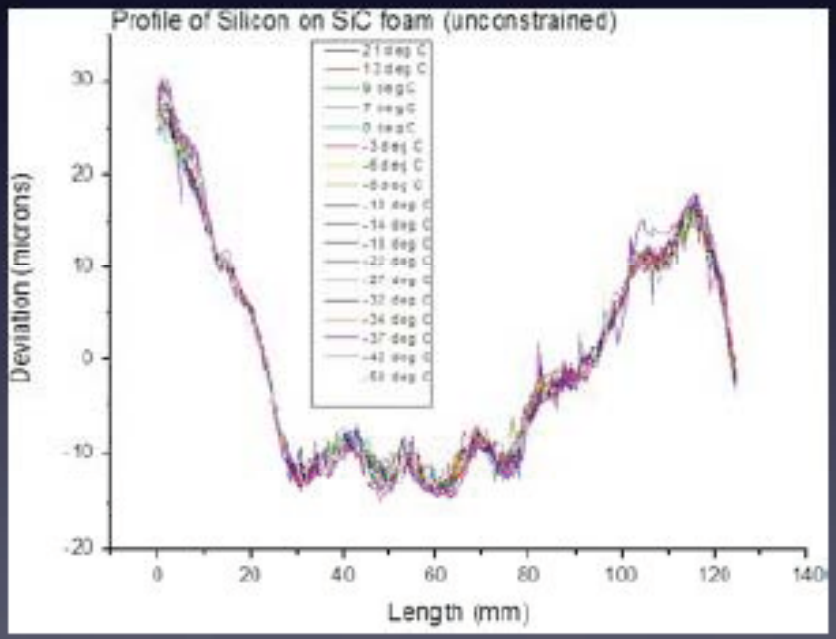
Mechanical Studies

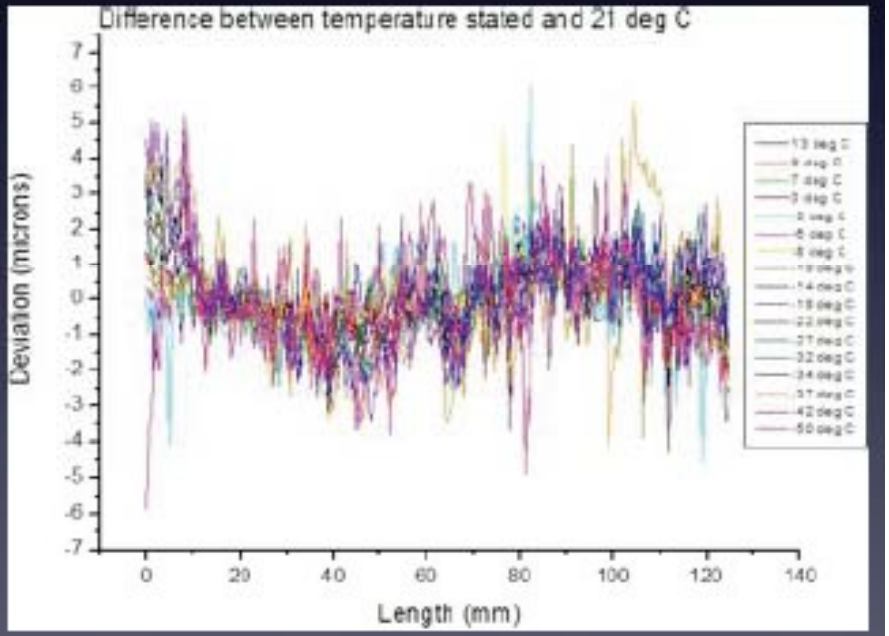
- 25 micron silicon on 1.5mm 8% SiC
  - Very rigid
  - Achieved 0.14% X_0

- 20 micron silicon sandwiching 1.5mm 2% carbon
  - Could be double-sided
  - Achieved 0.07% X_0

Mechanical Studies

- SiC Foam substrate ladder cooled
- Negligible thermal distortion over 70°C





Summary

- CPCCD demonstrated
  - Operation at 45 MHz with transformers
  - Low noise operation at 20 MHz
  - Operation with readout chip at 9 MHz, new readout chip under tests
  - 10 cm long sensors produced and tested
- ISIS proof of principle demonstrated
- ISIS2 ready for submission
- Good progress in Physics Studies and Mechanics
- Future uncertain.. But we hope to continue

Backups

Radiation Damage: What to Expect?

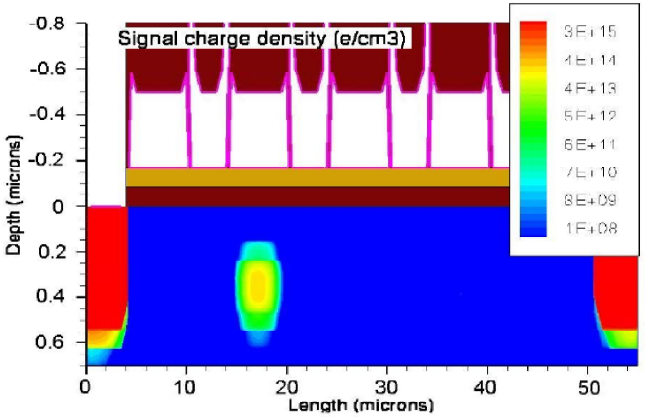
At R=14 mm

- Pair background from Beamstrahlung
  - 10 MeV electrons, 3.5 /bx/cm^2 → 0.5 10^{12} /year/cm^2 (→15 krad/year)
  - Surface damage: accumulation of charge at SiO_2/Si interfaces
  - Bulk damage: traps & leakage current
- Neutrons
  - 1 MeV n; 0.01 /bx/cm^2 → 1.6 10^9 /year/cm^2
  - Bulk damage

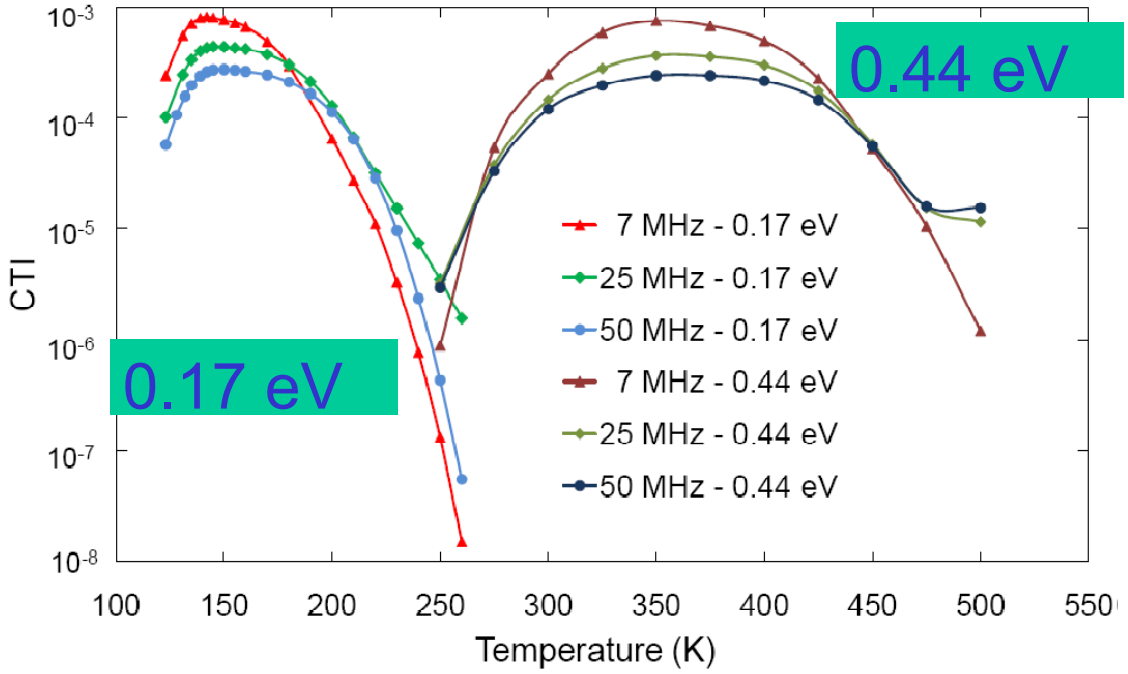
- Surface damage can be accommodated by adjustment of CCD biases
- Bulk damage translates to trap density
  - 0.17 eV trap; 3 10^{11} /year/cm^3; caused by electrons
  - 0.44 eV trap; 4 10^{10} /year/cm^3; caused by electrons and neutrons

Radiation Damage: Simulations

- ISE-TCAD simulations of charge propagation in the presence of traps
  - Charge trapped and later released: function of T and frequency
  - There is an optimum temperature window of low Charge Transfer Inefficiency (CTI) between -50 °C and 0 °C
- This should be confirmed experimentally in CPC2 and CPC-T

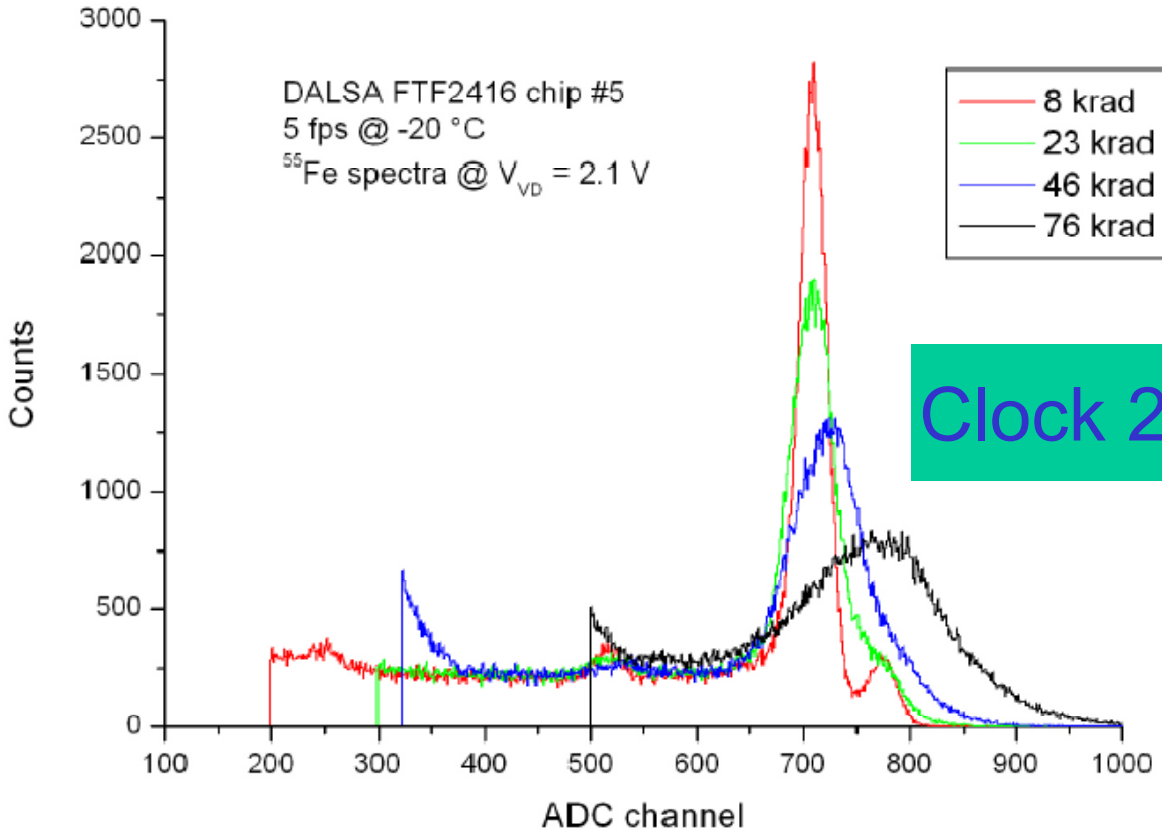


CCD model



Irradiations of DALSA CCDs

- Study to verify rad hardness of non-overlapping polySi gates
  - Charge-up of SiO_2 insulation between gates
  - Relevant for ISIS technologies with small cells
- DALSA CCD survived 70 krad from ^{90}Sr beta source
  - No change in minimal clock amplitude



Clock 2.1 V; 5.9 keV ^{55}Fe