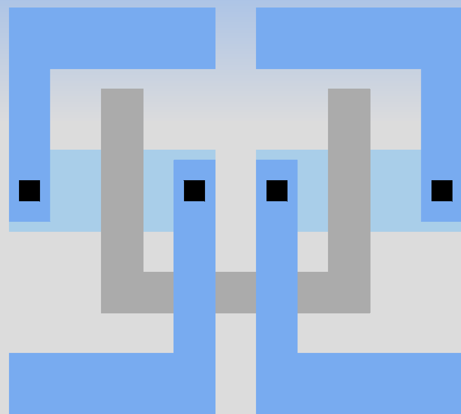
# Steering and Readout Chips for DEPFET Sensor Matrices




Prof. Peter Fischer,

Dr. Ivan Peric,

Christian Kreidl

christian.kreidl@ziti.uni-heidelberg.de

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# Outline

- Switcher3 Steering Chip
  - Requirement + Features
  - Block Diagrams
  - Test Results
- DCD2 Readout Chip
  - Requirement + Features
  - Block Diagrams
  - Test Results
- short: Bump Bonding Status
  - Bumping
  - Dummy-Chips
  - Flipping

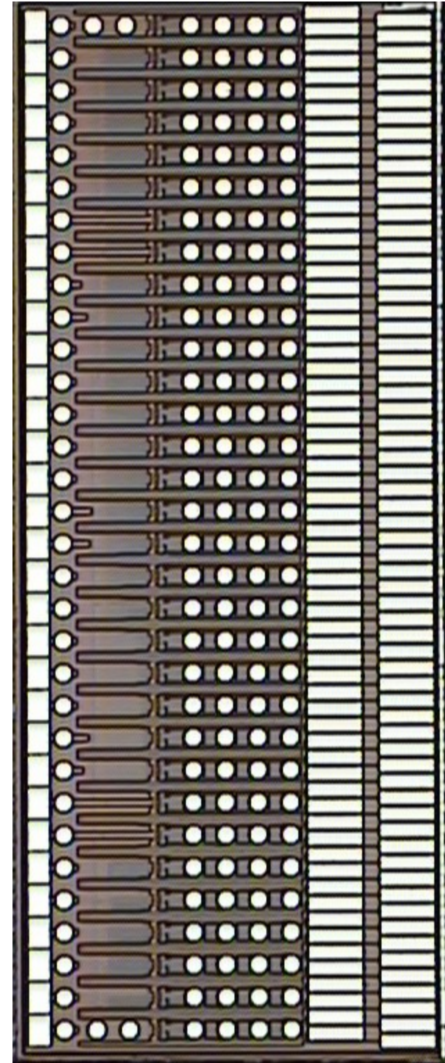
# Switcher3
# DEPFET Steering Chip

# Switcher3 Requirements

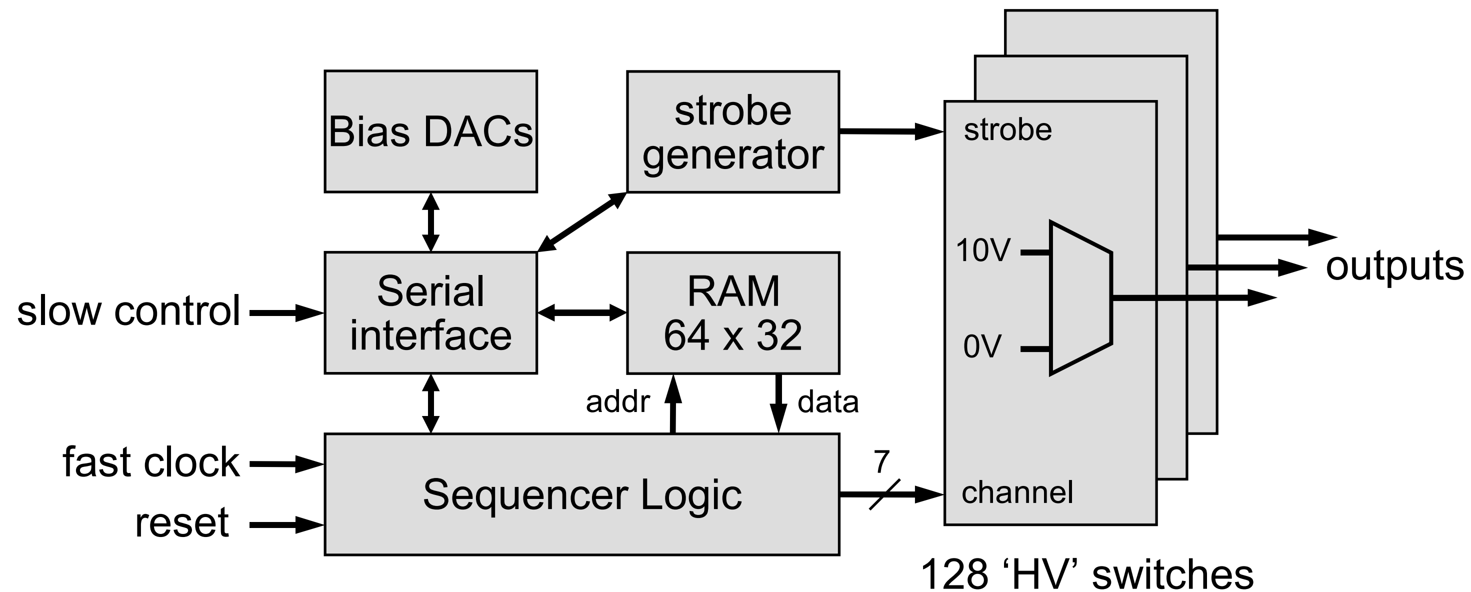
- steering chip for gate- and clear-signals
- high voltage **9V signals**
- **radiation hard** design
  - high voltage technology not suitable because of thick gate oxides
- 20pF matrix capacitance
- **fast** signal edges: <10ns risetime for 20pF load
- 128 channels
- not trivial **switching sequences**
- **bump** pitch of 180 µm, allows pixel sizes down to 24 µm
- <= 50MHz row rate

# Switcher3 features

- 9V switching using three **stacked** 3.3V transistors
  - needs twin-well technology (AMS h35b4)
  - capacitive coupling of digital and analog blocks
- **radiation hard** design, no HV-transistors
- 128 channels
  - **bump bonding**, wire bonding for compatibility
- sequencer
  - allows **non trivial switching sequences**
  - 4 commands, 64 lines program code length

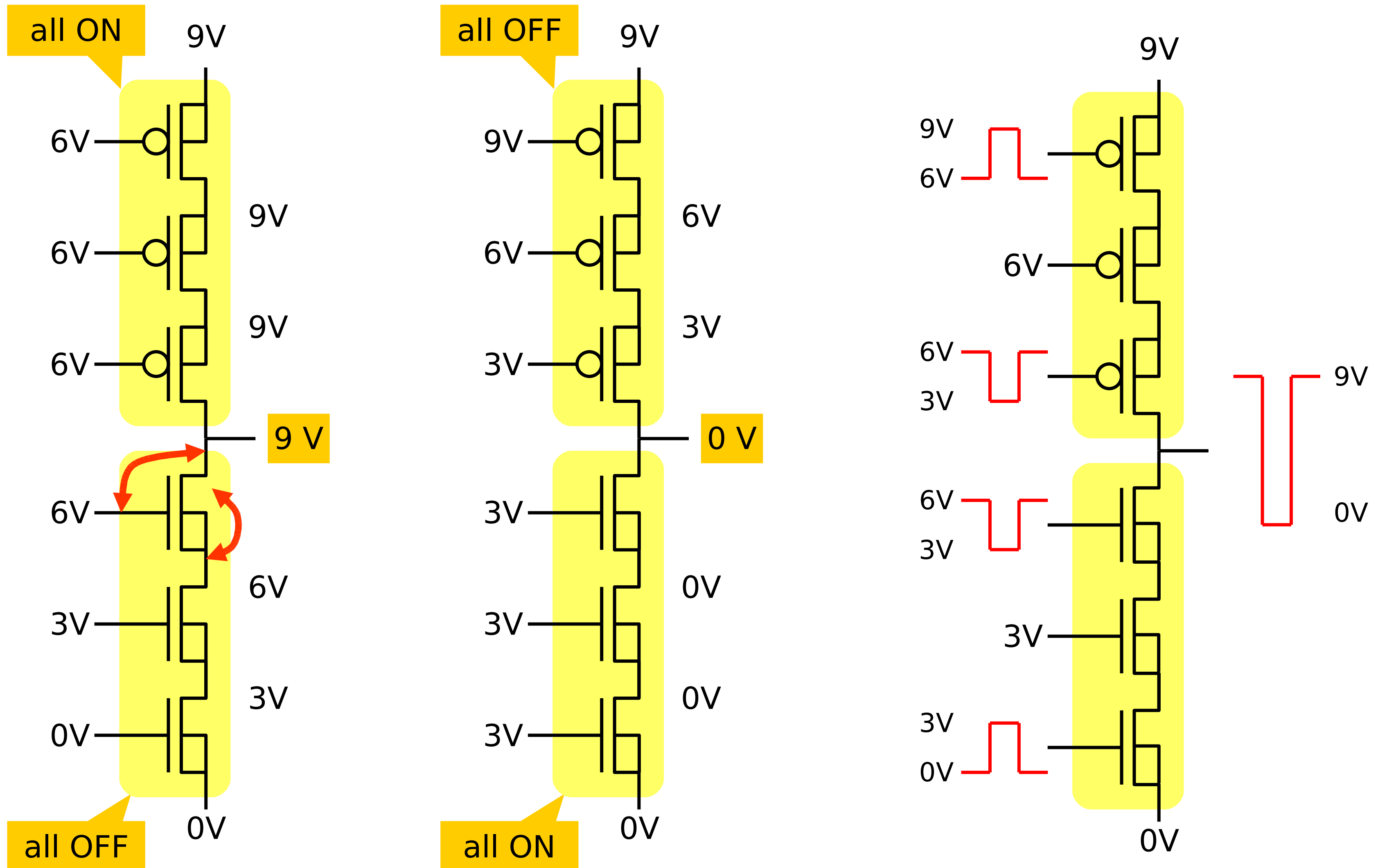


# Block Diagram



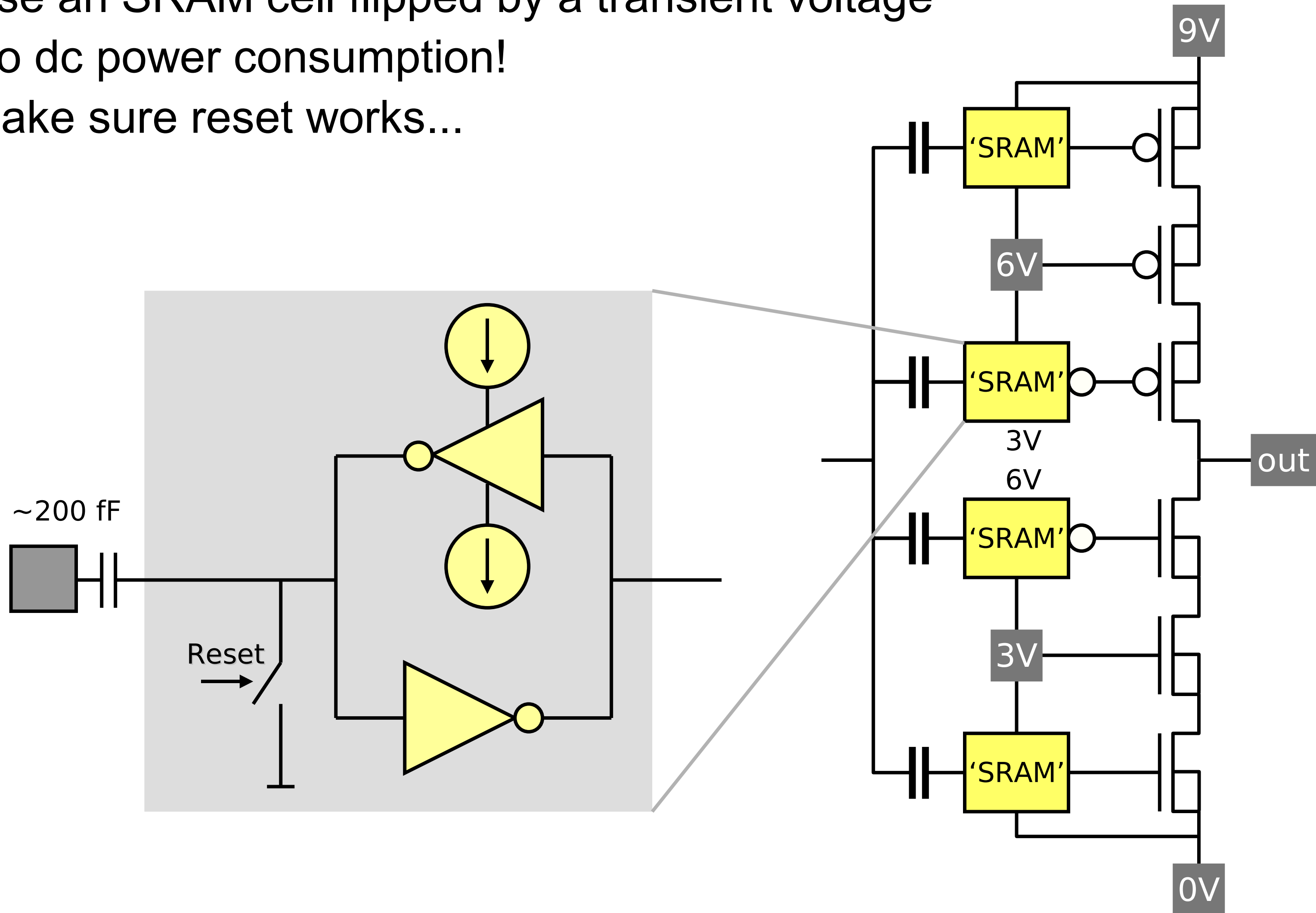
# Stacked Transistors

- Use 3 **stacked transistors**. Assume 3V per stage: VDD = 3 x 3V = 9V



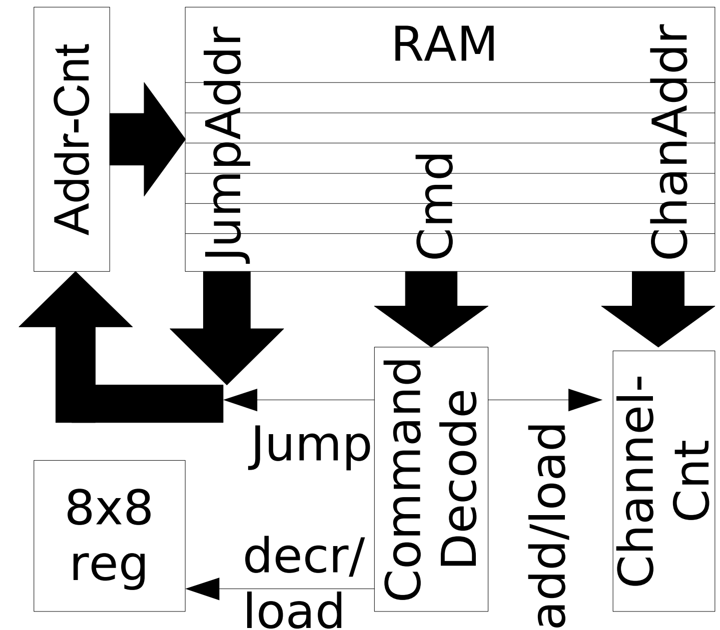
# Cap Coupling

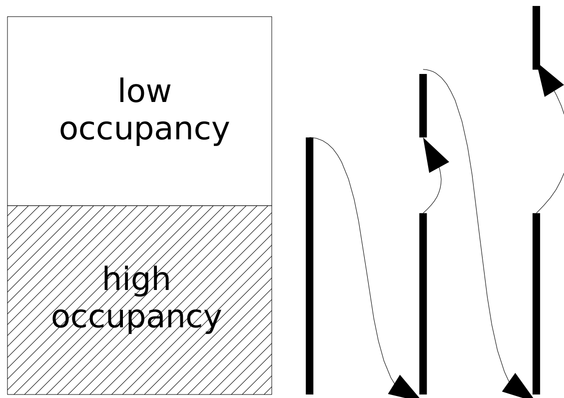
- Use an SRAM cell flipped by a transient voltage
- No dc power consumption!
- make sure reset works...



# Sequencer

- May need nonlinear scans
  - scan high occupancy more often
- Simple but flexible
  - jumping, looping,
  - absolute/relative channel addressing
- 64 words program length

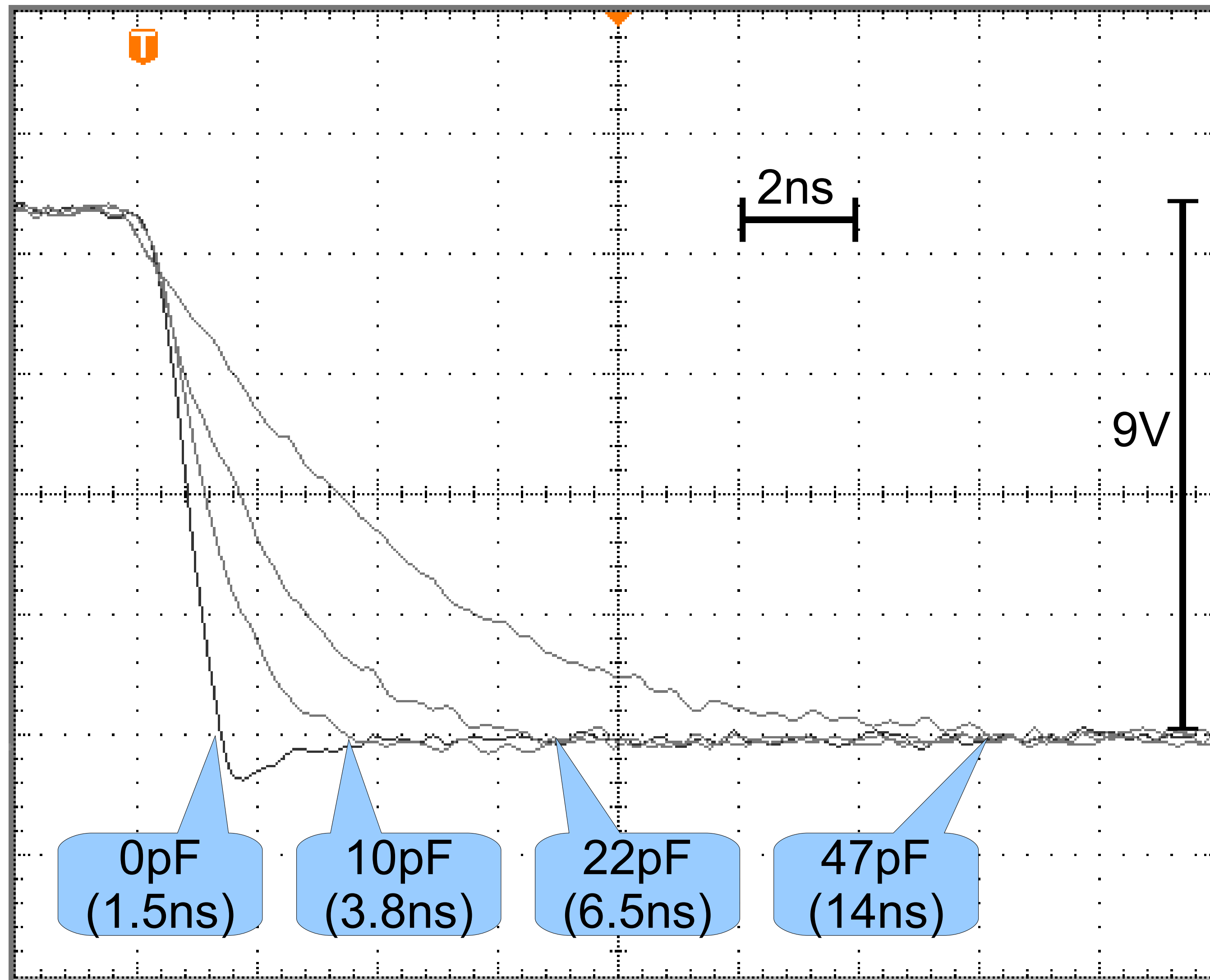


# Sequencer - Commands

- 64 RAM lines, i.e. command lines
- 4 commands
  - JUMP: jump <addr> <chanCMD> <chanNr>
  - LOAD: load <reg> <value> <chanCMD> <chanNr>
  - BNZDEC: bnzdec <reg> <jumpaddr> <chanCMD> <chanNr>
  - JMP_COND: jmp_cond <addr> <chanCMD> <chanNr>
- chanCMD
  - switches channel on or off
  - channel addressing can be absolute or indirect
  - on / off: add chanNr to channel counter, negative values allowed
  - onabs / offabs: chanNr is absolute
- 8 registers for looping using BNZDEC command
  - 8bit wide
  - coding done via complicated LFSR

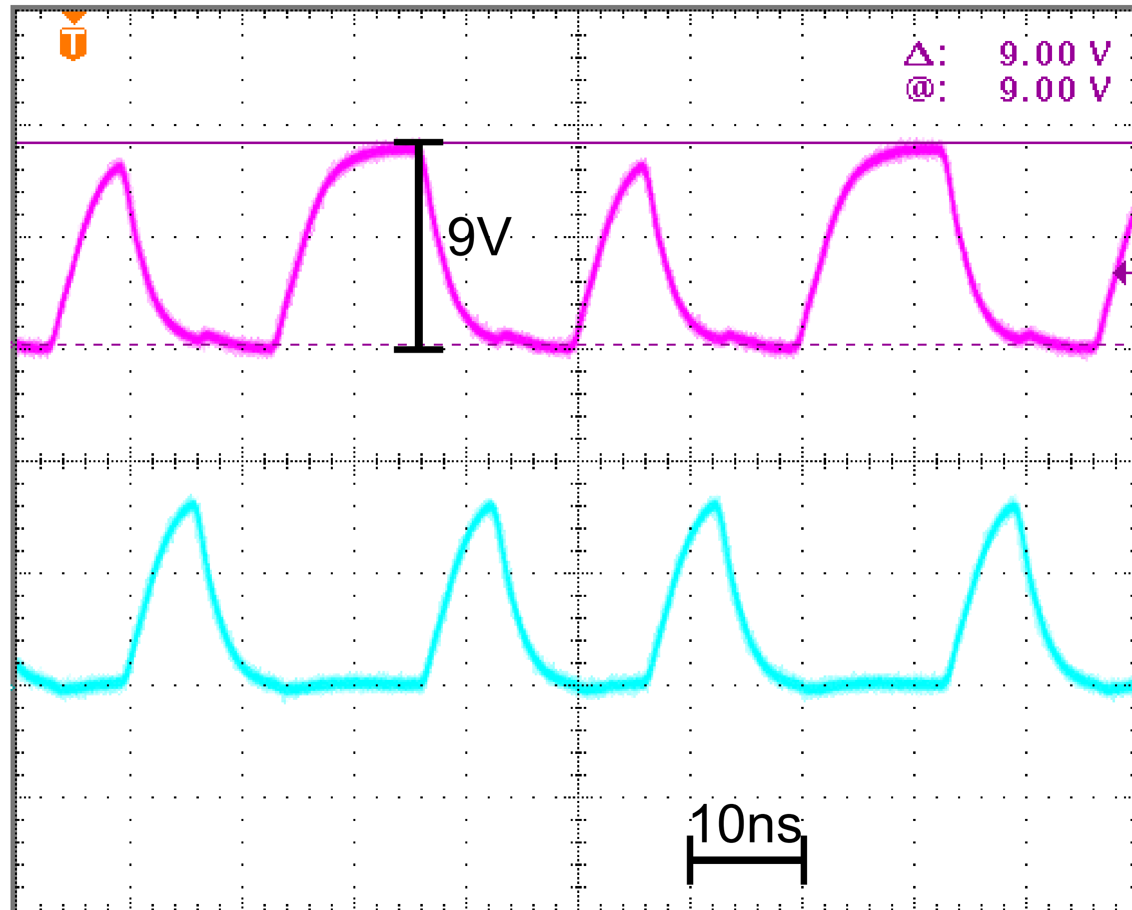
# Analog Test - Falling Edge vs. $C_{load}$



# Sequencer - Maximum Speed with $C_{load}$

150MHz
22pF

```
0: jump 1 onabs   29
1: jump 2 onabs   33
2: jump 3 offabs  33
3: jump 4 onabs   29
4: jump 5 onabs   29
5: jump 6 onabs   33
6: jump 0 offabs  33
```



# Summary

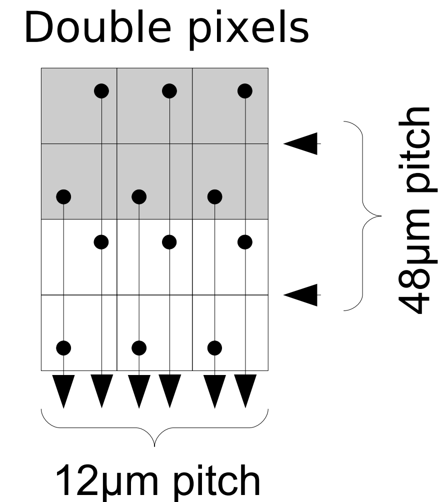
- Summary
  - all parts of chip are working
  - 150MHz max speed
  - 25mA on 9V supply for 22pF load @100MHz
  - 30mA on VDD @100MHz (0.4mW/output)
  - 8ns settling time from 0V to 9V on rising edge @22pF
  - 6.5ns settling time from 9V to 0V on falling edge @22pF
  - long term stress test passed

- Next Steps
  - irradiation (test structures were unaffected by ~1 Mrad)
  - operation with DEPFET matrices

# Drain Current Digitizer - DCD2 DEPFET readout chip

# DCD Requirements

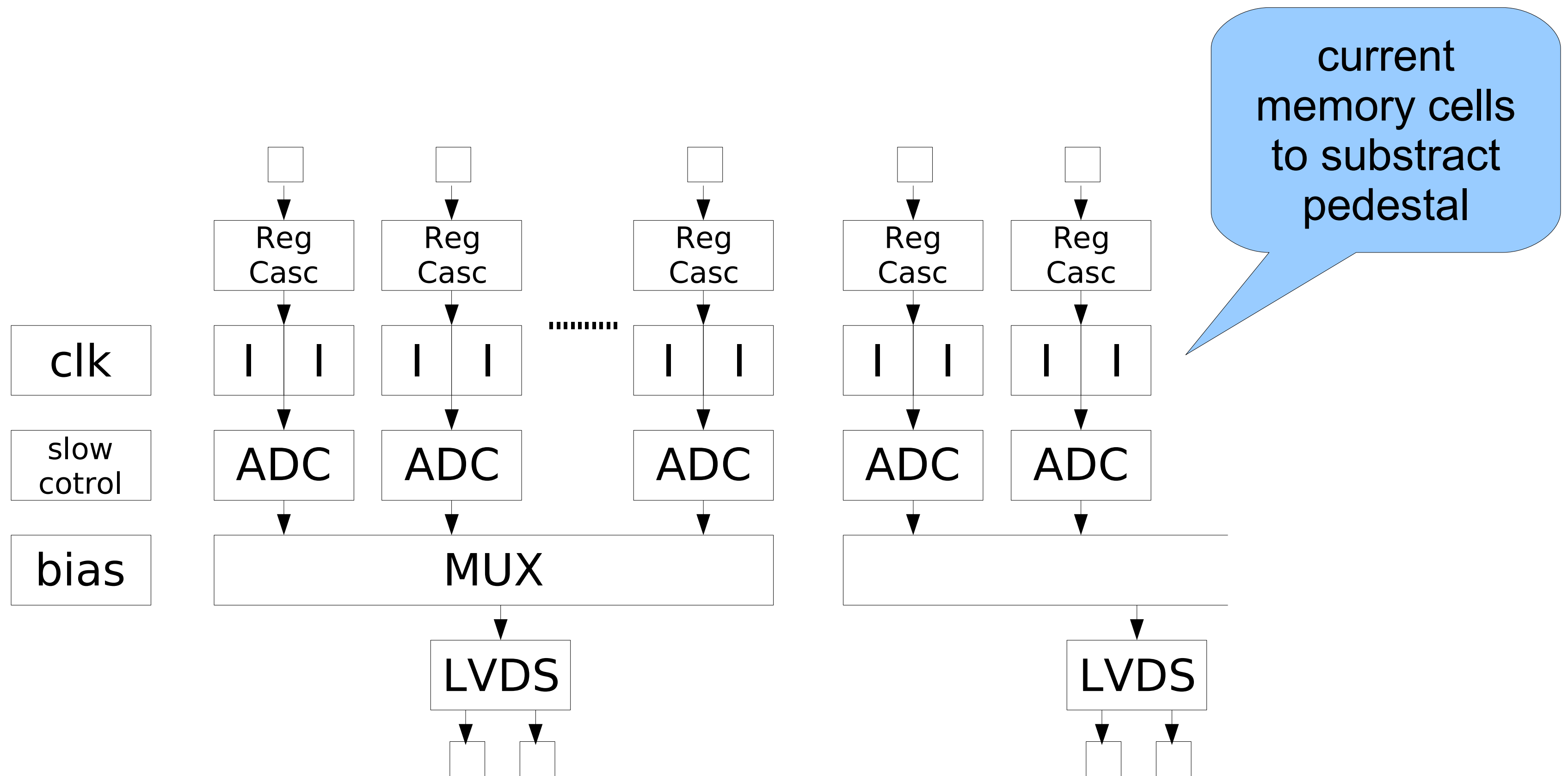
- Matrix organized as double pixels (24µm x 24µm)
  - 48µm Switcher steering pitch
  - **12µm** DCD readout pitch
- Iped ~ 30µA
- Isig ~ 6µA
- Large detector capacity ~40pF
  - 2000 pixels + 5cm bus
- Speed goal: 25MHz row rate, 12.5MHz double row rate



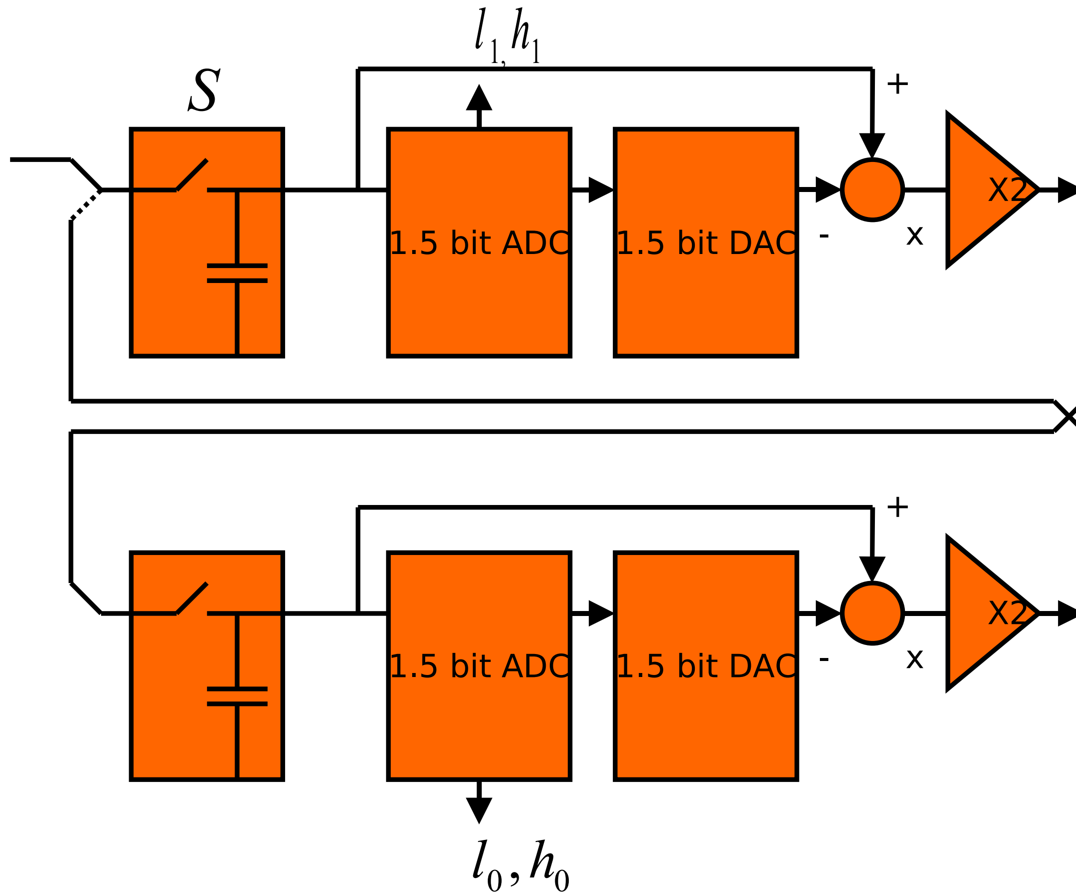
# DCD features

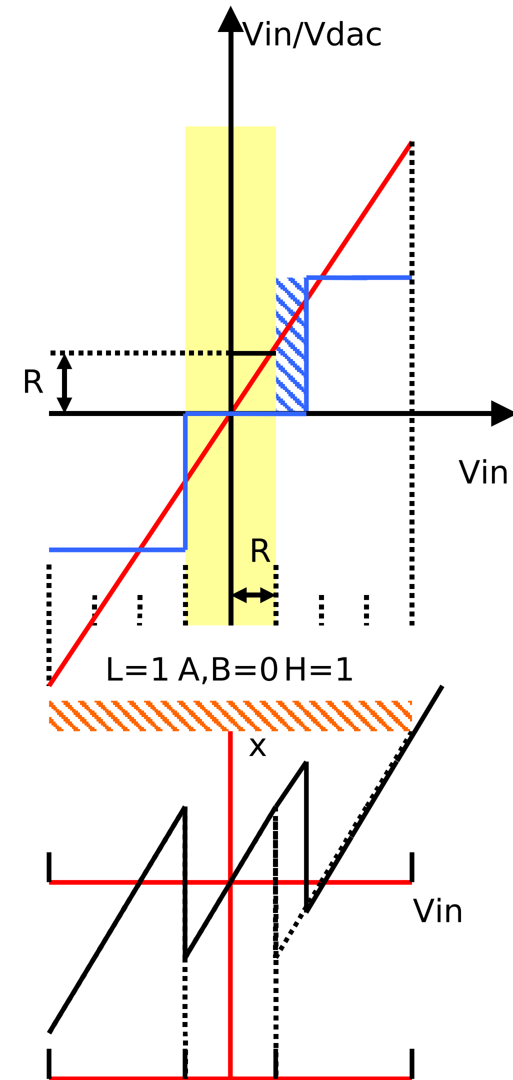
- UMC 0.18µm 1.8V technology
- regulated cascode
- offset substraction
- two 8bit algorithmic ADC per channel
  - 6.25MHz each, 12.5MHz sampling rate
  - small layout: 110µm x 50µm
  - low power: 2mW/channel
  - 144 ADCs on final chip, high speed output @600MHz LVDS
- consequent current mode signal processing
- no zero suppression
  - occupancy in ILC so high, that benefit of 0-supp too small
- Bump bonding with pixel logic & ADC placed around pad
- Radiation Hard Design
- NMOS in triple well, guard ring around analog part

# Block Diagramm



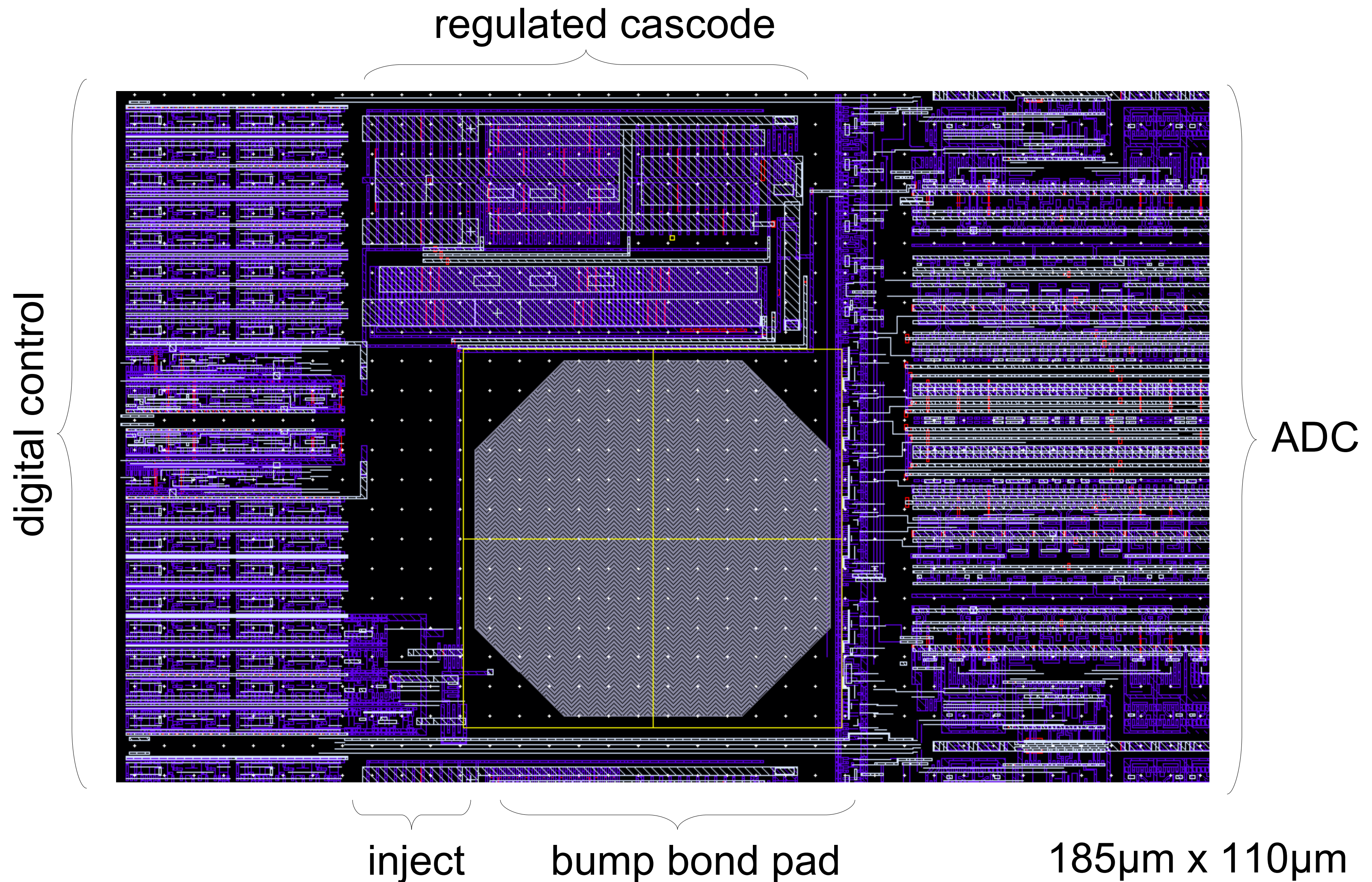
# ADC - working principle



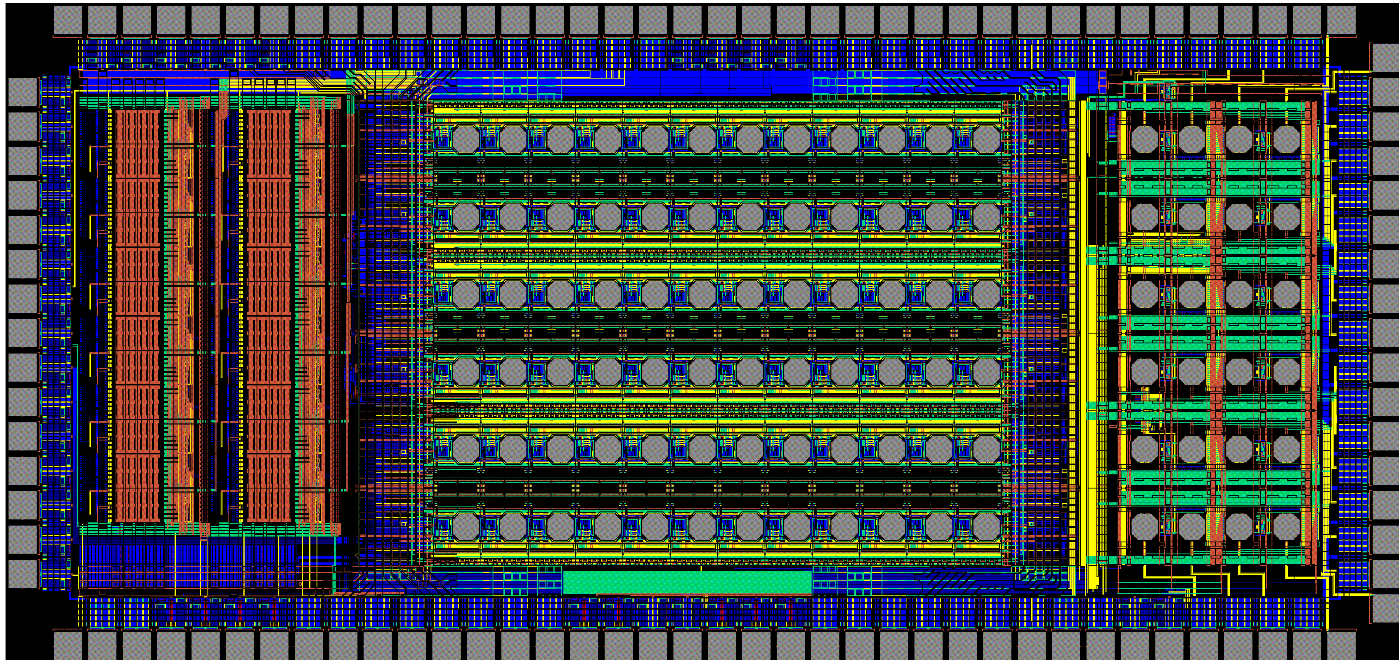

- algorithmic ADC
- insensitive to reference shifts by using 1.5bit

# Channel Layout




185µm x 110µm

# Chip Layout



DACs inputs with ADCs LVDS outputs

# Power

- Designed:
  - Cascode: 1.24mW
  - Curr. Mem. Cells: 0.19mW
  - ADC: 1.97mW
  - LVDS: 0.9mW

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  - Total: 4.3mW per channel
- Measured with present settings:
  - Total: 3.54mW per channel

# Regulated Cascode

Regulated Cascodes of 4 Pixels

Pixel (2,11)
Pixel (3,11)
Pixel (4,11)
Pixel (5,11)

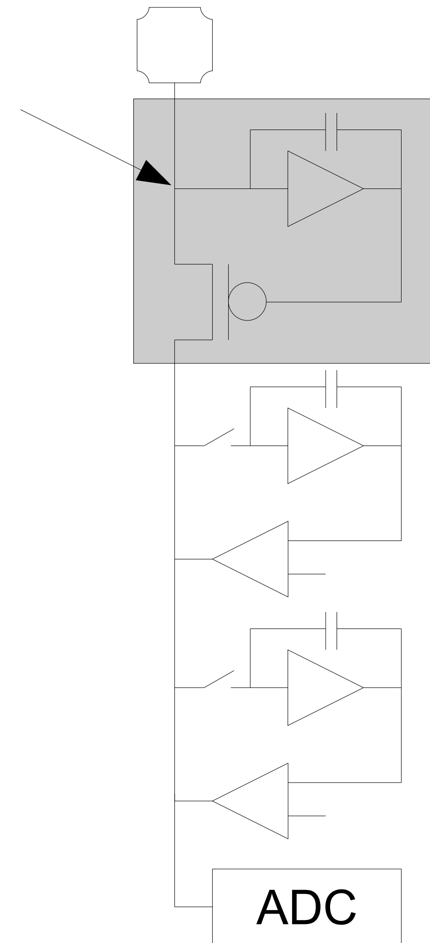
U [V]

1,55
1,5
1,45
1,4
1,35
1,3
1,25
1,2

0 5 10 15 20 25

I input [uA]

4mV change in 17µA range




- can regulate for currents up to 17µA
- only 4mV voltage changes

# Current Memory Cells

Current Memory Cells of 4 Pixels

Pixel (3,5)
Pixel (3,6)
Pixel (3,7)
Pixel (3,8)

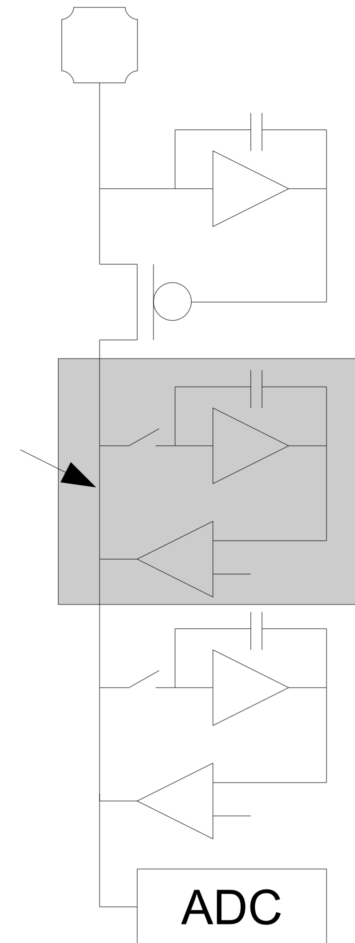
2
1.5
1
0.5
0
-0.5

U [V]

memory range

-15 -10 -5 0 5 10 15

I source [uA]




current memory cell for offset substraction can store in range -9µA..9µA

# ADC

ADC output of a Pixel

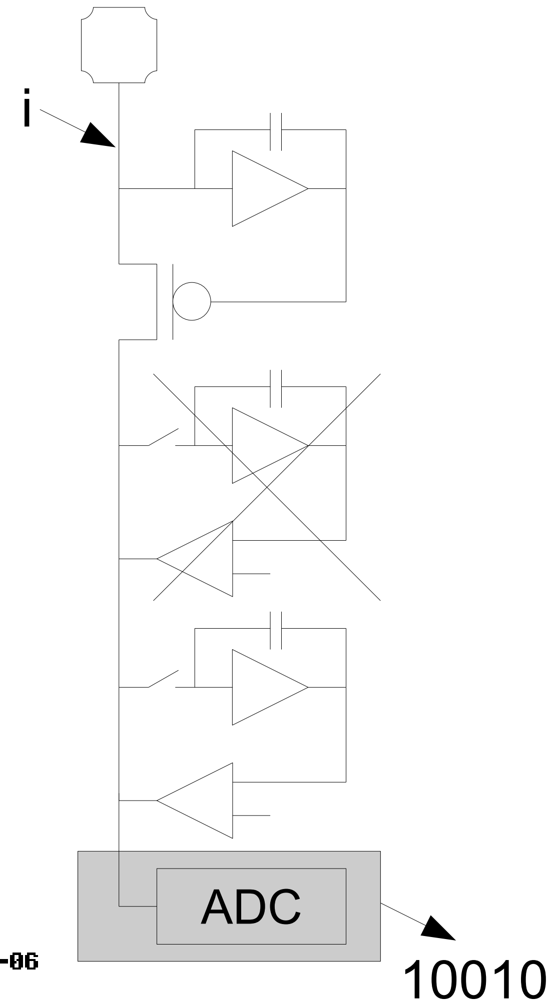
mean
linear fit

ADC output

300
250
200
150
100
50
0
-50

-6e-06 -4e-06 -2e-06 0 2e-06 4e-06 6e-06 8e-06

Test-Injection Current




full 8bit ADC range, good linearity of ADC

# Pedestal Substraction

Offset Substraction

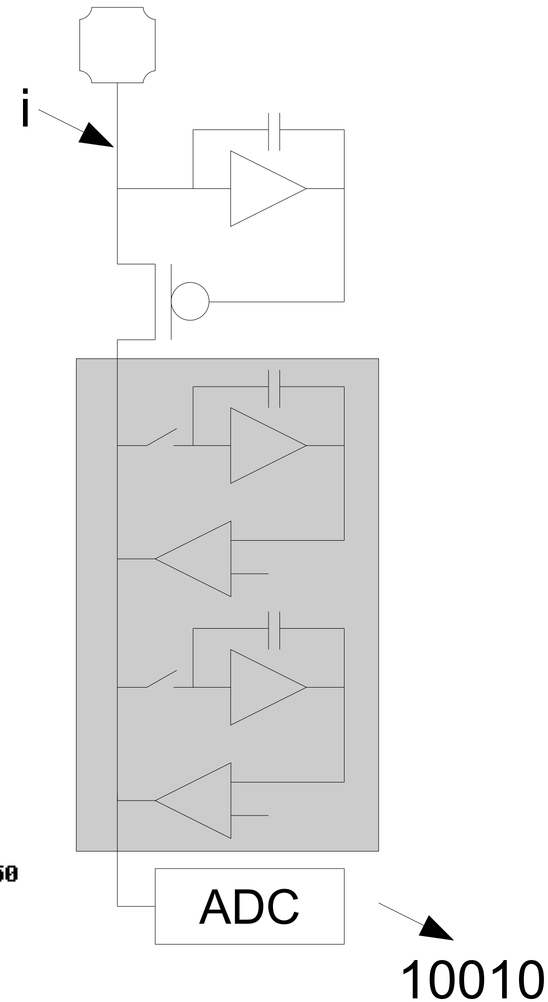
(sig+ped)-ped
ped-(sig+ped)

ADC output

300
250
200
150
100
50
0

0 50 100 150 200 250 300 350

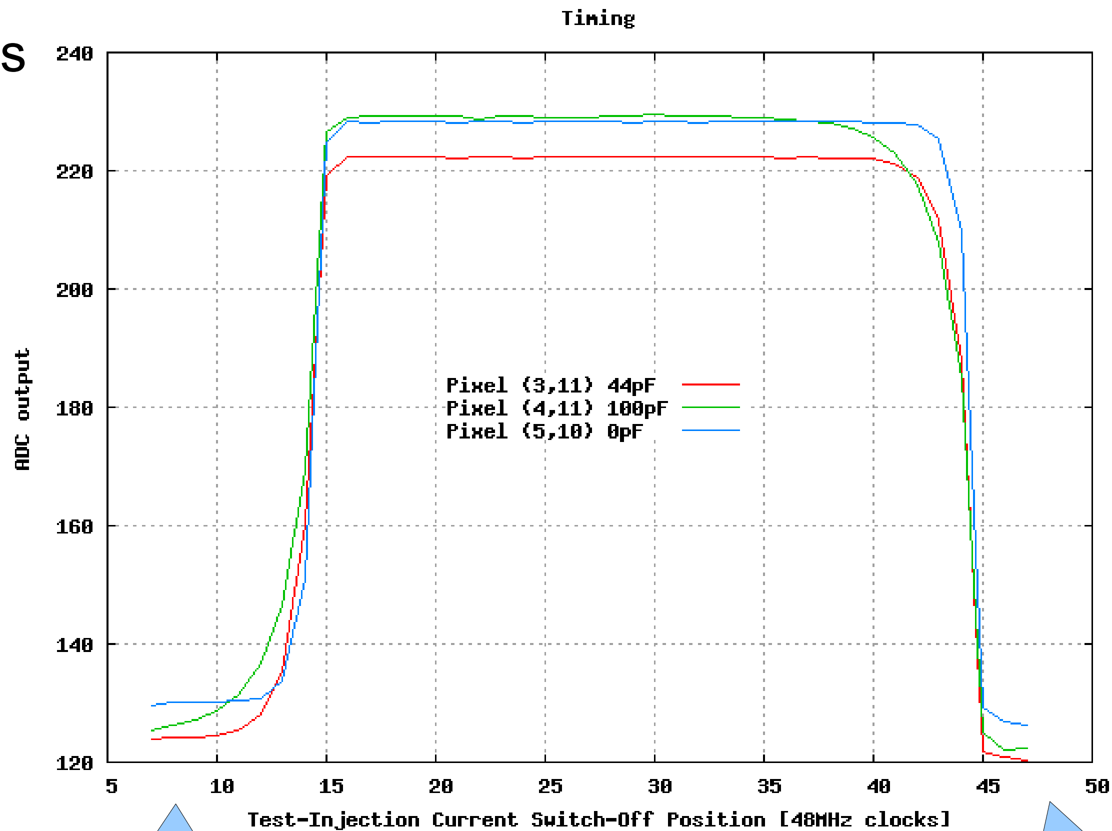
Test-Injection Current [DAC counts]




- substraction working
- design flaw: shifting current substracted as pedestal
  - only half ADC range available

# Current Sampling Speed: First Look

- 44pF: ~ 60ns



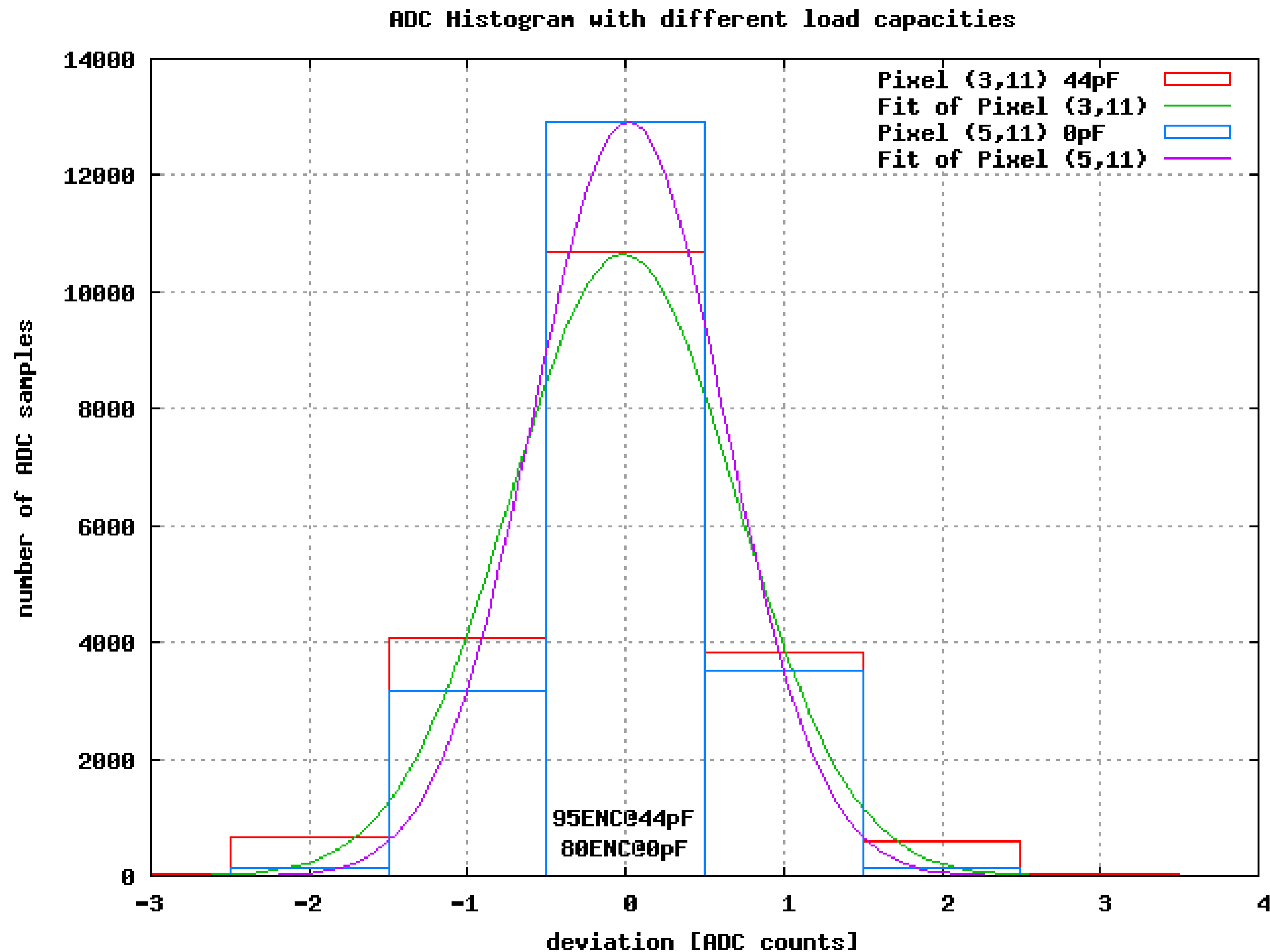

sampling
inject

sig+ped ped

sig+ped ped

sig+ped ped

# Noise




- ENC=95e$^-$ (47nA) for 44pF capacitor

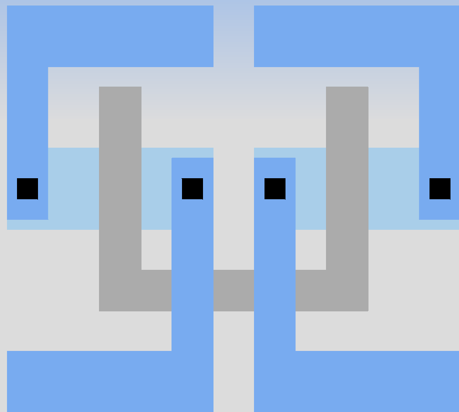
# High Speed

- DCD 600MHz clock input divided by 6 for ADC control -> 100MHz
- PCB not designed for high speed -> 48MHz max
- DCD debug mode: clock ADC control externally
  - ADC control runs currently at 48MHz
- High Speed Board is available at Uni-Bonn to run DCD with >600MHz
  - tests start soon

# Summary + Next Steps

- Summary
  - Chip working at half of the desired speed right now
  - all digital parts working
  - Regulated Cascode for up to 17µA with only 4mV
  - Current memory cells can store in range -9µA..9µA
  - ADC
    - full range ok
    - runs currently with half of possible speed
- Next Steps
  - Run DCD2 at 600MHz
  - Run DCD2 with DEPFET-Matrix and Switcher3
  - fix current shifting to digitize full range when in double sampling mode
  - submit full size chip
  - irradiation

# Bump Bonding Status




Christian Kreidl

christian.kreidl@ziti.uni-heidelberg.de

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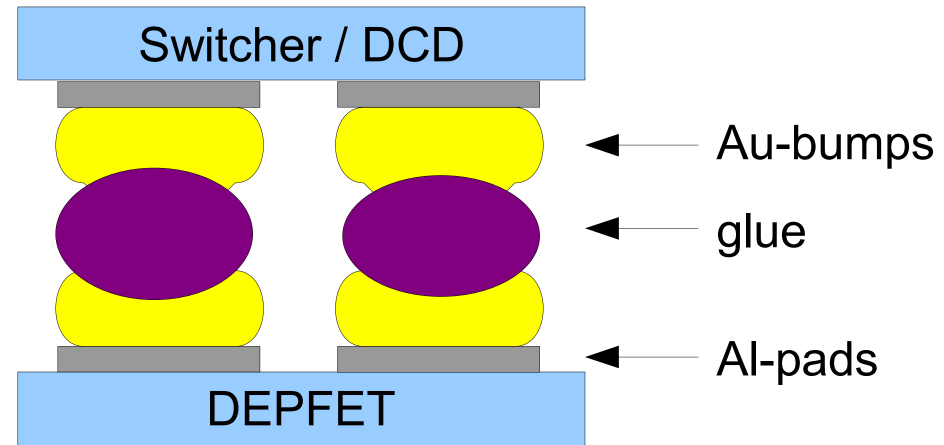
# Interconnect Technology

- 60µm bump-pad diameter
- 100µm pad pitch
- added material:

  4,5µm equivalent Si thickness

  across active area



SuS@Uni-Mannheim:

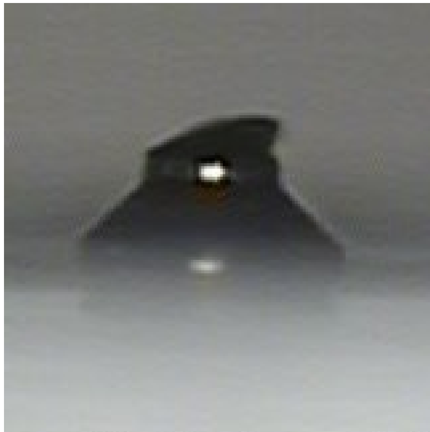
SuS@Uni-Mannheim:

smashed ball, 48µm free-air-ball, 17,5µm wire

65µm smashed
25µm wire

# New Bonder

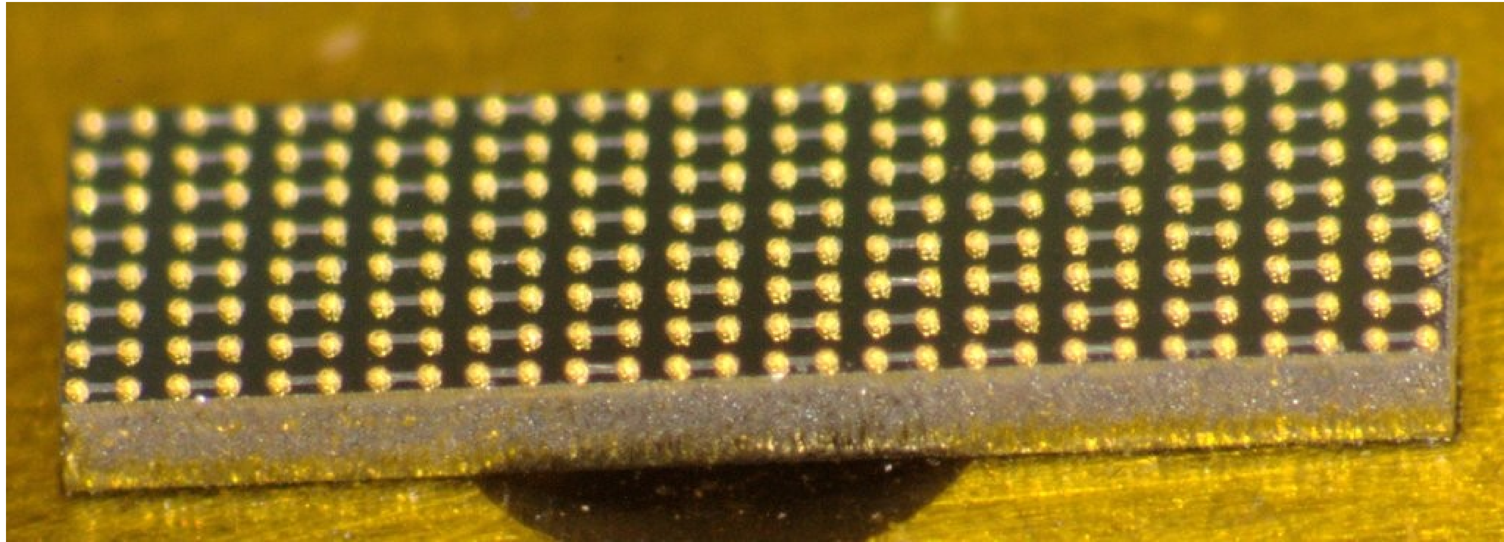
- half-automatic machine
  - manual placing and aligning of chip (3min)
  - automatic bondprocess (9min/160bumps)
- full size Switcher3 and DCD2 chips:
  - single die mounting on bonder works
  - programmed bumping works
- wire is sheared off



1 bump

2 stacked bumps

# bumped chip



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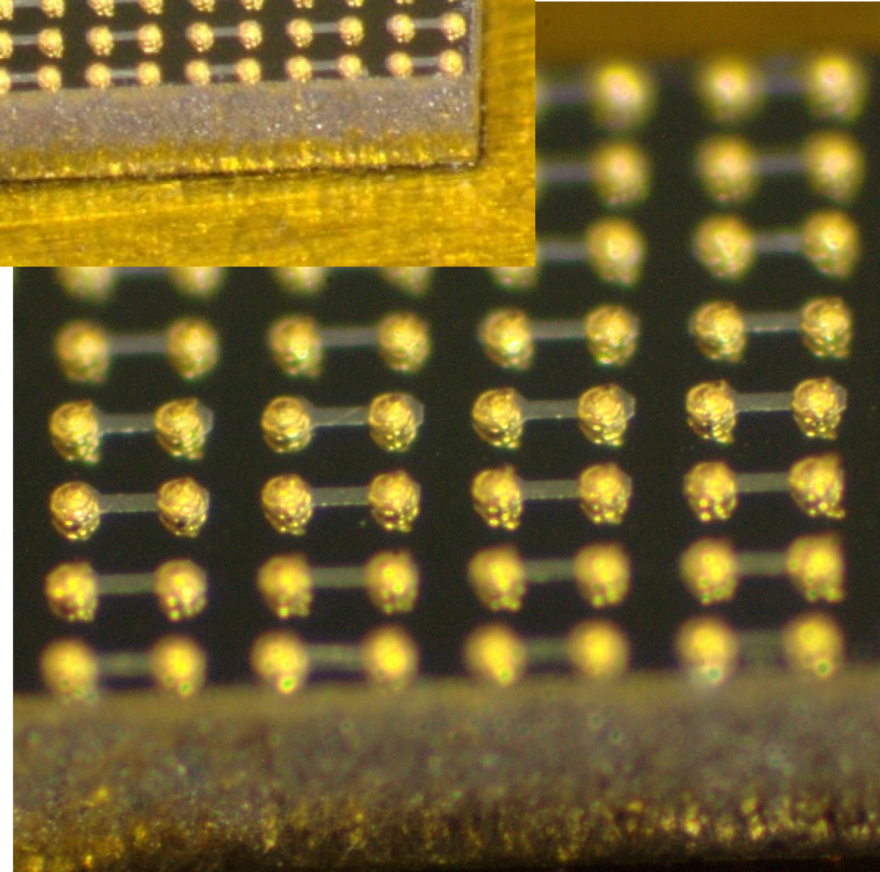
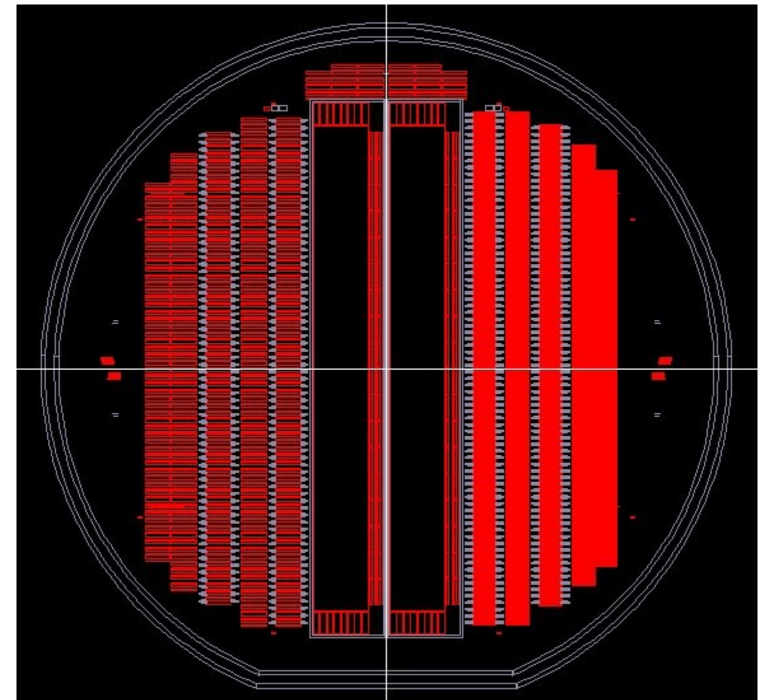


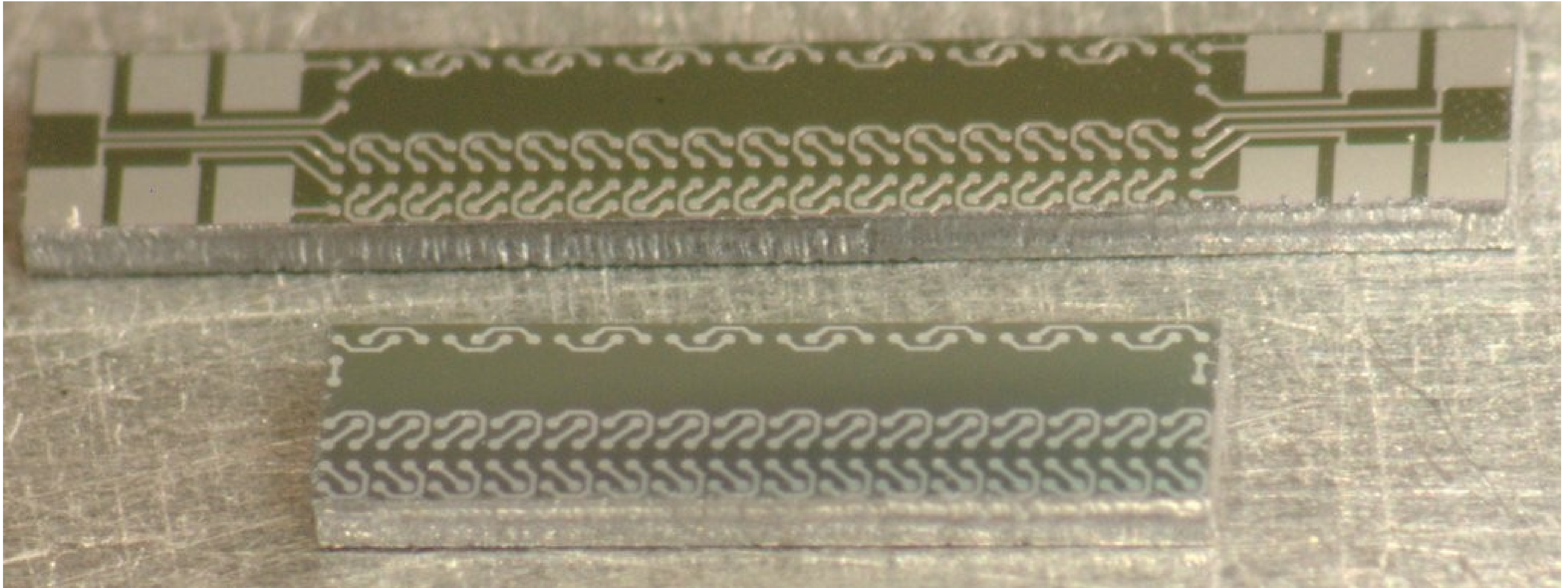
DCD dummy chip with 224 bumps

# Dummy Chips

- several wafers with dummy chips available
- manufactured in HLL, Munich (DEPFET process)
- snake structures for interconnect testing
- 130 full size Switcher3 chip-substrate pairs
- 150 full size DCD pairs
- 2 full size ILC dummy modules
- silicon chips with Al pads
- one metal layer

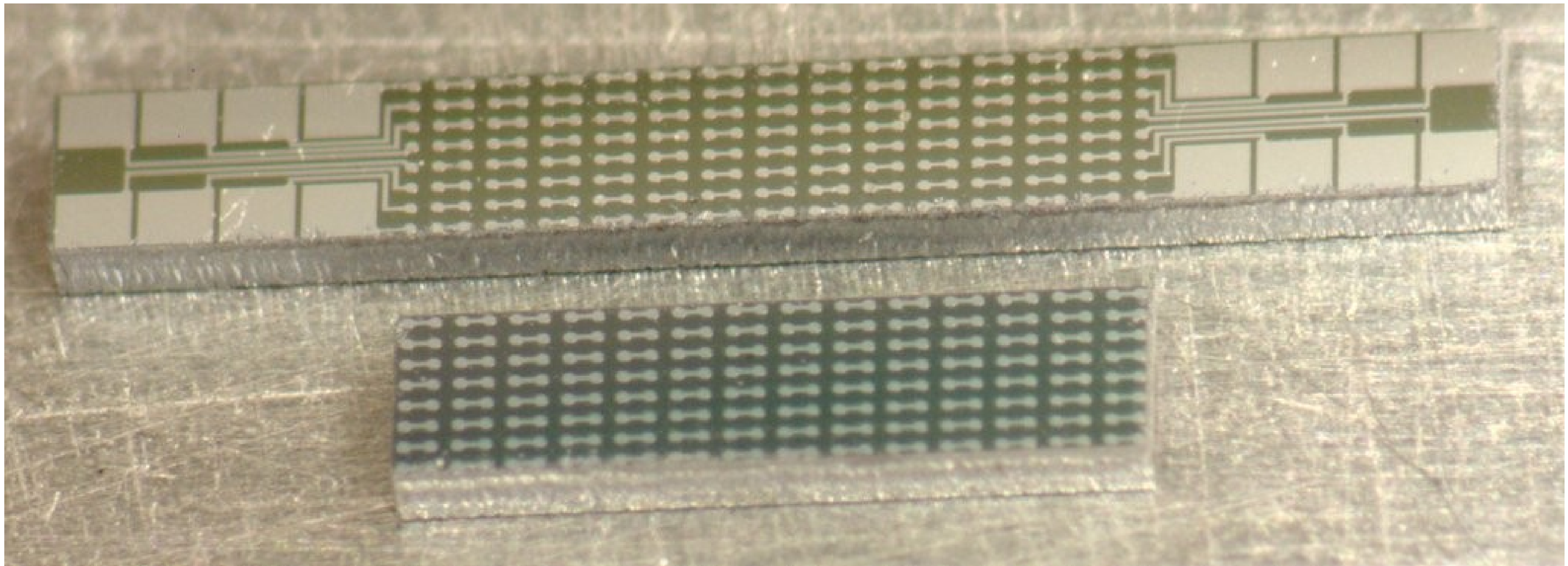


# Switcher3 dummy




Switcher3 dummy chip and substrate
164 pads

# DCD dummy



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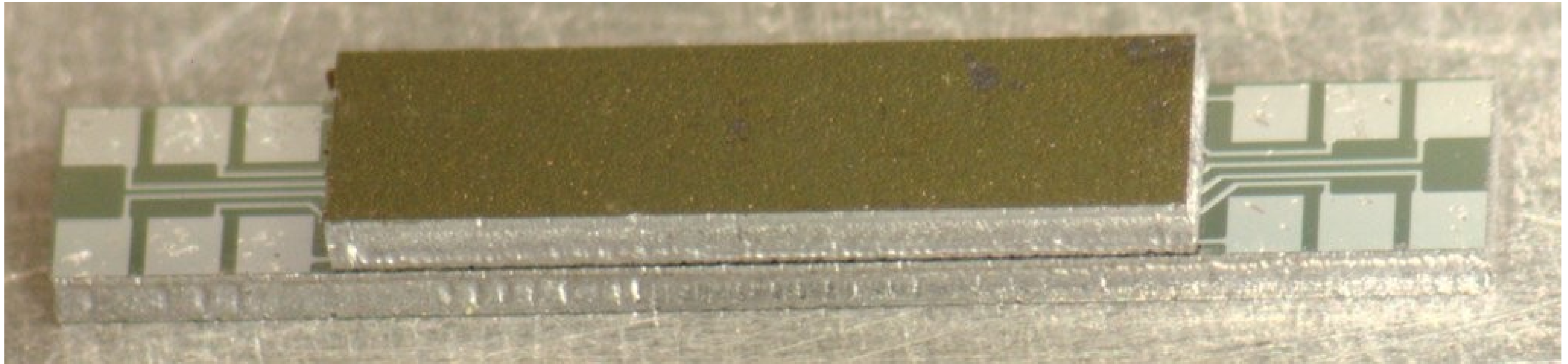
DCD dummy chip and substrate
224 pads

# ILC Dummy

- full size ILC module (mechanical demonstrator)
- 16 DCD
- 36 Switcher3
- 9488 bump-bonds
- 11,9cmx1,6cm

# Dummy Chip Flipping

- flipped Switcher3 and DCD dummies
- all bumps connected
- no shorts
- R of traces > R of bump bonds



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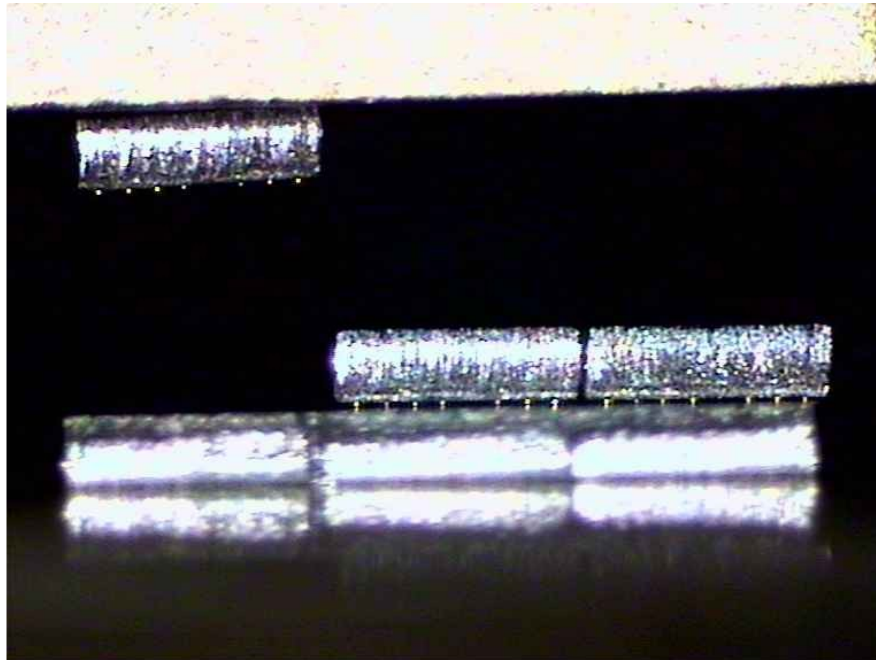
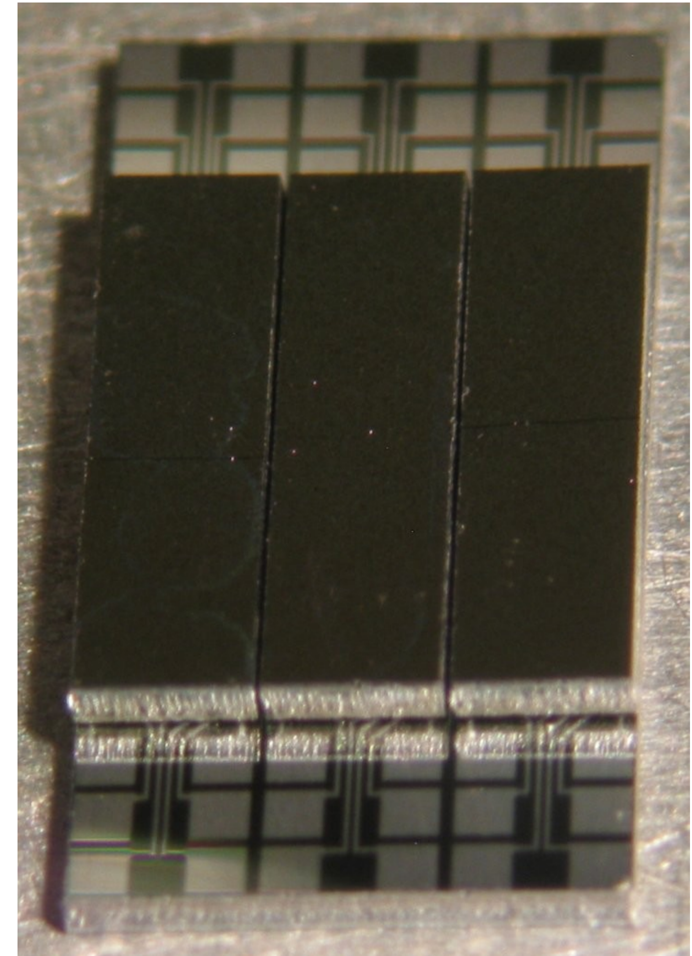
flipped Switcher3 dummy

# Triple Dummies

- to learn how to flip low chip-pitch
- chips broke due to non-flat bond head
- but flipping pitch is possible





# Next steps

- flip some more chips
- flip on tripple substrate
- create ILC module with Switchers and DCDs

# Thank you for your attention!