The ILC DEPFET prototype: Report of the Test Beam at CERN 2008

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Outline

Introduction

- The DEPFET principle
- ILC prototype system

CERN Test Beam

- Test Beam set-up
- EUDET & DEPFET
- Measurement program
- Preliminary results

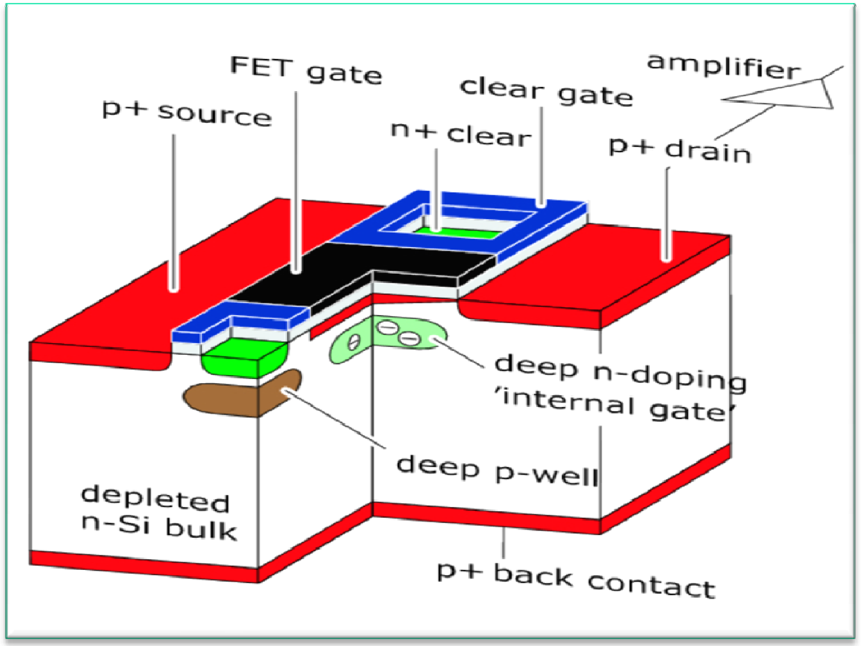
Summary

- Conclusions

The DEPFET principle

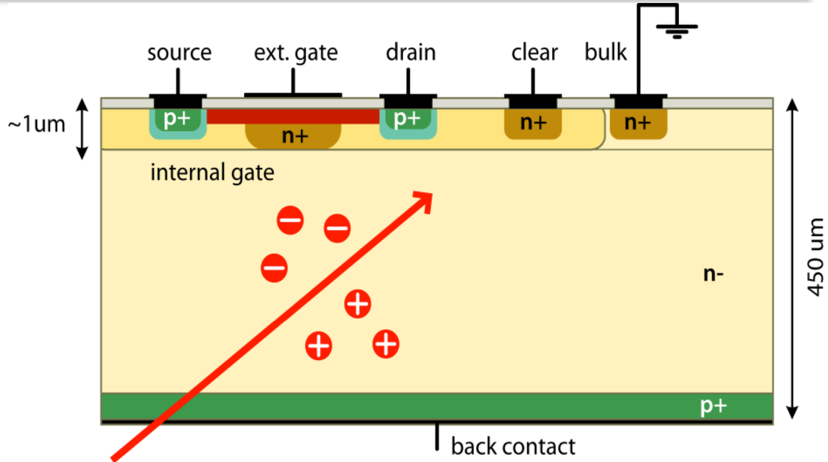
- Each pixel is a p-channel FET on a completely depleted bulk (sideward depletion). Charge is collected by drift
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)

- Signal electrons accumulate in the internal gate and modulate the transistor current ($g_q \approx 300pA/e^-$)
- Accumulated charge can be removed by a clear contact



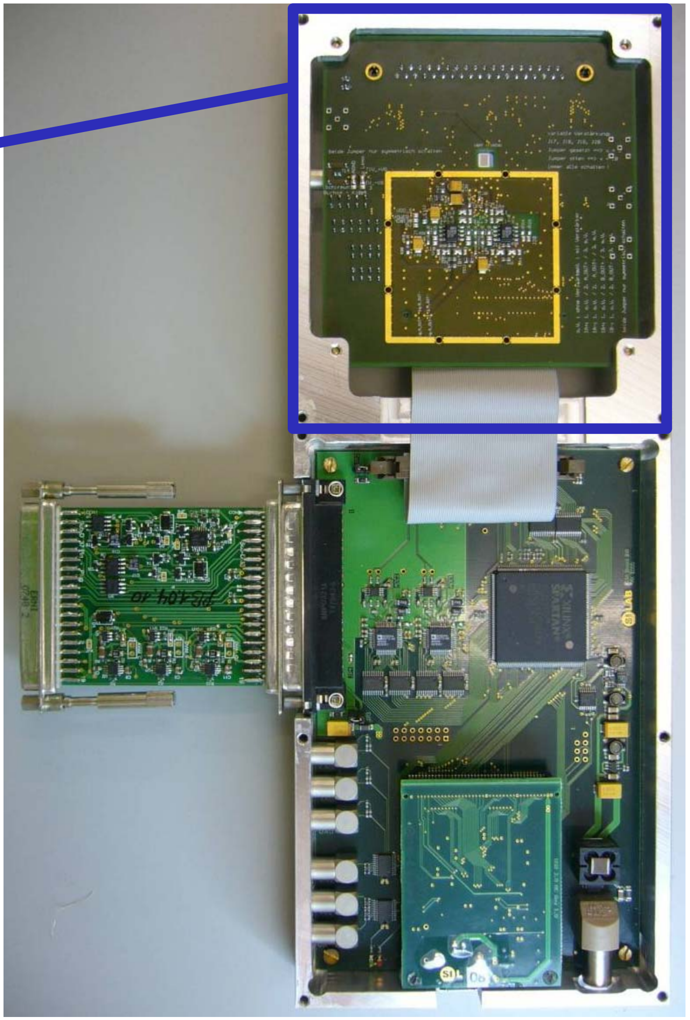
GOAL

- o Small pixel size ~25µm
- o r/o per row ~50ns (drain)→Fully depleted bulk
- o Noise≈100e⁻→Small capacitance and first in-pixel amplification
- o Thin Detectors≈50µm



ILC prototype system

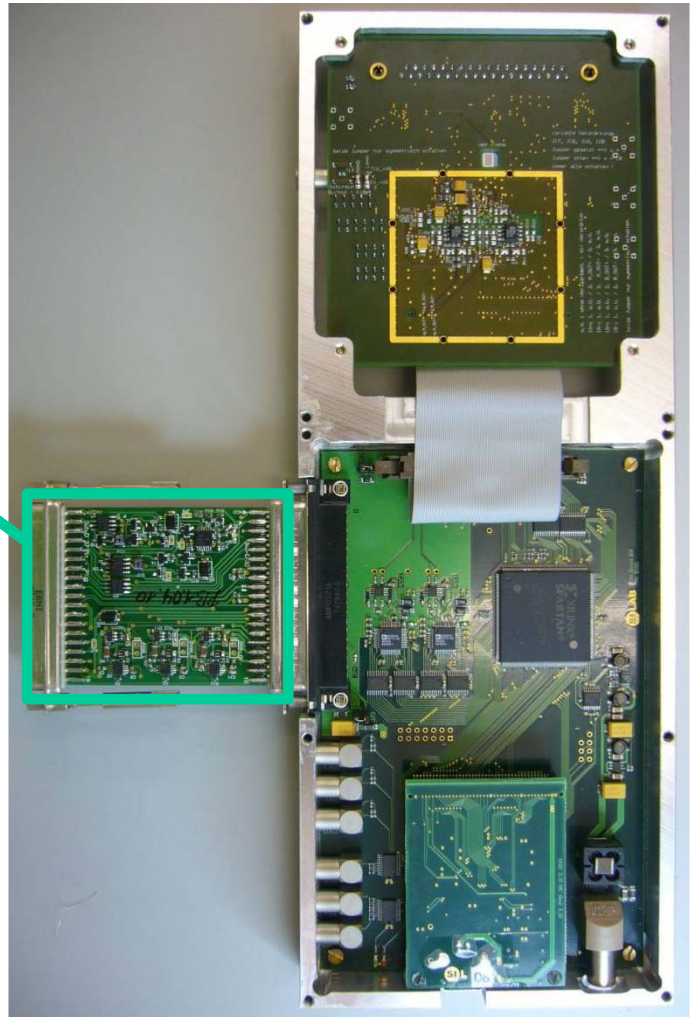
- Hybrid Board
  - DEPFET 64x128 matrix
  - Readout chip (CURO)
  - Steering chips (Switchers)



ILC prototype system

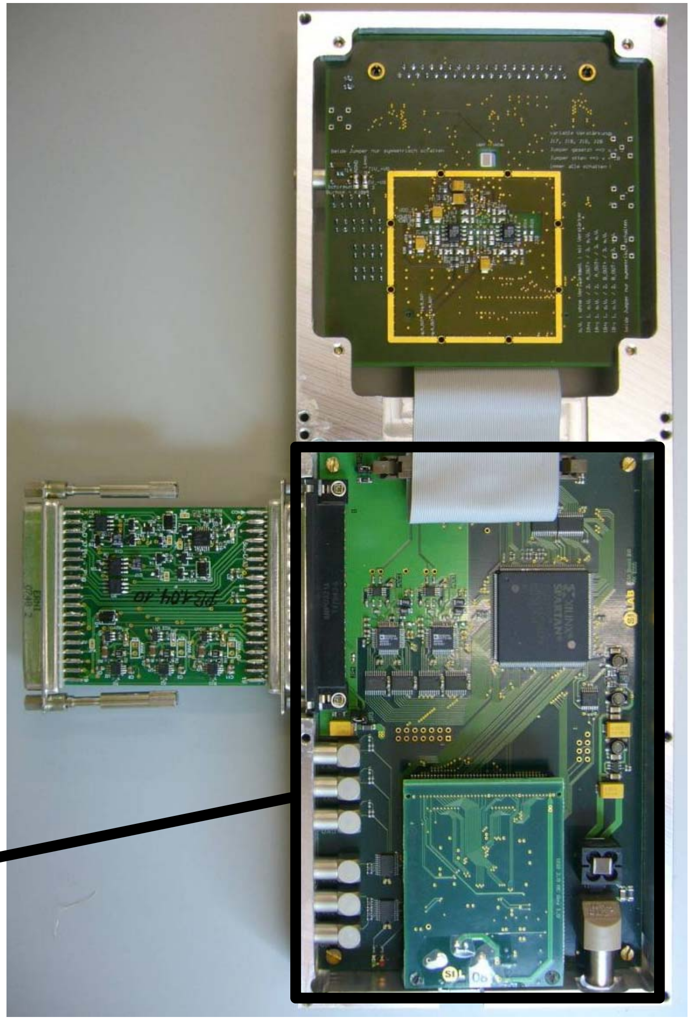
- **Hybrid Board**
  - DEPFET 64x128 matrix
  - Readout chip (CURO)
  - Steering chips (Switchers)

- **Protection Board**
  - Regulators→Saveguard the power supply voltages
  - Over voltage protection

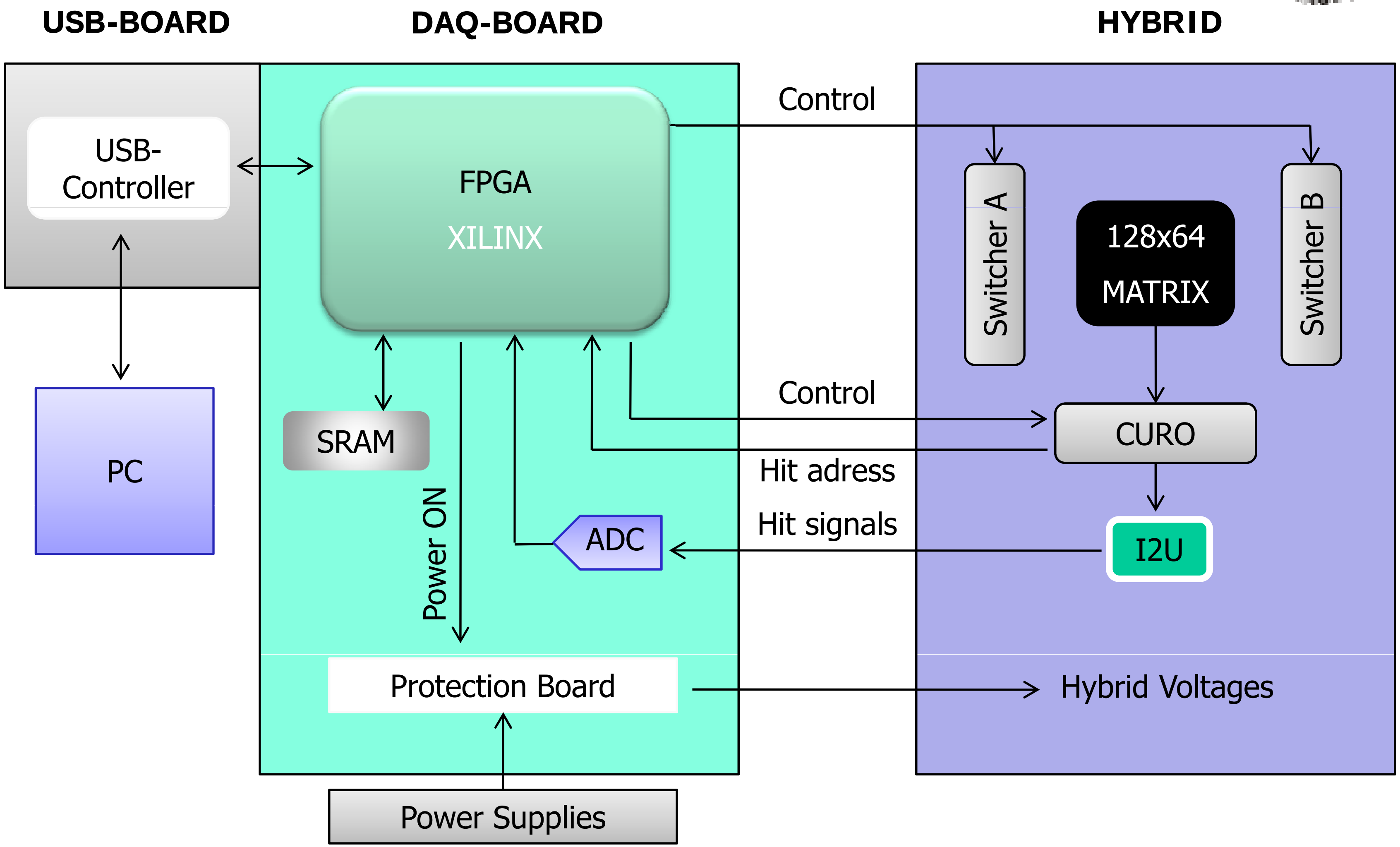


ILC prototype system

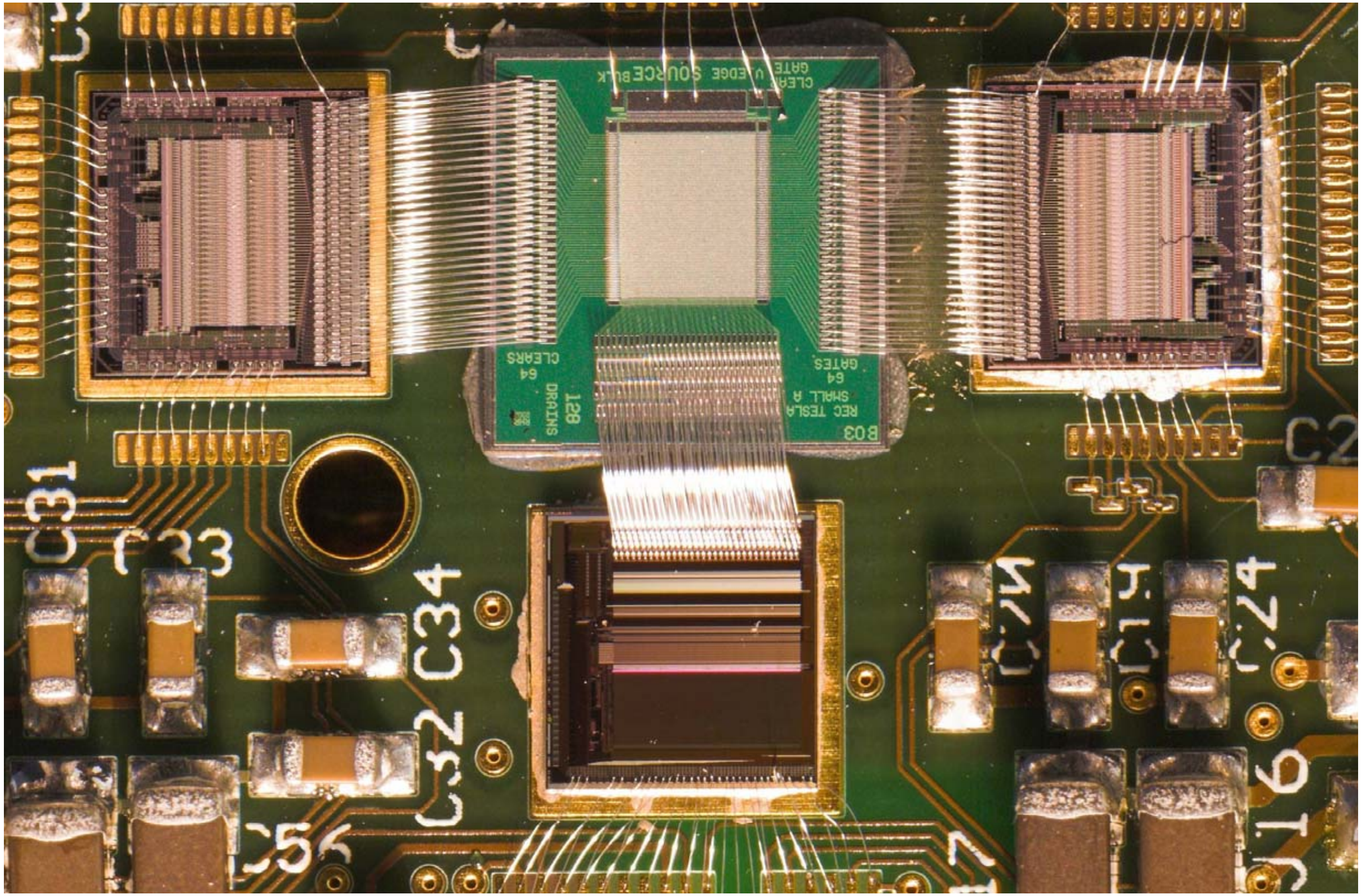
- **Hybrid Board**
  - DEPFET 64x128 matrix
  - Readout chip (CURO)
  - Steering chips (Switchers)
- **Protection Board**
  - Regulators
- **Readout Board**
  - 16 bit ADCs→Digitization
  - XILINX FPGA→Chip config. and synchronization during DAQ
  - 128 kB RAM→Data storage
  - USB 2.0 board→PC comm.



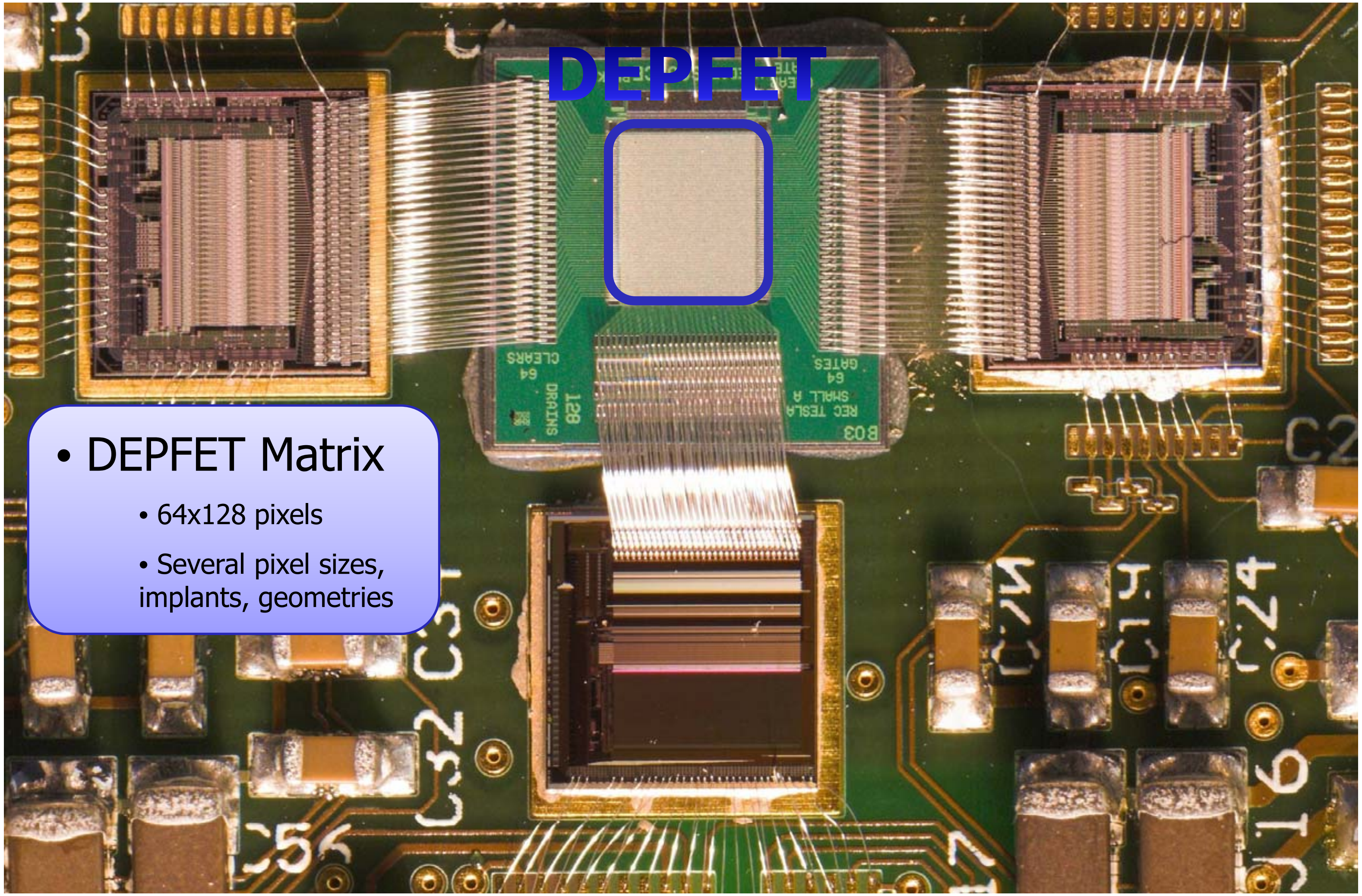
Schematic of the ILC DEPFET pixel system



Hybrid board

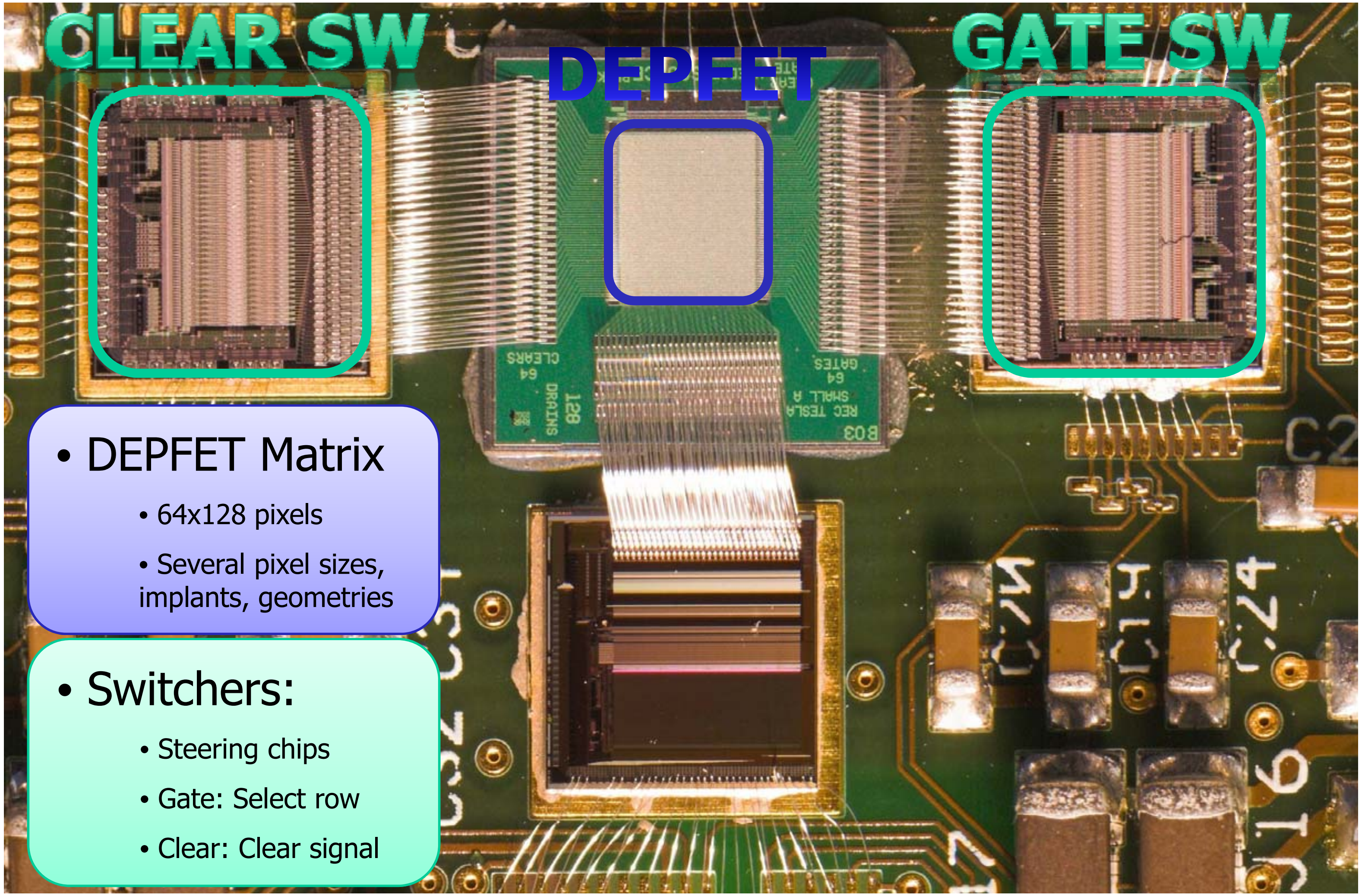


Hybrid board



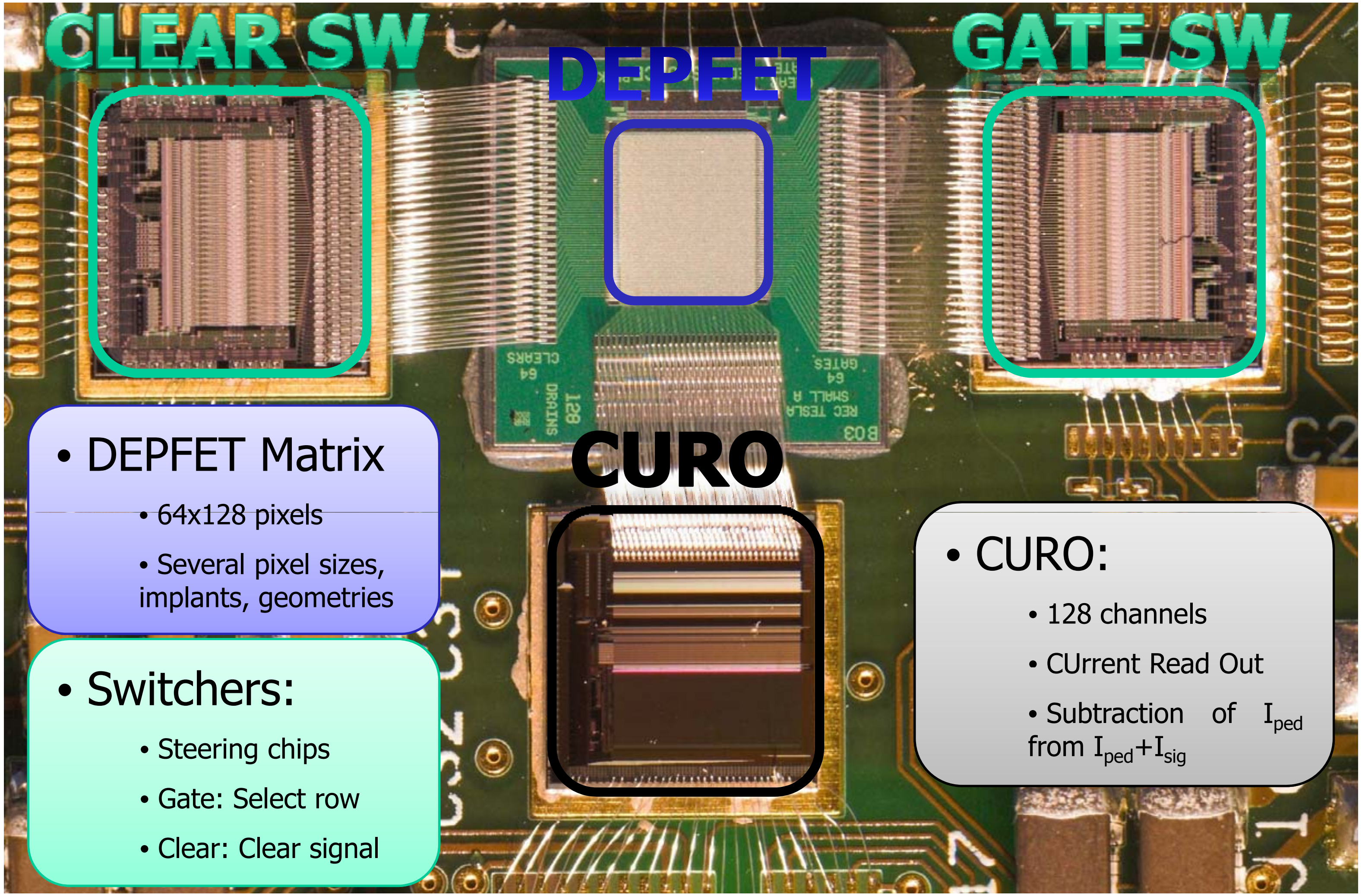
- DEPFET Matrix
  - 64x128 pixels
  - Several pixel sizes, implants, geometries

Hybrid board



- **DEPFET Matrix**
  - 64x128 pixels
  - Several pixel sizes, implants, geometries
- **Switchers:**
  - Steering chips
  - Gate: Select row
  - Clear: Clear signal

Hybrid board

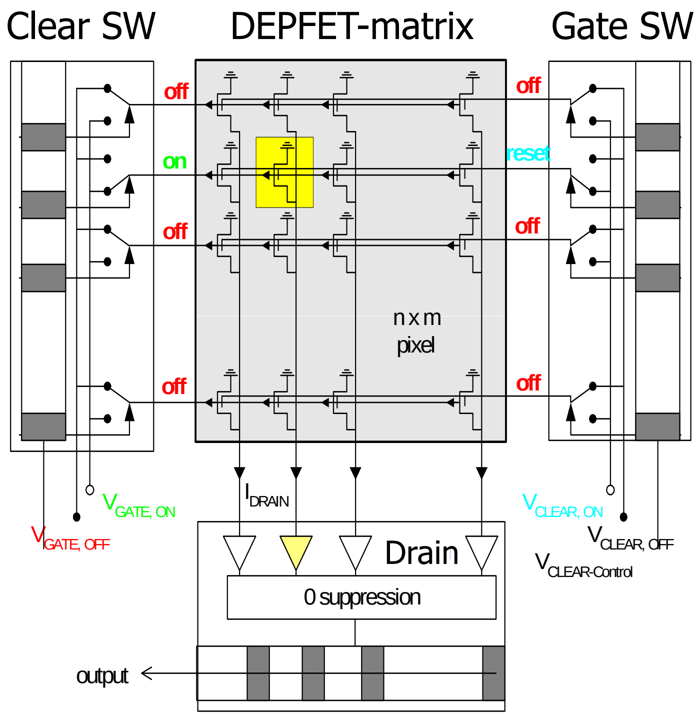


- DEPFET Matrix
  - 64x128 pixels
  - Several pixel sizes, implants, geometries

- Switchers:
  - Steering chips
  - Gate: Select row
  - Clear: Clear signal

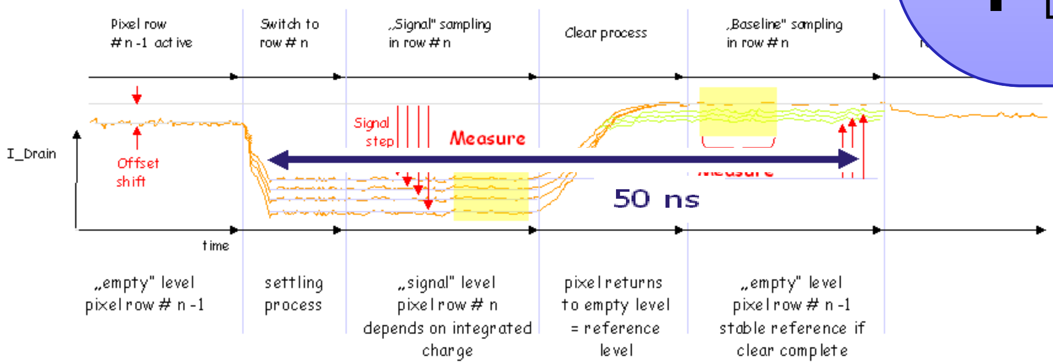
- CURO:
  - 128 channels
  - CUrrent Read Out
  - Subtraction of I_{ped} from $I_{ped}+I_{sig}$

Operation mode: Row wise readout



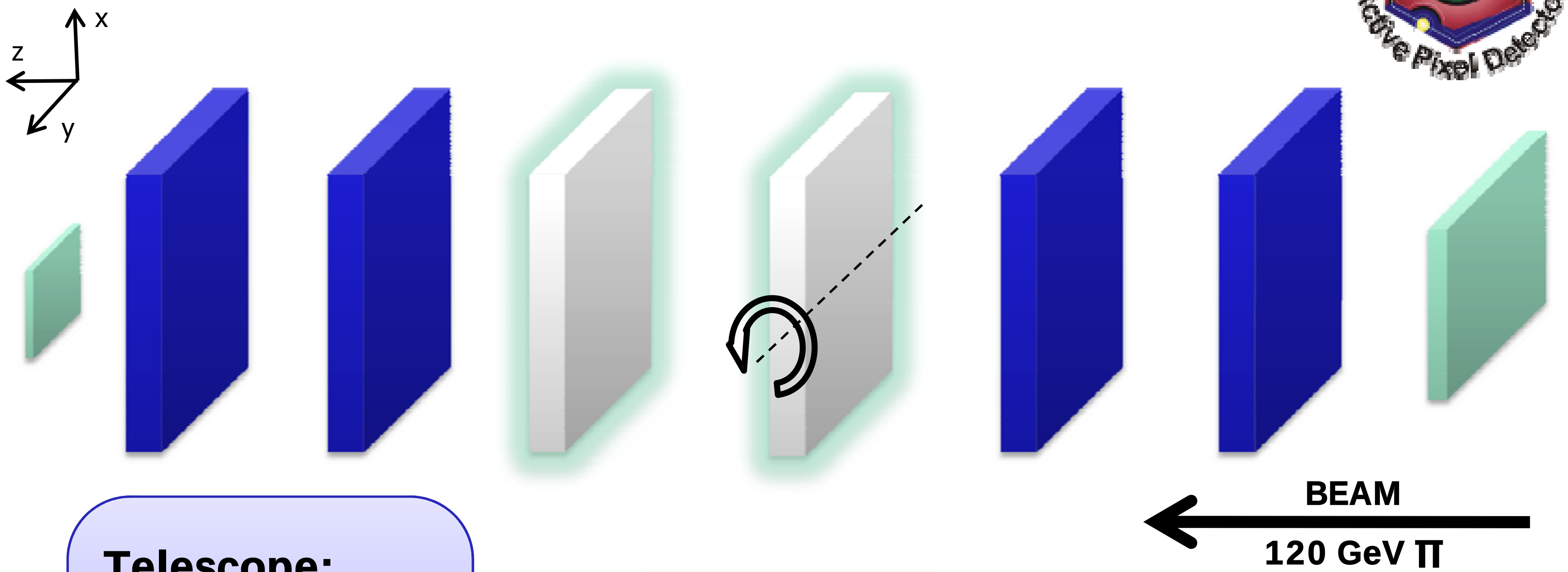
Row wise r/o (*Rolling Shutter*)

- Select row with external gate, read current, clear DEPFET, read current again → The difference is the signal
- Low power consumption: Only one row active at a time; Readout on demand (Sensitive all the time, even in OFF state)
- Two different auxiliary chips needed (Switchers)
- Limited frame rate



Enable row – Read current (I_{sig} + I_{ped}) – Clear – Read current (I_{ped}), Subtract – Move to next row

Test Beam Setup



Telescope:

- 4 DEPFET planes
- 33x24μm²
- CCG
- 450 μm thick

DUT:

- 2 DEPFET modules
- Various pixel sizes
- 450 μm thick
- 1 rotating motorstage

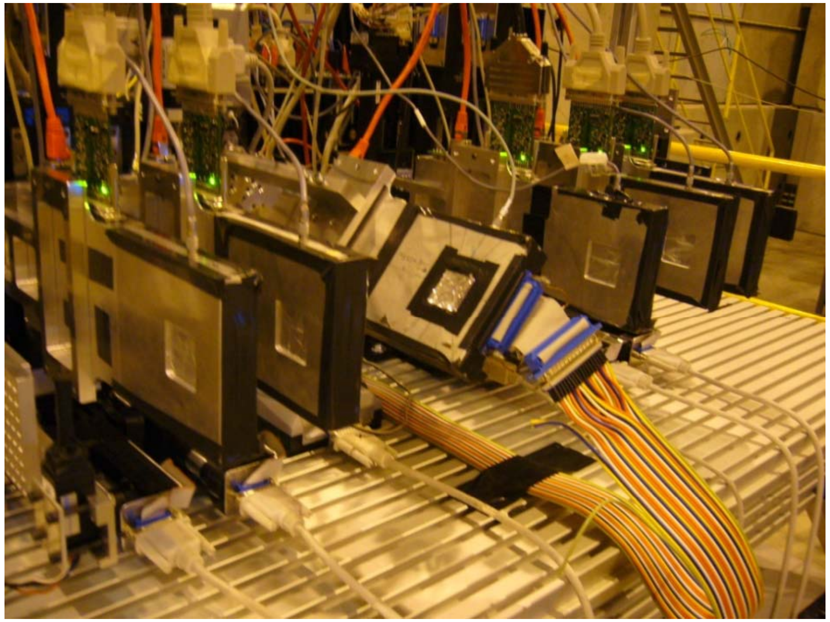
Scintillators:

- 1 Big "Beam finder"
- 1 Finger "Beam allignment"
- Triggering

Trigger Synchronization
via TLU[1] (Trigger Logic Unit)

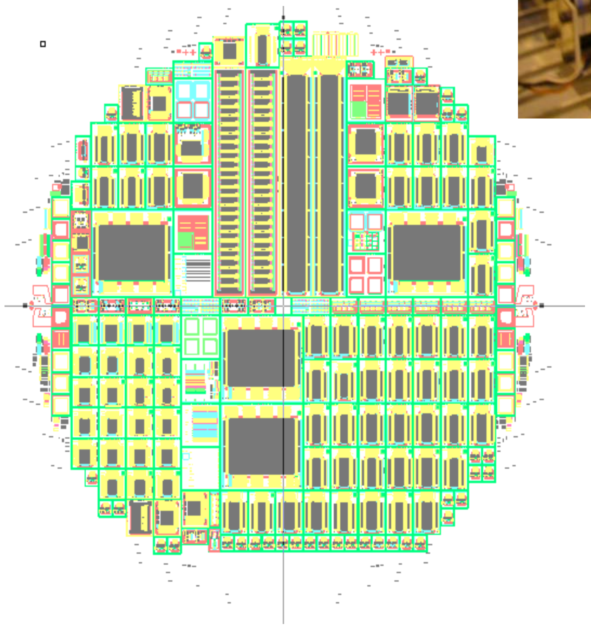
1.- D. Cussans, EUDET-Memo-2007-02

Test Beam Setup



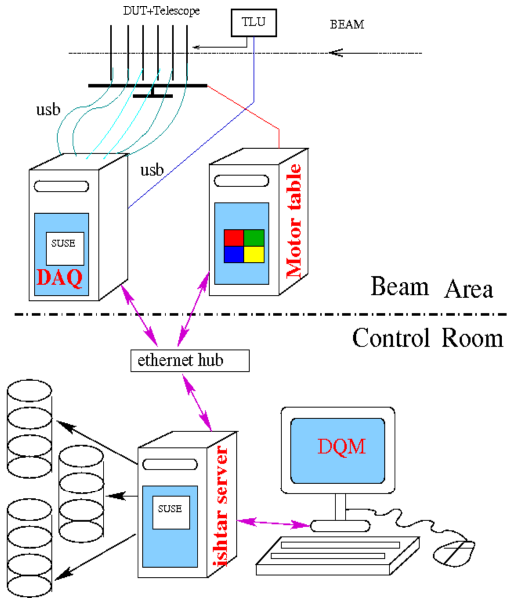
- General view
- 6 Modules at once
- 1 rotating module

Matrices distribution on the waffer



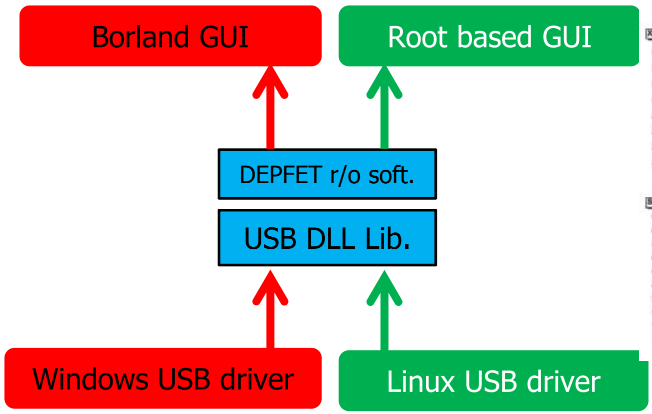
Trigger Logic Unit

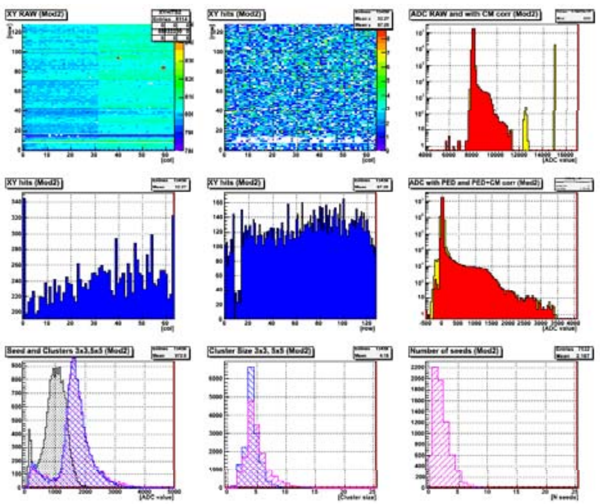
Test Beam DAQ

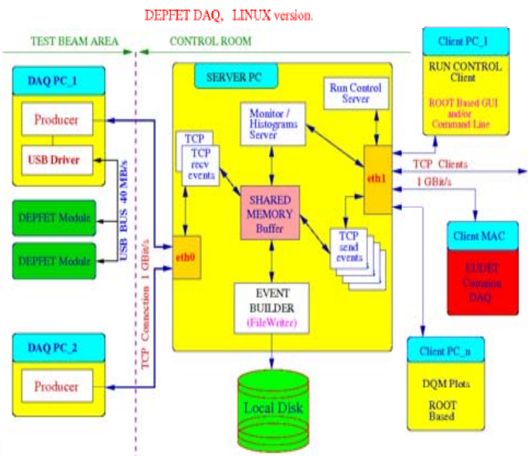


Old Windows DAQ ported to Linux:

- Network distributed system
- Remote control and monitoring
- Easy connection to common DAQ→EUDET DAQ compatible
- Only Open Source software





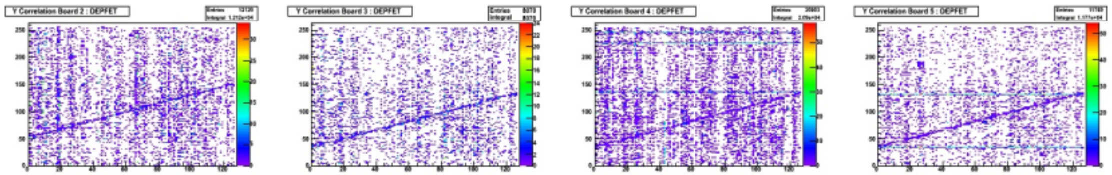


EUDET & DEPFET

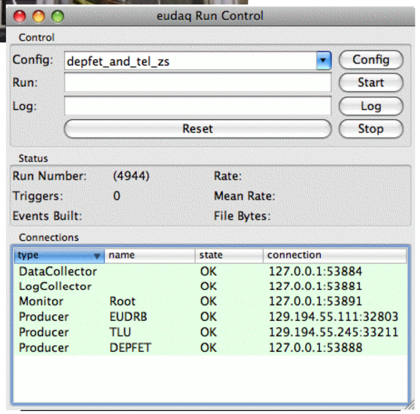
o EUDET → An EU initiative to support detector R&D for a future ILC

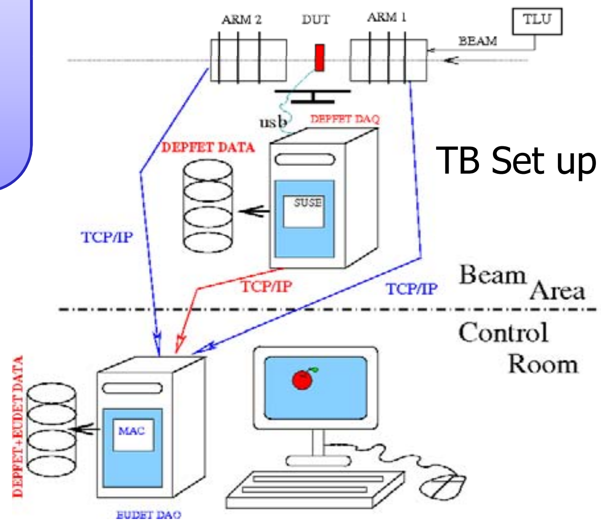
o Beam infrastructure → High resolution pixel telescope using Monolithic Active Pixel Sensors (MAPS) with 256x256 and a pitch of 30μm

o DEPFET → DUT for the EUDET Telescope in TB2008 at CERN (SPS). Significative presence in the EUDET program.



DEPFET & EUDET Correlations





TB Set up

✓ DEPFET was successfully integrated into the EUDET DQM

✓ DEPFET and EUDET Run controls were synchronized→DEPFET software was steered by the EUDET DAQ

✓ DEPFET and EUDET data was merged and stored in a common data file online, using an EUDET "DataCollector".

✓ Special "DEPFET Producer" running on EUDET DAQ responsible for synchronizing data.

✓ 1 Million of events as a DUT during this year

See the talk: **"Summary of one year operation of the EUDET CMOS pixel telescope"; Ingrid Gregor; DESY**

SPS Time Measurements: 3 weeks of data

- **Voltage scans:** Cross-check, we're running in optimal settings
  - V_{Bias} to the waffer 150-220V
  - V_{Edge}
  - $V_{ClearHigh}$
- **Angular scan:** To study resolution vs. Cluster size
  - -5, -4, -3, -2, -1.5, -1, -0.5, 0, 0.5, 1, 1.5, 2, 3, 4, 5, 6, 9, 12, 18, 36
- **Beam energy scan:** To analyse wheter the separation "multi-scattering-intrinsic resolution" is performed correctly
  - 20, 40, 60, 80, 120 GeV
- **Large statistics:**
  - Charge collection uniformity studies
  - In-pixel studies

3.5 TB of data

20 Million events

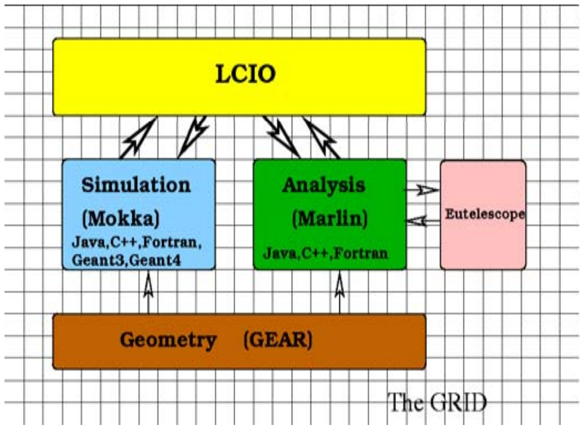
Analysis framework: ILC (EUTelescope[1]) Software

Standard analysis tools and reconstruction software used by the ILC community

EUTelescope

RAW DATA Reader/Converter	Convert DEPFET raw data to LCIO
PedestalNoiseProcessor	Pedestals and noise (adapted to DEPFET row wise com. mode correction)
ClusterFinder	Seed and neighbours cuts
ETACorrection	LCIO ETA→Center of cluster
HitMaker	From cluster to space point
Aligment	MILLEPEDE[2]→Alignment const.
TrackFit	
Analysis	

Tools used during processing chain →



1.- Bulgheroni et al, EUDET-Memo-2007-20

2.- Volker Blobel, Millepede II, desy.de/~blobel/

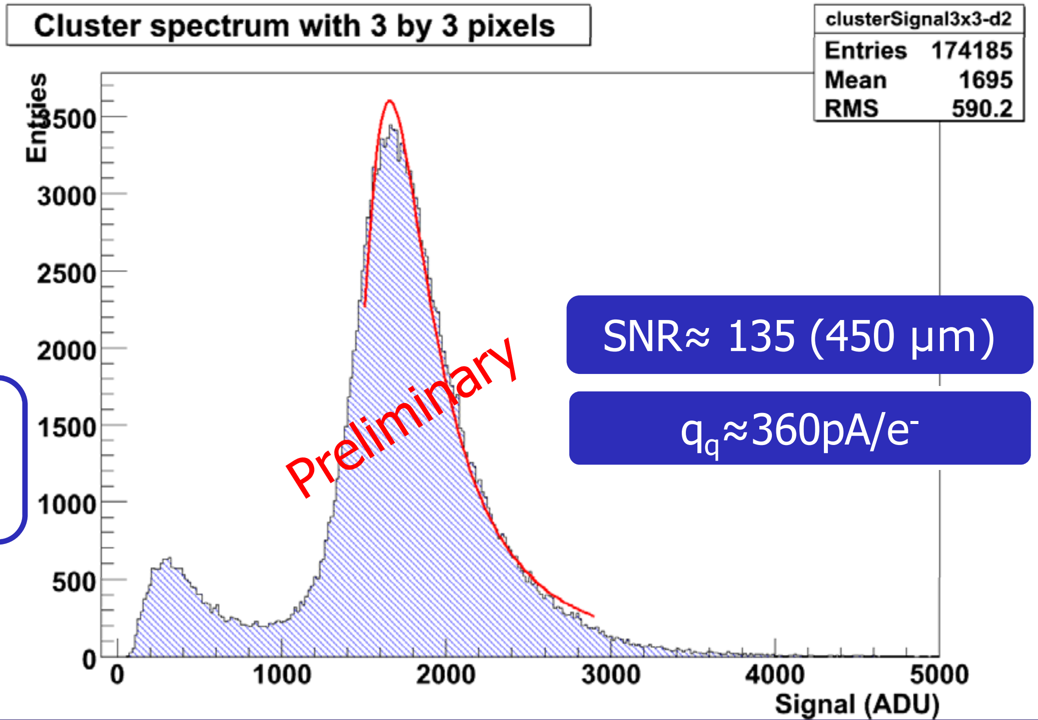
Signal clusters and SNR

- Clustering:
  - Seed: Pixel with largest signal. Requires signal >7σ (seed cut) in central area.
  - Neighbours: Pixels with signal ≥2σ in NxN region around the seed
- Noise:
  - Determined from pedestal variations after common mode substraction

Cluster size	Signal (ADU)
3x3	1710±1
5x5	1720±1

Signal is confined in 3x3 cluster

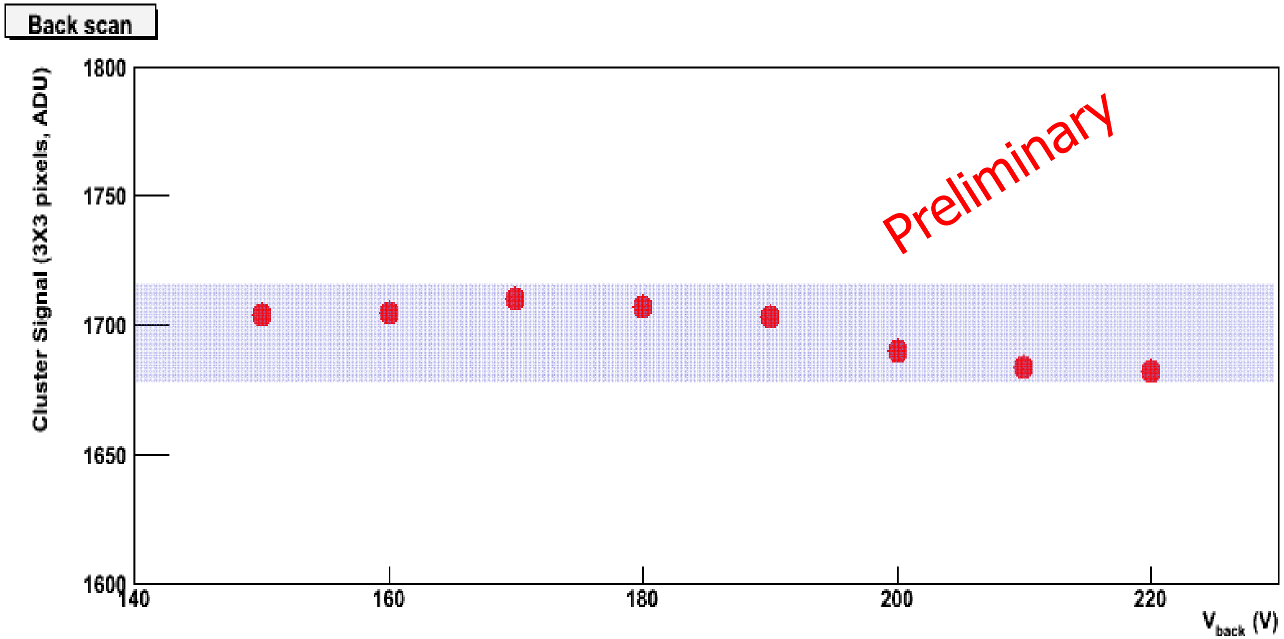
Noise≈ 12.5 ADU≈260e⁻



SNR≈ 135 (450 µm)

q_q≈360pA/e⁻

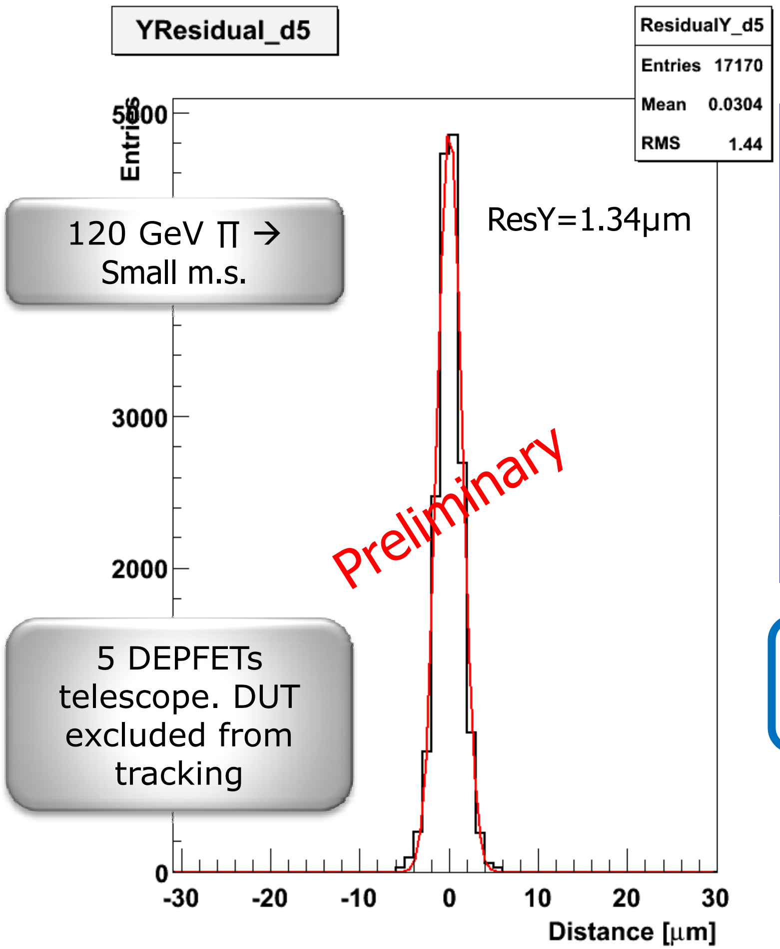
Cluster Signal vs. Bias Voltage



V_{back} (V)	Sig 3x3 (ADU)	Sig 5x5 (ADU)
-150	1704	1720
-160	1705	1717
-170	1710	1720
-180	1707	1707
-190	1703	1706
-200	1690	1691
-210	1684	1684
-220	1682	1686

- Allways working under fully depletion conditions→Charge collection plateau
- Depletion achieved at 'low' voltages ~160V

Position resolution



Module id	Pitch(µm²)	Res X(µm)	Res Y(µm)
d0	32x24	2.93	2.04
d1	32x24	2.26	1.88
d2	24x24	2.85	1.94
d3	32x24	3.34	2.01
d4	32x24	2.34	1.71
d5	32x24	2.11	1.34

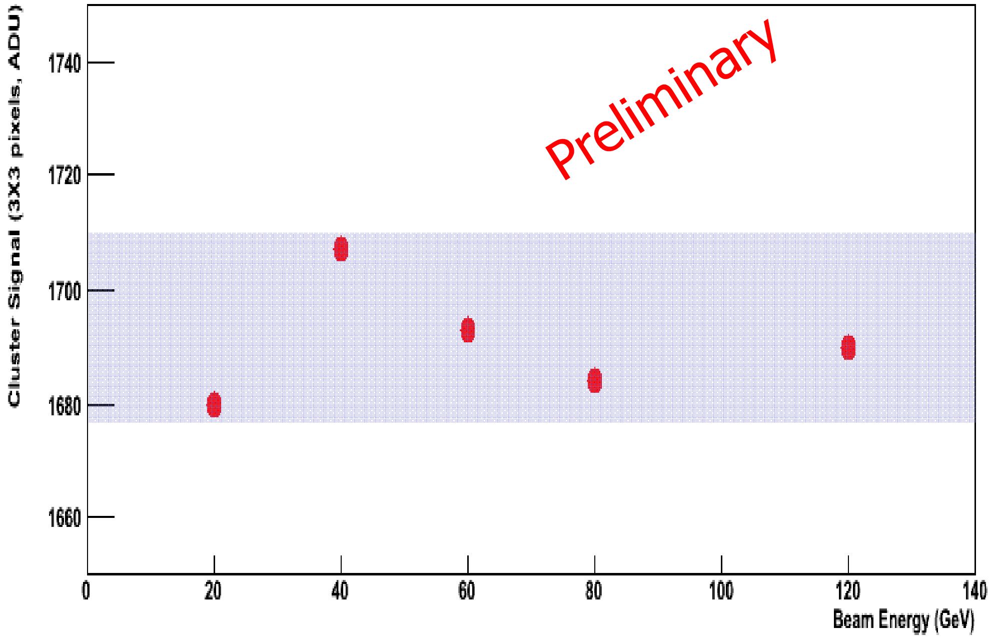
$$\sigma^2_{Total} = \sigma^2_{Telescope} + \sigma^2_{DUT} + \sigma^2_{MS}$$

This resolution includes telescope, intrinsic and multiple-scattering contributions

Residuals: Difference in position between the resulting track and the found hit

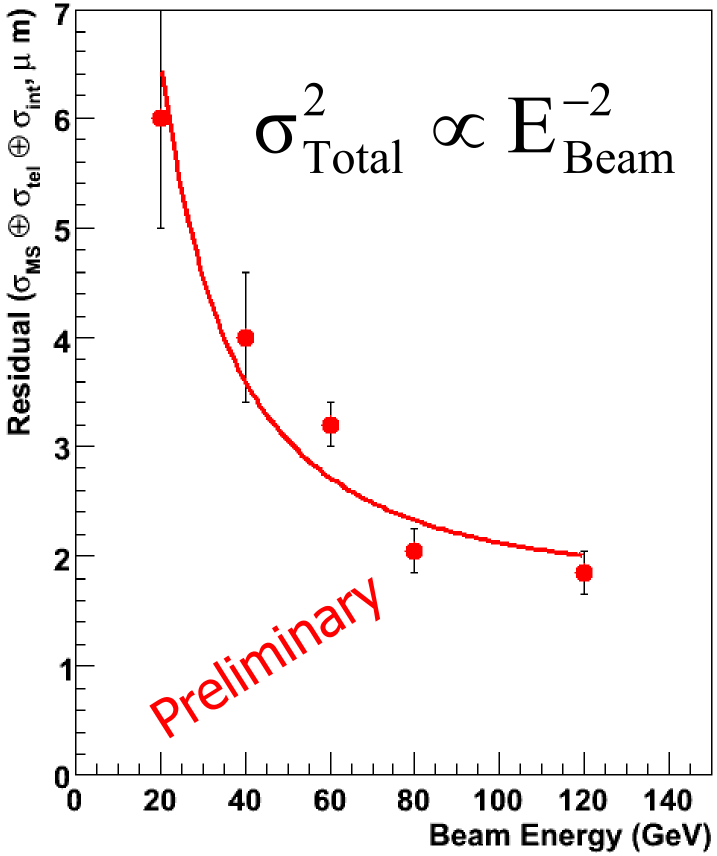
Resolution: Standard deviation of the residual distribution

Pion beam energy scan



E_{Beam} (V)	Sig 3x3 (ADU)
20	1704
40	1705
60	1710
80	1707
120	1703

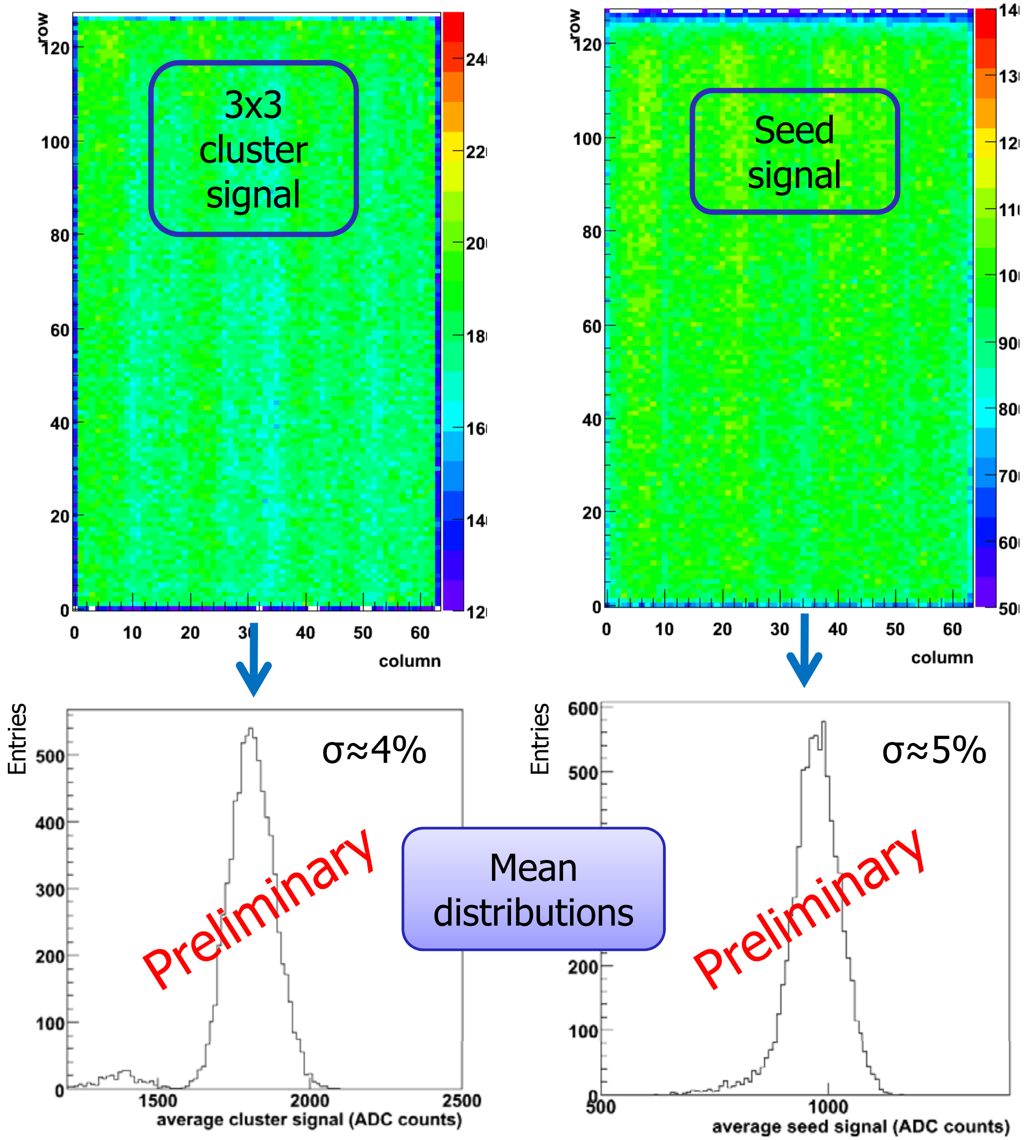
➢ No charge variation → No momentum dependence, as expected in this range![1]



Study the contribution of σ_{MS} to the σ_{Total}

1.- Hancock et al. Phys. Rev. A 28, 615-620 (1983)

Charge collection uniformity



Mean signal collected on each pixel using 400 MIP's

- Uniform charge collection over the surface of the matrix (less than 5% of variation)
- No masked pixels

Conclusions

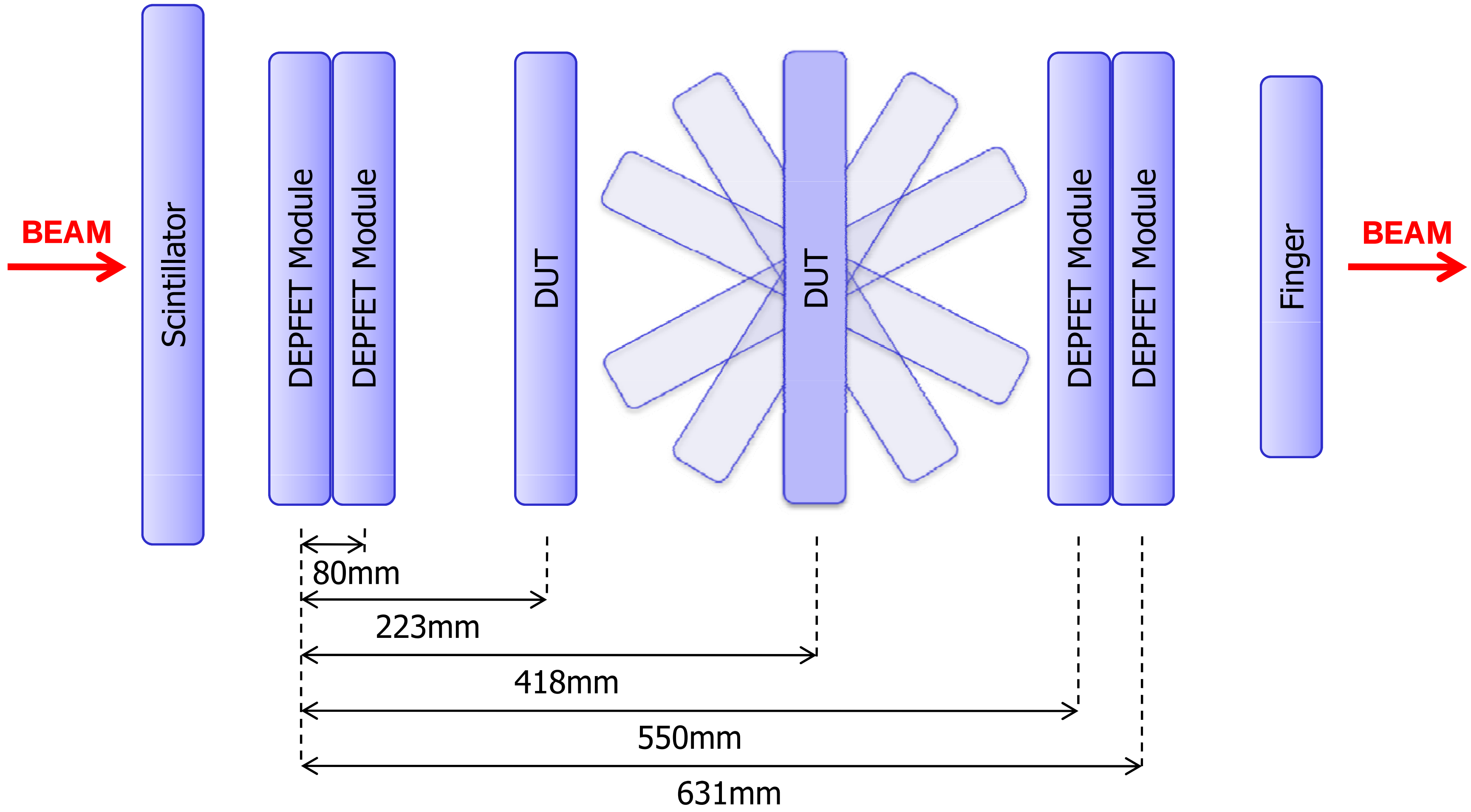
- Test Beam at CERN: Operational aspects
  - 6 DEPFET planes (64x128 pixels matrices) working at the same time on beam. 5 telescope planes and 1 DUT.
  - New functionalities and tools implemented/adapted and checked (linux DAQ and EUTelescope analysis framework).
  - Perfect integration with EUDET. Continue in the future.
  - 20 Mevents collected. Analysis in progress!

- Data analysis and processing
  - DUT (450μm thick) presents good SNR, low noise and high gain.
    - For 50μm, SNR will be smaller by a factor 9.
    - Noise factor 3 greater than desired (noisy current storage cells in CURO) → Fixed in next generation
  - Matrix working in optimal settings, cross check with lab measurements.
  - Position resolution ~2μm, including telescope, intrinsic and multiple-scattering contributions.
  - Energy scan allows to separate the m.s. resolution contribution.
  - Charge uniform over the matrix surface. No masked pixels.

Thank you very much!

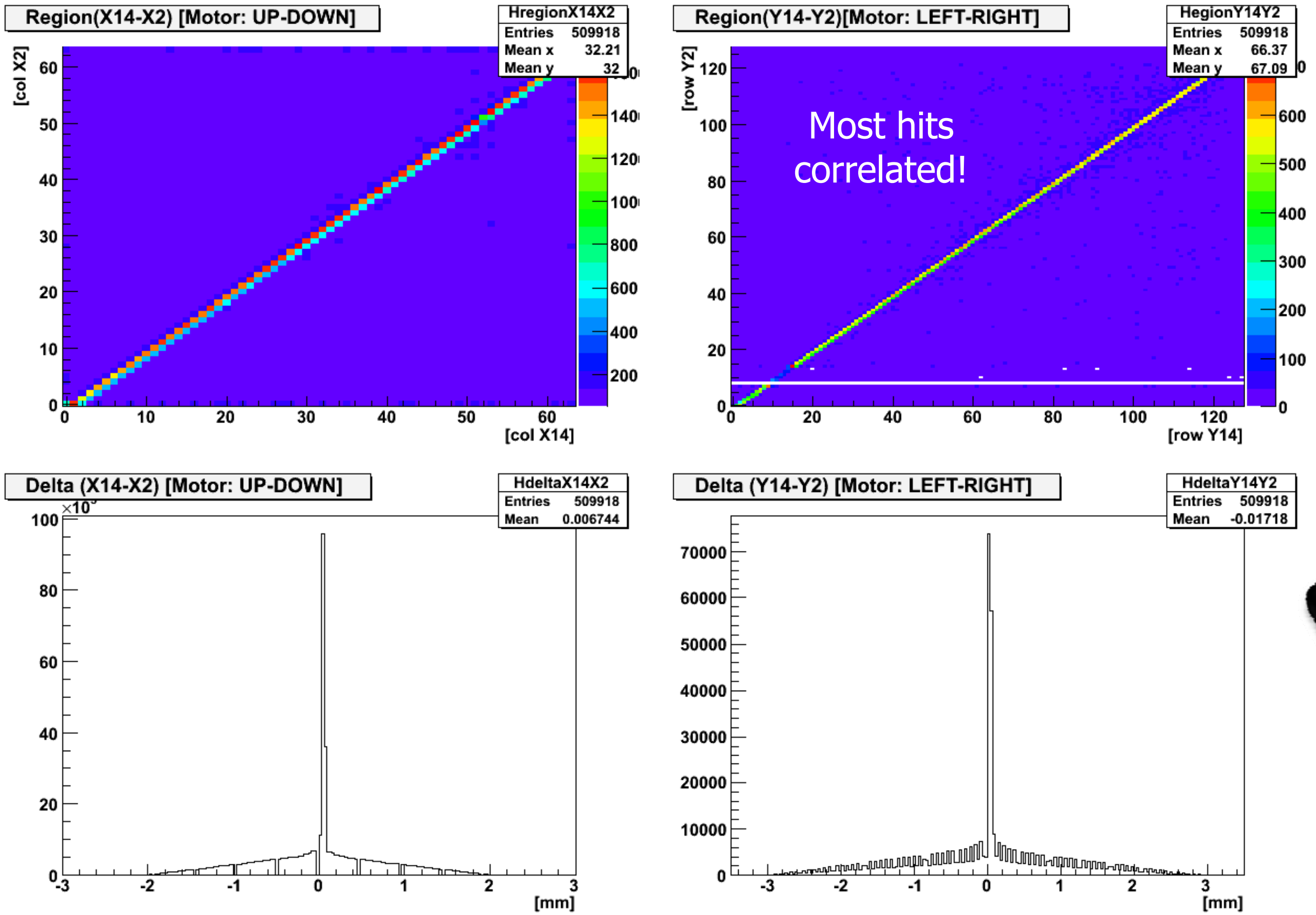
Backup slides

Test Beam Setup: Geometry



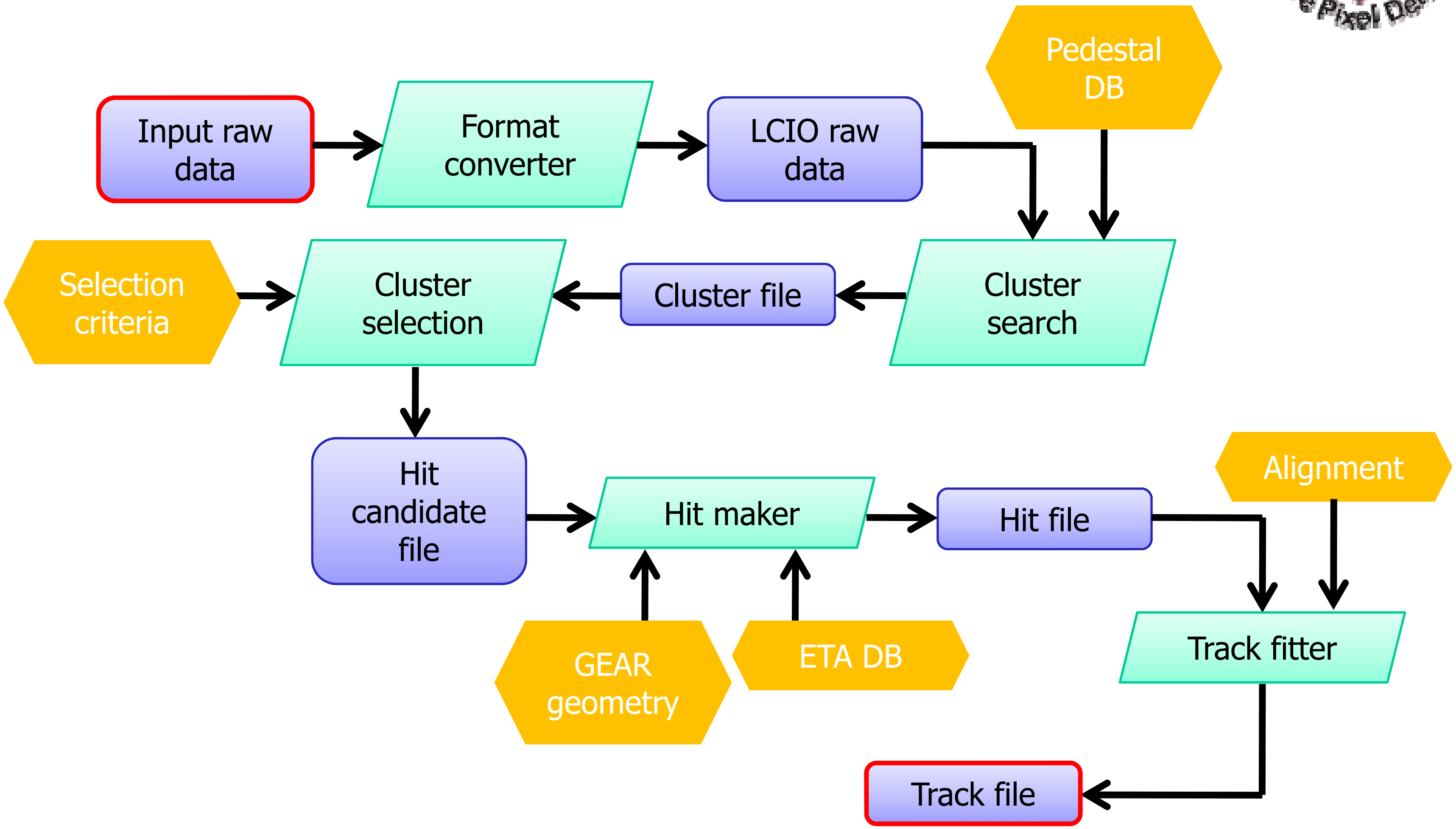
Correlation plots

X and Y hit coordinates in DEPFET plane 1 versus X and Y coordinates in plane 2

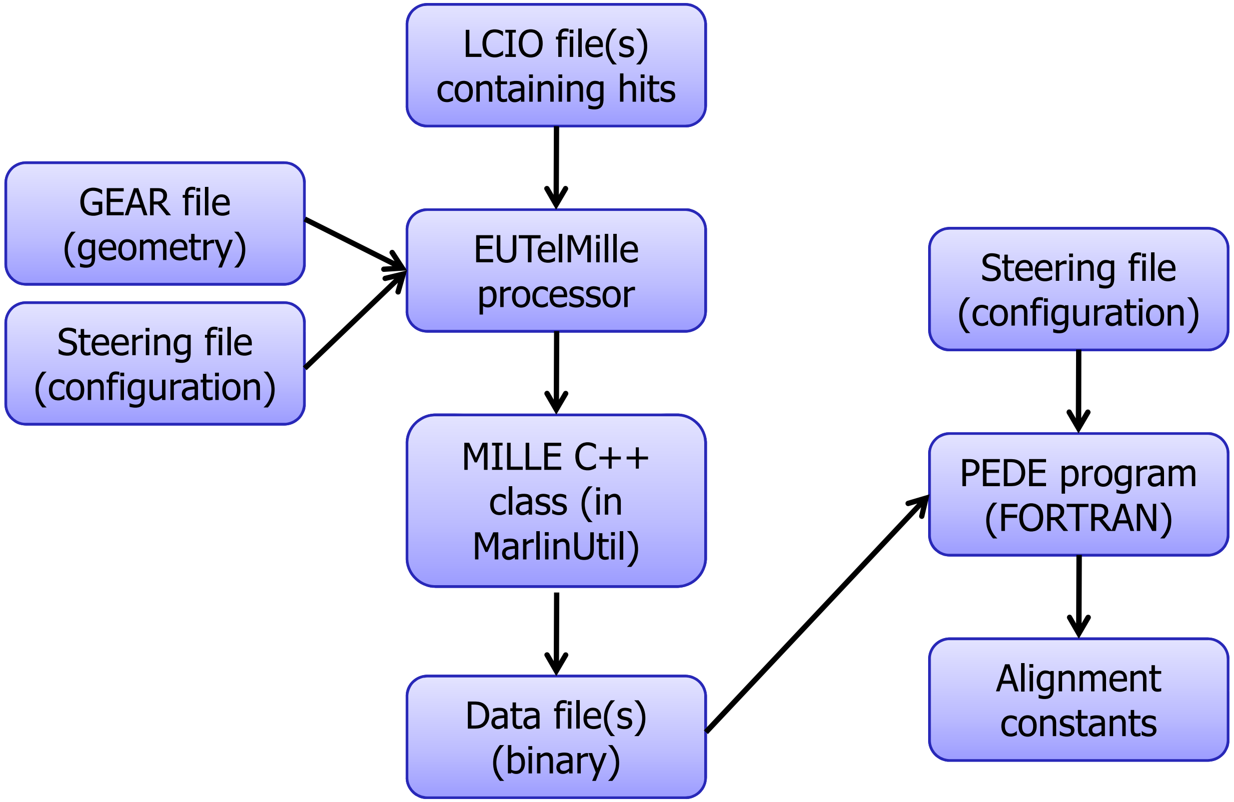


Used for pre-alignment!

Analysis framework: Overall analysis strategy



Analysis framework: MILLEPEDE II in EUTelescope



Analysis framework: ILC (EUTelescope) Software

RAW DATA Reader/Converter → Converts the native raw DEPFET format (.dat) to the LCIO (Linear Collider Input-Output) raw format, with the proper event structure and the correct event model

PedestalNoiseProcessor → Calibrate the output of each pixel detector in order to remove the constant and useless signal. Together with this pedestal value also the noise figure is estimated as the witdth of the pedestal distribution. This can be done in two different ways: Producing the pedestal and noise from a specific run or assuming a known initial value and then keep them update

ClusterFinder → Scan the matrix looking for clusters mean to look for a group of space correlated pixels all having signal above a certain threshold.

ETACorrection → Used to calculate the center of the cluster. It is used as a non linear weighting function in the charge center of mass calculation. Is an experimental approach based on the fact that the probability to find the cluster center is flat over the pixel sufrace. A certain region does not collect more cluster centers than another. The ETA correction is made in two orthogonal directions

HitMaker → This processor must convert a local cluster in the detector frame of reference to space point in the telescope frame of reference. This processor access to the geometry repository.

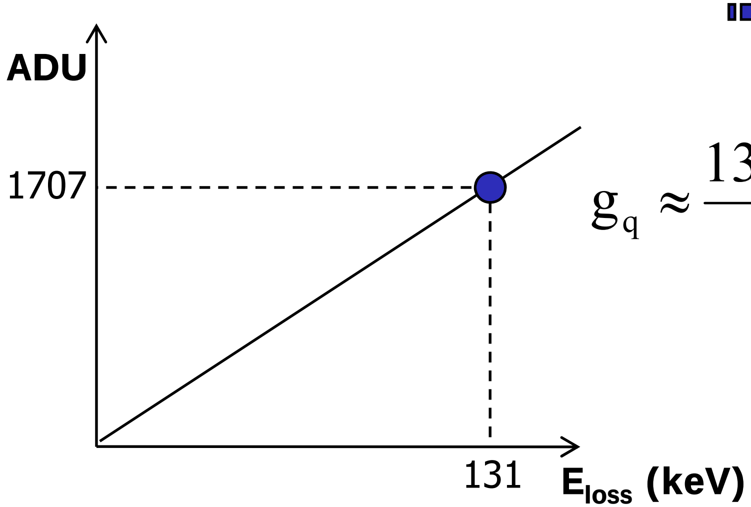
Alignment → MILLEPEDE II package. Loops over all events and finds track candidates. Obtain the global parameters → the alignment constants. Linear least squares problem solved by a simultaneous fit of all parameters. A large number of tracks can be considered for the alignment.

Gain and noise

- The most probably energy loss for a MIP in 450µm of Silicon is[1]:

$$\Delta_{mp} = 450\,\mu m \cdot 0.75 \cdot 388\,eV/\mu m = 35700e^{-} = 131keV$$

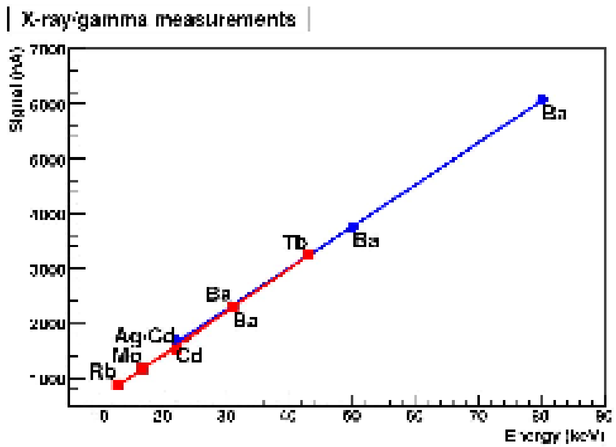
DEPFET Thickness | Scale factor | Mean loss per µm



FIT → y=a+bx → Slope=Gain

b=13.0 ADU/keV

$$g_q \approx \frac{13.0ADU}{keV} \cdot \frac{7.7nA}{1ADU} \cdot \frac{3.6 \cdot 10^{-3}keV}{1e^{-}} \approx 0.360\,nA/e^{-}$$

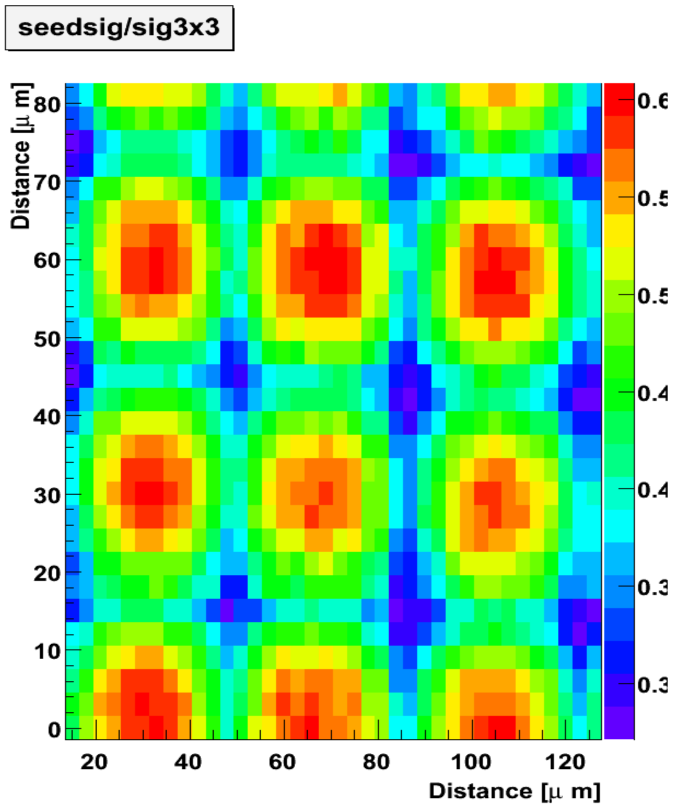


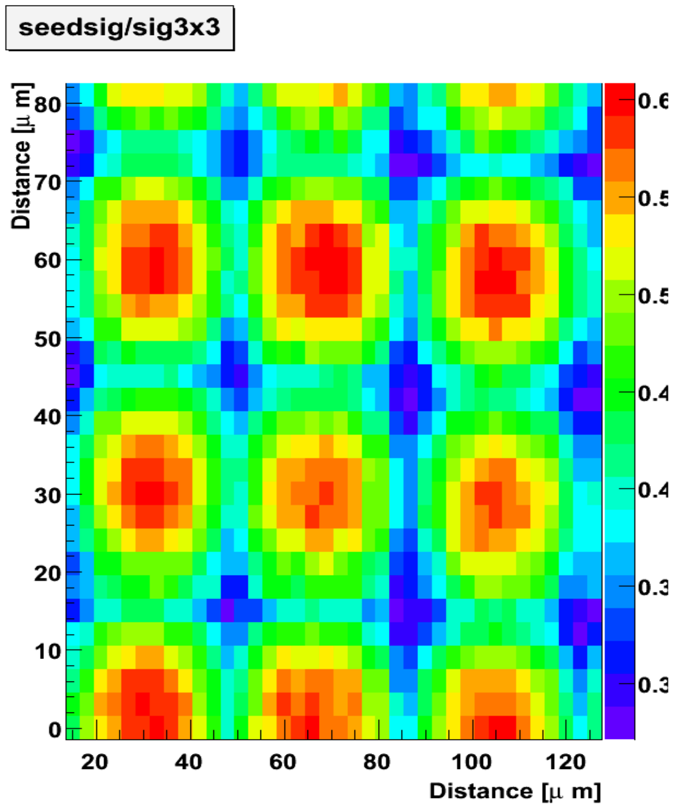
$$ENC = 12.5ADU \cdot \frac{1keV}{13.0ADU} \cdot \frac{1e^{-}h}{3.6 \cdot 10^{-3}keV} \approx 267e^{-}$$

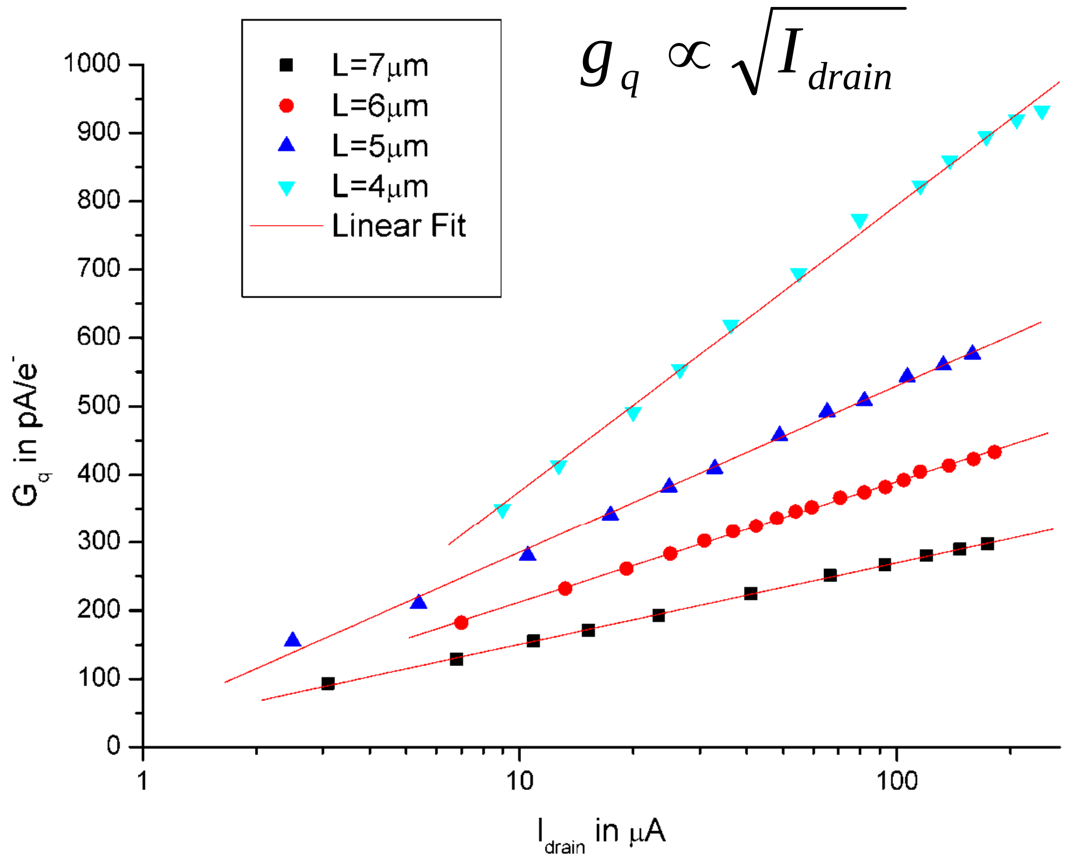
Noise in ADU | Gain | Energy to create e-h

1.- http://pdg.lbl.gov/2008/reviews/passagerpp.pdf

Double pixel structure

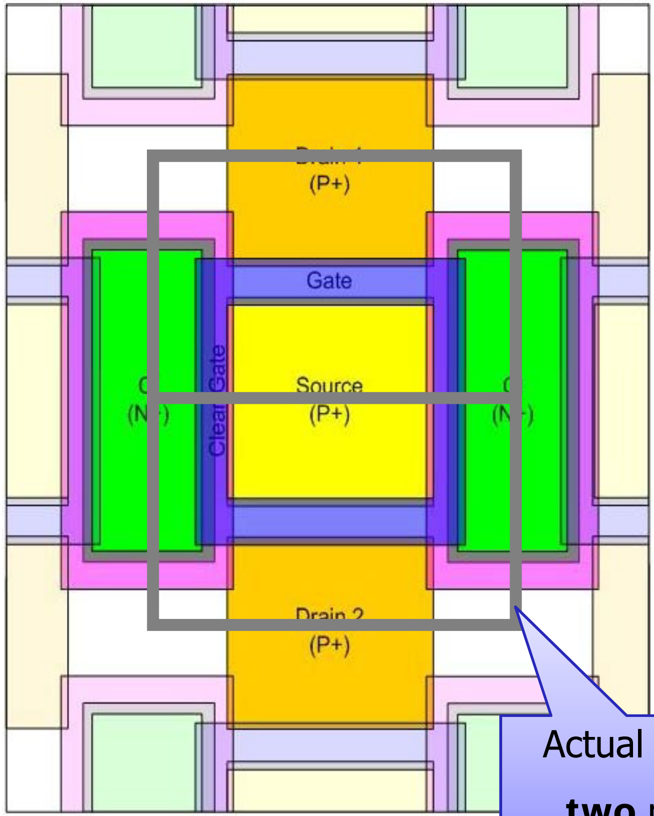






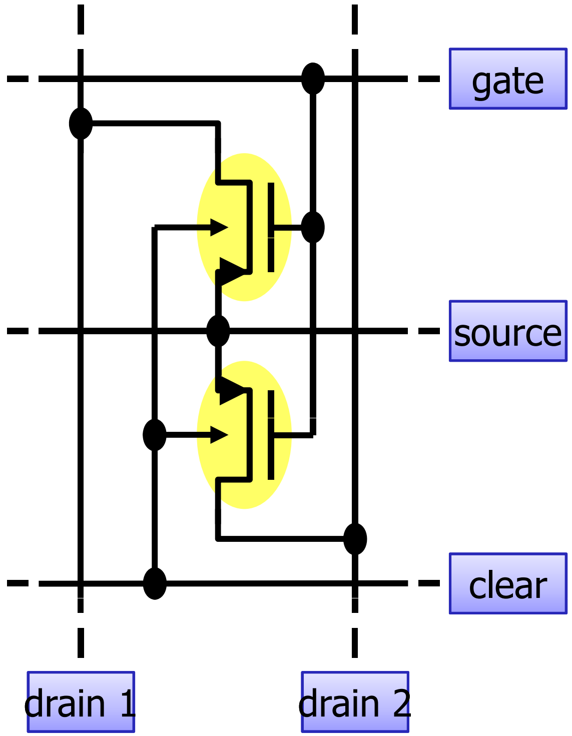
$g_q \propto \sqrt{I_{drain}}$
L=7μm
L=6μm
L=5μm
L=4μm
Linear Fit
G_q in pA/e⁻
I_{drain} in μA
0
100
200
300
400
500
600
700
800
900
1000
1
10
100

Double pixel structure



Actual size of **two** pixels

Merging two pixels (common source) for reduce the size

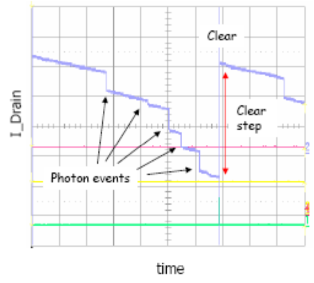


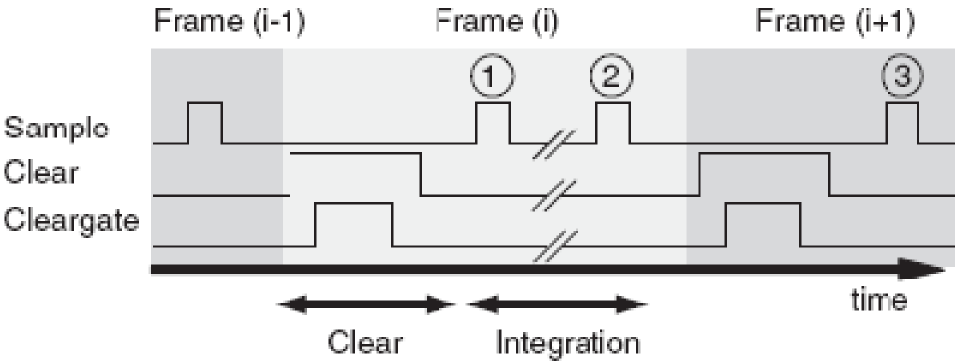
Readout scheme: Fast CDS

•Read-Clear-Read scheme:

- $I_3=I_1$=Pedestal Current (NO reset noise)
- I_2=Pedestal+Signal Current
- Signal= $I_2-I_1=I_2-I_3$

I_2-I_3 better than I_2-I_1 $\rightarrow$ No need of storing an entire data-frame during the CDS, making a row-wise operation possible





Correlated Double Sampling Scheme

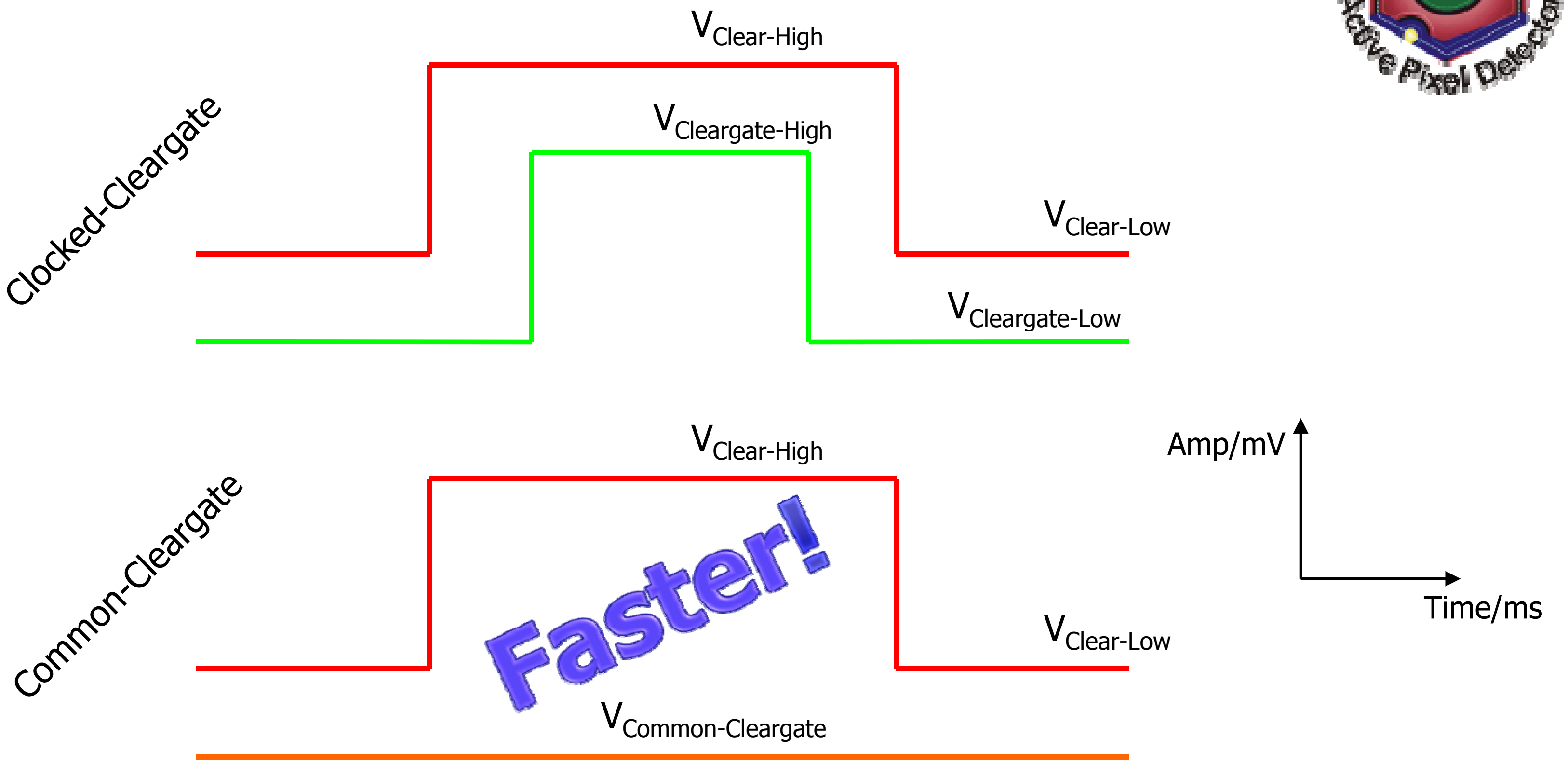
$t_3-t_2<15ns \rightarrow$ Fast Clear!

$t2-t1 \approx 50\mu s$

Row-rate~50MHz

For our readout mode, we need complete clearing of the internal gate charge (no reset noise) because we measure $I_{sig,i}+I_{ped,i}$ and substract $I_{ped,i+1}$, therefore we need $I_{ped,i+1}=I_{ped,i}$

Clearing scheme: CLG vs CCG

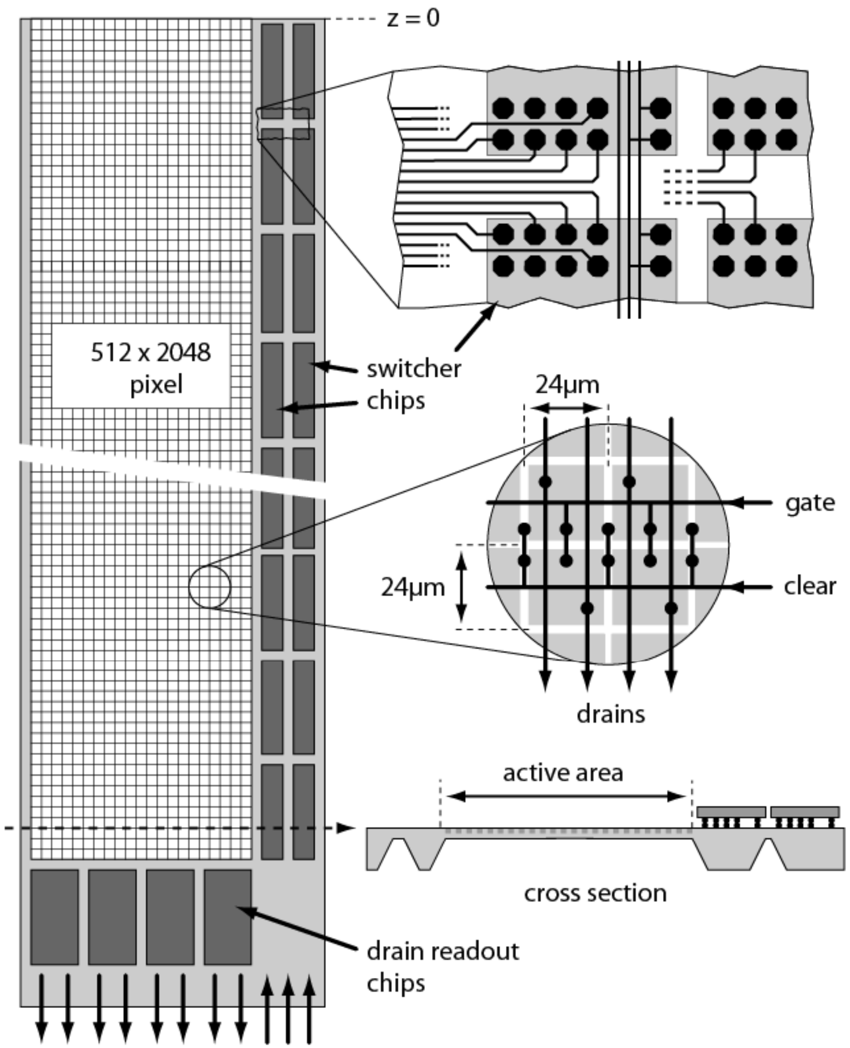


ClearGate: Additional MOS-structure

o CLG: Clocked ClearGate. Timing substructure of the clear is needed.

o CCG: Common ClearGate. Static ClearGate potential.

ILC VXD baseline design



Just as a starting point for the R&D!

- 5 layer, old TESLA layout
- 10 and 25 cm long ladders read out at the ends
- 24 micron pixel
- design goal 0.1% X_0 per layer in the sens. region

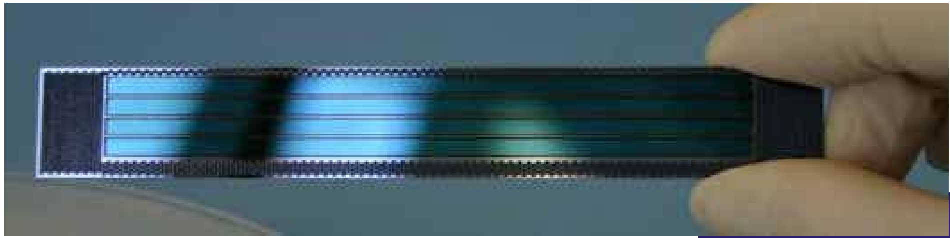
Strategy to cope with the background:

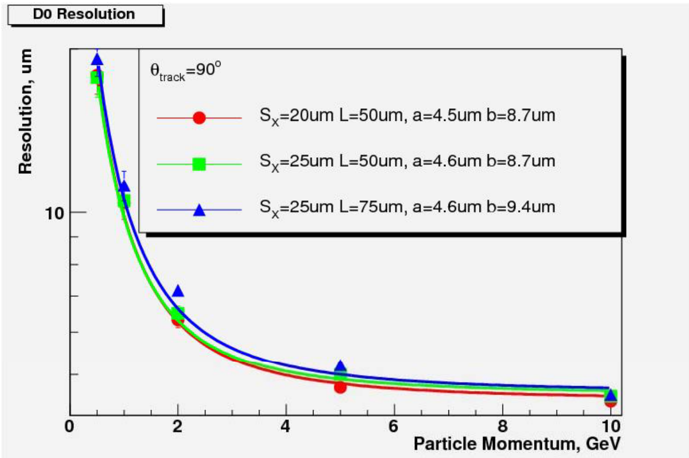
- read ~20 times per train
- store data on ladder
- transfer the data off ladder in the train pause

  → row rate of 40 MHz
- read two rows in parallel, doubles # r/o channels but:

  → row rate 20 MHz ☺

Achievements and status





- ✓ Prototype System with DEPFETs (450µm), CURO and Switcher
- ✓ test beam @ CERN:
  - ✓ S/N≈110 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - ✓ sample-clear-sample 320 ns ←→ goal 50 ns
  - ✓ s.p. res. 1.3 µm @ 450 µm ←→ goal ≈ 4 µm @ 50 µm
- ✓ Thinning technology established, thickness can be adjusted to the needs of the experiment (~20 µm … ~100 µm)
- ✓ radiation tolerance tested with single pixel structures up to 1 Mrad and ~10^{12} n_{eq}/cm^2
- ✓ Simulations show that the present DEPFET concept can meet the challenging requirements at the ILC VXD.

- ✓ New rad. hard Switcher3 chips tested and functional
- ✓ Production of 2nd iteration of DEPFETs under test
- ✓ New r/o chips DCD designed for read-out of large matrices are under test

DEPFET Pros & Cons

- Strong points of DEPFET:
  - **Low noise:** small capacitance and amplification in pixel
  - **Low power:** Charge collection in zero-power mode (transistor switched off)
  - **Very thin** sensors can be built
  - **Radiation tolerant** (up to 1Mrad at least)
  - **Fast signal collection** due to fully depleted bulk
  - **Spectroscopic** X-ray device: can collect charge from very thick sensor (~450 µm)
  - **Multiple readout** possible (non destructive charge measurement)
  - **One manufacturer: MPI-Semiconductor Lab Munich** ("in house production"). Full control on the technology. Long term technology maintenance.

- Disadvantages:
  - **Steering chips** at sides required to provide gate and **clear signal** ('high' voltage)
  - **Limited readout speed** because of **sequential readout** (line rate of some 10 MHz)

CURO Drain Current Readout Chip

- **Regulated cascode** keeps potential at input **constant** (Very important for speed!).
- Pedestal + signal is stored in (two step) **current memory cell**
- **Pedestal current** is subtracted at input node after reset (CDS)
- Current **comparator** finds hits
- Current Difference and hit-flag stored in **mixed FIFO**
- Fast Hit-Finder scans FIFO for up to 2 hits per cycle:
  - **analog currents** to outA, outB
  - digital hit position stored in HIT-RAM
- Analog and digital part operate with **independent clocks**