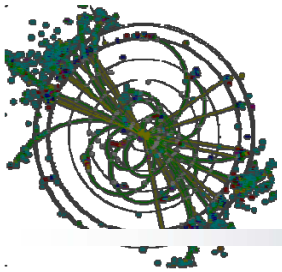

Status of the Chronopixel project

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University of Oregon, Eugene

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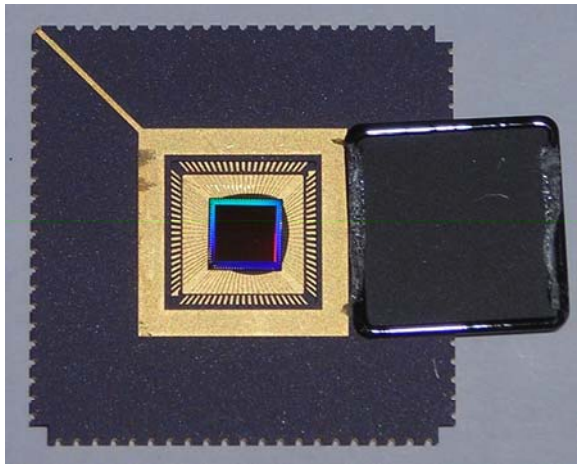
Yale University, New Haven

EE work is contracted to Sarnoff Corporation

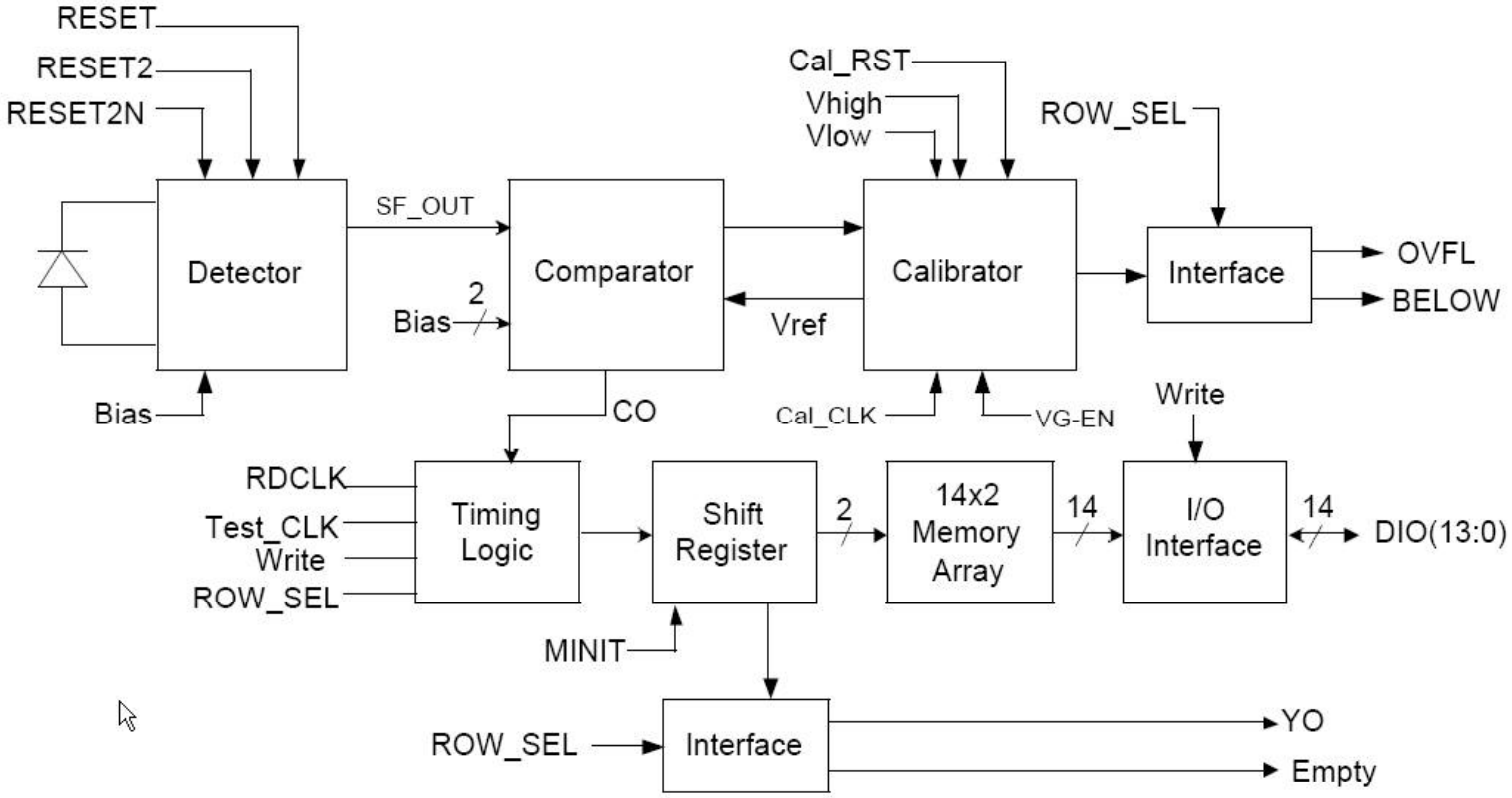
Chronopixel (CMOS)

Yale/Oregon/Sarnoff

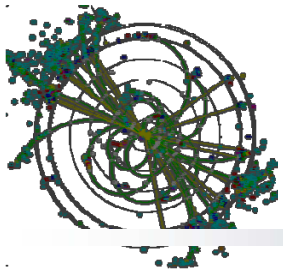
- January, 2007
  - Completed design – Chronopixel
    - **2 buffers, with calibration**
  - Deliverable – tape for foundry
  - 563 transistors
  - Spice simulation verified design
  - TSMC 0.18 μm ⇒ ~50 μm pixel
    - Epi-layer only 7 μm
    - Talking to JAZZ (15 μm epi-layer)
- May 2008
  - Fabricated 80 5x5 mm chips, containing 80x80 50 μm Chronopixels array (+ 2 single pixels) each
- October 2008
  - Design of test board started at SLAC
  - Simulation of the expected prototype performance done



Simplified Chronopixel Schematic



Essential features: Calibrator, special reset circuit



How Chronopixel works

- When signal generated by particle crossing sensitive layer exceeds threshold, snapshot of the time stamp, provided by 14 bits bus is recorded into pixel memory, and memory pointer is advanced.
- If another particle hits the same pixel before device readout was completed, second memory cell is used for this event time stamp.
- During readout, pixels which do not have any time stamp records, generate EMPTY signal, which advances IO-MUX circuit to next pixel without wasting any time. This speeds up readout by factor of about 100.
- Comparator offsets of individual pixels are determined in the calibration cycle, and reference voltage, which sets the comparator threshold, is shifted to adjust thresholds in all pixels to the same signal level.
- To achieve required noise level (about 25 e r.m.s.) special reset circuit (soft reset with feedback) was developed by Sarnoff designers. They claim it reduces reset noise by factor of 2.

Sensor design

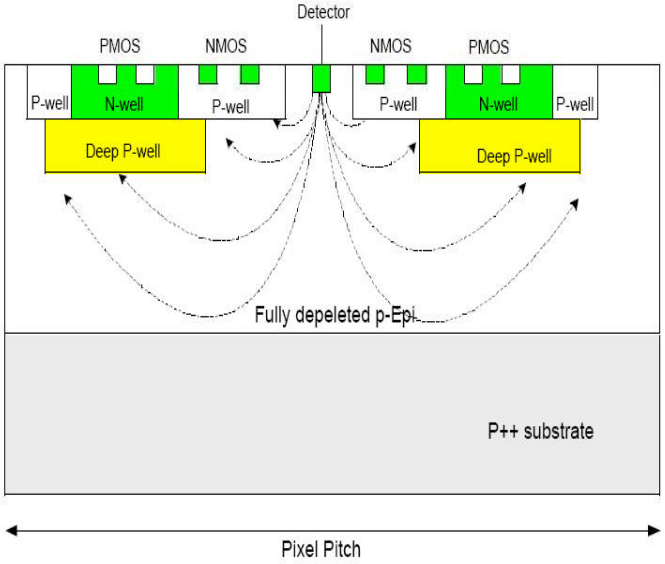


Figure 11.1 Proposed pixel architecture employing the deep p-well layer

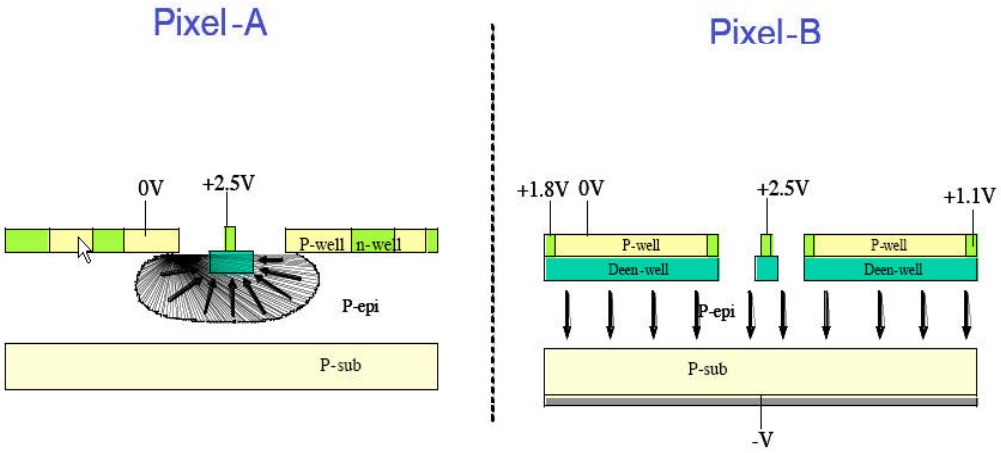


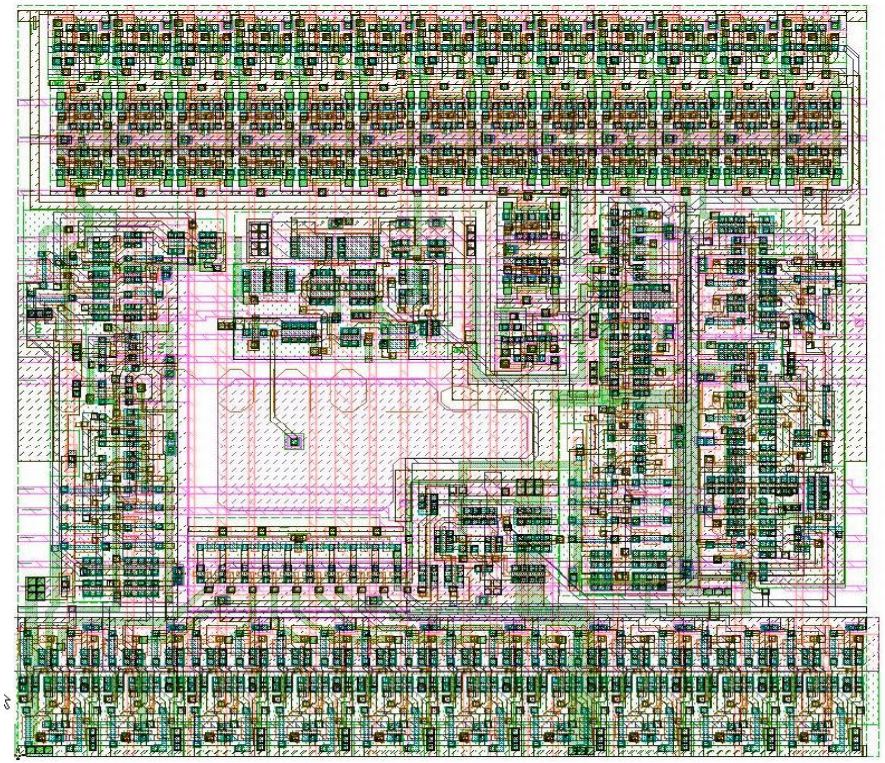
Figure 6.3 Comparison of the vertical cross section views of two pixels

Ultimate design, as envisioned

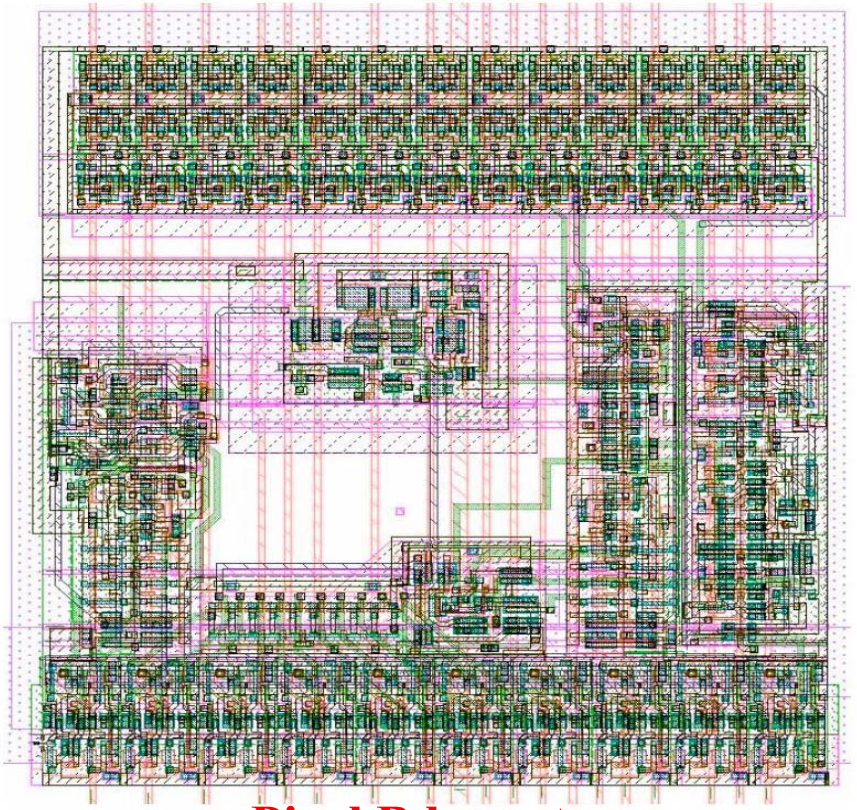
Two sensor options in the fabricated chips

- **TSMC process does not allow for creation of deep P-wells. Moreover, the test chronopixel devices were fabricated using low resistivity (~ 10 ohm*cm) epi layer. To be able to achieve comfortable depletion depth, Pixel-B employs deep n-well, encapsulating all p-well in the NMOS gates. This allow application of negative (up to -10 V) bias on substrate.**

Two layouts



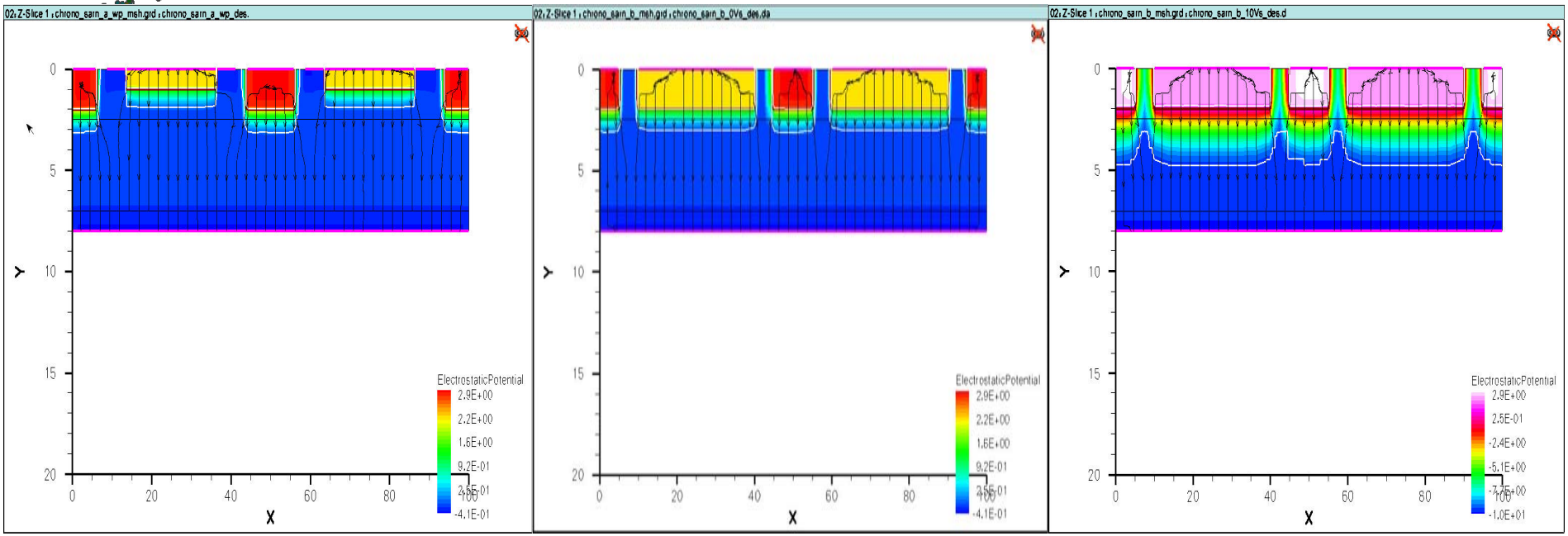
Pixel A layout



Pixel B layout

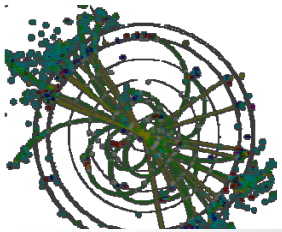
- Because of design rules for TSMC 0.18 process, requiring 5 µ spacing between deep P-wells, the charge collection electrode in the pixel B is smaller (10µ x 8µ) compare to pixel A (12µ x 10µ).

TCAD electric field simulations

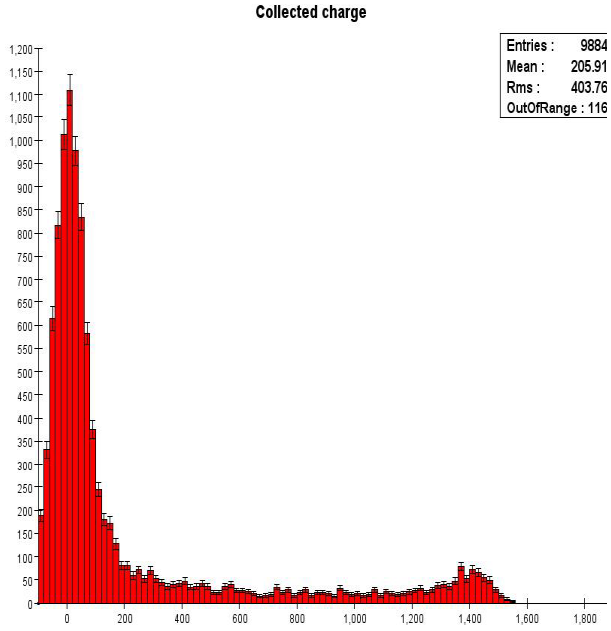


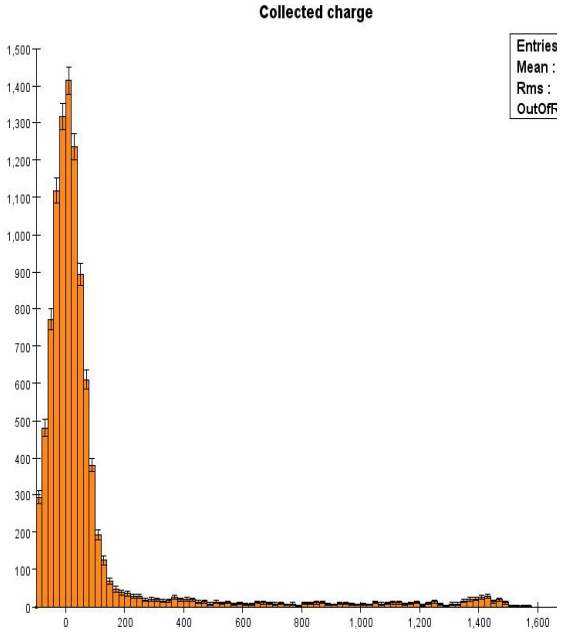
Pixel A **Pixel B: 0 V on substrate** **Pixel B: -10V on substrate**

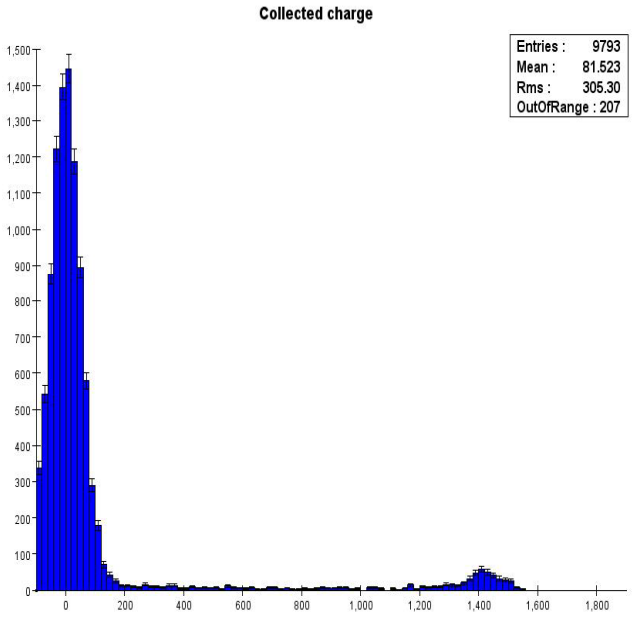
- **Depletion depth in pixel A and pixel B at 0 V on substrate is the same, but collection of the charge in pixel A is a little more efficient because of larger collection electrode size and p-wells surrounding collection electrodes reduce area of competing collection.**



Simulation of the signals from Fe55

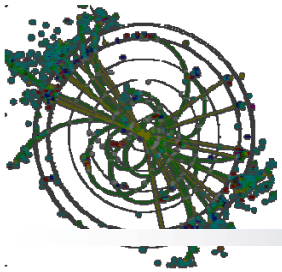




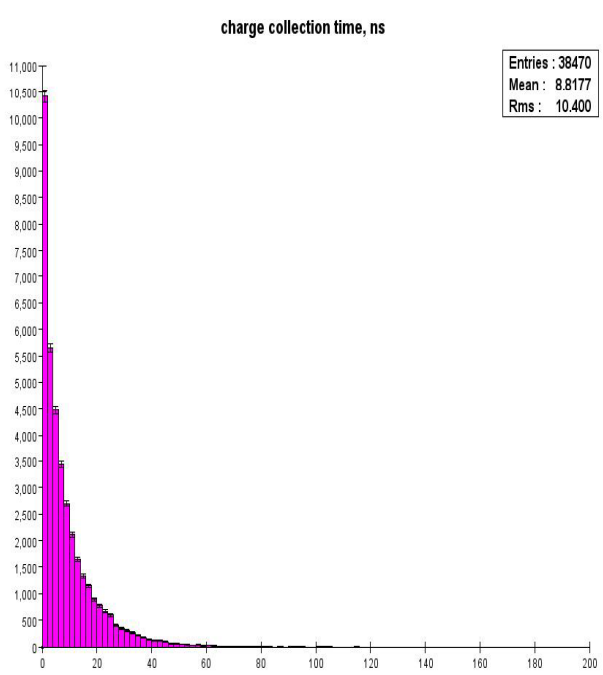


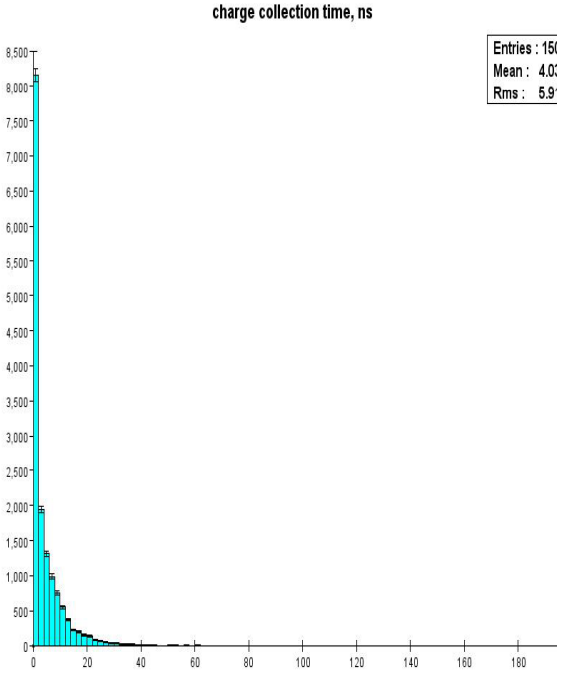
Pixel A **Pixel B at 0 V on subs.** **Pixel B at -10 V on subs**

- **Iron 55 signal will allow us to do sensitivity calibration. Of course, we do not have any means to measure signal in chronopixel, except using sliding discriminator threshold. And here, as well as for real operations, we need equality of the thresholds in the individual pixels.**



Charge collection time for Fe55 hits





Pixel A **Pixel B, 0V on substrate** **Pixel B, 10V on substrate**

- **As expected, pixel A configuration has the largest collection time, but still it is better than 10 ns on average.**

Calibration procedure

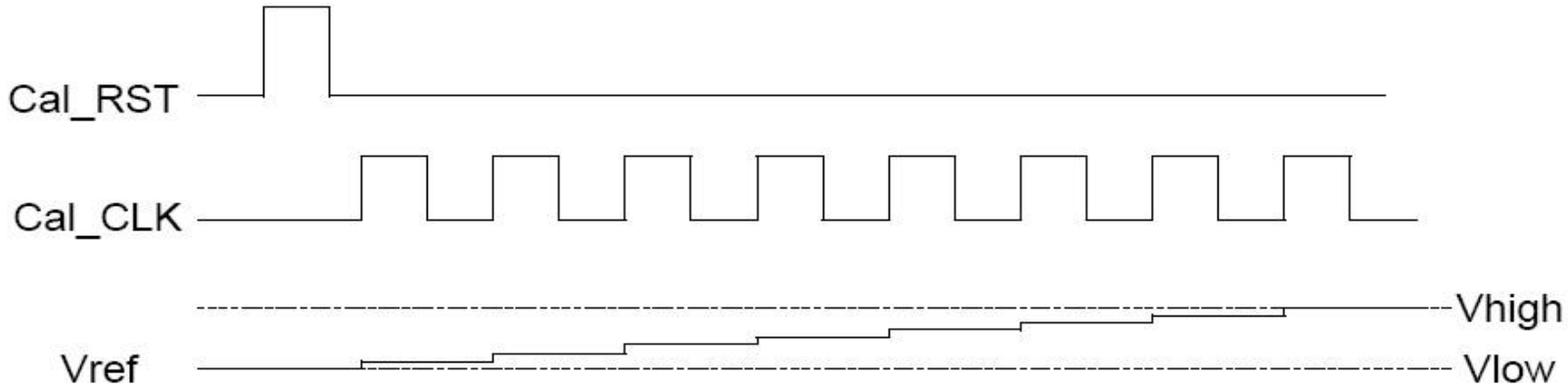
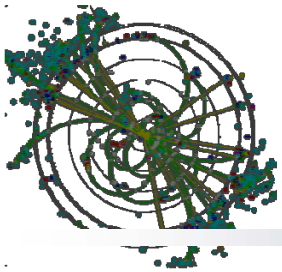


Figure 10.3 Timing diagram showing the calibrator operation

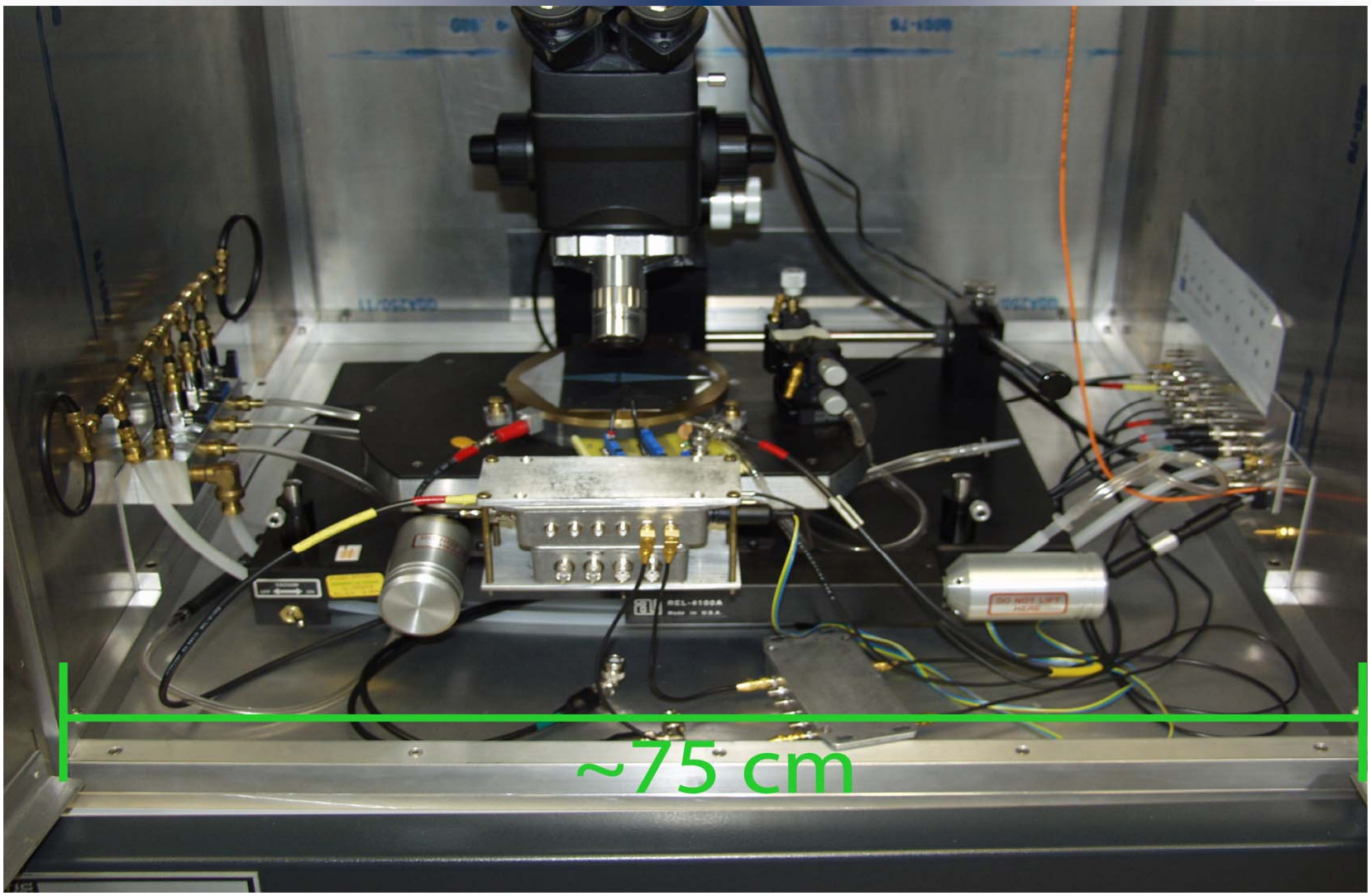
- **During calibration, comparator reference voltage changes from Vlow to Vhigh in 8 steps, controlled by Cal_CLK clock pulses. As soon as it reaches the value when comparato flips, state of the clock counter is recorded into calibration register – individual for each pixel. During normal operation this register is used to select comparator offset for given pixel.**

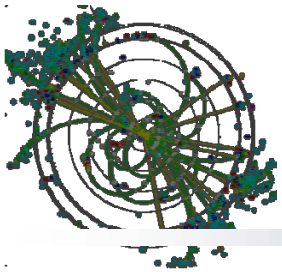


Tests plan

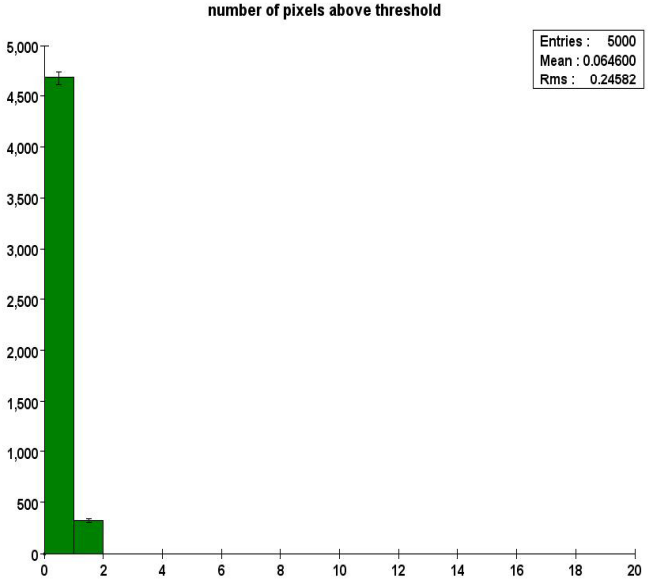
- The most important part of the tests is to check, if calibration procedure working, and is 2 mV range enough to cover offsets in all pixels.
- Second test will be to check memory operations. In principle, writing into time stamps memory is only done by pixel comparator, sensing signal. But for testing of memory proper operation, external write signal can be used to record any value into selected memory cell and when read it back.
- If everything goes smooth, even for some part of the pixels, Fe55 source can be used to determine sensitivity (expected 10 µV/e) and noise level (by the width of Fe55 peak).
- After that tests with IR laser will follow to check time stamping operations.
- Of course, power consumption, and all questions concerning 3MHz time stamp bus operation should be investigated.

IR laser with microscope at UO

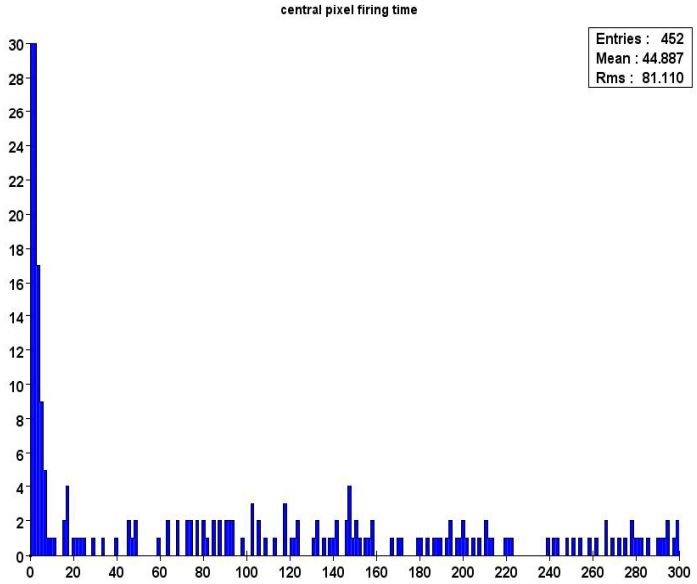




MIP test

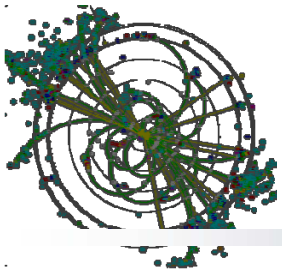


Number of fired pixels per MIP track
For pixel B at -10V on substrate



Firing time – about 80% of hits have
Less than 5 ns firing delay (Y axis is cut)

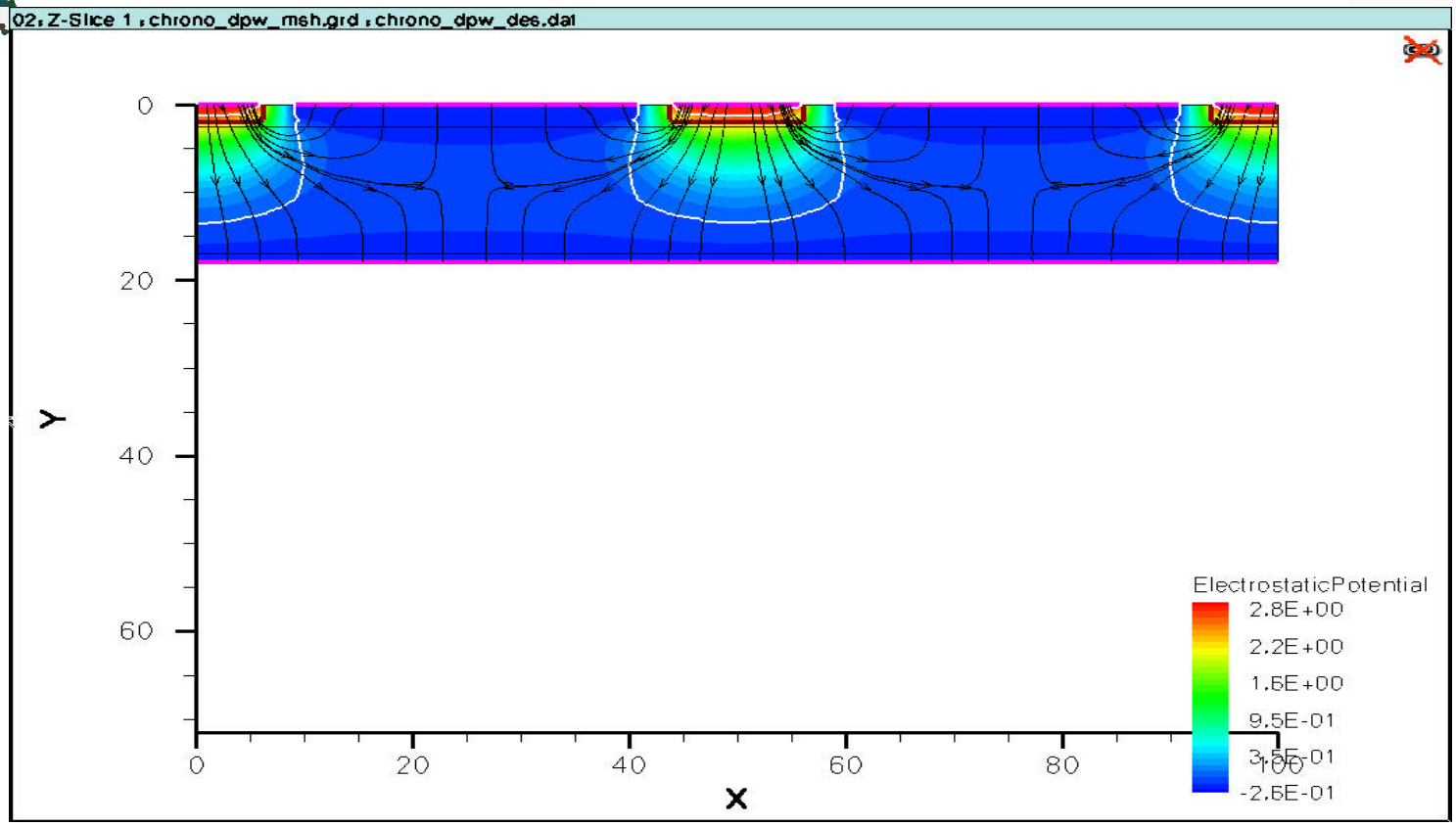
- **From simulation expected efficiency for pixel B at -10V on substrate will be around 6-7%. If the opportunity to have test beam (or even Ru106 source with thin telescope), we can check this number, as well as time stamping with real particles.**



Future plan for Chronopixel project

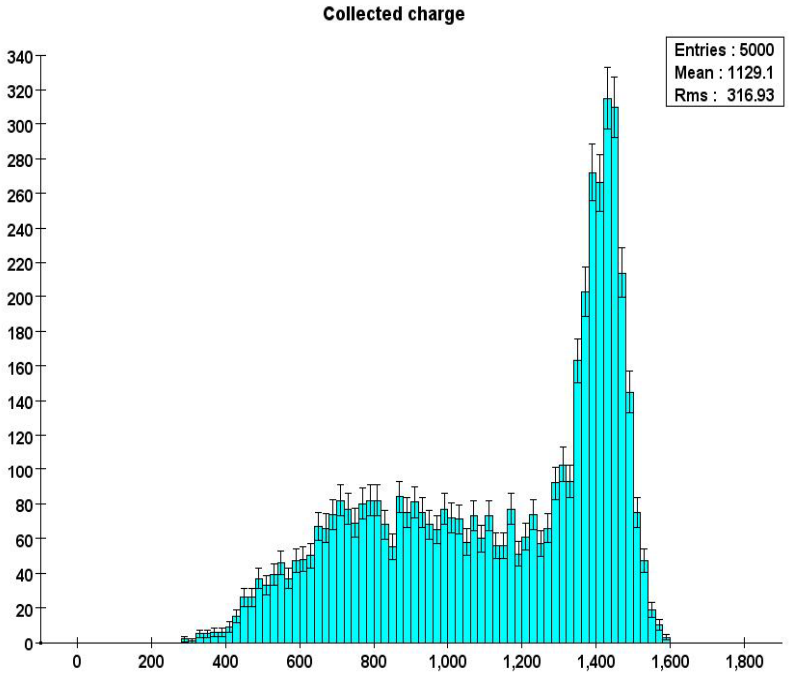
- **In the next production, if there will be enough funding, we should try to move to real detector configuration, even though still within 180 nm technology (so keeping 50x50 µm pixel size).**
  - **Increase epi layer thickness to 15-17 µm**
  - **Increase epi layer resistivity (reduce doping). We'd like to have resistivity of the order of few KOhm*cm, to have larger depleted volume, but as TCAD simulations show, it is not the critical issue. We never can have full depletion thorough all sensitive layer in the deep P-well case. So charge collection always will be by diffusion. However larger depleted volume will help capture carrier faster, limiting diffusion distance before collection, so boosting signal value in central pixel (helps efficiency) and reducing number of pixels fired by one particle (reduce occupancy).**
  - **Implement deep P-well.**

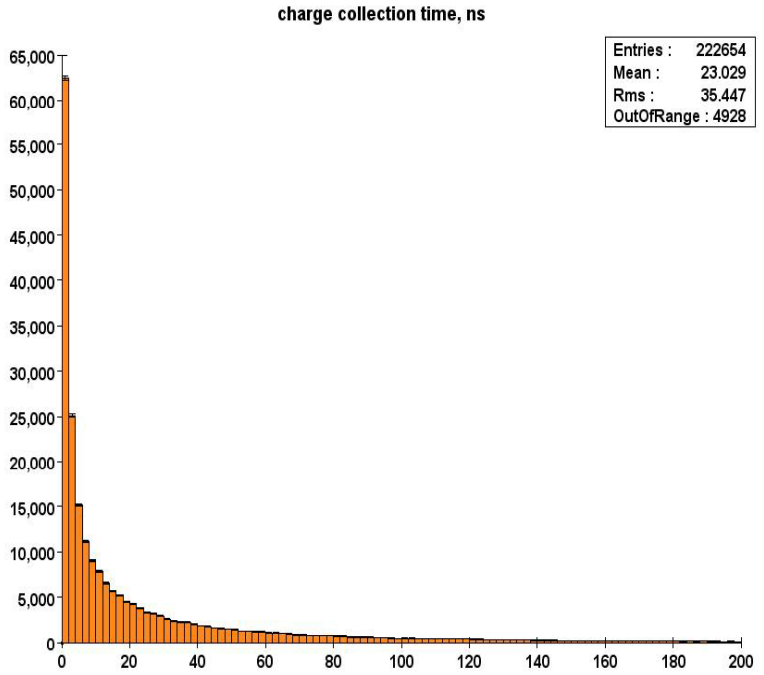
Simulation of deep P-well device



TCAD simulation of the field in the 17µm thick 50x50µm^2 pixel with deep P-wells encapsulating all electronics (the same 2µm deep as n-wells). White line shows the limits of fully depleted volume.

Charge collection in deep P-well pixel



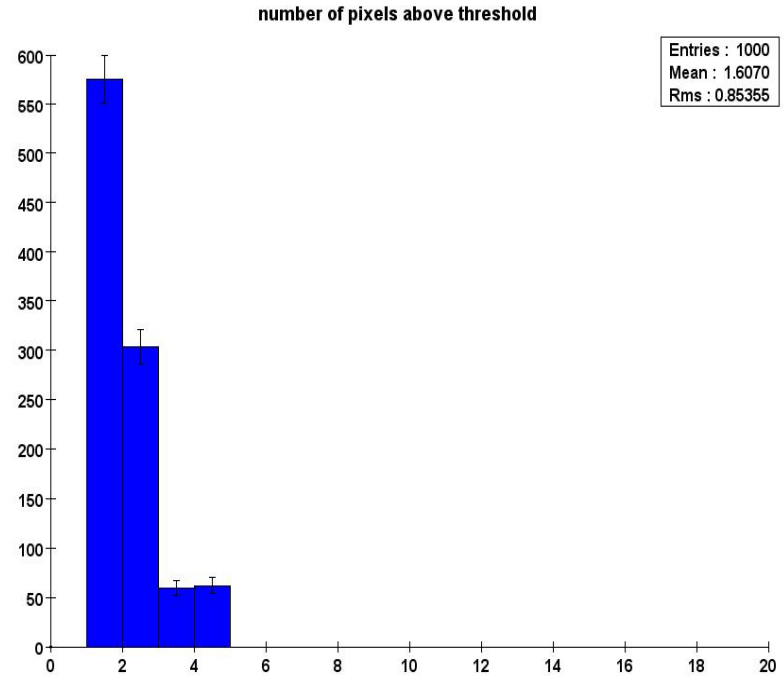


Fe55 signal value

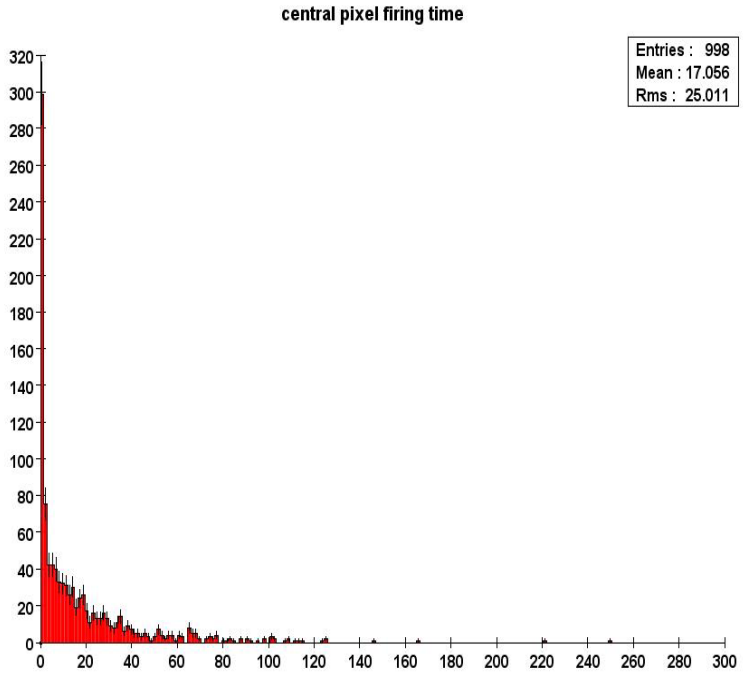
Charge collection time for Fe55

- **If Fe55 hit occurs in undepleted area, the charge is shared mostly by two pixels, as indicated by wide peak at half of main peak amplitude.**

Track efficiency for deep P-well pixel

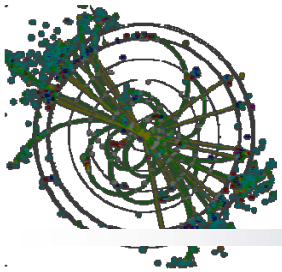


Number of pixels above threshold of 125 e (5 times expected noise r.m.s). We see 100% efficiency in that case



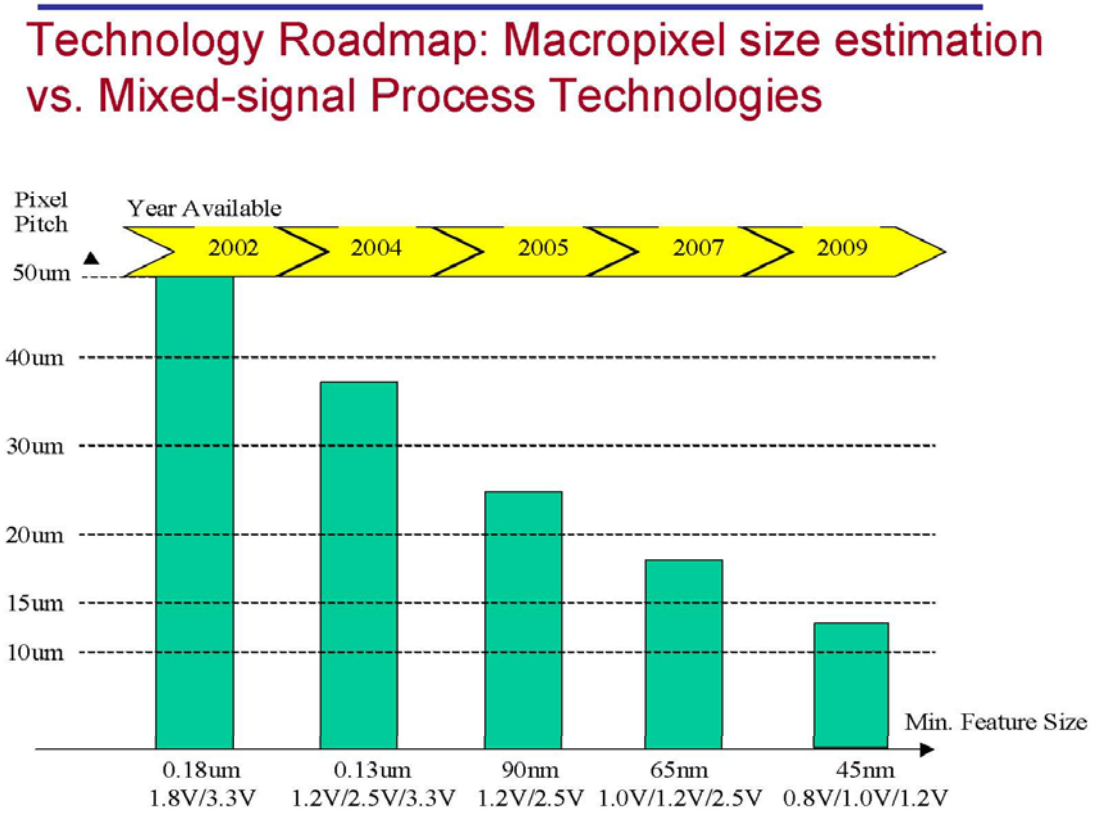
Firing time (time when signal reaches comparator threshold) distribution for central pixel.

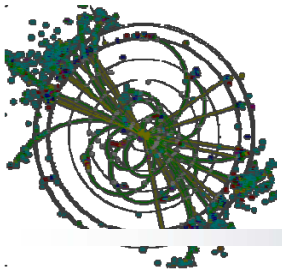
- **We can see, that if goal of 25 e noise will be achieved, such pixel will have 100% efficiency for min. ionizing particles. Efficiency drops with threshold rather quickly -> 98% with threshold 200e (40e noise), 94% with 250e (50e noise).**



Technology Roadmap

- Pixel size will scale down as technology advances
  - 180 nm -> 45 nm
  - 50 μm pixel -> 20 μm or smaller pixel





Conclusions

- First chronopixel prototypes have been fabricated, packaged and delivered to SLAC for testing.
- Test equipment at SLAC expected to be ready in January 2009
- We are looking for the manufacturer of the next prototype implementing deep P-well. Depending on how much correction to the design will be needed, next prototype may be ready for submission at the end 2009 – beginning 2010. It still will be 50x50 μm pixels, but completely operational, 100% efficient device.
- After that accomplished, scaling to 45 nm technology may be thought. So, funding depending, we can be ready to start design of final vertex detector sensors in 2011-2012.